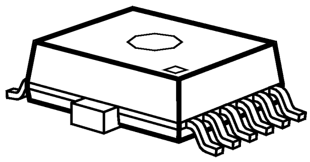
Dual Low Dropout Voltage Regulator

TLE 4473 GV55-2

Features

- Stand-by output 190 mA; 5 V ± 2%
- Main output: 300 mA, 5 V
  tracked to the stand-by output
- Low quiescent current consumption
- Disable function separately for both outputs
- Wide operation range: up to 42 V
- Very low dropout voltage
- 2 independent reset circuits
- Watchdog
- Output protected against short circuit
- Wide temperature range: -40 °C to 150 °C
- Overtemperature protection
- Overload protection
- Green product (RoHS compliant)
- AEC qualified



PG-DSO-12-11

Functional Description

The TLE 4473 is a monolithic integrated voltage regulator with two low dropout outputs, a main output Q1 for loads up to 300 mA and a stand by output Q2 providing a maximum of 190 mA. The stand-by regulator transforms an input voltage V_I in the range of 5.6 V ≤ V_I ≤ 42 V to an output voltage of V_{Q2} = 5.0 V (±2%). The main output is tracked to the stand by output voltage and provides also 5 V. A versions of this device with 5 V/3.3 V and 5 V/2.6 V are also available, please refer to the data sheet TLE 4473 G V53/ TLE 4473 G V52. The Inhibit input INH1 disables the output Q1 only, whereas Inhibit input INH2 disables both, Q1 and Q2 output. The quiescent current then is 1 µA.

The TLE 4473 is designed to supply microprocessor systems and sensors under the severe conditions of automotive applications and therefore is equipped with additional protection functions against overload, short circuit and overtemperature. The device operates in the wide junction temperature range of -40 °C to 150 °C.

Type	Package	Marking
TLE 4473 GV55-2	PG-DSO-12-11 (RoHS compliant)	TLE4473 GV55-2

The device features a reset with adjustable power on delay for each of the outputs. In addition the output for the microcontroller supply comes up with a watchdog in order to supervise a connected microcontroller

Reset and Watchdog Behavior

The reset output RO2 is in high-state if the voltage on the delay capacitor C_{D2} is greater or equal V_{DU2}. The delay capacitor C_{D2} is charged with the current I_{DC2} for output voltages greater than the reset threshold V_{RT2}. If the output voltage gets lower than V_{RT2} ('reset condition') a fast discharge of the delay capacitor C_{D2} sets in and as soon as V_{D2} gets lower than V_{DL2} the reset output RO2 is set to low-level. The time for the delay capacitor charge is the reset delay time. For the power-on case the charging process of C_{D2} starts from 0 V, which leads to the equation:

$$t_{D,\,on} = \frac{C_{D2} \times V_{DU2}}{I_{DC2}} \tag{1}$$

for the power-on reset delay time.

When the voltage on the delay capacitor has reached V_{DU2} and reset was set to high, the watchdog circuit is enabled and discharges C_{D2} with the constant current I_{DD2}.

If there is no rising edge observed at the watchdog input, C_{D2} will be discharge down to V_{DL2}. Then reset output RO2 will be set to low and C_{D2} will be charged again with the current I_{DC2} until V_{D2} reaches V_{DU2} and reset will be set high again.

If the watchdog pulse (rising edge at watchdog input WI) occurs during the discharge period C_{D2} is charged again and the reset output stays high. After V_{D2} has reached V_{DU2}, the periodical cycle starts again.

The watchdog timing is shown in **Figure 1**. The maximum duration between two watchdog pulses corresponds to the minimum watchdog trigger time $T_{WI,tr}$. Higher capacitances on pin D2 result in longer watchdog trigger times:

$$T_{WI,tr}\big|_{max} = 0.34\ \text{ms/nF} \times C_{D2} \tag{2}$$

If the output voltage Q1 decreases below V_{RT1} (typ. 4.65 V), the external capacitor C_{D1} is discharged by the reset generator of the main output. If the voltage on this capacitor drops below V_{DL1}, a reset signal is generated on pin 2 (RO1). If the output voltage rises above the reset threshold, C_{D1} will be charged with the constant current I_{DC1}. After the power-on-reset time the voltage on the capacitor reaches V_{DU1} and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of C_{D1} using the above given equation (1) analogous for Q1.

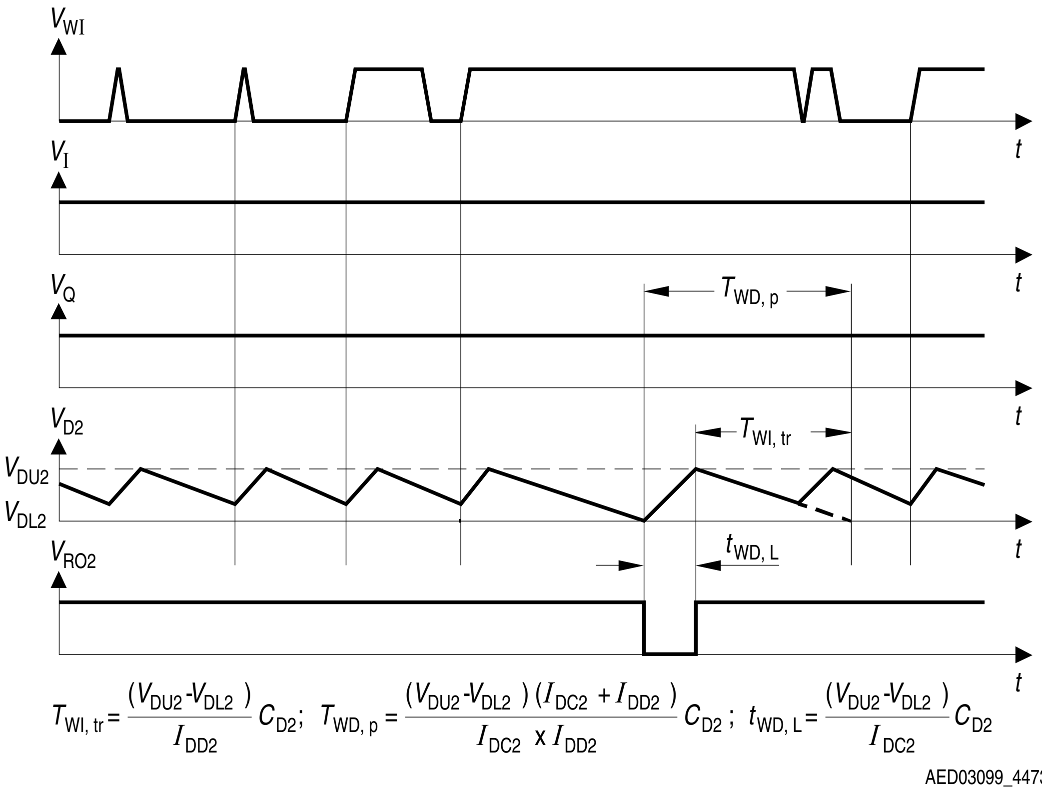


Figure 1 Watchdog Timing Schedule

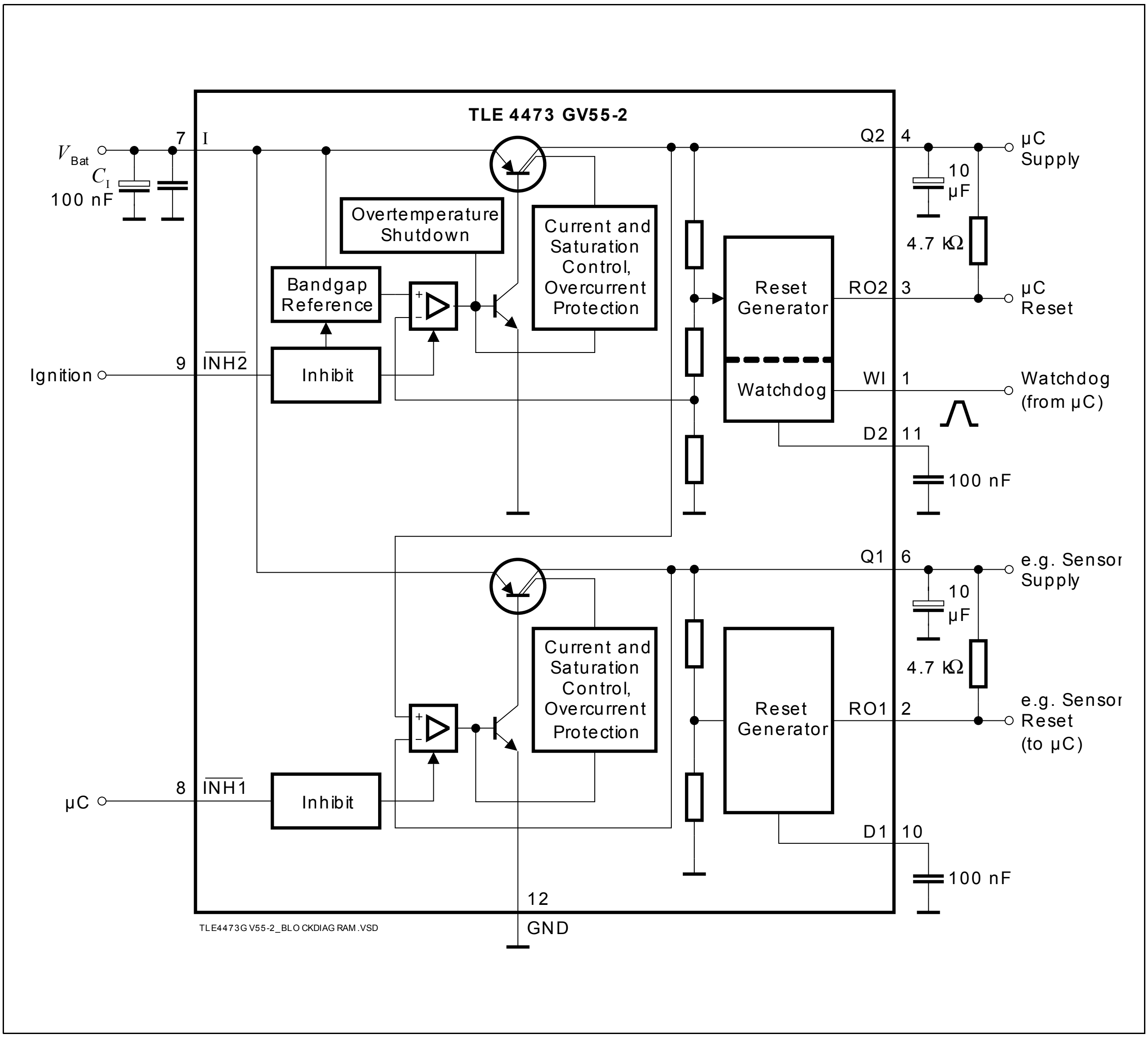


Figure 2 Block Diagram with Typical External Components

Application Information

The output voltage is divided by a voltage divider and compared to an internal reference voltage. A regulation loop controls the Q2 output in order to achieve a stable output voltage at the Q2 pin. A second regulation loop controls the Q1 output. The reference voltage for the Q1 is the regulated Q2 potential (tracking regulator).

Figure 2 includes the components needed for a typical application. Maintaining the stability of the regulation loops requires a capacitor of 10 µF both outputs. A maximum ESR of 5 Ω is permissible for the Q2 output, while the Q1 output requires a capacitor with a maximum ESR of 3 Ω. For both output blocking capacitors it is recommended to use tantalum types in order to stay in the permissible ESR range over the full operating temperature range.

At the input of the regulator a capacitor is necessary for compensating line influences. A minimum of 100 nF (ceramic capacitor) is recommended. In addition for compensation of long input lines of several meters an electrolytic input capacitor of 47 µF … 220 µF should be placed at the input.

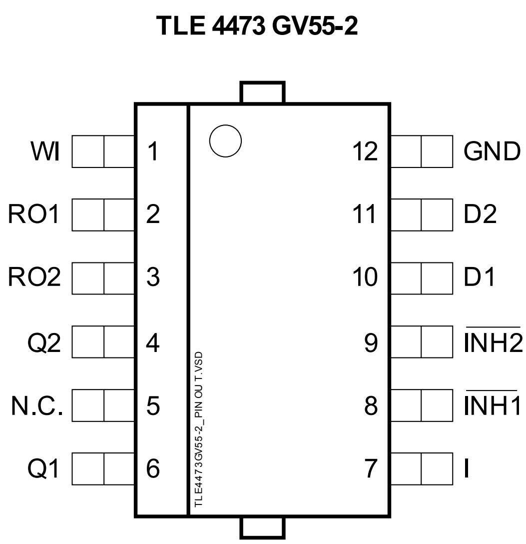


Figure 3 Pin Configuration (top view)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	WI	**Watchdog input;** input for watchdog pulses, positive edge triggered.
2	RO1	**Reset and watchdog output for Q1;** open collector output. Connect to pull-up resistor.
3	RO2	**Reset output 2;** open collector output. Connect to pull-up resistor.
4	Q2	**Stand-by regulator output voltage;** block to GND with a capacitor $C_{Q2} \geq 10\ \mu F$, ESR < 5 Ω at 10 kHz.
5	N.C.	**Internally not connected;** connect to GND.
6	Q1	**Main regulator output voltage;** output voltage tracked to Q2 voltage; block to GND with a capacitor $C_{Q1} \geq 10\ \mu F$, ESR < 3 Ω at 10 kHz
7	I	**Input voltage;** block to ground directly at the IC with a ceramic capacitor.
8	$\overline{\text{INH1}}$	**Inhibit input 1;** low level disables Q1, integrated pull-down resistor.
9	$\overline{\text{INH2}}$	**Inhibit input 2;** low level at $\overline{\text{INH2}}$ and $\overline{\text{INH1}}$ disables Q2 and Q1, integrated pull-down resistor.
10	D1	**Reset Delay 1;** connect to ground via a capacitor to set reset delay for Q1.
11	D2	**Reset Delay 2;** connect to ground via a capacitor to set reset delay and watchdog timing for Q2.
12	GND	**Ground;** connect to heatslug.
Heatslug		Interconnect with PCB heatsink area and GND.

Table 2 Absolute Maximum Ratings

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input I					
Voltage	V_I	-42	45	V	–
Current	I_I	–	–	mA	Internally limited
Stand-by Output Q2					
Voltage	V_{Q2}	-0.3	18	V	–
Current	I_{Q2}	–	–	mA	Internally limited
Main Output Q1					
Voltage	V_{Q1}	-0.3	18	V	–
Current	I_{Q1}	–	–	mA	Internally limited
Inhibit Input $\overline{INH1}$					
Voltage	$V_{\overline{INH1}}$	-42	45	V	–
Current	$I_{\overline{INH1}}$	-2	2	mA	–
Inhibit Input $\overline{INH2}$					
Voltage	$V_{\overline{INH2}}$	-42	45	V	–
Current	$I_{\overline{INH2}}$	-2	2	mA	–
Reset Output RO1					
Voltage	V_{RO1}	-0.3	18	V	–
Current	I_{RO1}	–	–	mA	Internally limited
Reset Output RO2					
Voltage	V_{RO2}	-0.3	18	V	–
Current	I_{RO2}	–	–	mA	Internally limited
Reset Delay D1					
Voltage	V_{D1}	-0.3	7	V	–
Current	I_{D1}	-5	5	mA	–
Reset Delay D2					
Voltage	V_D	-0.3	7	V	–
Current	I_D	-5	5	mA	–

Table 2 Absolute Maximum Ratings (cont'd)

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Watchdog Input WI					
Voltage	V_{RADJ}	-0.3	7	V	–
Current	I_{RADJ}	-5	5	mA	–
Temperatures					
Junction temperature	T_j	-50	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_I	5.6	42	V	–
Junction temperature	T_j	-40	150	°C	–
Thermal Resistances PG-DSO-12-11					
Junction pin	$R_{thj-pin}$	–	4	K/W	–
Junction ambient	R_{thj-a}	–	115	K/W	PCB Heat Sink Area 0 mm^2 1)
Junction ambient	R_{thj-a}	–	100	K/W	PCB Heat Sink Area 100 mm^2 1)
Junction ambient	R_{thj-a}	–	60	K/W	PCB Heat Sink Area 300 mm^2 1)
Junction ambient	R_{thj-a}	–	48	K/W	PCB Heat Sink Area 600 mm^2 1)

1) Package mounted on PCB 80 × 80 × 1.5 mm^3; 35µ Cu; 5µ Sn; zero airflow.

Note: In the operating range the functions given in the circuit description are fulfilled. Integrated protection functions are designed to prevent IC destruction under fault conditions. Protection functions are not designed for continuous repetitive operation.

Table 4 Electrical Characteristics

V_{I1} = 13.5 V; V_{INH1} = V_{INH2} = 5 V; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Stand-by Regulator						
Output Q2						
Output voltage	V_{Q2}	4.90	5.0	5.10	V	1 mA < I_{Q2} < 190 mA; 6 V < V_I < 28 V
Output current limitation	I_{Q2}	200	300	650	mA	V_{Q2} = 4.5 V
Output drop voltage; $V_{DRQ1} = V_{I1} - V_{Q1}$	V_{DRQ2}	–	200	600	mV	I_{Q2} = 100 mA[1)]
Load regulation	$\Delta V_{Q2,Lo}$	–	15	50	mV	1 mA < I_{Q2} < 190 mA
Line regulation	$\Delta V_{Q2,Li}$	–	5	20	mV	I_{Q2} = 1 mA; 6 V < V_I < 28 V
Power Supply Ripple Rejection	$PSRR$	–	65	–	dB	f_r = 100 Hz; V_r = 1 Vpp
Current Consumption						
Quiescent current; stand-by $I_q = I_I - I_{Q2}$	I_q	–	170	220	µA	I_{Q2} = 500 µA; T_j = 25 °C; $V_{INH1} < V_{INH1\ OFF}$ (Q1 off)
		–	–	245	µA	I_{Q2} = 500 µA; T_j = 85 °C; $V_{INH1} < V_{INH1\ OFF}$ (Q1 off)
		–	–	280	µA	I_{Q2} = 500 µA; $V_{INH1} < V_{INH1\ OFF}$ (Q1 off)
		–	4.5	5	mA	I_{Q2} = 100 mA; $V_{INH1} < V_{INH1\ OFF}$ (Q1 off)
Quiescent current; inhibited	I_q	–	0.1	1	µA	$V_{INH1} = V_{INH2}$ = 0 V; T_j < 85 °C
		–	0.1	20	µA	$V_{INH1} = V_{INH2}$ = 0 V

Table 4 Electrical Characteristics (cont'd)

V_{I1} = 13.5 V; V_{INH1} = V_{INH2} = 5 V; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Inhibit Input $\overline{INH2}$						
Turn-on Voltage	$V_{\overline{INH2}\,ON}$	–	–	2.3	V	V_{Q2} on
Turn-off Voltage	$V_{\overline{INH2}\,OFF}$	0.65	–	–	V	V_{Q2} off
H-input current	$I_{\overline{INH2}\,ON}$	-1	3.2	6	µA	V_{INH2} = 5.0 V (see Page 13)
L-input current	$I_{\overline{INH2}\,OFF}$	-1	0.1	1	µA	0 V < V_{INH2} < 0.8 V
Watchdog and Reset Timing D2						
Charge current	I_{DC2}	6.5	9.0	14.0	µA	V_{D2} = 1 V
Discharge current	I_{DD2}	2.0	3.5	5.0	µA	V_{D2} = 1 V
Upper timing threshold	V_{DU2}	1.5	1.85	2.4	V	–
Lower timing threshold	V_{DL2}	0.3	0.45	0.6	V	–
Saturation Voltage	$V_{D2,SAT}$	–	–	100	mV	V_{Q2} < V_{RT2}
Watchdog trigger time	$T_{WI,tr}$	34	42	51	ms	C_{D2} = 100 nF
Reset delay time	T_{RD2}	15	20	25	ms	C_{D2} = 100 nF
Reset reaction time	T_{rr}	–	–	5.0	µs	C_{D2} = 100 nF
Reset Output RO2						
Reset switching threshold	V_{RT2}	4.55	4.65	4.8	V	–
	V_{RT2}/V_{Q2}	90	93	96	%	–
Reset threshold headroom	V_{R2HEAD}	200	350	500	mV	V_{Q2} - V_{RT2}
Reset output sink current	I_{RO2}	1.0	–	–	mA	V_{Q2} = 5 V, V_{D2} = 0 V; V_{RO2} = 0.3 V
Reset output low voltage	V_{RO2L}	–	0.15	0.3	V	$V_{Q2} \geq$ 1 V; I_{RO2} = 1 mA
Reset high voltage	V_{RO2H}	4.5	–	–	V	$R_{RO2,ext}$ = 4.7 kΩ

Table 4 Electrical Characteristics (cont'd)

V_{I1} = 13.5 V; V_{INH1} = V_{INH2} = 5 V; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Main (Tracked) Regulator						
Output Q1						
Output voltage	V_{Q1}	4.875	5.0	5.125	V	1 mA < I_{Q1} < 200 mA; 6 V < V_I < 28 V
Output voltage tracking accuracy	$\Delta V_Q = V_{Q2} - V_{Q1}$	-25	5	25	mV	1 mA < I_{Q1} < 200 mA; 6 V < V_I < 28 V
Output voltage tracking accuracy	$\Delta V_Q = V_{Q2} - V_{Q1}$	-25	5	25	mV	1 mA < I_{Q1} < 300 mA; 8 V < V_I < 28 V
Output current limitation	I_{Q1}	350	500	–	mA	V_{Q1} = 4.5 V
Output drop voltage $V_{DRQ1} = V_I - V_{Q1}$	V_{DRQ1}	–	300	600	mV	I_{Q1} = 200 mA[1)]
Load regulation	$\Delta V_{Q1,Lo}$	–	5	50	mV	5 mA < I_{Q1} < 300 mA
Line regulation	$\Delta V_{Q1,Li}$	–	5	25	mV	I_{Q1} = 5 mA; 6 V < V_I < 28 V
Power Supply Ripple Rejection	$PSRR$	–	65	–	dB	f_r = 100 Hz; V_r = 1 Vpp
Current Consumption						
Quiescent current; $I_q = I_I - I_{Q1} - I_{Q2}$	I_q	–	10	20	mA	I_{Q1} = 300 mA; I_{Q2} = 500 µA; V_{Q1} and V_{Q2} on
Quiescent current; $I_q = I_I - I_{Q1} - I_{Q2}$	I_q	–	250	500	µA	I_{Q2} = I_{Q1} = 500 µA; V_{Q1} and V_{Q2} on
Inhibit Input $\overline{\text{INH1}}$						
Turn-on Voltage	$V_{\overline{INH1}\ ON}$	–	–	2.3	V	V_{Q1} on
Turn-off Voltage	$V_{\overline{INH1}\ OFF}$	0.7	–	–	V	V_{Q1} off
H-input current	$I_{\overline{INH1}\ ON}$	-1	3.5	5	µA	3.0 V < V_{INH1} < 5 V; (see **Page 14**)
L-input current	$I_{\overline{INH1}\ OFF}$	-1	0.1	1	µA	0 V < V_{INH1} < 0.8 V

Table 4 Electrical Characteristics (cont'd)

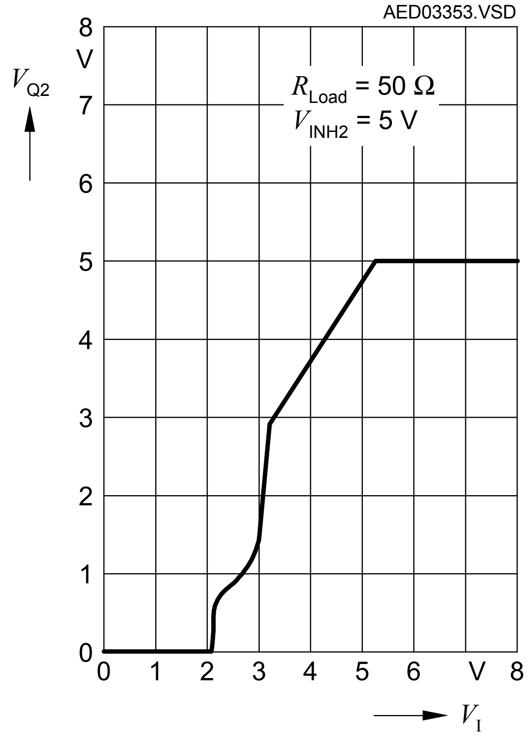
V_{I1} = 13.5 V; V_{INH1} = V_{INH2} = 5 V; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Reset Timing D1						
Charge current	I_{DC1}	4.0	8.0	14.0	µA	V_{D1} = 1 V
Upper timing threshold	V_{DU1}	1.6	1.8	2.2	V	–
Lower timing threshold	V_{DL2}	0.3	0.4	0.6	V	–
Saturation Voltage	$V_{D1,SAT}$	–	–	100	mV	V_{Q1} < V_{RT1}
Reset delay time	T_{RD1}	14	20	30	ms	C_{D1} = 100 nF
Reset reaction time	T_{rr}	–	–	10	µs	C_{D1} = 100 nF
Reset Output RO1						
Reset switching threshold	V_{RT1}	4.5	4.65	4.8	V	–
	V_{RT1}/V_{Q1}	90	93	96	%	–
Reset threshold headroom	V_{R1HEAD}	200	350	500	mV	V_{Q1} - V_{RT1}
Reset output sink current	I_{RO1}	1.0	–	–	mA	V_{Q1} = 5.0 V; V_{Q2} = 5.0 V; V_{D1} = 0 V; V_{RO1} = 0.3 V
Reset output low voltage	V_{RO1L}	–	0.15	0.3	V	V_{Q1} ≥ 1 V I_{RO1} = 1 mA
Reset output high voltage	V_{RO1H}	4.5	–	–	V	$R_{RO1,ext}$ = 4.7 kΩ

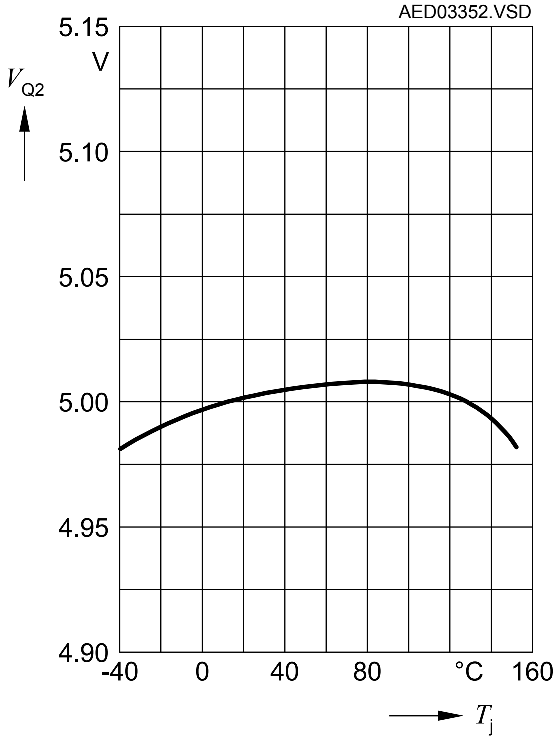
1) Drop voltage = V_I - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

Typical Performance Characteristics

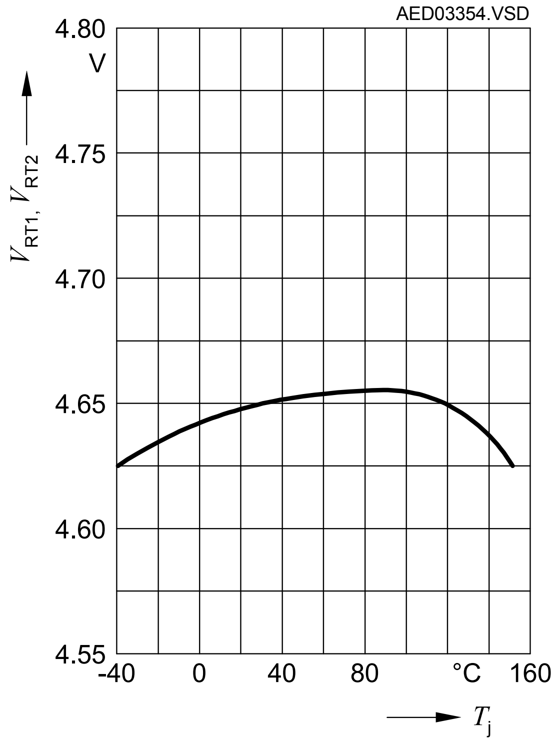
Output Voltage V_{Q2} versus Input Voltage V_I



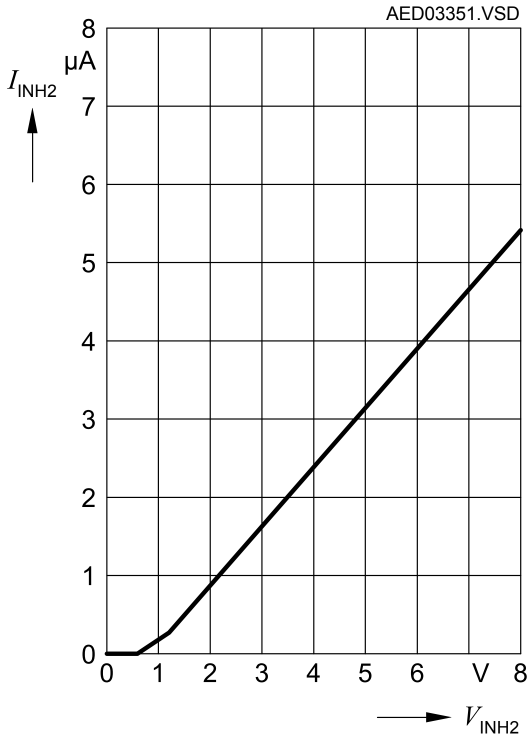
Output Voltage V_{Q2} versus Junction Temperature T_J



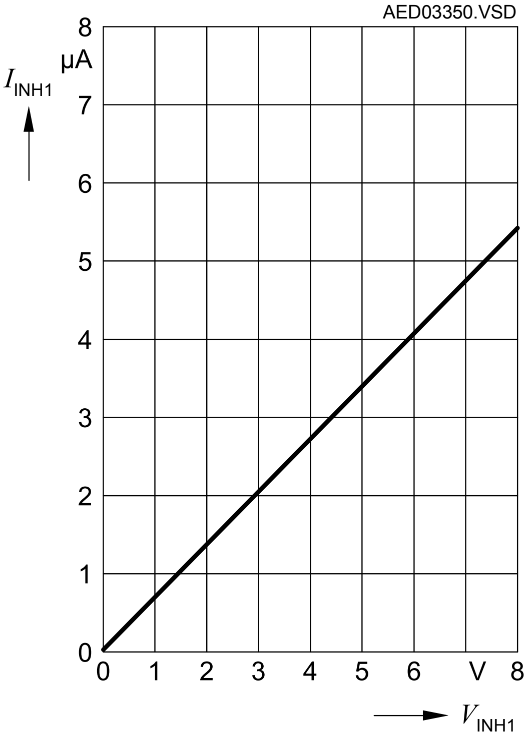
Reset Thresholds V_{RT1}, V_{RT2} versus Junction Temperature T_J



INH2 Input Current versus Inhibit Voltage



INH1 Input Current versus Inhibit Voltage



Package Outline

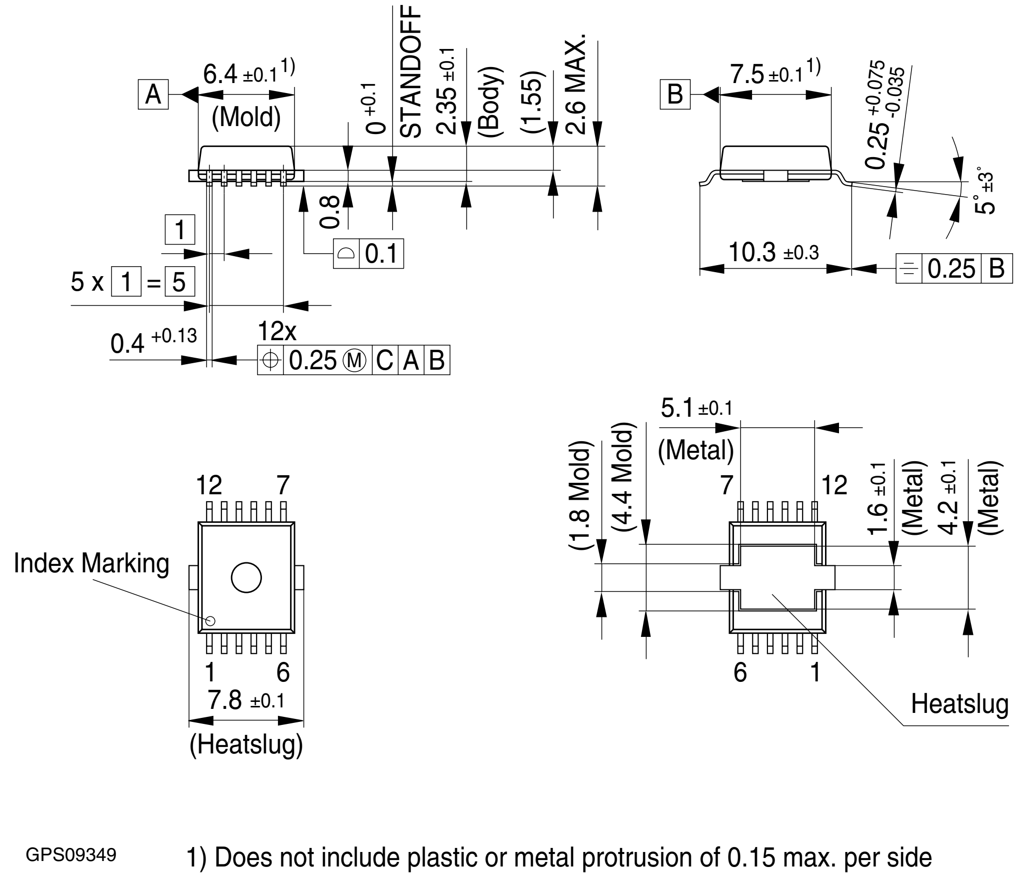


Figure 4 **PG-DSO-12-11** (Plastic Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our
Infineon Internet Page "Products": **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

Revision History

Version	Date	Changes
Rev. 1.2	2008-10-28	Modification according to PCN No. 2007-117-A: • **"Watchdog and Reset Timing D2" on Page 10**: Lower timing threshold V_{DL2}: Max limit change to 0.6V (was 0.5V) and typ. limit change to 0.45V (was 0.4V). The change does not impact watchdog or reset timing limits
Rev. 1.1	2007-12-19	Modification according to PCN No. 2007-117-A: • Page 9: Quiescent current I_q; inhibited (V_{INH1} = V_{INH2} = 0 V; T_j < 150 °C): Max. limit changed to 20µA (was 15µA).
Rev 1.0	2006-12-21	Initial version final datasheet

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