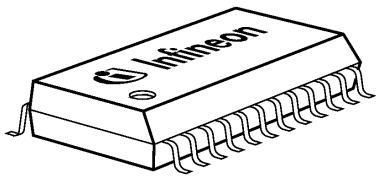
Quad Firing Airbag IC TLE 6714

Data Sheet

1 Overview



P-DSO-28-1

1.1 Features

- Four independent squib channels each consisting of a high- side & a low-side switch
- Thermal and short circuit protection for each switch
- Current limitation for each firing loop
- Firing current detection
- Voltage measurements
- Squib leakage detection to ground and to battery
- Precise squib resistance measurement with programmable gain
- Multiplexed analog output pin for measurement retrieval
- Unidirectional Serial Peripheral Interface (SPI)
- Security circuits and independent input signals included to prevent unwanted firing

1.2 Functional Description

This IC provides four independent actuator channels for firing loops in an safety restraint airbag system. Each channel is equipped with full diagnostic functions. Communication between the µC and Quad Firing Airbag IC is be performed via SPI and analog/digital interface pins.

Type	Ordering Code	Package
TLE 6714	on request	P-DSO-28-1

1.3 Pin Configuration

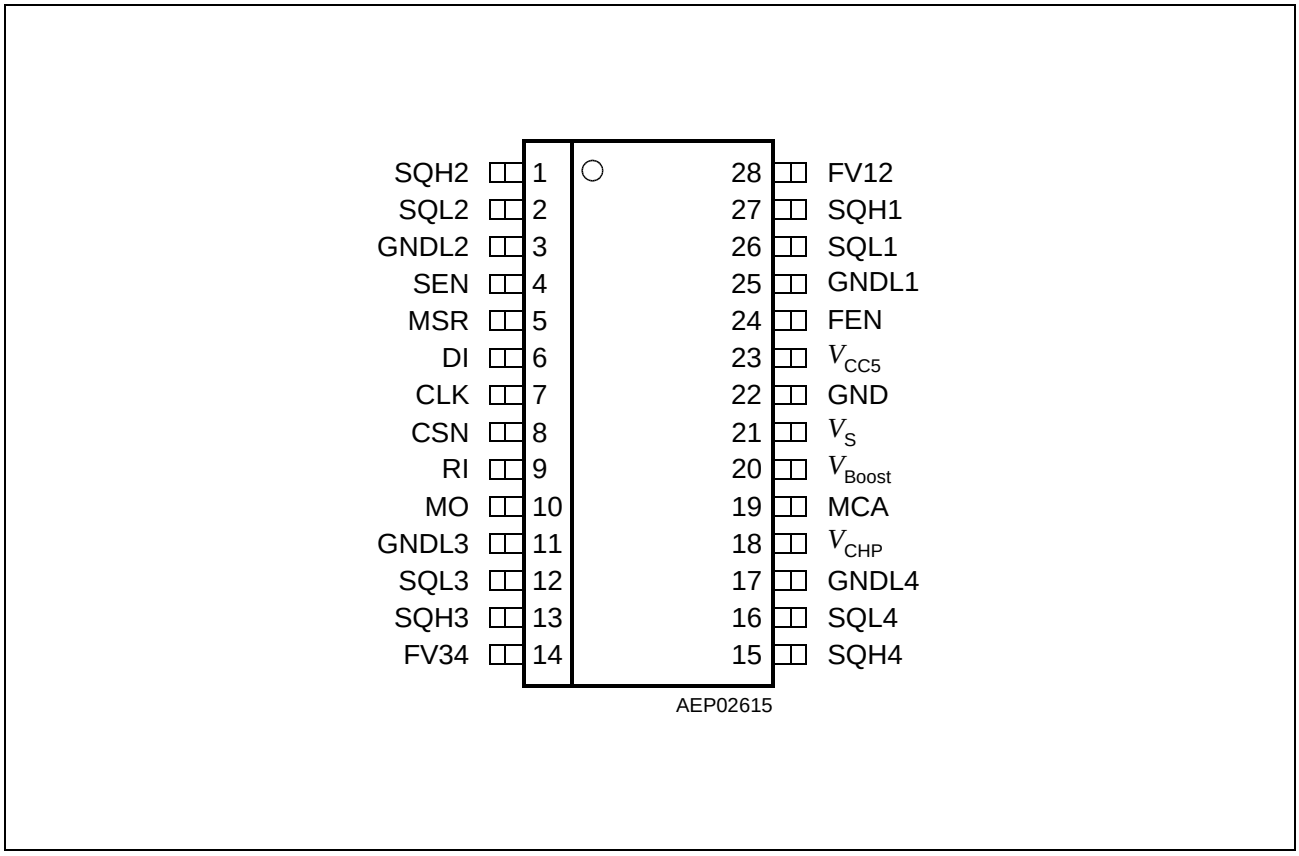


Figure 1 Chip Pin Configuration

1.4 Pin Definitions and Functions

Pin No.	Symbol	Function
1	SQH2	**Squib High-Side Driver for Firing Loop 2**; DMOS high-side switch output.
2	SQL2	**Squib Low-Side Driver for Firing Loop 2**; DMOS low-side switch input.
3	GNDL2	**Ground Terminal for Firing Loop 2**; directly connected to the ground terminal of the power reserve capacitor.
4	SEN	**Squib Enable**; input signal, that must be high during measurement and firing (see **Table 1** on page 9)
5	MSR	**Measurement Sense Resistor;** resistor to ground used for measurement current to voltage conversion (see **Figure 6**).
6	DI	**Serial Data Input**; receives data from the µC.
7	CLK	**Clock Input for SPI**.
8	CSN	**Chip Select Negative**; the device is selected if the input is low.
9	RI	**Reset In**; CMOS-level input. Logic high is needed for operation (see **Table 1** on page 9)
10	MO	**Measurement Output**; diagnostic pin for digital and analog measurements with an output range from 0 to 5 V (see **Figure 6**).
11	GNDL3	**Ground Terminal for Firing Loop 3**; directly connected to the ground terminal of the power reserve capacitor.
12	SQL3	**Squib Low-Side Driver for Firing Loop 3**; DMOS low-side switch input.
13	SQH3	**Squib High-Side Driver for Firing Loop 3**; DMOS high-side switch output.
14	FV34	**Firing Voltage Input for Loops 3 and 4**; input, directly connected to the boost supply voltage.
15	SQH4	**Squib High-Side Driver for Firing Loop 4**; DMOS high-side switch output.
16	SQL4	**Squib Low-Side Driver for Firing Loop 4**;DMOS low-side switch input.
17	GNDL4	**Ground Terminal for Firing Loop 4**; directly connected to the ground terminal of the power reserve capacitor.
18	V_{CHP}	**Supply Voltage for high side Gates**; Connection terminal to an external storage capacitor.V_{CHP} provides gate to source voltage for high side driver. If not connected $V_{CHP} = V_{Boost} - V_{Diode}$

1.4 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
19	MCA	**Measurement Current Adjust**; terminal to an external resistor R_{MCA} to ground, which determines the reference measurement current.
20	V_{Boost}	**Boost Power Supply Voltage**; input for the main supply voltage of the chip.
21	V_S	**Supply Voltage Input;** Battery voltage input
22	GND	**Ground Terminal**; provides ground reference for V_{CC5}, analog measurement block and digital logic.
23	V_{CC5}	**5 V Supply Input**
24	FEN	**Fire Enable**; CMOS-level input. Logic high voltage is required to activate the firing channels (see **Table 1** on page 9).
25	GNDL1	**Ground Terminal for Firing Loop 1**; directly connected to the ground terminal of the power reserve capacitor.
26	SQL1	**Squib Low-Side Driver for Firing Loop 1**;DMOS low-side switch input.
27	SQH1	**Squib High-Side Driver for Firing Loop 1**; DMOS high-side switch output.
28	FV12	**Firing Voltage Input for Loops 1 and 2**; input, directly connected to the boost supply voltage.

1.5 Block Diagram

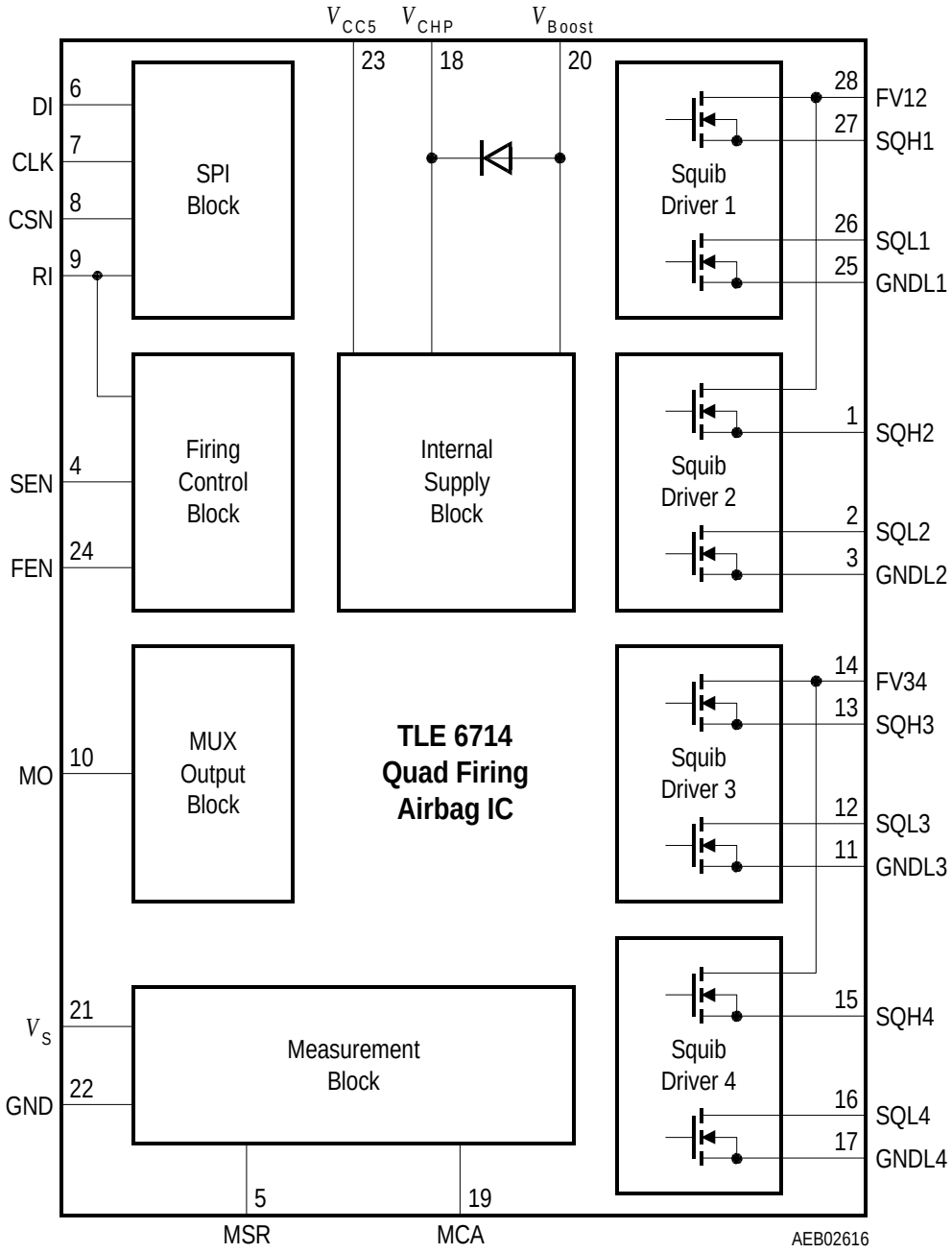


Figure 2 Block Diagram TLE 6714

2 Circuit Description

2.1 Internal Supply

Supply principles:

- The design of the internal supply is such that increasing or decreasing of the supply voltages V_{FV12}, V_{FV34}, V_{Boost}, V_{CHP}, V_S, V_{CC5} causes no unintended firing of the squibs.
- Losing the connection to one of the squib driver supply voltages V_{FV12} or V_{FV34} has no influence on the other squib driver function.
- Squib failures such as shorts to ground or battery do not have an influence on other chip functions.
- An open ground connection does not cause unwanted firing.

2.1.1 Logic Supply V_{CC5}

Input pin V_{CC5} is the 5 V logic supply for the Quad Firing Airbag IC.

2.1.2 Power Supply V_{Boost}

Input pin V_{Boost} is a supply voltage for the Quad Firing Airbag IC, that is generated by an external boost power supply. This Voltage is used for the firing circuits (V_{FV12}, V_{FV34}).

2.1.3 Supply Voltage for High Side Gates V_{CHP}

Input pin V_{CHP} is the supply for the high side DMOS Gates of the squib drivers. If V_{CHP} is not externally connected V_{CHP} is internally connected to V_{Boost} by a diode. This means that the high side switch has a higher voltage drop since the firing voltage is smaller than V_{CHP} in the case that $V_{FVxy} = V_{Boost}$.

2.2 Serial Peripheral Interface (SPI) and Decoder Logic

The SPI of the Quad Firing Airbag IC is controlled by three input pins: CSN, DI and CLK.

The Chip Select Negative pin CSN allows the individual selection of different slave SPI devices. Slave devices that are not selected do not interfere with SPI bus activities. A slave device will be selected by a low signal on pin CSN.

The Data Input pin DI is used for the serial data from the µC, synchronously clocked by the Clock input pin CLK.

All commands, no matter which function, consist of 16 Bits, therefore the airbag IC SPI consists of a 16 Bit input shift register, a 16 Bit latch and a decoder logic block for the generation of the SPI command signals.

To provide higher security and to suppress data transfer errors in the event that the clock signal includes spikes or glitches, a counter for 16 clock cycles is provided. Only if 16 clock cycles have occurred, the rising edge of CSN causes an internal signal LE (Latch

Enable) to transfer the data from the shift register to the 16 Bit latch. A logic block decodes the 16 Bit word of the latch to address the desired functional block.

The transfer of a 16 Bit command word starts with the falling CSN signal. At this time the CLK signal must be high. The DI signal must be valid during rising edge of the CLK signal. The transmission ends after the 16th rising edge of CLK and when the CSN signal becomes high again. The left side of **Figure 3** shows a correct transmission of a 16 Bit command. On the right side you can see a incorrect transmission. CSN signal returns high too late. A clock failure occurs and all latched data is be disregarded.

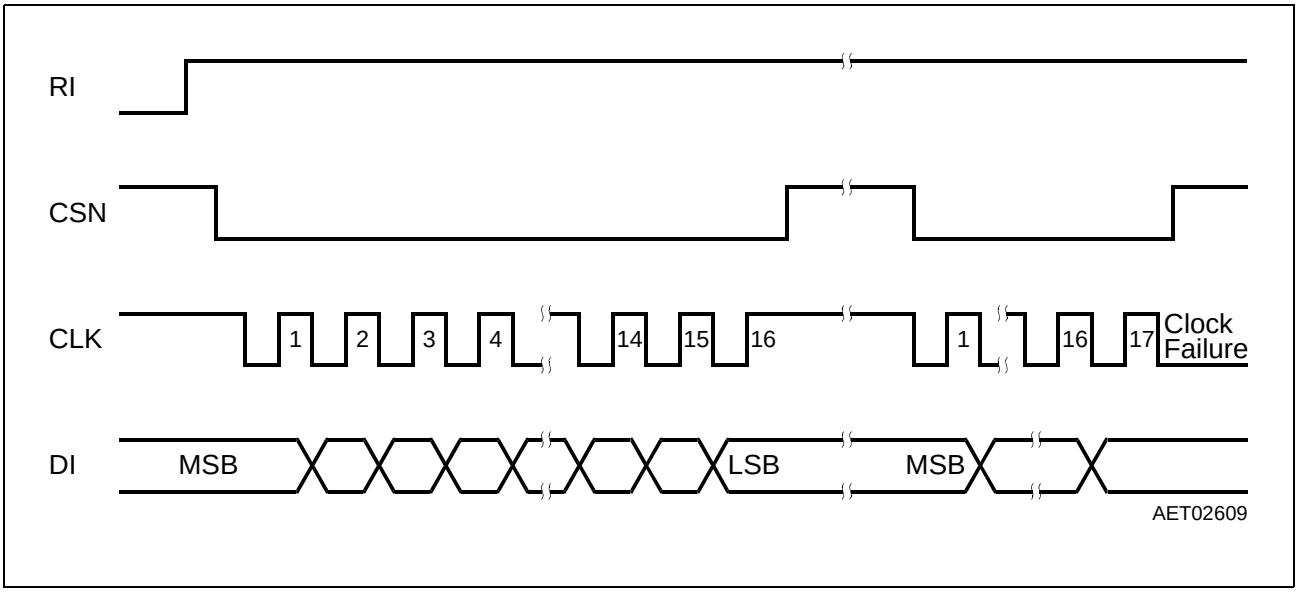


Figure 3 Timing of the Serial Peripheral Interface (SPI)

2.3 Squib Drivers

The Quad Firing Airbag IC includes four independent driver circuits. Every driver circuit consists of a high and a low-side DMOS switch. Between these switches a squib can be connected in series.

The four driver circuits are designed as follows. The Drain of the high-side switch is connected to the Firing Voltage pin (FVxy (xy=12, 34)) and its source is connectedto the output pin squib high-side x (SQHx (x=1, 2, 3, 4)). The drain of the low-side switch is connected to the input pin squib low-side x (SQLx (x=1, 2, 3, 4) and the source is connected to the Ground pin for the firing Loop (GNDLx (x=1, 2, 3, 4)). This is illustated in **Block Diagram Squib Driver Circuit** on page 8.

The squib will only be fired if all of the following signals are present: SPI firing command, RI, FEN, and SEN.
RI, FEN (Firing Enable) and SEN are external inputs which must be HIGH to enable firing. When activating the low-side transistor the firing current will be sensed and latched for all four squibs. If the current exceeds the firing current detection level, a bit will be set and latched. This bit will then be read out at pin MO by the micro controller after the SPI

command firing current detection (see **Chapter 3.5 DXXX$_H$: Channel Selection for High Current Detection**) is sent. If the programed channel has fired, the MO pin has low output voltage. All the latches will be reset when the special SPI command (FFFF$_H$ or DXXX$_H$ see **Chapter 3**) is sent or when the device is reset via external pin RI = low.

The gate of the high-side transistor is supplied via pin V_{CHP}. If V_{CHP} is not provided with an external charge pump voltage, the gates will be supplied by V_{Boost} by a diode.
To protect the integrated squib firing transistors in the event that the junction exceeds critical temperature, a thermal shutdown circuit is provided for each transistor. This feature prevents catastrophic failures from accidental device overheating.

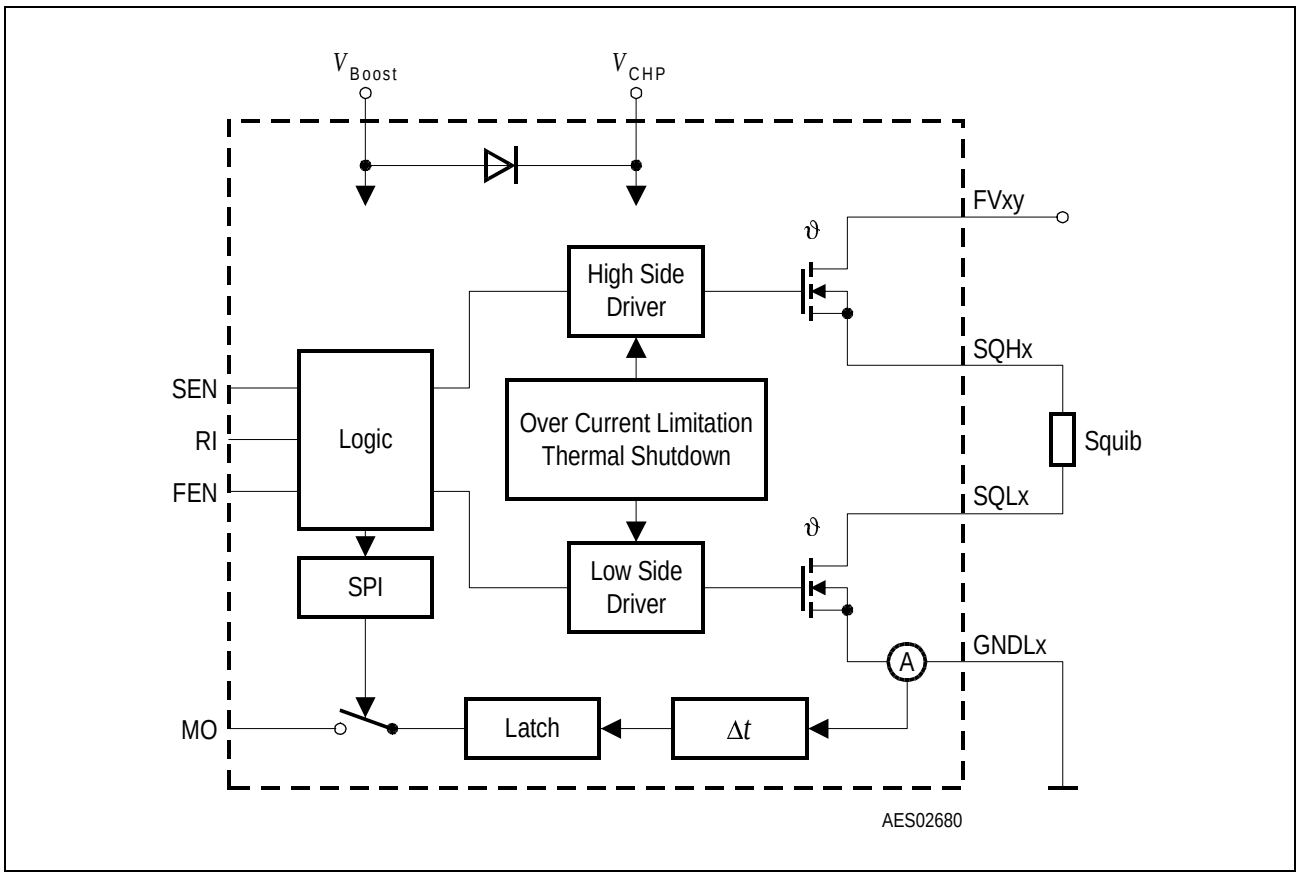
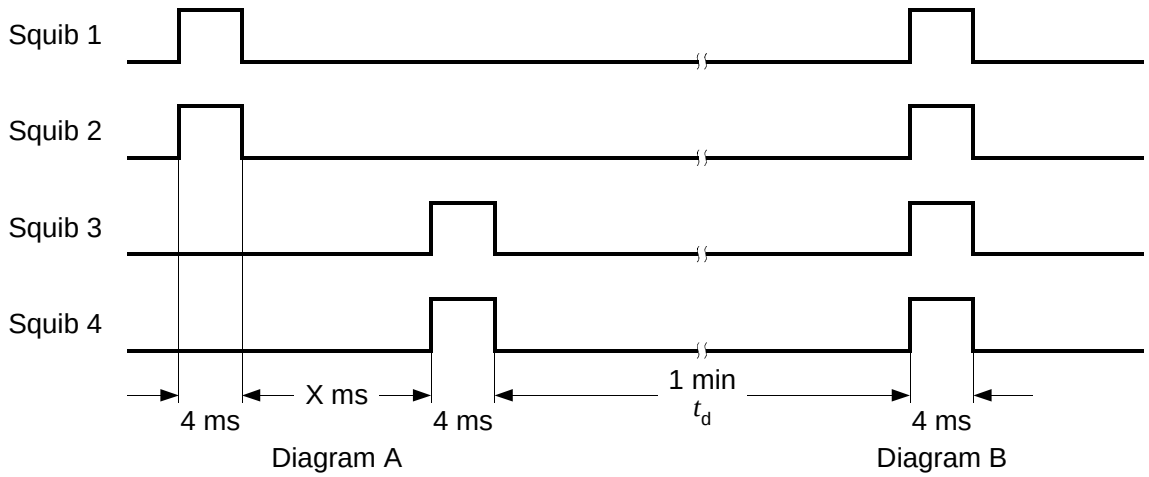


Figure 4 Block Diagram Squib Driver Circuit



Time delay between deployment of squibs 1, 2 and squibs 3, 4 can vary from 0 ms to infinity.

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Figure 5 Squib Firing On/Off-Timing Characteristics

Table 1 Functional Table of the Squib Drivers for Firing and Testing

RI	SEN	FEN	SPI: LSx	SPI: HSx	State LSx	State HSx	Function
0	x	x	x	x	OFF	OFF	Disable all drivers for all modes
1	0	x	x	x	OFF	OFF	NO firing
1	x	0	x	x	OFF	OFF	NO firing
1	1	0	OFF	ON	OFF	ON	Activation of HSx for measurements
1	1	0	ON	OFF	ON	OFF	Activation of LSx for measurements
1	1	0	ON	ON	OFF	OFF	Cannot activate both HSx and LSx together
1	1	1	ON	ON	ON	ON	Firing
1	1	1	ON	OFF	ON	OFF	Firing of LS
1	1	1	OFF	ON	OFF	ON	Firing of HS

LSx Low-side switch of the squib driver loop x (x = 1, 2, 3, 4)

HSx High-side switch of the squib driver loop x (x = 1, 2, 3, 4)

FEN/SEN Security function firing and squib enable input: 0 = Firing not allowed; 1 = Firing allowed

RI Reset input: 0 = All actions are deactivated and set to default; 1 = Firing or measurements allowed

2.4 Measurements

2.4.1 Squib Resistance Measurement

The squib resistance measurement module consists of several circuits and can be addressed by the SPI commands $4XXX_H$, $6XXX_H$ and $7XXX_H$.

2.4.1.1 Precise Squib Resistance Measurement with the SPI Command $4XXX_H$ and $6XXX_H$

For a precise measurement the commands $4XXX_H$ and $6XXX_H$ are used.
With the command $4XXX_H$, two bias point measurements can be done. The combination of the other two measurement eleminates the offset voltages of the OpAmp. The command activates a bias current source of I_{Bias} = 5 x I_{MCA}. This current flows through pin SQLx over the external resistor R_{MSR} (Measurement Sense Resistor) to ground. The pin SQLx is regulated to 8 V with the bias current.
The first measurements are used to eliminate the offset of OpAmp 1. Therefore bit b3 must be set to 0 and b2 to 0 (gain of OpAmp 1 is set to A_1 = 10) or bit 3 to 0 and bit 2 to 1 (gain A_1 = 30), see **Chapter 3.4.1**. Both inputs of the OpAmp 1 are set to its bias point of 8 V, so that no current flows through the squib. The offset voltage V_{IO1} of OpAmp 1 is amplified with the chosen gain factor A_1 and reported to pin MO (Measurement Out), this is illustrated in **Figure 6**.

I) 10: $V_{MO1} = (0.89 \times V_{CC5}) - V_{IO1} \times A_1$
30: $V_{MO1} = (0.86 \times V_{CC5}) - V_{IO1} \times A_1$

V_{IO1} offset voltage of OpAmp 1
A_1 gain of OpAmp 1 (10 or 30)

The second measurement is done by the µC A/D converter connected to the MSR pin to determine the measurement current.

II) $V_{MSR1} = I_{Bias} \times R_{MSR}$

With the next two measurements the precise evaluation of the squib resistance will be completed. In this casethe SPI command $6XXX_H$ is used. The command $6XXX_H$ activates the second measurement current I_{Main}. This current, I_{Main} = M x I_{MCA} (M = 16, 32 or 40 (set by the bits b6 and b5) see **Chapter 3.4.1**) flows through the squib resistance. At the pin SQLx the currents I_{Bias} and I_{Main} are added and flow together through the resistor R_{MSR} to ground.

For the third measurement bit b3 must be set to 0 and b2 to 0 (gain of OpAmp 1 is set to A_1 = 10) or bit 3 to 0 and bit 2 to 1 (gain A_1 = 30).The OpAmp 1 now reports the voltage drop across the squib including the offset voltage to the MO pin.

III) $V_{MO2} = V_{MO1} - I_{Main} \times R_{Squib} \times A_1$

V_{IO1} offset voltage of OpAmp 1

A_1 gain of OpAmp 1 (10 or 30)

Now the µC measures the sum of I_{Bias} and I_{Main}.

IV) $V_{MSR2} = (I_{Main} + I_{Bias}) \times R_{MSR}$

With the result of these four measurements the µC is able to calculate the precise resistance of the squib with the following equations:
Transforming equation III) to R_{Squib}:

V) $$R_{Squib} = \frac{V_{MO1} - V_{MO2}}{A_1 \times I_{Main}}$$

Transfoming equation IV) to I_{Main}:

VI) $$I_{Main} = \frac{V_{MSR2}}{R_{MSR}} - I_{Bias}$$

Combining equation V) and VI) gives:

VII) $$R_{Squib} = \frac{V_{MO1} - V_{MO2}}{A_1 \times \left(\frac{V_{MSR2}}{R_{MSR}} - I_{Bias} \right)}$$

Transforming equation II) to I_{Bias}:

VIII) $$I_{Bias} = \frac{V_{MSR1}}{R_{MSR}}$$

Equation VIII) in VII):

IX) $$R_{Squib} = \frac{V_{MO1} - V_{MO2}}{A_1 \times \left(\frac{V_{MSR2}}{R_{MSR}} - \frac{V_{MSR1}}{R_{MSR}} \right)}$$

The gain of measurement one and three of OpAmp1 have to be the same, the equation becomes:

X) $$R_{Squib} = \frac{R_{MSR}}{A_1} \times \frac{V_{MO1} - V_{MO2}}{V_{MSR2} - V_{MSR1}}$$

During these four measurements the pin MCA is set to V_{CC5} (see **Figure 6**). The current I_{MCA} is calculated as follows: $I_{MCA} = V_{CC5}/R_{MCA}$

The ratio between the resistances R_{MSR} and R_{MCA} must be set to a value that allows OpAmp3 to regulate pin SQLx to the voltage of 8 V.

The following resistor values are recommended:

R_{MCA} = 4 kΩ - 6 kΩ and
R_{MSR} = 50 Ω

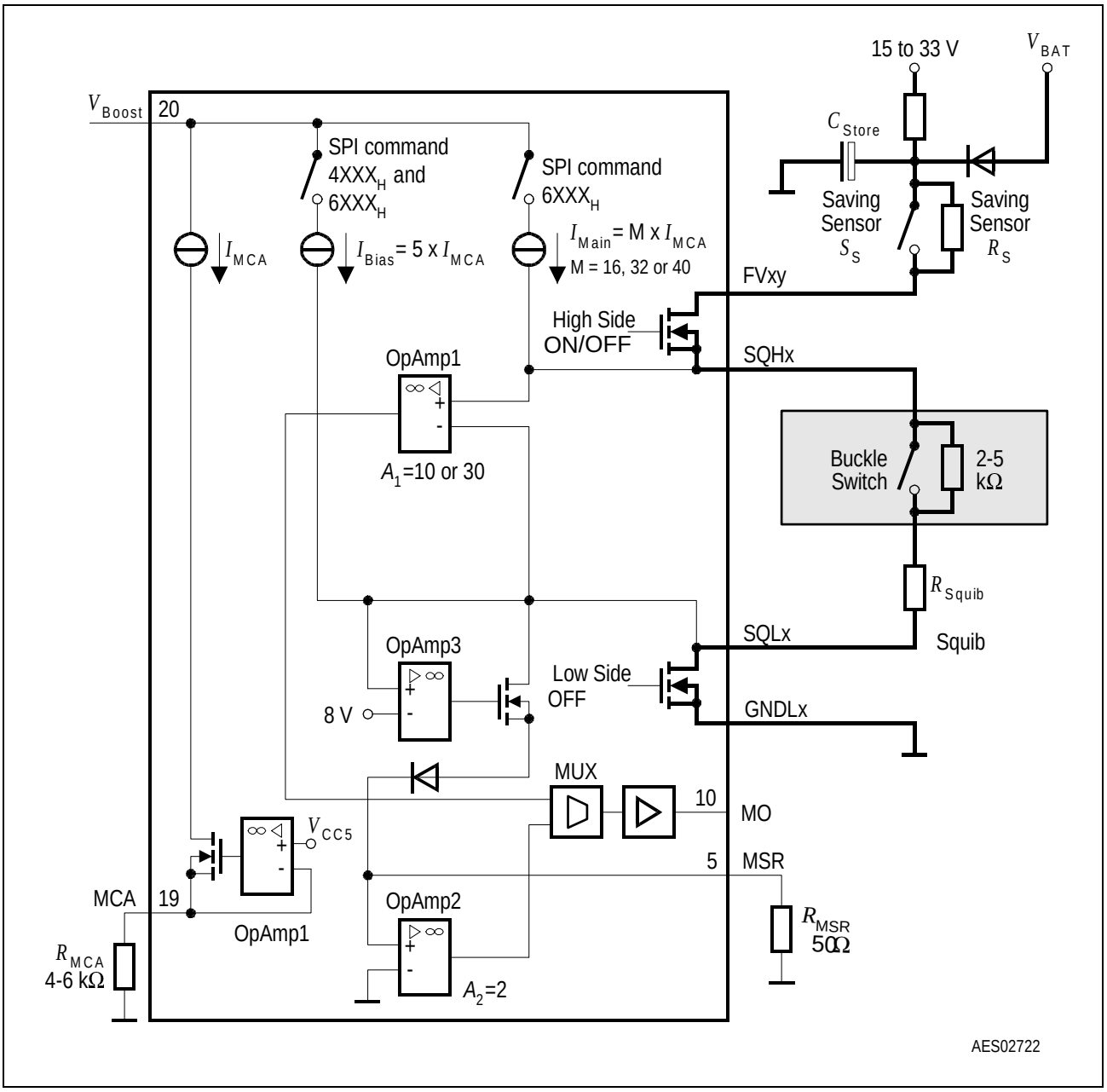


Figure 6 Precise Squib Resistance Measurement: Functional Schematic

2.4.1.2 Squib Measurement with Safing Sensor and Buckle Switch

There is another way to measure R_{Squib}, if a mechanical safing sensor (S_S) with a resistor (R_S) are used in parallel. Instead of activating the higher measurement current the high-side switch of a squib driver can be switched on via SPI: 7XXX$_H$. Now a current determined by the resistor R_S flows through the squib and is reported to MO and MSR.

For buckle switch measurement, an amplifier with a fixed gain of 2 is provided for applications where a buckle switch with an internal 2 kΩ to 5 kΩ resistor in parallel is connected in series with the pretension squib. To detect a broken/failed buckle switch,

the result of the gain 10/30 amplifier is out of range. To measure the seat belt switch resistance the voltage drop across pin MSR is multiplied by two and is reported to pin MO. Furthermore, voltage on pin SQHx can be measured to provide the diagnostics of the buckle switch (see **Figure 6**).

The measurement for each squib is activated separately, but the analog output signals on pins MO and MSR are common.

The pins MO and MSR of several ASICs can be connected together. Therefore the external resistor on pin MSR is only used once and is common for all IC's.

2.4.2 Squib Leakage Measurement

The leakage resistance measurement circuit can be addressed by the SPI command $1XXX_H$ (see **Chapter 3.4.4**). The programmed current for the leakage measurement I_{MCA} is derived from a 1:1 current mirror to I_{LL} and I_{LH}. During leakage resistor measurement, the pin MCA will be regulated to $V_S/3$. The measurement current will be calculated as $I_{MCA} = V_S / (3 \times R_{MCA})$. As menioned in the squib resistance description, the resistor R_{MCA} is fixed at 4 kΩ to 6 kΩ. This functional block is illustrated in the **Figure 7**.

$$I_{MCA} = \frac{V_S}{3 \times R_{MCA}} = I_{LL} = I_{LH}$$

(I_{LL} is the leakage to ground and I_{LH} is the leakage to battery)

The voltage drop V_{LL} across the leakage resistor R_{LL} is the drop between pin SQHx and ground. V_{LL} is calculated as follows:

$$V_{LL} = I_{LL} \times R_{LL} = \frac{V_S}{3 \times R_{MCA}} \times R_{LL}$$

The voltage drop V_{LH} across the leakage resistor R_{LH} is the drop between pin SQHx and V_S. V_{LH} is calculated as follows:

$$V_{LH} = I_{LH} \times R_{LH} = \frac{V_S}{3 \times R_{MCA}} \times R_{LH}$$

If the voltage drop across leakage resistance to ground or the drop to V_S falls below a quarter of V_S the window comparator is switched by the leakage and reports it to pin MO.

$$V_{LL} \leq \frac{1}{4} V_S$$

$$V_{LH} \leq V_S - \frac{3}{4} V_S = \frac{1}{4} V_S$$

As both voltages drop across the leakage resistors (R_{LL}, R_{LH}) are the same, the calculation is only shown for R_{LL}.

$$\frac{1}{4}V_S = I_{LL} \times R_{LL} = \frac{V_S}{3 \times R_{MCA}} \times R_{LL}$$

$$R_{LL} = R_{LH} = \frac{3}{4}R_{MCA}$$

If R_{LL} or R_{LH} falls below this value a leakage will be reported.

Two comparators, which are referenced to 1/4 x V_S and 3/4 x V_S, determine the leakage to ground or leakage to a higher voltage. This is transmitted as either an analog or digital data to the µC depending on the SPI command. The following table summarizes the possible output of the leakage measurement.

To prevent jitter on the output pins a hysteresis of 1/48 x V_S is provided in both comparators.

	Voltage on MO	
Output (MO)	Digital Output (b3 = 0)	Analog Output (b3 = 1)
Leakage to ground	0 V	0 V
Leakage to battery	0 V	V_{CC5}
No leakage	V_{CC5}	V_{CC5}/2

Leakage resistance malfunction can be simulated in a test mode by switching on only the squib driver high-side transistor for a leakage to battery, as well as by switching on only the low-side transistor for a leakage to ground, by SPI command $CXXX_H$ (see **Chapter 3**). Furthermore, cross coupling between squibs can be detected by activating a leakage measurement command $CXXX_H$ and switching on the DMOS of an adjacent channel, one after the other.

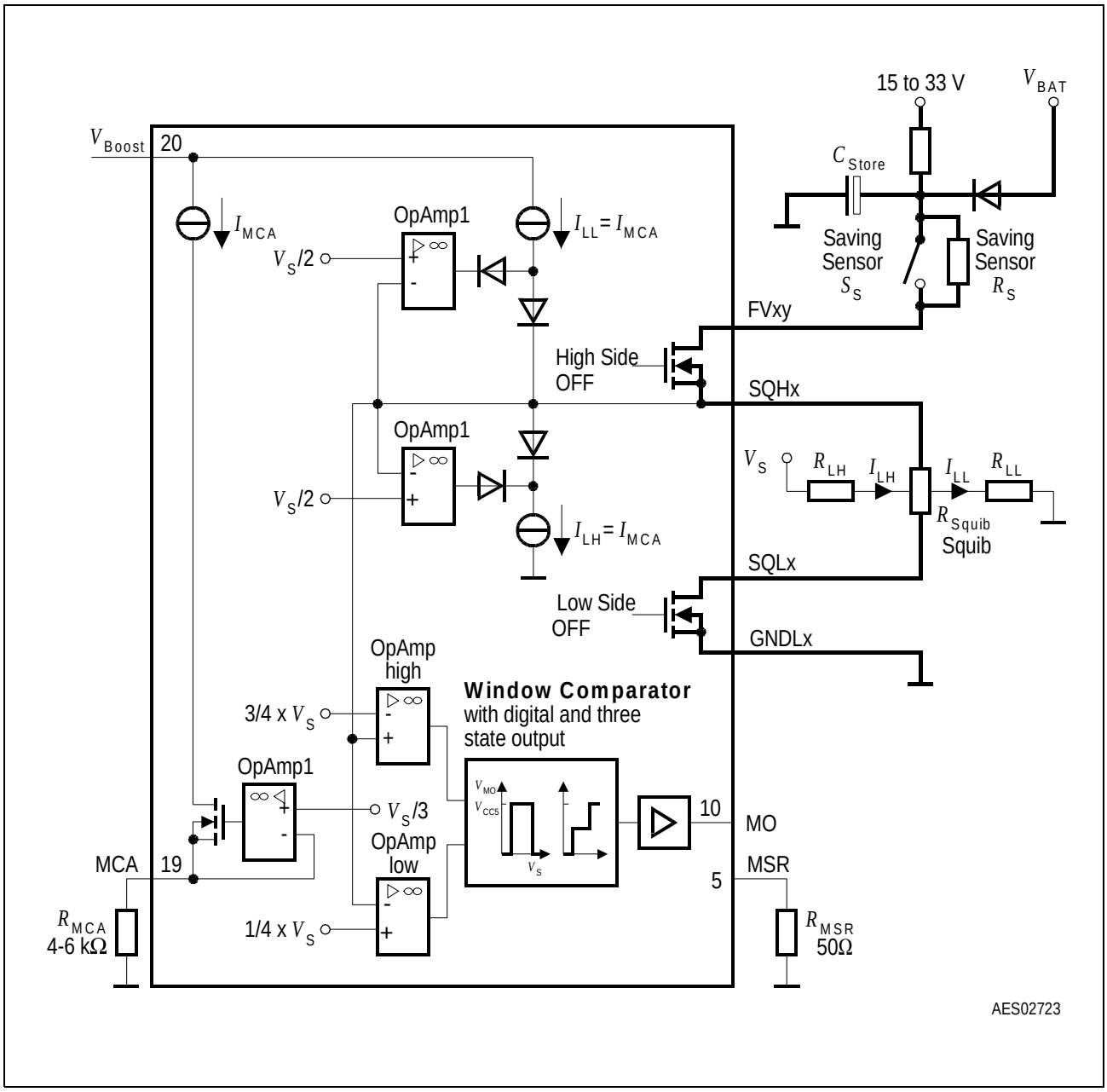


Figure 7 Squib Leakage Measurement

2.4.3 Supply and Pin Voltage Measurements

With SPI commands $1XXX_H$ (see **Chapter 3.4.4**) different voltage measurements can be activated. The result of the measurement will be reported to the analog output pin MO. Because the MO pin has a voltage range between 5 V and ground, the measured voltages will be divided by a factor, depending on which voltage is measured. The table below shows the divider factor for the different voltages.

Name of the Measured Voltage	MO Voltage / Measured Voltage
V_S	1/5
V_{Boost}, V_{CHP}, FVxy (xy = 12, 34), SQHx (x = 1, 2, 3, 4)	1/8
FEN, SEN	1/1

The internal reference voltage V_{REF} can be measured by addressing the SPI command REFH and REFL.

Name of the Measured Voltage	MO Voltage / Measured Voltage
REFH ($AAAA_H$): 0.56 x V_{CC5}	1/1
REFL (5555_H): (V_{REF} x V_{CC5})	1/5

2.5 Grounding Requirements for External Components on PCB

The external components for the following pins to ground are necessary to be grounded to pin GND. The connections must be low ohmic and without any voltage shift to the ground pin GND.

Critical pins: MO, MSR, MCA

3 SPI Commands

3.1 General Information on SPI Command Structure

All functions e.g. 'Firing' or 'Measurement' are controlled by a 16 Bit instruction command. The 16 Bit word consists of two bytes (8 Bit) which are decoded by the decoder logic circuit. The Quad Firing Airbag IC has latcherd and not latched commands.

After a hardware reset all internal control registers and decoded signals are reset to its default value. The default settings are, that all squib drivers are off and all measurements are deactivated. The IC can although be set to the default values by the SPI command $FFFF_H$.

Byte A: Function Byte								**Byte B: Selection Byte**							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
MSB							LSB	MSB							LSB

Function Byte	
a0	Indicates valid control command
a1...a3	Control bits
a4...a7	SPI command bits

Selection Byte	
b0...b3	Channel selection/firing and test commands
b4...b6	Switch or measurement selection
b7	Not used except firing and test commands
In case of firing command	
b0...b7	Selects the squib driver transistors, all combinations are allowed.

3.2 Summary of SPI Commands

Code (hex)	Name	Short Description
$0XXX_H$	NO MEAS	All actions deactivated, but latches are not affected *This command is recommended to be used as a no-op command.*
$1XXX_H$	MSUPL	Measurement of the supply voltages, FEN, SEN and squib leakage measurement with squib switches in OFF state (**Chapter 3.4.4**)
$2XXX_H$		Not used
$3XXX_H$	MFSUP	Firing voltage measurement command (**Chapter 3.4.2**)
$4XXX_H$	RES5	Resistance measurement ‘reference current’ active (**Chapter 3.4.1**)
5555_H	REFL	Reference test mode command (**Chapter 3.8**)
$6XXX_H$	RES40	Resistance measurement ‘main current’ active by programming the MAIN current and ‘reference current’ active (**Chapter 3.4.1**)
$7XXX_H$	RES5H	Resistance measurement with ‘activated high-side switch and ‘reference current’ active (**Chapter 3.4.1**)
$8XXX_H$	FIRE	Firing command (**Chapter 3.3**)
$9XXX_H$		Not used
$AAAA_H$	REFH	Reference test mode command (**Chapter 3.7**)
$BXXX_H$		Not used
$CXXX_H$	MSQL	Squib leakage measurement command with one of eight squib switches in ON state (**Chapter 3.4.3**)
$DXXX_H$	FIREDET	Read out of firing current detection latches and clearing them (**Chapter 3.5**)
$EXXX_H$		Reserved for test only.
$FFFF_H$	RESET	Reset by SPI command. All actions are deactivated and clear all latches for firing detection (**Chapter 3.6**)

3.3 8XXX$_H$: Firing Commands

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
1	0	0	0	x	x	x	x	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

bx	Squib Driver Switch Selection
b7 = 1	High-Side Switch of squib 4 active
b6 = 1	High-Side Switch of squib 3 active
b5 = 1	High-Side Switch of squib 2 active
b4 = 1	High-Side Switch of squib 1 active
b3 = 1	Low-Side Switch of squib 4 active
b2 = 1	Low-Side Switch of squib 3 active
b1 = 1	Low-Side Switch of squib 2 active
b0 = 1	Low-Side Switch of squib 1 active

Valid control signals on the external enable pins are required to activate the high-side switch and/or low-side switch (SEN = 1 and FEN = 1 and RI = 1).
All combinations of high & low side switches are allowed.

3.4 Measurement

Below you can find all measurements of the IC. The necessary external signals are listed at the end of this chapter.

3.4.1 Squib Resistance Measurement Commands

4XXX$_H$: Resistance Measurement 'Bias Current' Active
V_{MCA} voltage source switched to V_{CC5}

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
0	1	0	0	x	x	x	x	x	x	x	x	0/1	0/1	0/1	0/1

Settings of bit b3 to b0, see table below.

6XXX$_H$: Resistance Measurement 'Main Current' and 'Bias Current' Active

V_{MCA} voltage source switched to V_{CC5}

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
0	1	1	0	x	x	x	x	x	0/1	0/1	x	0/1	0/1	0/1	0/1

Settings of bit b6, b5 and b3 to b0, see table below.

7XXX$_H$: Resistance Measurement with 'Activated High-Side Switch' and 'Reference Current' Active

V_{MCA} voltage source switched to V_{CC5}

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
0	1	1	1	x	x	x	x	x	x	x	x	0/1	0/1	0/1	0/1

Settings of bit b3 to b0, see table below.

b6, b5: Main current level selection

b6	b5	Channel Selection
0	1	MAIN current set to 16 x I_{MCA} mA
1	0	MAIN current set to 32 x I_{MCA} mA
1	1	MAIN current set to 40 x I_{MCA} mA
0	0	MAIN current set to 40 x I_{MCA} mA

b3, b2: Selection of additional functions

b3	b2	Additional Function Selection
0	0	Gain 10 amplifier [$-\Delta V_{MO}/\Delta(V_{SQHx} - V_{SQLx}) = 10$] (x = 1, 2, 3, 4) switched to MO pin
0	1	Gain 30 amplifier [$-\Delta V_{MO}/\Delta(V_{SQHx} - V_{SQLx}) = 30$] (x = 1, 2, 3, 4) switched to MO pin
1	0	Gain 2 amplifier [$-\Delta V_{MO}/\Delta V_{MSR} = 2$] switched to MO pin
1	1	Squib voltage to MO [$V_{SQHx} = 8 \times V_{MO}$] (x = 1, 2, 3, 4) switched to MO pin

b1, b0: Channel select

b1	b0	Channel Selection
0	0	Resistance measurement channel 1
0	1	Resistance measurement channel 2
1	0	Resistance measurement channel 3
1	1	Resistance measurement channel 4

3.4.2 $3XXX_H$: Firing Voltage Measurement Commands

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	1	1	x	x	x	x	x	x	x	x	x	x	0/1	0/1

b1, b0: Channel select

b1	b0	Channel Selection
0	0	Firing voltage V_{FV12} measurement channel 1 active and switched to MO pin
0	1	Firing voltage V_{FV34} measurement channel 3 active and switched to MO pin

3.4.3 $CXXX_H$: Squib Leakage Measurement Commands with One of Four Squib Switches in ON-State

V_{MCA} voltage source switched to $V_S/3$

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
1	1	0	0	x	x	x	x	x	1/0	1/0	1/0	1/0	x	0/1	0/1

b6...b4: HS-/ LS-switch selection

b6	b5	b4	HS-/ LS-Switch Selection
0	0	0	Low-Side Switch of squib 1 active
0	0	1	Low-Side Switch of squib 2 active
0	1	0	Low-Side Switch of squib 3 active
0	1	1	Low-Side Switch of squib 4 active
1	0	0	High-Side Switch of squib 1 active
1	0	1	High-Side Switch of squib 2 active
1	1	0	High-Side Switch of squib 3 active
1	1	1	High-Side Switch of squib 4 active

b3: Channel select

b3	Channel Selection
0	Leakage measurement - Digital output to MO
1	Leakage measurement - Analog output to MO

b1, b0: Channel select

b1	b0	Channel Selection
0	0	Leakage measurement channel 1 active, V_{MCA} voltage source switched to $V_S/3$
0	1	Leakage measurement channel 2 active, V_{MCA} voltage source switched to $V_S/3$
1	0	Leakage measurement channel 3 active, V_{MCA} voltage source switched to $V_S/3$
1	1	Leakage measurement channel 4 active, V_{MCA} voltage source switched to $V_S/3$

3.4.4 $1XXX_H$: Supply Voltage-, Squib Leakage Measurement with Squib Switches in OFF-State Commands

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	1	x	x	x	x	x	1/0	1/0	1/0	1/0	1/0	0/1	0/1

b3: Select digital or analog output from window comparator to measurement output MO

b3	Channel Selection
0	Leakage measurement - Digital output to MO
1	Leakage measurement - Analog output to MO

b2: Leakage measurement active or inactive, b1, b0: Channel select

b2	b1	b0	Channel Selection
1	0	0	Leakage measurement channel 1 active, V_{MCA} voltage source switched to $V_S/3$
1	0	1	Leakage measurement channel 2 active, V_{MCA} voltage source switched to $V_S/3$
1	1	0	Leakage measurement channel 3 active, V_{MCA} voltage source switched to $V_S/3$
1	1	1	Leakage measurement channel 4 active, V_{MCA} voltage source switched to $V_S/3$
0	x	x	Leakage measurement INACTIVE. Voltage measurements can be selected

b6...b4: Select voltage measurement (b2 = 0)

Name	b6	b5	b4	Select Voltage Measurement
MV_{Boost}	0	0	0	V_{Boost} voltage measurement active and connect to pin MO (ratio 8:1)
MV_{CHP}	0	0	1	V_{CHP} voltage measurement active and connect to pin MO (ratio 8:1)
MV_{FEN}	0	1	0	V_{FEN} voltage measurement active and connect to pin MO (ratio 1:1)
MV_S	0	1	1	V_S voltage measurement active and connect to pin MO (ratio 5:1)
MV_{SEN}	1	0	0	SEN voltage measurement active and connect to pin MO (ratio 1:1)
Not used	1	0	1	X
Not used	1	1	0	X
Not used	1	1	0	X

Truth table for the squib measurements

RI	SEN	FEN	SPI: LSx	SPI: HSx	State LSx	State HSx	Function
0	x	x	x	x	off	off	Disable all drivers for all modes
1	1	0	off	on	off	on	Allowed to activate HSx for tests
1	1	0	on	off	on	off	Allowed to activate LSx for tests
1	1	0	on	on	off	off	Cannot activate both HSx and LSx together
1	0	0	x	x	off	off	x
1	0	1	x	x	off	off	x

LSx Low-side switch of the squib driver (x = 1, 2, 3, 4)

HSx High-side switch of the squib driver (x = 1, 2, 3, 4)

FEN Safing function Firing Enable input: 0 = Firing not allowed
1 = Firing allowed

3.5 DXXX$_H$: Channel Selection for High Current Detection

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
1	1	0	1	x	x	x	x	x	x	x	x	1/0	1/0	0/1	0/1

b3,b2: current detect and clear, b1, b0: Channel selection

b3	b2	b1	b0	Channel Selection
1	0	0	0	High current detection on channel 1 active, MO switched to latched bit for channel 1
1	0	0	1	High current detection on channel 2 active, MO switched to latched bit for channel 2
1	0	1	0	High current detection on channel 3 active, MO switched to latched bit for channel 3
1	0	1	1	High current detection on channel 4 active, MO switched to latched bit for channel 4
0	1	0	0	Clear current detection latch on channel 1
0	1	0	1	Clear current detection latch on channel 2
0	1	1	0	Clear current detection latch on channel 3
0	1	1	1	Clear current detection latch on channel 4

3.6 FFFF$_H$: Reset by SPI Command

By applying this command, the SPI-decoder is reset to its default state.

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: This command also clears all four latches for high current detection.

3.7 AAAA$_H$: Reference Test Mode Command REFH

If RI = 0 is generated, then the test mode is interrupted and the SPI-decoder is reset.

After activating the ‘Reference Test Mode’ the internally generated voltage reference of (2.72 x V_{VCC5}/5) V is reported to the pin MO.

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

3.8 5555$_H$: V_{REF} Reference Test Mode Command REFL

If RI = 0 is generated, then the test mode is interrupted and the SPI-decoder is reset.

After activating the voltage of V_{REF} as a 'Reference Test Mode’ the internally generated voltage reference of ($0{,}35$ x V_{CC5}/5) V is reported to the pin MO.

Byte A: Function Byte								Byte B: Selection Byte							
a7	a6	a5	a4	a3	a2	a1	a0	b7	b6	b5	b4	b3	b2	b1	b0
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

T_j = -40 to 150 °C

Pos	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
	Supply Pins					
1.1	Voltage	V_S, V_{Boost}, V_{FV12}, V_{FV34}, V_{CHP}, V_{CC5}	-0.3 -0.3 -0.3 -0.3	40 40 44 6.8	V	
1.2	Current	I_S	-30	3	mA	
	Squib Driver Pins					
1.3	Voltage	V_{SQHx}, V_{SQLx}, (x = 1, 2, 3, 4)	-0.3	40	V	
1.4	Current See **Figure 5** (Diagram A)	I_{SQHx}, I_{SQLx}, (x = 1, 2, 3, 4)	-4	4	A	
	Input-/Output-Signal Pins					
1.5	Digital input voltages	V_{SEN}, V_{RI}, V_{DI}, V_{CLK}, V_{CSN}, V_{FEN}	-0.3	V_{CC5} + 0.3	V	
1.6	Digital input current	I_{SEN}, I_{DI}, I_{CLK}, I_{CSN}, I_{RI}, I_{FEN}	-10	10	mA	
	Resistance Measurement Pins					
1.9	Voltage	V_{MSR}	-0.3	6.8	V	
1.10	Current	I_{MSR}	-100	100	mA	
1.10A	Current	I_{MSR}	-220	100	mA	t_{on} < 5 ms
1.11	Voltage	V_{MO}	-0.3	6.8	V	
1.12	Current	I_{MO}	-10	10	mA	
	Leakage Measurement Pins					
1.15	Input differential voltage	V_{SQHx}, V_{SQLx}, (x = 1, 2, 3, 4)	-40	40	V	
1.16	Voltage	V_{MCA}	-0.3	50	V	
1.17	Current	I_{MCA}	-10	5	mA	

4.1 Absolute Maximum Ratings (cont'd)

T_j = - 40 to 150 °C

Pos	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
	Squib Deployments					
1.31	Number of firings per squib driver and lifetime of the IC. See **Figure 5** (Diagram A and B) cooling delay time between two cycles	N_{max}	100			t_d = 1min R_{Squib} = 2 Ω
	Temperatures					
1.32	Ambient temperature	T_a	-40	90	°C	
1.33	Storage temperature	T_{stg}	-55	150	°C	
1.34	Junction temperature	T_j	-40	150	°C	
	Thermal Resistance					
1.35	Junction to ambient	R_{thja}		70	K/W	
	ESD Classification					
1.37	Human body model (100 pF / 1.5 kΩ)	V_{HBM}	-2000	2000	V	
1.38	Machine model (200 pF / 0 Ω)	V_{MM}	-200	200	V	

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. Furthermore, the values within these maximum ranges must not result in inadvertent deployment of squibs.

4.2 Functional Range

T_j = -40 to 150 °C

Pos	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
2.4	Rate of supply voltage rise	dV_S/dt, dV_{Boost}/dt, dV_{CHP}/dt, dV_{FV12}/dt, dV_{FV34}/dt, dV_{SQxx}/dt			30	V/ms	
2.5	Supply voltage V_{Boost}	V_{Boost}	4.5		40	V	
2.6	Supply voltage V_{CHP}	V_{CHP}	10		44	V	
2.7	Supply voltage of squib drivers	V_{FV12}, V_{FV34},	6		40	V	
2.8	Supply voltage on pin V_{CC5}	V_{CC5}	4.3	5	6.2	V	
2.9	Voltage on pin V_S	V_S	-0.3		40 18	V	$t_{Vs} \leq 400$ ms continuous
2.13	Voltage on pin SQHx (x = 1, 2, 3, 4)	V_{SQHx}	-0.3		40	V	$V_{FVxy} \geq V_{SQHx}$
2.18	Lifetime	t_{lt}			15	years	
2.19	Operating time on battery; conditions: T_j = 90 °C T_j = 110 °C T_j = 125 °C T_j = 150 °C	t_{op}			 10k 7k 4.5k 3k	h	

Note: In the maximum functional range, the functions given in the circuit are fulfilled. However, deviations from these characteristics are possible.

4.3 AC/DC Characteristics

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Supply Currents T_j = -40 to 125 °C, V_{FV12}, V_{FV34}= 6 to 40 V, V_{Boost} = 8.5 V to 40 V, V_{CC5} = 4.3 to 5.5 V							
3.1	Supply current on pin V_S	I_S	0.05		0.5	mA	V_S = 5.25 to 18 V, V_{Boost}, V_{CC5} open
3.2	Quiescent current on pin V_{CC5}	I_{VCC5}	0.04		0.3	mA	
3.3	Current on pin V_{CC5}	I_{VCC5}	0.05		0.7	mA	No diagnostic, voltage measurement allowed, SPI commands active.
3.4	Operating current on pin V_{Boost}	I_{Boost}	0.3		2.5	mA	Drivers off, no diagnostic, V_{CHP} = open.
3.4A	Operating current on pin V_{Boost}	I_{Boost}	1		3.2	mA	Drivers off, no diagnostic, voltage measurement allowed, SPI commands active, MO open.
3.5	Current on pin V_{Boost} during squib leakage measurement	I_{Boost}	4		7	mA	V_{CHP} = 30 V, V_{Boost} = 30 V V_S = 18 V, V_{CC5} = 4.8 V, I_{MCA} = 1.5 mA
3.6	Current on pin V_{CHP}	I_{CHP}	-1500		-500	µA	V_{CHP} = 0 V, V_{Boost} = 30 V, drivers off
3.7	Current on pin V_{CHP}	I_{CHP}	50		250	µA	V_{CHP} = 30 V, $V_{Boost} \geq$ 8 V, drivers off

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
3.8	Current on pin V_{CHP}	I_{CHP}	150		500	µA	V_{CHP} = 30 V, $V_{Boost} \geq$ 20 V all drivers on
3.9	Quiescent currents on squib driver supply pins FV12, FV34	I_{FV12}, I_{FV34}	1		20	µA	Drivers off
3.10	Opperating current on pins FV12, FV34, V_{CHP}, V_S	I_{FV12}, I_{FV34}, I_{CHP}, I_S	0		150	µA	Drivers off, voltage measurements active.
3.11	Voltage difference between pins V_{Boost} and V_{CHP}	V_{Boost} - V_{CHP}	0.3		0.9	V	Drivers off, squibs off, V_{Boost} = 30 V, I_{CHP} = -300 µA

Logic Inputs

Inputs: SEN, DI, CLK, CSN, RI, FEN

T_j = -40 to 125 °C, V_{Boost} = 8.5 [1] to 40 V, V_{CC5} = 4.3 to 5.5 V

4.1	Input voltage-high level	V_{IH}	2.4			V	
4.2	Input voltage-low level	V_{IL}			0.8	V	
4.3	Input hysteresis	ΔV_I	20		200	mV	
4.4	Input pull-up resistance internal to V_{CC5} on pin: CSN	R_{CSN}	12		48	kΩ	V_{CC5} = 5 V, V_I = 0 V
4.4A	Input pull-up resistance internal to V_{CC5} on pins: DI	R_{DI}	40	100	190	kΩ	V_{CC5} = 5 V, V_I = 0 V
4.5	Input pull-down resistor internal to ground on pins: SEN, FEN	R_{EN}	30	100	190	kΩ	V_I = 5 V
4.5A	Input pull-down current source to ground on pin: RI	I_{RI}	1		5	µA	V_I = 5 V

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
4.5B	Input pull-down current source to ground on pin: CLK	I_{CLK}	10		35	µA	V_I = 5 V

[1] V_{Boost} = 8.5 V will be guaranteed by design. ATE tests are performed at min. 10 V

Squib Driver: High-Side [1]

T_j = -40 to 150 °C, V_{FV12}, V_{FV34}= 6 to 40 V, V_{Boost} = 8.5 V to 40 V, V_{CC5} = 4.75 to 5.25 V, $V_{CHP} \geq$ FV + 6 V

14.1	Saturation voltage of switch x = 1, 2, 3, 4	V_{FVxy} - V_{SQHx}		1.3	1.6	V	V_{Boost} =21 V V_{CHP} = 21 V, FVxy = 12 V, -I_{SQHx} = 1.75 A
14.2	Output current limitation of switch x = 1, 2, 3, 4	I_{SQHx}	-3.50		-2.25	A	V_{Boost} = V_{CHP} = 21 V, FVxy - $V_{SQHx} \geq$ 4 V [7]
14.2A	Clamping voltage on pin SQHx during firing (x = 1, 2, 3, 4)	V_{SQHx}	24		27	V	I_{SQHx} = value of spec. **15.3**
14.3	Switch off time delay of switch x = 1, 2, 3, 4	t_{off}	0.1		5	µs	R_{Load} = 2.2 Ω [2] from SQHx to GND
14.4	Switch on time delay of switch x = 1, 2, 3, 4 (R_{Load} from SQHx to GND)	t_{on}	1		20	µs	R_{Load} = 2.2 Ω, V_{FVxy} = 12 V [2], trigger V_{SQHx} = 0.5 V
14.5	Switch on time delay of switch x = 1, 2, 3, 4 (R_{Load} from SQHx to GND)	t_{on}	1		35	µs	R_{Load} = 2.2 Ω, V_{FVxy} = 12 V [2], trigger V_{SQHx} = 4.4 V
14.6	Over temperature limitation	T_{OT}	180		300	°C	Not tested, guaranteed by design

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Squib Driver: Low-Side [1] T_j = -40 to 150 °C, V_{FV12}, V_{FV34} = 6 to 40 V, V_{Boost} = 8.5 to 40 V, V_{CC5} = 4.75 to 5.25 V, $V_{CHP} \geq V_{FVxy}$ + 6 V							
15.1	Saturation voltage of switch x = 1, 2, 3, 4	V_{SQLx}		1.3	1.6	V	V_{Boost} = 21 V V_{CHP} = 21 V, I_{SQLx} = 1.75 A [4]
15.2	Driver current detection of switch x	$I_{SQLxdet}$	1.75	2	2.25	A	$V_{SQLx} \geq$ 4 V [3]
15.3	Output current limitation of switch x = 1, 2, 3, 4	$I_{SQLxlim}$	2.0	2.5	3.0	A	$V_{SQLx} \geq$ 4 V [5]
	Current difference $I_{SQLxlim}$ - $I_{SQLxdet}$	$I_{\Delta SQ}$	0.05			A	guaranteed by design
15.4	Switch off time delay of switch x = 1, 2, 3, 4	t_{off}	0.1		5	µs	R_{Load} = 2.2 Ω [2] from SQLx to 12 V
15.5	Switch on time delay of switch x = 1, 2, 3, 4 (R_{Load} from SQLx to 12 V)	t_{on}	3		20	µs	R_{Load} = 2.2 Ω, [2], trigger V_{SQLx} = 11.6 V
15.6	Switch on time delay of switch x = 1, 2, 3, 4 (R_{Load} from SQLx to 12 V)	t_{on}	5		35	µs	R_{Load} = 2.2 Ω [2], trigger V_{SQLx} = 8.5 V
15.7	Over temperature limitation	T_{OT}	180		300	°C	Not tested, guaranteed by design

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
	Output MO for Firing Current Detection						
15.8	Voltage on pin MO	V_{MO}	0		0.8	V	$I_{SQLx} > I_{SQLxdet}$
15.8A	Voltage on pin MO	V_{MO}	2.4		V_{CC5}	V	$I_{SQLx} < I_{SQLxdet}$
15.9	Lag time to activate high current detection latch	t_{Latch}	4		40	µs	$I_{SQLx} > I_{SQLxdet}$
15.10	Response time to report the information of the current detection latch to pin MO	T_{MO}			100	µs	$I_{SQLx} > I_{SQLxdet}$

1) The limits are valid for a switch on duration of 4 ms and firing on/off- timing characteristics (Diagram A and B) as described in **Figure 5**. From any squib output SQHx a short to ground or a connection to the automotive supply voltage V_{BAT} has no influence to other squib drivers, and vice versa.

2) The timing measurements of pos. **14.3**, **14.4**, **14.5**, **15.4**, **15.5** and **15.6** will be started either with the rising edge of CSN or a transition of FEN/SEN, and stopped by the specified voltage transition

3) The hysteresis of the driver current detection is typically 50 mA.

4) The maximum saturation voltage FVx - V_{SQHx} = 2.6 V is met by design.
The test conditions are V_{Boost} = V_{CHP} = 15 V, V_{FVxy} = 12 V, -I_{SQHx} = 1.75 A

5) Level of current limitation always greater than the level of spec. **15.2** is fullfilled by design (LS current detection)

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Squib Driver: High-Side and Low-Side T_j = -40 to 150 °C, V_{FV12}, V_{FV34} = 6 to 40 V, V_{Boost} = 8.5 V to 40 V, V_{CC5} = 4.75 to 5.25 V							
15.13	Total sum of saturation voltages of high and low-side switches (x = 1, 2, 3, 4) of pos.: **14.1** and **15.1**	V_{SQHx} + V_{SQLx}			3.2	V	See test conditions for specification **14.1** and **15.1**
15.14	Total absorbed energy of one high-side switch	W_{HS}			120	mJ	Starting temperature: $T_j \leq 85$ °C, squib firing on/ off timing see **Figure 5** and pos. **1.31** [1]
15.15	Total absorbed energy of one low-side switch	W_{LS}			140	mJ	Starting temperature: $T_j \leq 85$ °C, squib firing on/ off timing see **Figure 5** and pos. **1.31** [1]

[1] $W_{HS} = I_{SQHx}$ x (FVx - V_{SQHx}) x t_{on}, $W_{LS} = I_{SQLx}$ x V_{SQLx} x t_{on}

*Note: ATE-testing for **14.1**, **15.1** and **15.13** will be performed at maximum T_j = 125 °C.*

Squib Resistance Measurement

T_j = -40 to 125 °C, V_{FV12}, V_{FV34} = 6 to 40 V, V_{Boost} = 15 to 40 V, V_{CC5} = 4.75 to 5.25 V

	Basic Reference Current:						
16.1A	Base current source	I_{Bias}	-7%	5 x I_{MCA}	7%	mA	[1]
16.1B	Output voltage on pin MCA during squib resistance measurement	V_{MCA}	V_{CC5} -40 mV		V_{CC5} +20 mV	V	R_{MCA} = 4.99 kΩ
16.1C	Output voltage on pin MCA during squib resistance measurement	V_{MCA}	V_{CC5} -50 mV		V_{CC5} +30 mV	V	R_{MCA} = 4 - 6 kΩ

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
	Measurement Current Reference Input MAIN						
16.2	Operating voltage range on pin SQHx, if the MAIN current activated.	V_{SQHx}	0		V_{Boost} - 6	V	SPI: $6XXX_H$
16.3	Programmable operating range of I_{MAIN}. 3 step settings: M x I_{MCA} M = 16 [$6XXX_H$, b6 = 0, b5 = 1] M = 32 [$6XXX_H$, b6 = 1, b5 = 0] M = 40 [$6XXX_H$, b6 = 1, b5 = 1]	I_{MAIN}	-5%	M x I_{MCA}	5%	mA	
16.4	Current limitation on pin MCA during squib resistance measurement	$-I_{MCA}$	1.8		4.4	mA	V_{MCA} = 0 V
	Measurement Current Output MSR						
16.5	Voltage range for measurement on pin MSR	V_{MSR}	0		V_{CC5}	V	I_{MSR} = 0 to 61 mA
16.5A	Clamping voltage on pin MSR	V_{MSR}	V_{CC5}		V_{CC5} + 0.6	V	R_{MSR} > V_{CC5}/61 mA [4)]
16.6	Leakage current on pin MSR (measurement inactive)	I_{MSR}	-10		0	µA	V_{SQLx} = 33 V (x = 1, 2, 3, 4)
16.7	Current difference between I_{SQLx} (x = 1, 2, 3, 4) and $-I_{MSR}$	ΔI_1	-0.2		0.2	%	V_{MSR} = 3 V [2)] I_{SQLx} = 0 to 61 mA

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
16.9	Current difference between I_{MAIN} and -I_{MSR} (measurement of channel 1 to 4 active)	ΔI_2	-2.5		2.5	%	SPI: $6XXX_H$ V_{MSR} = 3 V [3] I_{MAIN} = 40 x I_{MCA} and 16 x I_{MCA}, squibs connected

[1] By design, the tolerance must be within 3% for each device.

[2] $\Delta I_1 = \frac{(I_{MSR2} - I_{MSR1}) - 55\ mA}{55\ mA} \times 100$

(I_{MSR2}: at I_{SQLx} = 55 mA, I_{MSR1}: at I_{SQLx} = 0 mA, V_{CC5} = 5 V, R_{MCA} = 5 kΩ)

[3] $\Delta I_2 = \frac{(I_{MSR2} - I_{MSR1}) - 24 \times I_{MCA}}{24 \times I_{MCA}} \times 100$

(I_{MSR2}: at I_{MAIN} = 40 x I_{MCA}, I_{MSR1}: at I_{MAIN} = 16 x I_{MCA}, V_{CC5} = 5 V, R_{MCA} = 5 kΩ)

[4] Met by design. This also applies to note [2] and [3]

	MO Voltage Output for Resistance Measurement						
16.10	Voltage on pin MO (measurement active)	V_{MO}	0		V_{CC5} + 0.6	V	
16.10 A	Voltage on pin MO (Gain = 10x amplifier)	V_{MO}	0.85 x V_{CC5}		0.93 x V_{CC5}	V	V_{SQHx} = V_{SQLx}
16.10 B	Voltage on pin MO (Gain = 30x amplifier)	V_{MO}	0.81 x V_{CC5}		0.91 x V_{CC5}	V	V_{SQHx} = V_{SQLx}
16.11	Voltage on pin MO (measurement inactive)	V_{MO}	0		30	mV	
16.12	Current on pin MO (measurement active)	I_{MO}	-3		-1	mA	V_{SQHx} - V_{SQLx} = 0 V, V_{MO} = 0 V
16.13	Internal pull down resistor on pin MO (measurement active)	R_{MO}	8		35	kΩ	V_{MO} = 3 V $6XXX_H$, SQHx and SQLx are open

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
	Measurement Amplifier						0), 1), 2)
16.14	Voltage gain	a10	9.9		10.3		V_{SQHX} - V_{SQLX} = 400 mV V_{CM} = V_{SQLX} ± 0.4 V, the value of V_{SQLX} is the actual measurement result of pos. **16.21**
16.18	Common mode rejection ratio	CMRR10	45			dB	V_{CM} = V_{SQLX} ± 0.4 V, the value of V_{SQLX} is the actual measurement result of pos. **16.21** 3)
16.19	Voltage gain	a30	29.0		32.0		V_{SQHX} - V_{SQLX} = 130 mV V_{CM} = V_{SQLX} ± 0.4 V, the value of V_{SQLX} is the actual measurement result of pos. **16.21**
16.20	Common mode rejection ratio	CMRR30	50 3)			dB	V_{CM} = V_{SQLX} ± 0.4 V, the value of V_{SQLX} is the actual measurement result of pos. **16.21**

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
	Pins SQL1, SQL2 Voltage Regulator						
16.21	Regulated voltage on pins SQLx	V_{SQLx}	-2.5%	V_{CC5} x(8/5)	2.5%	V	$I_{MSR} = I_{Bias}$ $4XXXX_H$, V_{CC5} = 5 V
16.22	Voltage difference of the regulated voltage on pins SQLx	ΔV_{SQLx} = $V_{SQLx\ (I)}$- $V_{SQLx\ (II)}$			100	mV	$V_{SQLX(I)}$: I_{MSR} = I_{Bias} $V_{SQLX(II)}$: I_{MSR} = I_{Bias} + I_{MAIN} V_{CC5} = 5 V
16.23	Current limit on pin MSR	I_{MSR}	-220		-65	mA	V_{SQLx} = 40 V, R_{MSR} = 0 Ω activated by SPI t_{on} < 5 ms
	Settling Time						
16.24	Total settling time on pin MO	t_{MO}	5		200	µs	I_{MSR} = -5 to -61 mA for 90% of the final value on pin MO no capacitance on pins SQx initial V_{SQx} to 0...33 V

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
	Pin MSR Voltage Measurement Amplifier (gain = 2)						[4]
16.25	Voltage gain	a2	1.90		2.25		V_{MSR} = 340 mV to 1 V
16.25A	Voltage gain	a2	1.95		2.5		V_{MSR} = 1 V to 2.5 V
16.26	Input Offset Voltage	V_{OS}			20	mV	[5]

[0] The Gain-10 or Gain-30 Amplifier measurements will be done between pin MO (as an output) and pins SQHx, SQLx (as differential inputs)

[1] From one squib output SQHx/SQLx a short to ground or a connection to the automotive supply voltage V_{BAT} has no influence to the other squib resistance measurement function and vice-versa.

[2] A squib difference voltage > 0.4 V has no influence to the other squib resistance measurement function and vice-versa. In this case the output voltage on pin MO will be set to values as specified under pos. **16.10**.

[3] CMRR = 20 x log [a_x x $\Delta V_{SQLX}/\Delta V_{MO}$].

[4] The Gain-2 Amplifier measurements will be done between pin MO (as an output) and pin MSR (as an input).

[5] Met by design. ($V_{OS} = V_{MO}/2 - V_{MSR}$)

Squib Leakage Measurement

T_j = -40 to 125 °C, V_S = 5.25 to 18 V, V_{FV12}, V_{FV34} = 6 to 40 V, V_{Boost} = 15 to 40 V, V_{CC5} = 4.75 to 5.25 V, $V_S \leq V_{Boost}$

	Output MO Leakage Measurement						
17.1	Voltage on MO (digital)	V_{MO}	0 2.4		0.8 V_{CC5}	V	Leakage to ground $V_{SQHx} < 1/4 \times V_S$ Leakage to battery $V_{SQHx} > 3/4 \times V_S$ No leakage
17.2	Voltage on MO (analog (three state))	V_{MO}	0 2 4	0.5 2.5 4.5	1 3 V_{CC5}	V	Leakage to ground No leakage Leakage to battery
17.2A	Current on pin MO (measurement active)	I_{MO}	-3		-1	mA	$CXXX_H$, $1XXX_H$ no leakage on SQHx, V_{MO} = 0 V
17.2B	Internal pull down resistor on pin MO (measurement active)	R_{MO}	8		35	kΩ	$CXXX_H$, $1XXX_H$ leakage to ground on SQHx, V_{MO} = 3 V

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
	Reference Output MCA						
17.3	Output voltage on pin MCA	V_{MCA}	0.32 x V_S		0.34 x V_S	V	R_{MCA} = 4.99 kΩ
17.4	Output current on pin MCA during measurement	I_{MCA}	-1.8		0	mA	Stable state
17.4A	Current limit on pin MCA during measurement	I_{MCA}	-4.4		-2	mA	V_{MCA} = 0 V
17.7	Current ratio of pin MCA to pin SQHx	$\lvert I_{MCA}/ I_{SQHx}\rvert$	0.9		1.1		Stable state $I_{MCA} \geq$ -2.2 mA
17.9	Resistance ratio of resistor on pin MCA to leakage resistance	R_{MCA}/ R_{Leak}		4/3			
	Leakage Detection Voltages $V_{Boost} \geq 3/4\ V_S + 2.5$ V						
17.10	Leakage low threshold voltage	V_{SQHx}	-5%	1/4 x V_S	5%	V	Leakage to ground V_{SQHx} is decreasing target: V_{MO} ='low'
17.11	Leakage high threshold voltage	V_{SQHx}	-5%	3/4 x V_S	5%	V	Leakage to battery V_{SQHx} is increasing target: V_{MO} = 'low'
17.12	Leakage detection hysteresis	ΔV_{SQHx}	-20%	1/48 x V_S	20%	V	Leakage to ground or leakage to battery
	Reference Input V_S						
17.13	Internal resistor at pin V_S	R_S	35		400	kΩ	V_S < 24 V

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
	Settling Time						
17.14	Total settling time on pin MO	t_{MO}			50	µs	I_{MCA} = -0.5 mA no capacitance on pins SQHx and SQLx initialize: V_{SQLx} = 0 to 33 V
17.15	MO output response after squib low-side switch activation via SEN	t_{MO}			30	µs	No external leakage
17.16	MO output response after squib high-side switch activation via SEN	t_{MO}			30	µs	No external leakage

Internal Dummy Squib Resistance
T_j = -40 to 125 °C, V_{Boost} = 15 to 40 V

	Squib Outputs:						
18.1	Leakage current of switch x = 1, 2, 3, 4	I_{SQx}	-20		20	µA	Switch off; SQHx = SQLx V_{FVxy} = 33 V V_{SQx} = 16.5 V
18.1A	Leakage current of switch x = 1, 2, 3, 4	I_{SQx}	-20		20	µA	Switch off; SQHx = SQLx FVxy = 33 V V_{SQx} = 0 V
18.2	Internal dummy resistor from SQHx to SQLx (x = 1, 2, 3, 4)	$R_{SQHx\text{-}SQLx}$	20		50	kΩ	No firing or measure V_{SQHx} - V_{SQLx} = 20 V, V_{SQHx} - V_{SQLx} ≤ V_{Boost}

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Supply and Pin Voltage Measurements T_j = -40 to 125 °C, V_S = 5.25 to 18 V, V_{FV12}, V_{FV34} = 6 to 40 V, V_{Boost} = V_{CHP} = 15 to 40 V, V_{CC5} = 4.75 to 5.25 V							
	MO Voltage Output for Supply Voltage Measurements:						
19.1	Voltage on pin MO (measurement inactive)	V_{MO}	0		30	mV	
19.2	Voltage on pin MO (measurement active)	V_{MO}	0		V_{CC5} + 0.6	V	
19.2A	Current on pin MO (measurement active)	I_{MO}	-3		-1	mA	Input pin voltage = 3 V x (division factor); V_{MO} = 0 V
19.2B	Internal pull down resistor on pin MO (measurement active)	R_{MO}	8		35	kΩ	Input pin voltage = 0 V, V_{MO} = 3 V, $1XXX_H$
19.4	V_S voltage to MO output voltage ratio	V_S/V_{MO}	-5%		5%		Selection via SPI: MV_S $V_S \leq V_{Boost}$ - 6 V
19.5	V_{Boost} voltage to MO output voltage ratio	V_{Boost}/V_{MO}	-5%	8	5%		Selection via SPI: MV_{Boost} $V_{Boost} \geq$ 6 V
19.6	V_{CHP} voltage to MO output voltage ratio	V_{CHP}/V_{MO}	-5%	8	5%		Selection via SPI: MV_{CHP} $V_{CHP} \geq$ 6 V
19.7	V_{FVxy} Voltage to MO output voltage ratio (x = 12, 34)	V_{FVxy}/V_{MO}	-5%	8	5%		Selection via SPI: MFSUP $V_{FVxy} \geq$ 6 V
19.8	Total settling time on pin MO	t_{MO}			100	µs	For 90% of the final value on pin MO
19.9A	Reference voltage high on MO pin	V_{MO}	-5%	V_{CC5} x (2.72/5)	5%	V	Selection via SPI: REFH; $AAAA_H$ [1)]

4.3 AC/DC Characteristics (cont'd)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
19.9B	Reference voltage low on MO pin	V_{MO}	-10%	V_{CC5} x (0.35/5)	10%	V	Selection via SPI: REFL; 5555_H [1]
19.9C	FEN voltage to MO output voltage ratio	V_{FEN}/V_{MO}	-5%	1	5%	V	Selection via SPI: V_{FEN}; $1XXX_H$
19.9D	SEN voltage to MO output voltage ratio	V_{SEN}/V_{MO}	-5%	1	5%	V	Selection via SPI: V_{SEN}; $1XXX_H$
19.10	SQHx voltage to MO output voltage ratio (x = 1, 2, 3, 4)	V_{SQHx}/V_{MO}	-5%	8	5%3		Selection via SPI: MSQx $V_{SQHx} \leq V_{Boost}$ - 6 V
19.11	Test voltage on pin MO	V_{MO}	-5%	V_{CC5}	5%	V	RI = Low, FEN = High, SEN = High [2]

[1] The specification **19.9A**/**19.9B** can be used to test the SPI block and to detect ground loss in the IC.

[2] During this test condition, SPI commands will not be decoded as a result of low on RI.

4.4 Serial Peripheral Interface (SPI)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
SPI Timing Characteristics T_j = -40 to 150 °C, V_{CC5} = 4.75 to 5.25 V							
22.1	CSN lead time	t_{Lead}	40			ns	
22.2	CSN lag time	t_{Lag}	100			ns	
22.3	Fall time for CSN, CL, DI (70% to 20% of V_{CC5}; C_L = 47 pF)	t_f			25	ns	
22.4	Rise time for CSN, CL, DI (20% to 70% of V_{CC5}; C_L = 47 pF)	t_r			25	ns	
22.5	DI data setup time	t_{SU}	40			ns	
22.6	DI data hold time	t_h	40			ns	
22.10	DI data valid time	t_v			120	ns	
22.12	Clock frequency	f_{CL}	0		4	MHz	

Note: All timing is shown with respect to 20% and 70% of V_{CC5}.

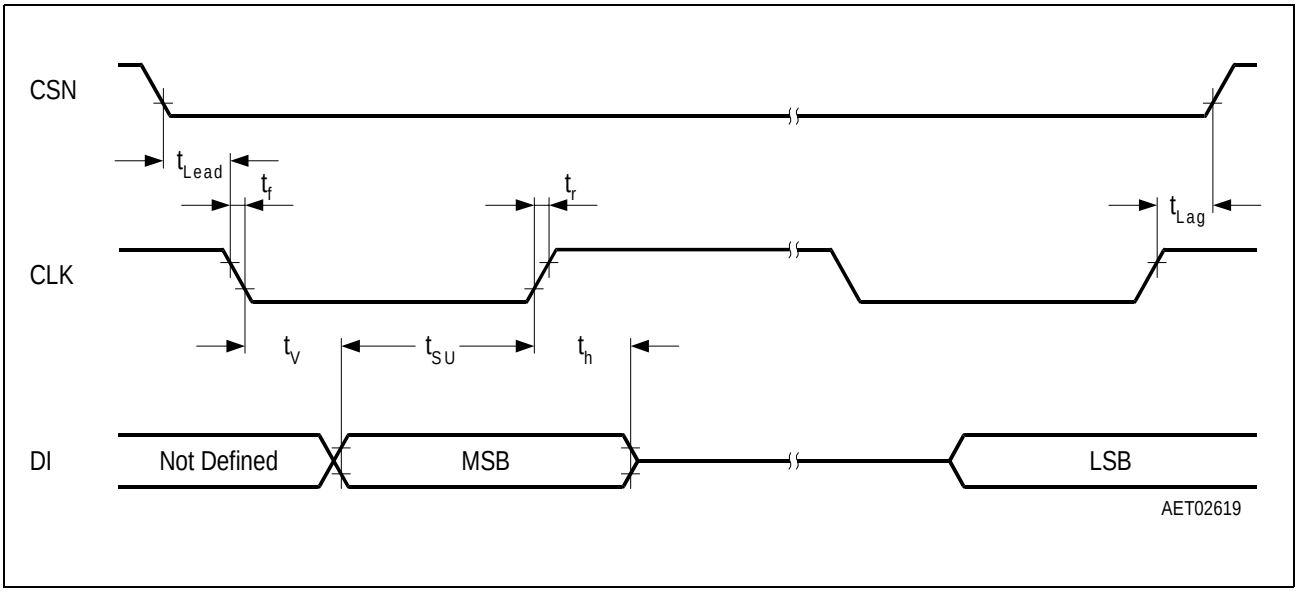


Figure 8 SPI Timing

5 Application Circuit

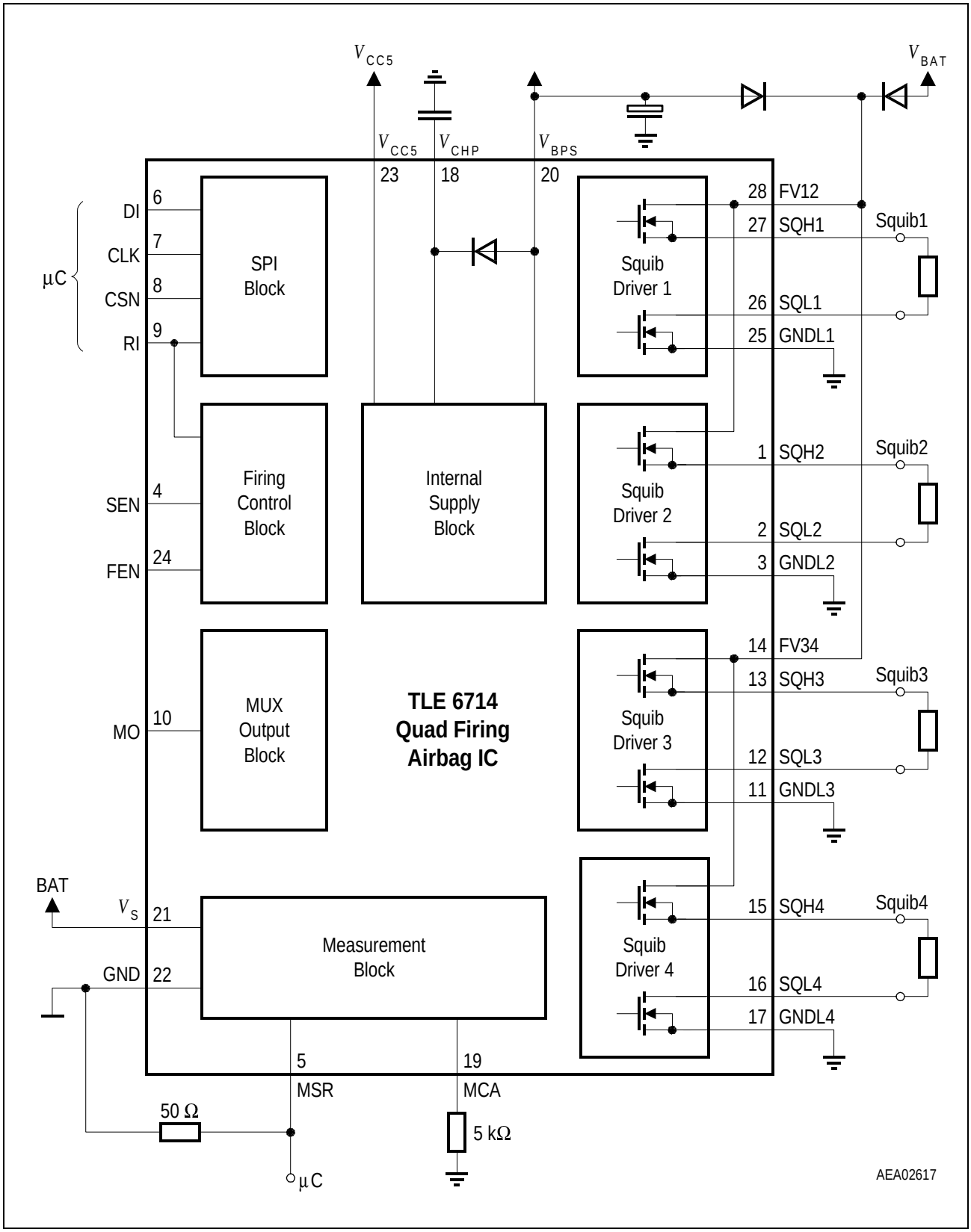
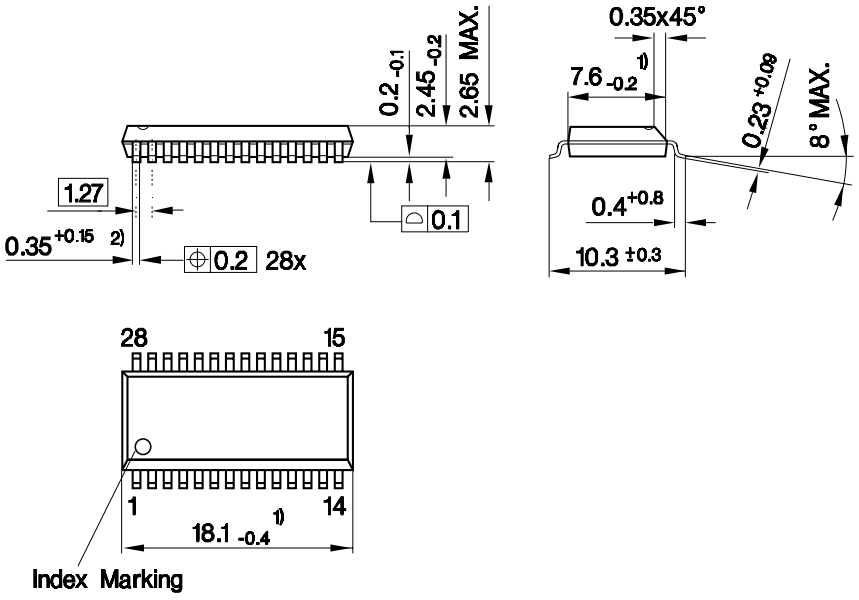


Figure 9

6 Package Outlines

P-DSO-28-1
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05123

Figure 10

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Edition 03.2001

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