

[www.DataSheet4U.net](http://www.DataSheet4U.net)

# SPIDER

SPI Driver for Enhanced Relay Control

# TLE7239SL

SPI Driver for Enhanced Relay Control

## Data Sheet

Rev. 1.0, 2010-02-18

## Table of Contents

|           |  |    |
|-----------|--|----|
|           | <b>Table of Contents</b>                 | 2  |
| <b>1</b>  | <b>Overview</b>                          | 3  |
| <b>2</b>  | <b>Block Diagram</b>                     | 6  |
| 2.1       | Terms                                    | 7  |
| <b>3</b>  | <b>Pin Configuration</b>                 | 8  |
| 3.1       | Pin Assignment                           | 8  |
| 3.2       | Pin Definitions and Functions            | 8  |
| <b>4</b>  | <b>Electrical Characteristics</b>        | 10 |
| 4.1       | Absolute Maximum Ratings                 | 10 |
| 4.2       | Functional Range                         | 11 |
| 4.3       | Thermal Resistance                       | 12 |
| <b>5</b>  | <b>Power Supply</b>                      | 13 |
| 5.1       | Operation Modes                          | 13 |
| 5.2       | Limp Home Mode                           | 13 |
| 5.3       | Reset                                    | 14 |
| 5.4       | Electrical Characteristics               | 15 |
| <b>6</b>  | <b>Power Stages</b>                      | 16 |
| 6.1       | Input Circuit                            | 16 |
| 6.2       | Channels 4 and 5                         | 16 |
| 6.3       | Inductive Output Clamp                   | 17 |
| 6.4       | Timing Diagrams                          | 18 |
| 6.5       | Electrical Characteristics               | 19 |
| 6.6       | Command Description                      | 20 |
| <b>7</b>  | <b>Protection Functions</b>              | 21 |
| 7.1       | Over Load Protection                     | 21 |
| 7.2       | Over Temperature Protection              | 21 |
| 7.3       | ESD protection                           | 21 |
| 7.4       | Reverse Polarity Protection              | 21 |
| 7.5       | Loss of $V_{bb}$                         | 21 |
| 7.6       | Electrical Characteristics               | 22 |
| <b>8</b>  | <b>Diagnostic Features</b>               | 23 |
| 8.1       | Electrical Characteristics               | 24 |
| 8.2       | Command Description                      | 25 |
| <b>9</b>  | <b>Serial Peripheral Interface (SPI)</b> | 27 |
| 9.1       | SPI Signal Description                   | 27 |
| 9.2       | Daisy Chain Capability                   | 28 |
| 9.3       | SPI Protocol                             | 29 |
| 9.4       | Register Overview                        | 30 |
| 9.5       | Timing Diagrams                          | 31 |
| 9.6       | Electrical Characteristics               | 32 |
| <b>10</b> | <b>Package Outlines</b>                  | 34 |
| <b>11</b> | <b>Application Information</b>           | 35 |
| <b>12</b> | <b>Revision History</b>                  | 36 |

## SPI Driver for Enhanced Relay Control TLE7239SL

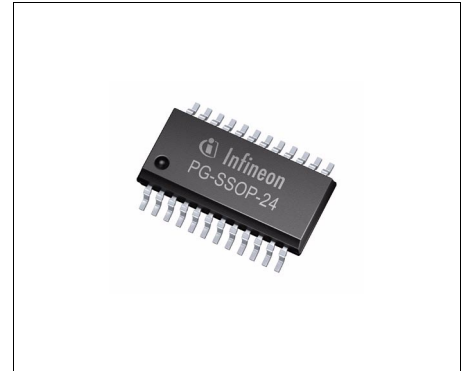
TLE7239SL



### 1 Overview

#### Features

- 8 bit SPI for diagnostics and control, providing daisy chain capability
- Very wide range for digital supply voltage
- Two configurable input pins offer complete flexibility for PWM operation
- Stable behavior at under voltage
- Green Product (RoHS compliant)
- AEC Qualified



PG-SSOP-24-5

#### Description

The TLE7239SL is an eight channel high-side and low-side power switch in PG-SSOP-24-5 package providing embedded protective functions. It is especially designed for standard relays and LEDs in automotive applications. The output stages incorporate two low-side, four high-side and two auto configuring high-side or low-side switches.

A serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the load. For direct control, there are two input pins available.

The TLE7239SL provides a micro controller fail-safe function which is activated via a high signal at the limp home input pin. There is a power supply integrated in the device to ensure this functionality even without digital supply voltage. The integrated power supply is designed to fulfill cranking mode requirements.

The power transistors are built by N-channel power MOSFETs. The device is monolithically integrated in Smart Power Technology.

| Type      | Package      | Marking   |
|-----------|--------------|-----------|
| TLE7239SL | PG-SSOP-24-5 | TLE7239SL |

**Table 1 Product Summary**

|  |                    |               |
|--|--------------------|---------------|
| Operating range power supply voltage           | $V_{bb}$           | 4.0 ... 28 V  |
| Digital supply voltage                         | $V_{DD}$           | 3.0 ... 5.5 V |
| Typical On-State resistance at 25 °C           | $R_{DS(ON)}$       |               |
| high-side: 2 channels (Relay)                  |                    | 0.9 $\Omega$  |
| high-side: 2 channels (Generic, LED)           |                    | 1.6 $\Omega$  |
| auto configuring: 2 channels (Relay, Supplies) |                    | 0.9 $\Omega$  |
| low-side: 2 channels (Relay)                   |                    | 0.9 $\Omega$  |
| Nominal load current (all channels active)     | $I_{L(nom, min)}$  |               |
| Relay  |                    | 260 mA        |
| LED, Generic                                   |                    | 130 mA        |
| Over load switch off threshold                 | $I_{DS(OVL, min)}$ | 500 mA        |
| Output leakage current per channel at 25 °C    | $I_{DS(OFF, max)}$ | 1 $\mu$ A     |
| Drain to source clamping voltage               | $V_{DS(CL, min)}$  | 41 V          |
| Source to ground clamping voltage              | $V_{bb(CL, max)}$  | -40 V         |
| SPI clock frequency                            | $f_{SCLK(max)}$    | 5 MHz         |

#### Protective Functions

- Over load and short circuit protection
- Thermal shutdown
- Electrostatic discharge protection (ESD)

#### Diagnostic Functions

- Latched diagnostic information via SPI
- Open load detection in OFF-state
- Over load detection in ON-state
- Over temperature

#### Crank Mode

- Integrated power supply enables secure operation at low battery voltage

#### Limp Home / Fail-Safe Functions

- Limp home activation via pin LHI
- Limp home configuration via input pins

#### Applications

- Especially designed for driving relays and LEDs in automotive applications
- All types of resistive and inductive loads
- Suitable to switch 5 V power supply lines by auto configuring channels

**Detailed Description**

The TLE7239SL is an eight channel high-side and low-side relay switch providing embedded protective functions. The output stages incorporate two low-side switches ( $0.9\ \Omega$  per channel), four high-side switches (two channels with  $0.9\ \Omega$  and two channels with  $1.6\ \Omega$ ) and two auto-configuring high-side or low-side switches ( $0.9\ \Omega$  per channel). The auto-configuring switches can be utilized in high-side or low-side configuration just by connecting the load accordingly. They are also suitable to switch a 5 V supply line in high-side configuration. Protective and diagnostic functions adjust automatically to the chosen configuration.

The 8 bit serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the loads. The SPI interface provides daisy chain capability in order to assemble multiple devices in one SPI chain by using the same number of micro-controller pins.

The outstanding feature of this octal relay switch enables the output channels to keep their state at low battery voltage. This is realized by an integrated power supply, especially designed to fulfill cranking mode requirements ( $V_{\text{bat}} = 4\ \text{V}$ ) independent from digital power supply ( $V_{\text{DD}}$ ). The SPI functionality is given only when the digital power supply is available.

Furthermore, the TLE7239SL is equipped with two input pins that can be individually routed to the output control of each channel thus offering complete flexibility in design and PCB-layout. The input multiplexer is controlled via SPI.

In limp home mode (fail-safe mode), the input pins are directly routed to the configurable output channels 4 and 5. The limp home mode operates independently of digital power supply and is activated via pin LHI.

The device provides full diagnosis of the load via open load, over load and short circuit detection. SPI diagnosis flags indicate latched fault conditions that may have occurred.

Each output stage is protected against short circuit. In case of over load, the affected channel switches off. There are temperature sensors available for each channel to protect the device against over temperature.

The device protects itself with a built in reverse polarity protection which prohibits intrinsic current flow through the logic during reverse polarity. However the output stages still incorporate a reverse diode where current can flow through during reverse polarity.

The power transistors are built by N-channel power MOSFETs. The inputs are ground referenced CMOS compatible. The device is monolithically integrated in Smart Power Technology.

## 2 Block Diagram

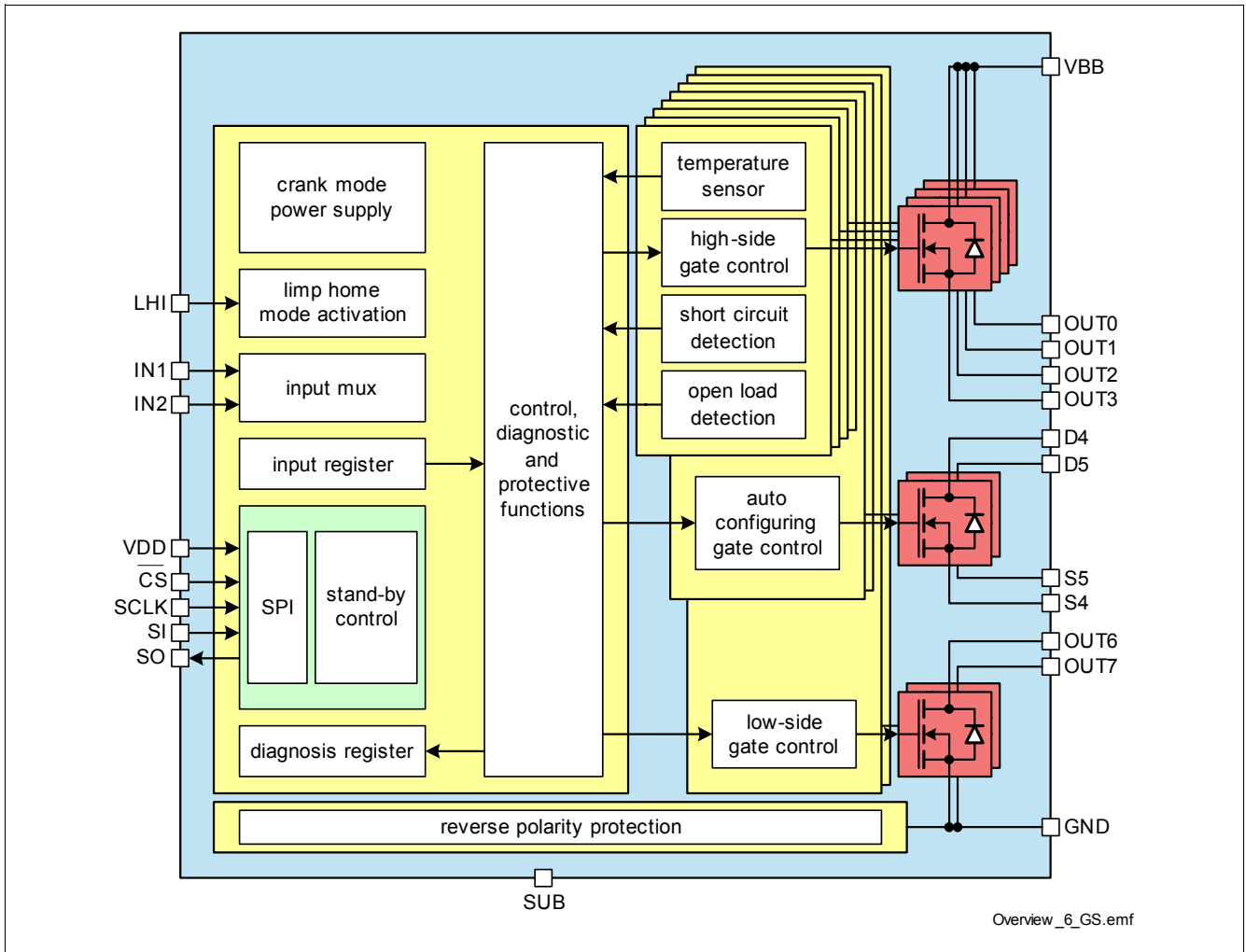
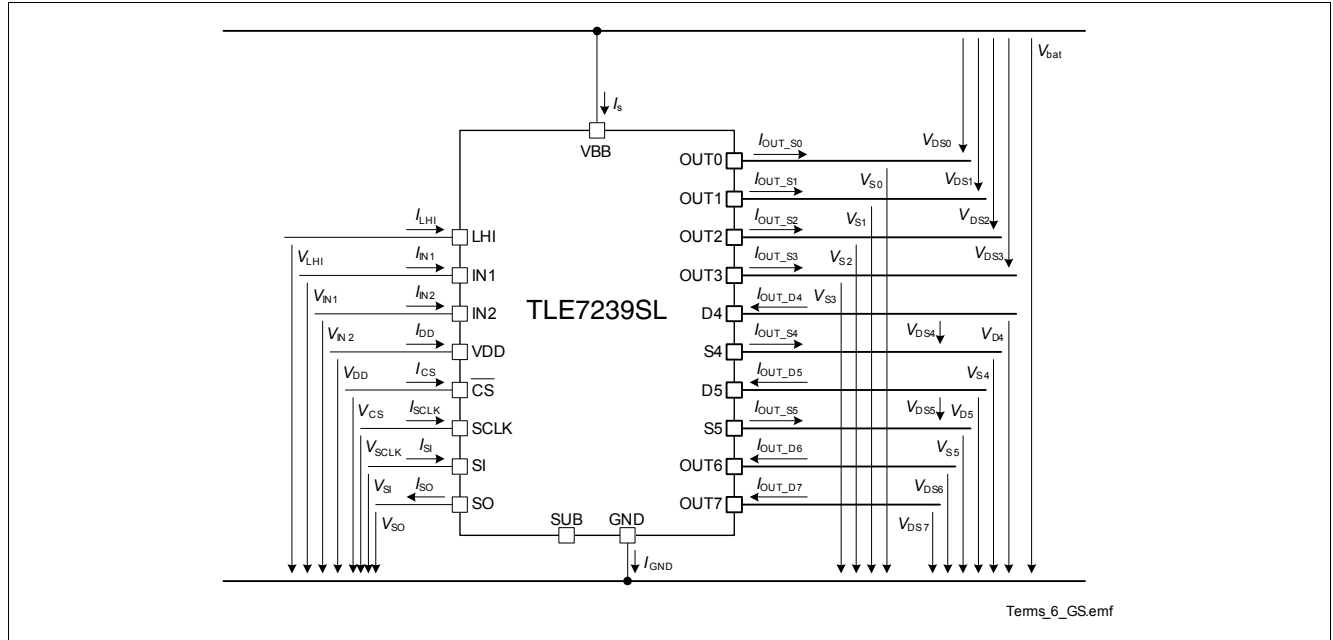


Figure 1 Block Diagram

### 2.1 Terms

Figure 2 shows all terms used in this data sheet.



**Figure 2** Terms

In all tables of the electrical characteristics is valid:

Channel related symbols without channel number are valid for each channel separately (e.g.  $V_{DS}$  specification is valid for  $V_{DS0} \dots V_{DS7}$ ). In order to make the description of output currents easier, the load current  $I_{Out}$  is equivalent to the drain current  $I_{OUT\_D}$  in low-side configuration and the source current  $I_{OUT\_S}$  in high-side configuration.

All SPI register bits are marked as follows: ADDR.PARAMETER (e.g. ICR01.INX1). In SPI register description, the values in bold letters (e.g. **0**) are default values.



## 3 Pin Configuration

### 3.1 Pin Assignment

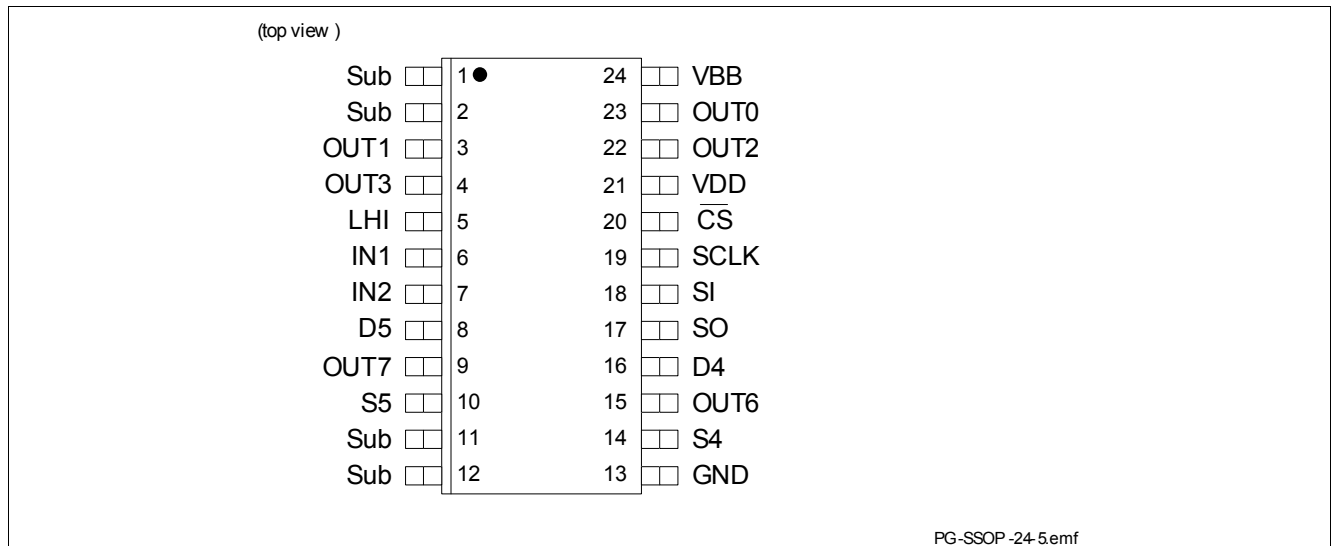


Figure 3 Pin Configuration PG SSOP24-5

### 3.2 Pin Definitions and Functions

| Pin                 | Symbol | I/O | Function   |
|---------------------|--------|-----|--|
| <b>Power Supply</b> |        |     |  |
| 21                  | VDD    | -   | Digital power supply   |
| 24                  | VBB    | -   | Power supply   |
| 13                  | GND    | -   | Digital, analog and power ground   |
| 1,2,11,12           | SUB    | -   | Substrate pins for thermal connection.<br><b>To enable reverse polarity protection these pins must be floating</b> |
| <b>Power Stages</b> |        |     |  |
| 23                  | OUT0   | O   | Source of high side power transistor channel 0   |
| 3                   | OUT1   | O   | Source of high side power transistor channel 1   |
| 22                  | OUT2   | O   | Source of high side power transistor channel 2   |
| 4                   | OUT3   | O   | Source of high side power transistor channel 3   |
| 16                  | D4     | O   | Drain of auto configuring power transistor 4   |
| 14                  | S4     | O   | Source of auto configuring power transistor 4  |
| 8                   | D5     | O   | Drain of auto configuring power transistor 5   |
| 10                  | S5     | O   | Source of auto configuring power transistor 5  |
| 15                  | OUT6   | O   | Drain of low side power transistor channel 6   |
| 9                   | OUT7   | O   | Drain of low side power transistor channel 7   |
| <b>Inputs</b>       |        |     |  |
| 5                   | LHI    | I   | Limp home activation input pin (pull down)   |
| 6                   | IN1    | I   | Input multiplexer input 1 pin (pull down)  |
| 7                   | IN2    | I   | Input multiplexer input 2 pin (pull down)  |



---

**Pin Configuration**

| Pin        | Symbol                 | I/O | Function                  |
|------------|------------------------|-----|---------------------------|
| <b>SPI</b> |                        |     |                           |
| 20         | $\overline{\text{CS}}$ | I   | SPI Chip select (pull up) |
| 19         | SCLK                   | I   | Serial clock              |
| 18         | SI                     | I   | Serial data in            |
| 17         | SO                     | O   | Serial data out           |

## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings <sup>1)</sup>

Stresses above the ones listed here may affect device reliability or may cause permanent damage to the device. The values below are not considering combinations of different maximum conditions at one time

$T_j = -40\text{ °C to }+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

| Absolute Maximum Ratings <sup>1)</sup> |   |               |              |      |      |   |
|--|---|---------------|--------------|------|------|---|
| Pos.                                   | Parameter   | Symbol        | Limit Values |      | Unit | Test Conditions   |
|  |   |               | min.         | max. |      |   |
| Power Supply                           |   |               |              |      |      |   |
| 4.1.1                                  | Power supply voltage  | $V_{bb}$      | -40          | 40   | V    | -40V max. 2 minutes   |
| 4.1.2                                  | Digital supply voltage  | $V_{DD}$      | -0.3         | 5.5  | V    | –   |
| 4.1.3                                  | Power supply voltage for short circuit protection (single pulse)  | $V_{bat(SC)}$ | 0            | 28   | V    | –   |
| Power Stages                           |   |               |              |      |      |   |
| 4.1.4                                  | Load current  | $I_L$         |              |      | A    | –   |
|  | channel 0, 1, 4, 5, 6, 7  |               | -0.5         | 0.5  |      |   |
|  | channel 2, 3  |               | -0.25        | 0.25 |      |   |
| 4.1.5                                  | Voltage at power transistor   | $V_{DS}$      | –            | 41   | V    | –   |
| 4.1.6                                  | Power transistor's source voltage   | $V_{Out\_S}$  | -16          | –    | V    | –   |
| 4.1.7                                  | Power transistor's drain voltage  | $V_{Out\_D}$  | –            | 41   | V    | –   |
| 4.1.8                                  | Max. energy dissipation one channel single pulse for ch. 0, 1, 4, 5, 6, 7                                       | $E_{AS}$      |              |      | mJ   | 2)<br><br>$T_{j(0)} = 105\text{ °C}$<br>$I_{D(0)} = 0.35\text{ A}$  |
|  |   |               | –            | 65   |      |   |
|  |   |               | –            | 50   |      |   |
| 4.1.9                                  | Maximum energy dissipation one channel repetitive pulses for ch. 0, 1, 4, 5, 6, 7<br>1 · 10 <sup>4</sup> cycles | $E_{AR}$      |              |      | mJ   | 2)<br><br>$T_{j(0)} = 105\text{ °C}$<br>$I_{D(0)} = 0.250\text{ A}$ |
|  |   |               | –            | 18   |      |   |
|  | 1 · 10 <sup>6</sup> cycles  |               | –            | 13   |      |   |
| 4.1.10                                 | Max. energy dissipation one channel single pulse for ch. 2,3  | $E_{AS}$      |              |      | mJ   | 2)<br><br>$T_{j(0)} = 105\text{ °C}$<br>$I_{D(0)} = 0.250\text{ A}$ |
|  |   |               | –            | 50   |      |   |
|  |   |               | –            | 30   |      |   |

1) not subject to production test

**Electrical Characteristics**

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

**Absolute Maximum Ratings<sup>1)</sup>**

| Pos.   | Parameter   | Symbol   | Limit Values |      | Unit | Test Conditions  |
|--------|---|----------|--------------|------|------|--|
|        |   |          | min.         | max. |      |  |
| 4.1.11 | Maximum energy dissipation one channel repetitive pulses for ch. 2,3<br>$1 \cdot 10^4$ cycles | $E_{AR}$ | –            | 12   | mJ   | <sup>2)</sup><br>$T_{j(0)} = 105\text{ °C}$<br>$I_{D(0)} = 0.180\text{ A}$ |
|        | $1 \cdot 10^6$ cycles   |          | –            | 11   |      | $T_{j(0)} = 105\text{ °C}$<br>$I_{D(0)} = 0.180\text{ A}$                  |

**Logic Pins**

|        |                              |            |      |                |   |               |
|--------|------------------------------|------------|------|----------------|---|---------------|
| 4.1.12 | Voltage at input pins        | $V_{IN}$   | -0.3 | $V_{DD} + 0.3$ | V | <sup>3)</sup> |
| 4.1.13 | Voltage at LHI pin           | $V_{LHI}$  | -0.3 | 5.5            | V | –             |
| 4.1.14 | Voltage at chip select pin   | $V_{CS}$   | -0.3 | $V_{DD} + 0.3$ | V | <sup>3)</sup> |
| 4.1.15 | Voltage at serial clock pin  | $V_{SCLK}$ | -0.3 | $V_{DD} + 0.3$ | V | <sup>3)</sup> |
| 4.1.16 | Voltage at serial input pin  | $V_{SI}$   | -0.3 | $V_{DD} + 0.3$ | V | <sup>3)</sup> |
| 4.1.17 | Voltage at serial output pin | $V_{SO}$   | -0.3 | $V_{DD} + 0.3$ | V | <sup>3)</sup> |

**Temperatures**

|        |                      |           |     |     |    |   |
|--------|----------------------|-----------|-----|-----|----|---|
| 4.1.18 | Junction Temperature | $T_j$     | -40 | 150 | °C | – |
| 4.1.19 | Storage Temperature  | $T_{stg}$ | -55 | 150 | °C | – |

**ESD Susceptibility**

|        |                                |           |    |   |    |                   |
|--------|--------------------------------|-----------|----|---|----|-------------------|
| 4.1.20 | ESD susceptibility on all pins | $V_{ESD}$ | -2 | 2 | kV | HBM <sup>4)</sup> |
|--------|--------------------------------|-----------|----|---|----|-------------------|

1) not subject to production test

2) Pulse shape represents inductive switch off:  $I_L(t) = I_L(0) \cdot (1 - t / t_{pulse})$ ;  $0 < t < t_{pulse}$

3)  $V_{DD} + 0.3\text{ V} < 5.5\text{ V}$

4) ESD susceptibility, HBM according to EIA/JESD 22-A114

## 4.2 Functional Range

| Pos.  | Parameter   | Symbol            | Limit Values |      | Unit | Conditions                    |
|-------|---|-------------------|--------------|------|------|-------------------------------|
|       |   |                   | Min.         | Max. |      |                               |
| 4.2.1 | Supply Voltage Range for Nominal Operation        | $V_{bb(nom)}$     | 9            | 16   | V    | –                             |
| 4.2.2 | upper Supply Voltage Range for Extended Operation | $V_{bb(ext),up}$  | 16           | 28   | V    | Parameter Deviations possible |
| 4.2.3 | lower Supply Voltage Range for Extended Operation | $V_{bb(ext),low}$ | 4            | 9    | V    | Parameter Deviations possible |
| 4.2.4 | Junction Temperature                              | $T_j$             | -40          | 150  | °C   | –                             |

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

### 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards.

For more information, go to [www.jedec.org](http://www.jedec.org).

| Thermal Resistance <sup>1)</sup> |   |                 |              |      |      |      |            |
|----------------------------------|---|-----------------|--------------|------|------|------|------------|
| Pos.                             | Parameter   | Symbol          | Limit Values |      |      | Unit | Conditions |
|                                  |   |                 | Min.         | Typ. | Max. |      |            |
| 4.3.1                            | Junction to Case, bottom                            | $R_{thJC,back}$ | —            | —    | 25   | K/W  | 2)         |
| 4.3.2                            | Junction to Case, top                               | $R_{thJC,top}$  | —            | —    | 25   | K/W  | 2)         |
| 4.3.3                            | Junction to Pin (1,2,11 or 12)                      | $R_{thJPin}$    | —            | —    | 17   | K/W  | 2)         |
| 4.3.4                            | Junction to Ambient<br>(1s0p, min. footprint)       | $R_{thJA,min}$  | —            | 90   | —    | K/W  | 3)         |
| 4.3.5                            | Junction to Ambient<br>(1s0p+300mm <sup>2</sup> Cu) | $R_{thJA,300}$  | —            | 70   | —    | K/W  | 4)         |
| 4.3.6                            | Junction to Ambient<br>(1s0p+600mm <sup>2</sup> Cu) | $R_{thJA,600}$  | —            | 65   | —    | K/W  | 5)         |
| 4.3.7                            | Junction to Ambient (2s2p)                          | $R_{thJA,2s2p}$ | —            | 55   | —    | K/W  | 6)         |

1) Not subject to production test

2) Specified  $R_{thJSP}$  value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature).  $T_a = 85^\circ\text{C}$ . Ch1 to Ch8 are dissipating 1 W power (0.125 W each).

3) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with minimal footprint copper area and 70  $\mu\text{m}$  thickness.  $T_a = 85^\circ\text{C}$ . Ch1 to Ch8 are dissipating 1 W power (0.125 W each).

4) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 300mm<sup>2</sup> and 70  $\mu\text{m}$  thickness.  $T_a = 85^\circ\text{C}$ . Ch1 to Ch8 are dissipating 1 W power (0.125 W each).

5) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm<sup>2</sup> and 70  $\mu\text{m}$  thickness.  $T_a = 85^\circ\text{C}$ . Ch1 to Ch8 are dissipating 1 W power (0.125 W each).

6) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70  $\mu\text{m}$  Cu, 2 x 35  $\mu\text{m}$  Cu).  $T_a = 85^\circ\text{C}$ . Ch1 to Ch8 are dissipating 1 W power (0.125 W each).

## 5 Power Supply

The TLE7239SL is supplied by two supply voltages  $V_{bb}$  and  $V_{DD}$ . The  $V_{bb}$  supply line is connected to a battery feed and used by the power switches and by an integrated power supply for the register banks. The internal power supply is designed to hold the state of the power switches including the configuration stored in the control register bank during cranking down to 4V. There is an under voltage reset function implemented for the  $V_{bb}$  power supply, which is triggered if  $V_{bb}$  is below the undervoltage threshold. After start-up of the power supply, all SPI registers are reset to their default values and the device is in sleep mode (standby). Sending the SPI command  $CMD.WAKE = 1$  switches the device to operation mode (ON), while a command  $CMD.STB = 1$  send the device to sleep mode (standby) again. Please note that the device needs the time  $t_{wu(Sleep)}$  to initialize itself. No SPI command should be send after changing the power state via  $CMD.WAKE = 1$  before this time is elapsed. A SPI frame send during  $t_{wu(Sleep)}$  could be ignored.

The  $V_{DD}$  supply line is used to power the circuitry related to the SPI shift register and for driving the SO line. As a result, the daisy chain function is available as soon as  $V_{DD}$  is provided in the specified range independent of  $V_{bb}$ . A capacitor between pins  $V_{DD}$  and GND is recommended (especially in case of EMI disturbances).

Please see **Figure 14 “Application Diagram” on Page 35** for details.

### 5.1 Operation Modes

There is a limp home functionality implemented in the TLE7239SL, which is activated via pin LHI. Please refer to **Section 5.2** for details.

The device provides a sleep mode (stand by) to minimize current consumption, which also resets the register banks. It is entered and left by dedicated SPI commands. The sleep mode current is minimized only when limp home is inactive. After limp home, the device enters sleep mode automatically.

The internal power supply is designed for low voltage cranking condition down to  $V_{bb} = 4\text{ V}$ . During cranking, the output channels keep their state as before configured via SPI independent of  $V_{DD}$  supply voltage. If  $V_{DD} = 0\text{ V}$  the SPI can not be used as the output and input levels refer to  $V_{DD}$ , but the device keep the current state until either the limp home mode is triggered or the  $V_{DD}$  voltages comes back and therefore the SPI Interface works again.

The following table shows the operation modes depending on  $V_{bb}$ ,  $V_{DD}$  and the limp home input signal LHI.

**Operation Modes**

|                      |       |       |       |     |       |     |      |       |      |       |
|----------------------|-------|-------|-------|-----|-------|-----|------|-------|------|-------|
| VBB                  | 0 V   | 0 V   | 0 V   | 4 V | 4 V   | 4 V | 12 V | 12 V  | 12 V | 12 V  |
| VDD                  | 0 V   | 5 V   | 5 V   | 0 V | 0 V   | 3 V | 0 V  | 0 V   | 5 V  | 5 V   |
| LHI                  | X     | 0 V   | 5 V   | 0 V | 4 V   | 0 V | 0 V  | 5 V   | 0 V  | 5 V   |
| Switches operating   | -     | -     | -     | ✓   | ✓     | ✓   | ✓    | ✓     | ✓    | ✓     |
| Limp Home            | -     | -     | -     | -   | ✓     | -   | -    | ✓     | -    | ✓     |
| SPI & daisy-chain    | -     | ✓     | ✓     | -   | -     | ✓   | -    | -     | ✓    | ✓     |
| Register Banks       | reset | reset | reset | ✓   | reset | ✓   | ✓    | reset | ✓    | reset |
| Diagnostic functions | -     | -     | -     | -   | -     | -   | ✓    | -     | ✓    | -     |

### 5.2 Limp Home Mode

The TLE7239SL offers the capability of driving dedicated channels during fail-safe operation of the system. This limp home mode is activated by a high signal at pin LHI. In limp home mode, the SPI registers are reset and the input pins are directly routed to the auto configuring channels (channel 4 and 5). As a result, the limp home operation can be chosen for high-side and low-side driven loads. Due to the integrated power supply, limp home operation is independent of digital power supply  $V_{DD}$ . In case of stand-by, a high signal at pin LHI will wake up the device. After limp home operation, the device enters sleep mode in any case.

### **5.3 Reset**

There are several reset trigger implemented in the device. A reset switches off all channels and sets the registers to default values. After any kind of reset, the transmission error flag (TER) is set and the device is in sleep mode.

#### **Under Voltage Reset:**

During this device condition a read on SPI delivers the Standard Diagnostic Frame with a TER flag, if  $V_{DD}$  is above the under voltage threshold already, if not SPI is not working.

This under voltage reset is released when  $V_{DD}$  and  $V_{bb}$  supply voltage levels are above under voltage threshold.

**Reset Command:** There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as `CMD.RST = 1`, a reset is triggered.

**Limp Home Mode:** In limp home mode, the SPI write-registers are reset. The SPI interface is operating normally, so the limp home bit LHI as well as the diagnosis flags can be read, but no command is accepted until the device leaves the Limp home operation.

## 5.4 Electrical Characteristics

Unless otherwise specified:

$V_{DD} = 3.0 \text{ V to } 5.5 \text{ V}$ ,  $V_{BAT} = 9.0 \text{ V to } 16 \text{ V}$ ,  $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$

| Pos.                          | Parameter   | Symbol            | Limit Values |      |      | Unit          | Test Conditions  |
|-------------------------------|---|-------------------|--------------|------|------|---------------|--|
|                               |   |                   | min.         | typ. | max. |               |  |
| Power Supply $V_{bb}$         |   |                   |              |      |      |               |  |
| 5.4.1                         | Supply Voltage Range for Nominal Operation                      | $V_{bb(nom)}$     | 9            |      | 16   | V             | –  |
| 5.4.2                         | upper Supply Voltage Range for Extended Operation               | $V_{bb(ext),up}$  | 16           |      | 28   | V             | Parameter Deviations possible  |
| 5.4.3                         | lower Supply Voltage Range for Extended Operation               | $V_{bb(ext),low}$ | 4            |      | 9    | V             | $R_L = 80\ \Omega$<br>$V_{DS} < 1.5\text{ V}$<br>Parameter Deviations possible                     |
| 5.4.4                         | Under voltage reset threshold                                   | $V_{bb(UV)}$      | –            | –    | 4    | V             | $V_{DD} = 0\text{V}$   |
| 5.4.5                         | Operating current drawn from $V_{bb}$                           | $I_{S(ON)}$       | –            | –    | 15   | mA            | <sup>1)</sup> $V_{bb} = 16\text{ V}$   |
|                               |   |                   | –            | –    | 12   | mA            | $V_{bb} = 16\text{ V}$<br>all diagnosis off  |
| 5.4.6                         | Sleep mode operating current with disconnected loads (stand by) | $I_{S(Sleep)}$    |              |      |      | $\mu\text{A}$ | $V_{bb} = 16\text{ V}$<br>$V_{LHI} = 0\text{ V}$ ; AWK= 0<br>$T_j = 25\text{ }^\circ\text{C}^{1)}$ |
|                               |   |                   | –            | –    | 10   |               | $T_j = 85\text{ }^\circ\text{C}^{1)}$  |
|                               |   |                   | –            | –    | 13   |               |  |
|                               |   |                   | –            | –    | 20   |               | $T_j = 150\text{ }^\circ\text{C}$  |
| Digital Power Supply $V_{DD}$ |   |                   |              |      |      |               |  |
| 5.4.7                         | Logic supply voltage  | $V_{DD}$          | 3.0          | –    | 5.5  | V             |  |
| 5.4.8                         | Under voltage reset threshold                                   | $V_{DD(PO)}$      | –            | –    | 3.0  | V             |  |
| 5.4.9                         | Logic supply current  | $I_{DD(ON)}$      | –            | –    | 0.4  | mA            | $f_{SCLK} = 0\text{ Hz}$<br>AWK= 1<br>$V_{CS} = 0\text{V}$   |
| 5.4.10                        | Logic supply current during VBB dropout                         | $I_{DD(DO)}$      | –            | 3    | 5    | mA            | <sup>1)</sup> $f_{SCLK} = 0\text{ Hz}$<br>$V_{bb} < V_{bb(UV)}$<br>AWK= 1<br>$V_{CS} = 0\text{V}$  |
| 5.4.11                        | Logic supply sleep mode current                                 | $I_{DD(Sleep)}$   |              |      |      | $\mu\text{A}$ | $V_{CS} = V_{DD}$<br>AWK = 0<br>$T_j = 25\text{ }^\circ\text{C}^{1)}$                              |
|                               |   |                   | –            | –    | 20   |               | $T_j = 85\text{ }^\circ\text{C}^{1)}$  |
|                               |   |                   | –            | –    | 40   |               | $T_j = 150\text{ }^\circ\text{C}$  |

### Timings

|        |   |                 |   |   |     |               |               |
|--------|---|-----------------|---|---|-----|---------------|---------------|
| 5.4.12 | Sleep mode wake-up time                 | $t_{wu(Sleep)}$ | – | – | 200 | $\mu\text{s}$ | <sup>1)</sup> |
| 5.4.13 | $V_{bb}$ under voltage reset delay time | $t_{bb(UVR)}$   | – | – | 1   | $\mu\text{s}$ | <sup>1)</sup> |
| 5.4.14 | $V_{DD}$ under voltage reset delay time | $t_{DD(UVR)}$   | – | – | 1   | $\mu\text{s}$ | <sup>1)</sup> |

<sup>1)</sup> Not subject to production test, specified by design.

*Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature.*

*Typical values show the typical parameters expected at  $V_{bb} = 13.5 \text{ V}$ ,  $V_{DD} = 5.0 \text{ V}$ ,  $T_j = 25 \text{ }^\circ\text{C}$ .*



## 6 Power Stages

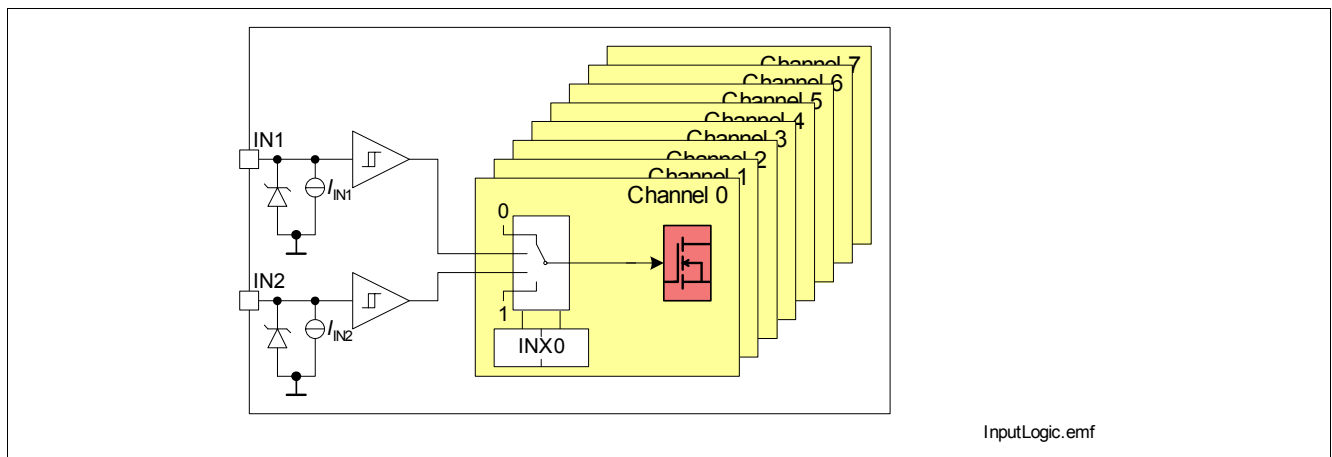
The TLE7239SL is an eight channel high-side and low-side relay switch. The power stages are built by N-channel vertical power MOSFET transistors. The gates of the high-side switches are controlled by charge pumps.

### 6.1 Input Circuit

There are two input pins available at TLE7239SL, which can be configured to be used for control of the output stages. The INXn parameter of the input configuration register provide following possibilities:

- channel is switched off
- channel is switched according to signal level at input pin IN1
- channel is switched according to signal level at input pin IN2
- channel is switched on

**Figure 4** shows the input circuit of TLE7239SL.



**Figure 4 Input Multiplexer**

The current sink to ground ensures that the channels switch off in case of open input pin. The zener diode protects the input circuit against ESD pulses.

### 6.2 Channels 4 and 5

The TLE7239SL provides two auto-configuring high-side or low-side switches (channels 4 and 5). They adjust the diagnostic and protective functions according their potentials at drain and source automatically.

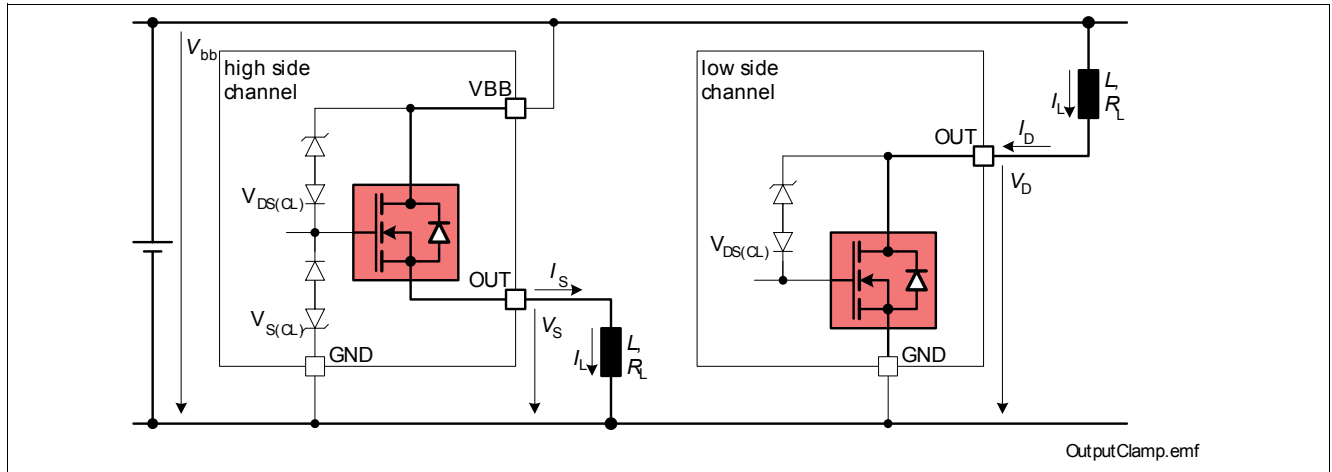
In high-side configuration, the load is connected between ground and source of the power transistors (S4 or S5). The drain of the power transistors (D4 and D5) can be connected to any potential between GND-pin potential and VBB-pin potential. When the drain is connected to VBB, the channel behave like the other high side channels. The drain can also be connected to a 5 V power supply and the source pin will be utilized as switched 5 V supply line.

In low-side configuration, the source of the power transistors are to be connected to GND.

The configuration can be chosen for each of these channels individually, so it is feasible to connect one channel in low-side and the other in high-side configuration.

### 6.3 Inductive Output Clamp

When switching off inductive loads with low-side switches, the potential at pin OUT rises to  $V_{DS(CL)}$  potential, because the inductance intends to continue driving the current. For the high-side channels, the potential at pin OUT drops below ground potential to  $V_{S(CL)}$ . The voltage clamping is necessary to prevent destruction of the device, see **Figure 5** for details. Nevertheless, the maximum allowed load inductance is limited by the max. clamping energy  $E_{AR}$  see electrical characteristics “ $E_{AR}$ ” on **Page 10**.



**Figure 5 Output Clamp Implementation**

#### Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the TLE7239SL. This energy can be calculated with following equations:

$$E = V_{DS(CL)} \cdot \left[ \frac{V_{bb} - V_{DS(CL)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_{bb} - V_{DS(CL)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad \text{Low-side} \quad (1)$$

$$E = (V_{bb} - V_{S(CL)}) \cdot \left[ \frac{V_{S(CL)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_{S(CL)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad \text{High-side} \quad (2)$$

These equations simplify under the assumption of  $R_L = 0$ :

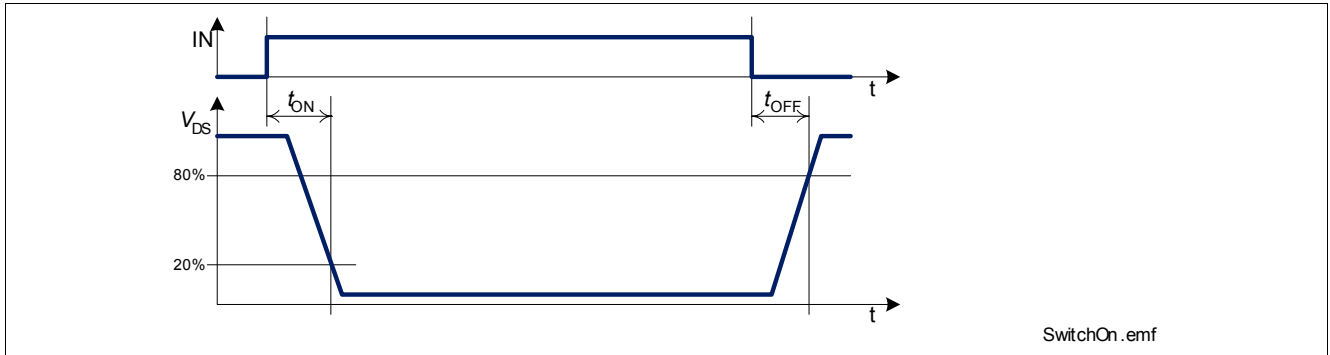
$$E = \frac{1}{2} L I_L^2 \cdot \left( 1 - \frac{V_{bb}}{V_{DS(CL)}} \right) \quad \text{Low-side} \quad (3)$$

$$E = \frac{1}{2} L I_L^2 \cdot \left( 1 - \frac{V_{bb}}{V_{S(CL)}} \right) \quad \text{High-side} \quad (4)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component.

## 6.4 Timing Diagrams

The power transistors are switched on and off with a dedicated slope via the  $INX$  bits of the serial peripheral interface (SPI). The switching times  $t_{ON}$  and  $t_{OFF}$  are designed equally.



**Figure 6 Switching a Resistive Load**

In input mode, a high signal at the input pin is equivalent to a SPI ON command and a low signal to SPI OFF command respectively. Please refer to [Section 9.3](#) for details on SPI protocol.

## 6.5 Electrical Characteristics

Unless otherwise specified:  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

typical values:  $V_{DD} = 5.0\text{ V}$ ,  $V_{BAT} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos. | Parameter | Symbol | Limit Values |      |      | Unit | Test Conditions |
|------|-----------|--------|--------------|------|------|------|-----------------|
|      |           |        | min.         | typ. | max. |      |                 |

### Output Characteristics

|       |   |                   |     |     |     |               |  |
|-------|---|-------------------|-----|-----|-----|---------------|--|
| 6.5.1 | On-State resistance<br>channel 0, 1, 4, 5, 6, 7 | $R_{DS(ON)}$      | –   | 0.9 | –   | $\Omega$      | $I_L = 220\text{ mA}$<br>$T_j = 25\text{ °C}$  |
|       |   |                   | –   | 1.4 | 1.9 |               | $T_j = 150\text{ °C}$  |
|       | channel 2, 3                                    |                   | –   | 1.6 | –   |               | $I_L = 110\text{ mA}$<br>$T_j = 25\text{ °C}$  |
|       |   |                   | –   | 2.6 | 3.9 |               | $T_j = 150\text{ °C}$  |
| 6.5.2 | Nominal load current                            | $I_{Out(nom)}$    |     |     |     | mA            | all channels on<br>$T_a = 100\text{ °C}$<br>$T_{j,max} = 150\text{ °C}$<br>based on $R_{thja}$ |
|       | channel 0, 1, 4, 5, 6, 7                        |                   | 260 | 380 | –   |               | 1)   |
|       | channel 2, 3                                    |                   | 130 | 175 | –   |               | 1)   |
| 6.5.3 | Output leakage current in sleep mode            | $I_{Out(Sleep)}$  | –   | –   | 1   | $\mu\text{A}$ | $V_{DS} = 13.5\text{ V}$<br>$T_j = 25\text{ °C}^{1)}$  |
|       |   |                   | –   | –   | 2   |               | $T_j = 85\text{ °C}^{1)}$  |
|       |   |                   | –   | –   | 5   |               | $T_j = 150\text{ °C}$  |
| 6.5.4 | Output clamping voltage                         | $V_{OUT\_S(CL)}$  | –   | –   | –16 | V             | –  |
|       |   | $V_{OUT\_DS(CL)}$ | 41  | –   | –   | V             | –  |

### Input Characteristics (IN & LHI)

|       |                           |                 |     |     |     |               |                              |
|-------|---------------------------|-----------------|-----|-----|-----|---------------|------------------------------|
| 6.5.5 | L level                   | $V_{IN(L)}$     | 0   | –   | 0.6 | V             | –                            |
| 6.5.6 | H level                   | $V_{IN(H)}$     | 1.8 | –   | 5.5 | V             | –                            |
| 6.5.7 | Input voltage hysteresis  | $\Delta V_{IN}$ | –   | 0.1 | –   | V             | 1)                           |
| 6.5.8 | L-input pull-down current | $I_{IN(L)}$     | 1.5 | –   | –   | $\mu\text{A}$ | $V_{IN} = 0.6\text{ V}^{1)}$ |
| 6.5.9 | H-input pull-down current | $I_{IN(H)}$     | 10  | 40  | 80  | $\mu\text{A}$ | $V_{IN} = 5\text{ V}$        |

### Timings

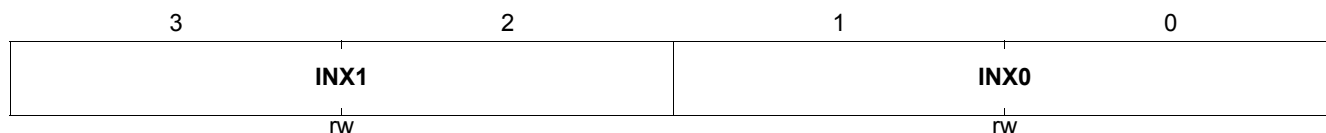
|        |   |           |   |   |     |               |  |
|--------|---|-----------|---|---|-----|---------------|--|
| 6.5.10 | Turn-on time<br>$V_{DS} = 20\% V_{bat}$<br>channel 0, 1, 4, 5<br>channel 2, 3<br>channel 6, 7           | $t_{ON}$  | – | – | 100 | $\mu\text{s}$ | $V_{bb} = 13.5\text{ V}$<br>resistive load<br>$I_{DS} = 250\text{ mA}$ |
|        |   |           | – | – | 100 |               | $I_{DS} = 120\text{ mA}$   |
|        |   |           | – | – | 100 |               | $I_{DS} = 250\text{ mA}$   |
| 6.5.11 | Turn-off time<br>$V_{DS} = 80\% V_{bb}$<br>channel 0, 1, 4, 5<br>channel 2, 3 (HS)<br>channel 6, 7 (LS) | $t_{OFF}$ | – | – | 100 | $\mu\text{s}$ | $V_{bb} = 13.5\text{ V}$<br>resistive load<br>$I_{DS} = 250\text{ mA}$ |
|        |   |           | – | – | 100 |               | $I_{DS} = 120\text{ mA}$   |
|        |   |           | – | – | 100 |               | $I_{DS} = 250\text{ mA}$   |

1) Not subject to production test, specified by design.

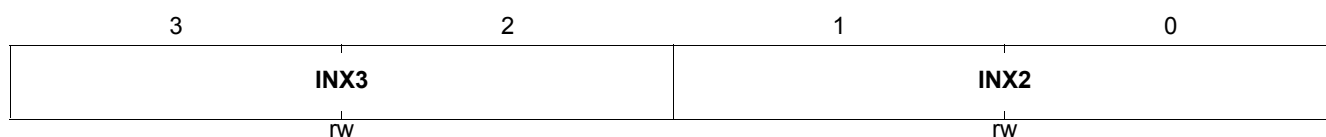
## 6.6 Command Description

### Input Configuration Registers

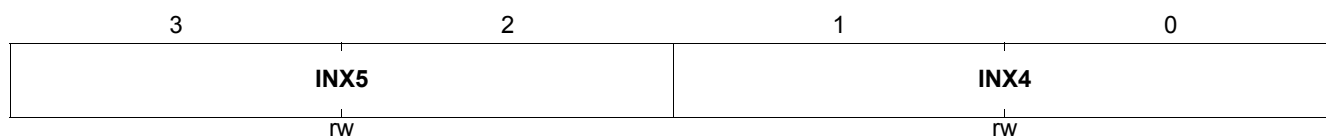
ICR01 000<sub>B</sub>



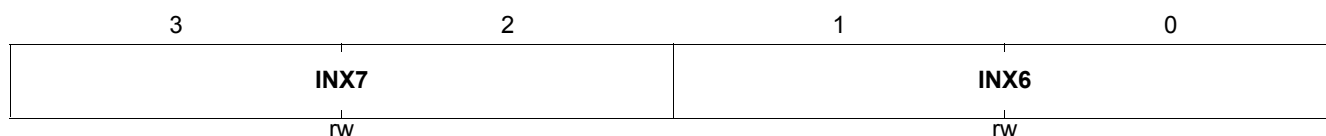
ICR23 001<sub>B</sub>



ICR45 010<sub>B</sub>



ICR67 011<sub>B</sub>



| Field              | Bits         | Type | Description   |
|--------------------|--------------|------|---|
| INXn<br>n = 7 to 0 | [3:2], [1:0] | rw   | <b>Input Multiplexer Configuration Channel n</b><br><b>00</b> Channel n is switched off<br><b>01</b> Channel n is switched by input 1<br><b>10</b> Channel n is switched by input 2<br><b>11</b> Channel n is switched on |

## 7 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

### 7.1 Over Load Protection

The TLE7239SL is protected in case of over load or short circuit of the load. After time  $t_{\text{OFF(OVL)}}$ , the over loaded channel  $n$  switches off and the according diagnosis flag  $D_n$  is set. The channel can be switched on after clearing the protection latch by command  $\text{CMD.CPL} = 1$ . The CPL command clears itself with the next valid SPI communication frame. Please refer to [Figure 7](#) for details.

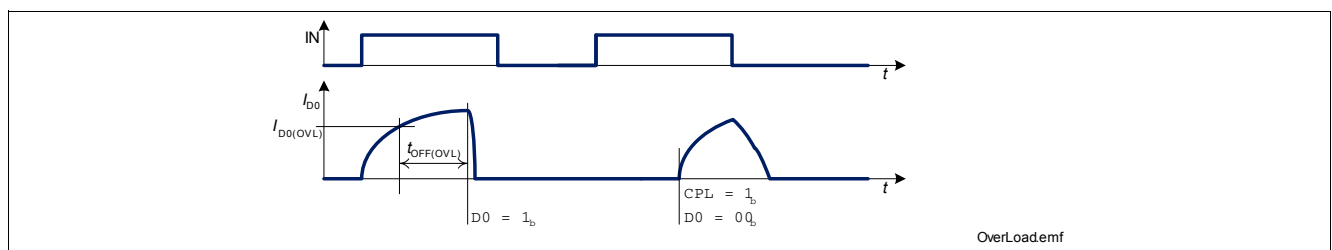


Figure 7 Shut Down at Over Load

### 7.2 Over Temperature Protection

A temperature sensor for each channel causes an overheated channel to switch off to prevent destruction. The according diagnosis flag is set. This flag is also set in OFF state, if the regarding channel temperature is too high. The channel can be only switched on after clearing the protection latch by SPI command  $\text{CMD.CPL} = 1$ . The CPL command clears itself with the next valid SPI communication frame. Please refer to [“Diagnostic Features” on Page 23](#) for information on diagnosis features.

### 7.3 ESD protection

There is a designed in protection against ESD disturbances up to the specified limit by using the defined model. Please see electrical characteristics [“ESD susceptibility on all pins” on Page 11](#)

### 7.4 Reverse Polarity Protection

There is a reverse polarity protection implemented in the TLE7239SL. This protection has to be divided into two parts. First the protection of the control circuits and second in the protection of the power transistors.

The control circuits are reverse polarity protected by protective measures in the ground connection. In case of reverse polarity, there is no current flow through the control circuits. To ensure this functionality, the GND pin and the substrate connections SUB must not be connected to the same potential. This means, the copper area dedicated for cooling should be connected at SUB and needs to be electrically isolated from GND.

The power transistors contain intrinsic body diodes that cause power dissipation. The reverse current through these intrinsic body diodes has to be limited by the connected loads. The over temperature and over load protection are not active during reverse polarity.

### 7.5 Loss of $V_{bb}$

In case of loss of  $V_{bb}$  connection in on-state, all inductances of the loads have to be demagnetized through the an additional path from  $V_{bb}$  to ground. Usually this path is given somewhere in the PCB circuitry, for example, as a suppressor diode like in the application diagram (see D1 in [Figure 14 “Application Diagram” on Page 35](#)).

## 7.6 Electrical Characteristics

Unless otherwise specified:

$V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

typical values:  $V_{DD} = 5.0\text{ V}$ ,  $V_{BAT} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos.                        | Parameter  | Symbol         | Limit Values |                   |      | Unit | Test Conditions |
|-----------------------------|--|----------------|--------------|-------------------|------|------|-----------------|
|                             |  |                | min.         | typ.              | max. |      |                 |
| Over Load Protection        |  |                |              |                   |      |      |                 |
| 7.6.1                       | Over load detection current at channel 0,1,4,5,6,7 | $I_{Out(OVL)}$ | 0.5          |                   | 1.0  | A    |                 |
| 7.6.2                       | Over load detection current at channel 2,3         | $I_{Out(OVL)}$ | 0.22         |                   | 0.5  | A    |                 |
| 7.6.3                       | Over load shut-down delay time                     | $t_{OFF(OVL)}$ |              |                   | 60   | μs   |                 |
| Over Temperature Protection |  |                |              |                   |      |      |                 |
| 7.6.4                       | Thermal shut down temperature                      | $T_{j(SC)}$    | 150          | 170 <sup>1)</sup> |      | °C   |                 |

1) Not subject to production test, specified by design



## 8 Diagnostic Features

The SPI of TLE7239SL provides diagnosis information about the device and about the load. The diagnosis information of the protective functions of channel  $n$  is latched in the diagnosis flags  $D_n$ . It is cleared by the SPI command  $CMD.CPL = 1$ . The CPL command clears itself with the next valid SPI communication frame.

The open load diagnosis of channel  $n$  is latched in the diagnosis flag  $OL_n$ . This flag is cleared by reading the according diagnosis register.

Following table shows possible failure modes and the according protective and diagnostic action.

| Failure Mode                 | Comment   |
|------------------------------|---|
| Open Load                    | <p>Diagnosis, when channel <math>n</math> is switched on: none</p> <p>Diagnosis, when channel <math>n</math> is switched off: according to voltage level at the output pin, flag <math>OL_n</math> is set after time <math>t_{d(OL)}</math>.</p> <p>A diagnosis current can be enabled by SPI command <math>DCCR.DCEN_n = 1</math>.</p> |
| Over Temperature             | <p>When over temperature occurs, the according diagnosis flag <math>D_n</math> is set. If the affected channel <math>n</math> was active it is switched off.</p> <p>The diagnosis flags are latched until they have been cleared by SPI command <math>CMD.CPL = 1</math>.</p>   |
| Over Load<br>(Short Circuit) | <p>When over load is detected at channel <math>n</math>, the affected channel is switched off after time <math>t_{OFF(OVL)}</math> and the dedicated diagnosis flag <math>D_n</math> is set.</p> <p>The diagnosis flags are latched until they have been cleared by SPI command <math>CMD.CPL = 1</math>.</p>                           |

## 8.1 Electrical Characteristics

Unless otherwise specified:

$V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

typical values:  $V_{BAT} = 13.5\text{ V}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos.   | Parameter   | Symbol          | Limit Values |      |      | Unit    | Test Conditions                   |
|--|---|-----------------|--------------|------|------|---------|-----------------------------------|
|  |   |                 | min.         | typ. | max. |         |                                   |
| OFF State Diagnosis  |   |                 |              |      |      |         |                                   |
| 8.1.1  | Open load diagnosis delay time  | $t_{d(OL)}$     | 100          | —    | 250  | $\mu s$ | —                                 |
| High Side Channels 0,1,2,3   |   |                 |              |      |      |         |                                   |
| 8.1.2  | Open load detection threshold voltage for Channel 0,1,2,3                   | $V_{D(OL0..3)}$ | 3            | 4    | 5    | V       | 1)                                |
| 8.1.3  | Output diagnosis current channel 0,1,2,3                                    | $I_{L(DC0..3)}$ | 100          | 200  | 300  | $\mu A$ | measured at $V_{D(OL)}$ threshold |
| Configurable Channels 4,5  |   |                 |              |      |      |         |                                   |
| 8.1.4  | Open load detection threshold voltage for Channel 4,5 in all configurations | $V_{D(OL4,5)}$  | 3            | 4    | 5    | V       | 1)                                |
| 8.1.5  | Output diagnosis current channel 4,5 in high side configuration             | $I_{L(DCHS)}$   | 100          | 200  | 300  | $\mu A$ | measured at $V_{D(OL)}$ threshold |
| 8.1.6  | Output diagnosis current channel 4,5 in low side configuration              | $I_{L(DCLS)}$   | 100          | 200  | 300  | $\mu A$ | measured at $V_{D(OL)}$ threshold |
| Low side Channels 6,7  |   |                 |              |      |      |         |                                   |
| 8.1.7  | Open load detection threshold voltage for Channel 6,7                       | $V_{D(OL6,7)}$  | 3            | 4    | 5    | V       | 1)                                |
| 8.1.8  | Output diagnosis current channel 6,7  | $I_{L(DC6,7)}$  | 100          | 200  | 300  | $\mu A$ | measured at VOL threshold         |
| ON State Diagnosis (see also Protection in <a href="#">Chapter 7</a> ) |   |                 |              |      |      |         |                                   |
| 8.1.9  | Over load detection current at channel 0,1,4,5,6,7                          | $I_{L(OVL)}$    | 0.5          | —    | 1.0  | A       | —                                 |
| 8.1.10   | Over load detection current at channel 2,3                                  | $I_{L(OVL)}$    | 0.22         | —    | 0.5  | A       | —                                 |
| 8.1.11   | Over load detection delay time at all channels                              | $t_{OFF(OVL)}$  | —            | —    | 60   | $\mu s$ | —                                 |

1) Open load detection voltages are referenced to ground

## 8.2 Command Description

**Diagnosis Registers** (read only, register bank RB = 1)

### DR01 00<sub>B</sub>

| 3          | 2         | 1          | 0         |
|------------|-----------|------------|-----------|
| <b>OL1</b> | <b>D1</b> | <b>OL0</b> | <b>D0</b> |
| r          | r         | r          | r         |

### DR23 01<sub>B</sub>

| 3          | 2         | 1          | 0         |
|------------|-----------|------------|-----------|
| <b>OL3</b> | <b>D3</b> | <b>OL2</b> | <b>D2</b> |
| r          | r         | r          | r         |

### DR45 10<sub>B</sub>

| 3          | 2         | 1          | 0         |
|------------|-----------|------------|-----------|
| <b>OL5</b> | <b>D5</b> | <b>OL4</b> | <b>D4</b> |
| r          | r         | r          | r         |

### DR67 11<sub>B</sub>

| 3          | 2         | 1          | 0         |
|------------|-----------|------------|-----------|
| <b>OL7</b> | <b>D7</b> | <b>OL6</b> | <b>D6</b> |
| r          | r         | r          | r         |

| Field             | Bits | Type | Description  |
|-------------------|------|------|--|
| Dn<br>n = 7 to 0  | 2, 0 | r    | <b>Diagnostic Feedback of Channel n</b><br>0 normal operation<br>1 over load or over temperature switch off occurred |
| OLn<br>n = 7 to 0 | 3, 1 | r    | <b>Open Load Detection of Channel n</b><br>0 normal operation<br>1 Open load at OFF-state occurred                   |

### CMD

#### Command Register 110<sub>B</sub>

| 3           | 2          | 1          | 0          |
|-------------|------------|------------|------------|
| <b>Wake</b> | <b>STB</b> | <b>RST</b> | <b>CPL</b> |
| r/w         | r/w        | r/w        | r/w        |

| Field | Bits | Type | Description   |
|-------|------|------|---|
| CPL   | 0    | r/w  | please refer to <a href="#">Section 7</a> for description   |
| RST   | 1    | r/w  | please refer to <a href="#">Section 5.3</a> for description |
| STB   | 2    | r/w  | please refer to <a href="#">Section 5</a> for description   |
| Wake  | 3    | r/w  | please refer to <a href="#">Section 5</a> for description   |

### Diagnosis Current Configuration Register

DCCR0

100<sub>B</sub>

| 3     | 2     | 1     | 0     |
|-------|-------|-------|-------|
| DCEN3 | DCEN2 | DCEN1 | DCEN0 |
| r/w   | r/w   | r/w   | r/w   |

DCCR1

101<sub>B</sub>

| 3     | 2     | 1     | 0     |
|-------|-------|-------|-------|
| DCEN7 | DCEN6 | DCEN5 | DCEN5 |
| r/w   | r/w   | r/w   | r/w   |

| Field               | Bits   | Type | Description  |
|---------------------|--------|------|--|
| DCENn<br>n = 7 to 0 | 3 to 0 | r/w  | <b>Diagnosis Current Enable Channel n</b><br><b>0</b> Diagnosis current disabled<br><b>1</b> Diagnosis current enabled |

## 9 Serial Peripheral Interface (SPI)

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and  $\overline{\text{CS}}$ . Data is transferred by the lines SI and SO at the data rate given by SCLK. The falling edge of  $\overline{\text{CS}}$  indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of  $\overline{\text{CS}}$ . A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. The interface provides daisy chain capability.

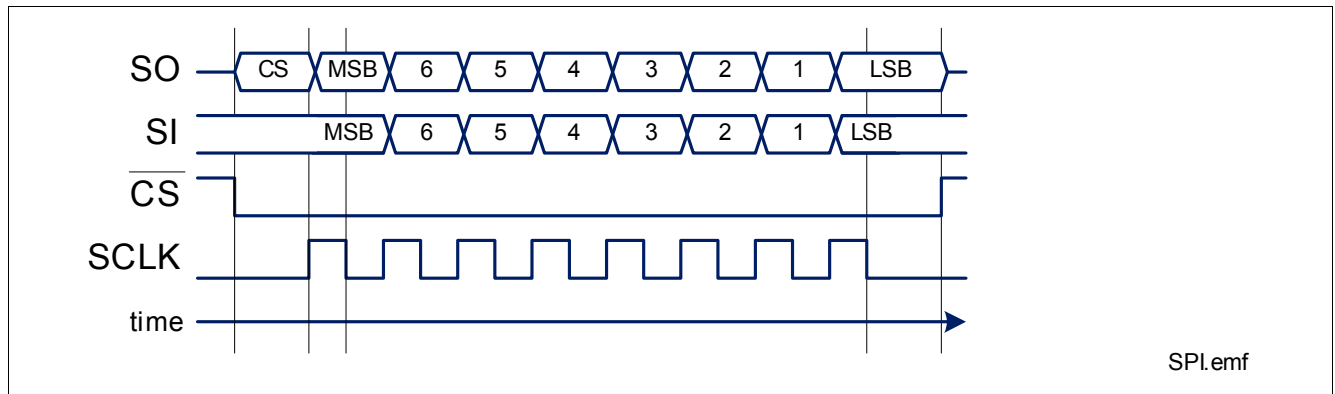


Figure 8 Serial Peripheral Interface

The SPI protocol is described in [Section 9.3](#). It is reset to the default values after reset.

### 9.1 SPI Signal Description

**$\overline{\text{CS}}$  - Chip Select:** The system micro controller selects the TLE7239SL by means of the  $\overline{\text{CS}}$  pin. Whenever the pin is in low state, data transfer can take place. When  $\overline{\text{CS}}$  is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

**$\overline{\text{CS}}$  High to Low transition:** 

- The diagnosis information is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. As a result, even in daisy chain configuration, a high signal indicates a faulty transmission. For details, please refer to [Figure 9](#). This information stays available to the first rising edge of SCLK.

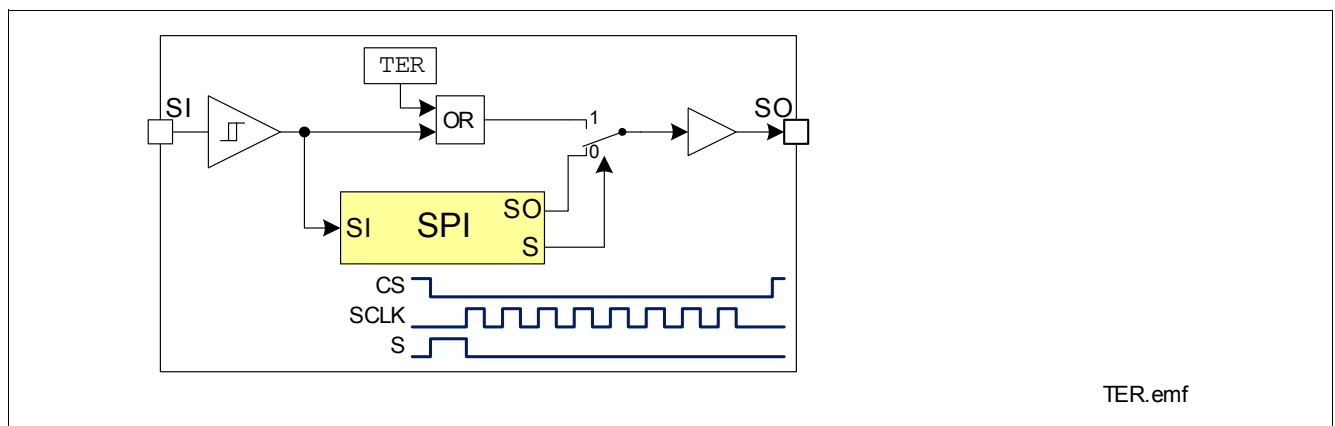


Figure 9 Transmission Error Flag on SO Line

### $\overline{CS}$ Low to High transition:

- Command decoding is only done, when after the falling edge of  $\overline{CS}$  exactly a multiple (1, 2, 3, ...) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag ( $TER$ ) is set and the command is ignored.
- Data from shift register is transferred into the input matrix register.

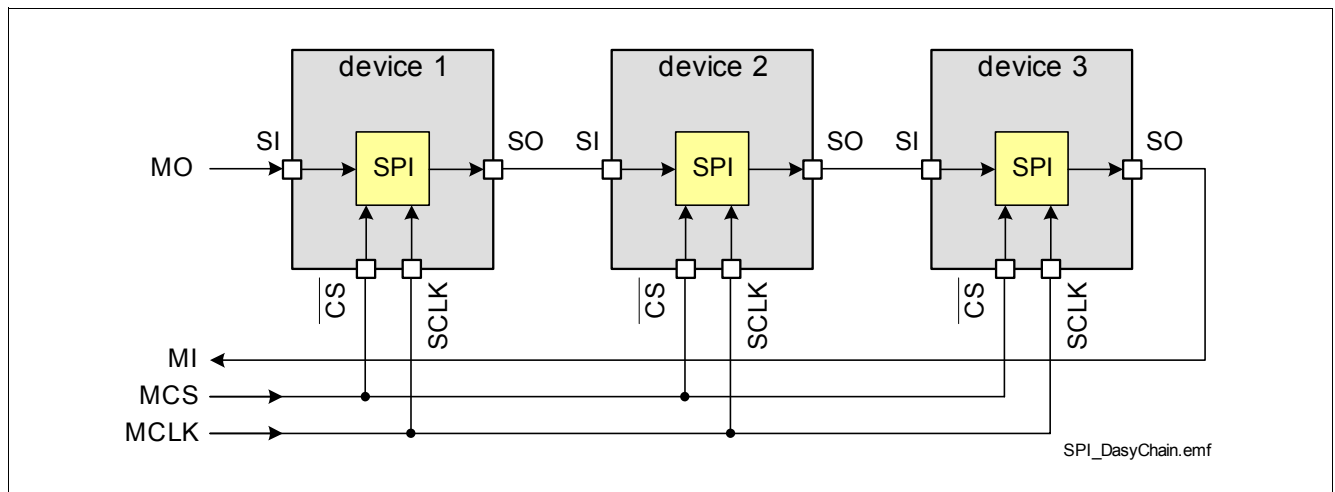
**SCLK - Serial Clock:** This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select  $\overline{CS}$  makes any transition.

**SI - Serial Input:** Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The 8 bit input data consist of two parts (control and data). Please refer to [Section 9.3](#) for further information.

**SO Serial Output:** Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the  $\overline{CS}$  pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to [Section 9.3](#) for further information.

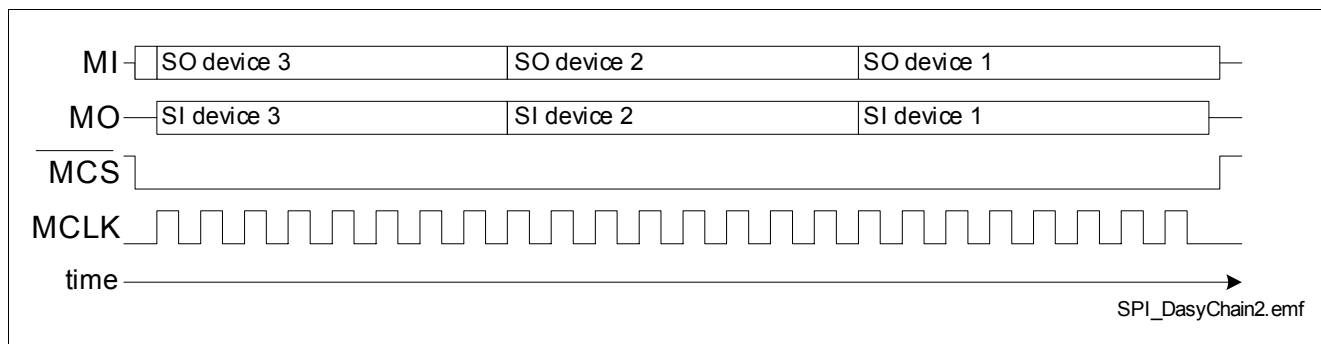
## 9.2 Daisy Chain Capability

The SPI of TLE7239SL provides daisy chain capability. In this configuration several devices are activated by the same  $\overline{CS}$  signal MCS. The SI line of one device is connected with the SO line of another device (see [Figure 10](#)), which builds a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK, which is connected to the SCLK line of each device in the chain.



**Figure 10** Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out can be seen at SO. After 8 SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the  $\overline{CS}$  line must go high to make the device accept the transferred data. In daisy chain configuration the data shifted out at device #1 has been shifted in to device #2. When using three devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the  $\overline{MCS}$  line must go high (see [Figure 11](#)).



**Figure 11 Data Transfer in Daisy Chain Configuration**

### 9.3 SPI Protocol

The control and diagnosis function of the TLE7239SL is based on two register banks which are accessed via following SPI protocol. The control register bank contains eight registers (with 4 bit each) addressed by a 3 bit pointer. The diagnosis register bank contains four registers (with 4 bit each) addressed by a 2 bit pointer. An additional indication bit is available to differentiate between standard diagnosis information and data read from a register bank.

#### Control and Diagnosis Mode

|                              | CS <sup>1)</sup> | 7 | 6              | 5                | 4  | 3    | 2   | 1   | 0   |
|------------------------------|------------------|---|----------------|------------------|----|------|-----|-----|-----|
| Write Register Command       |                  |   |                |                  |    |      |     |     |     |
| SI                           |                  | 1 | ADDR           |                  |    | DATA |     |     |     |
| Read Register Command        |                  |   |                |                  |    |      |     |     |     |
| SI                           |                  | 0 | ADDR           |                  |    | x    | x   | 0   | RB  |
| Read Standard Diagnosis      |                  |   |                |                  |    |      |     |     |     |
| SI                           |                  | 0 | x              | x                | x  | x    | x   | 1   | x   |
| Standard Diagnosis           |                  |   |                |                  |    |      |     |     |     |
| SO                           | TER              | 0 |                | AWK              | LH | D67  | D45 | D23 | D01 |
| Second Frame of Read Command |                  |   |                |                  |    |      |     |     |     |
| SO                           | TER              | 0 | 1              | ADDR (Diagnosis) |    | DATA |     |     |     |
| SO                           | TER              | 1 | ADDR (Control) |                  |    | DATA |     |     |     |

1) This bit is valid between CS hi -> lo and first SCLK lo -> hi transition.

*Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame, the output at SPI signal SO will contain the requested information. Any command can be executed in the second frame.*



| Field       | Bits | Type | Description  |
|-------------|------|------|--|
| <b>TER</b>  |      |      | <b>Transmission Error</b><br>0 Previous transmission was successful (modulo 8 clocks received)<br>1 Previous transmission failed or first transmission after reset |
| <b>RB</b>   | 0    |      | <b>Register Bank</b><br>0 CONTR Control Register Bank<br>1 DIAG Diagnosis Register Bank (read only)  |
| <b>ADDR</b> | 6:4  |      | <b>Address</b><br>Pointer to register for read and write command   |
| <b>DATA</b> | 3:0  |      | <b>Data</b><br>Data written to or read from register selected by address ADDR  |

#### Standard Diagnosis:

| Field      | Bits       | Type | Description   |
|------------|------------|------|---|
| <b>AWK</b> | 5          |      | <b>Awake, Device active</b>                                       |
| <b>LH</b>  | 4          |      | <b>Limp home mode active</b>                                      |
| <b>Dxy</b> | 3, 2, 1, 0 |      | <b>Failure mode alert of channel x and y (Overtemp, Overload)</b> |
| <b>OL</b>  | ?          |      | <b>common open load flag for all channels</b>                     |

## 9.4 Register Overview

### Control Register Bank

| Name   | Addr             | 3     | 2     | 1     | 0                 | default <sup>1)</sup> | type |
|--------|------------------|-------|-------|-------|-------------------|-----------------------|------|
| ICR01  | 000 <sub>B</sub> | INX1  |       | INX0  |                   | 0 <sub>H</sub>        | r/w  |
| ICR23  | 001 <sub>B</sub> | INX3  |       | INX2  |                   | 0 <sub>H</sub>        | r/w  |
| ICR45  | 010 <sub>B</sub> | INX5  |       | INX4  |                   | 0 <sub>H</sub>        | r/w  |
| ICR67  | 011 <sub>B</sub> | INX7  |       | INX6  |                   | 0 <sub>H</sub>        | r/w  |
| DCCR0  | 100 <sub>B</sub> | DCEN3 | DCEN2 | DCEN1 | DCEN0             | 0 <sub>H</sub>        | r/w  |
| DCCR1  | 101 <sub>B</sub> | DCEN7 | DCEN6 | DCEN5 | DCEN4             | 0 <sub>H</sub>        | r/w  |
| CMD    | 110 <sub>B</sub> | WAKE  | STB   | RST   | CPL <sup>2)</sup> | 0 <sub>H</sub>        | w    |
| unused | 111 <sub>B</sub> | –     | –     | –     | –                 | 0 <sub>H</sub>        | –    |

1) The default values are set after  $V_{bb}$  power-on, STB-command and RST-command

All command bits are cleared at the end of transmission, respectively after execution

2) CPL bit needs a valid next SPI communication frame to be cleared

### Input word (see Chapter 6.6 for detailed description)

| Name        | State      | 1        | 0        |
|-------------|------------|----------|----------|
| INX0 - INX7 | <b>OFF</b> | <b>0</b> | <b>0</b> |
|             | IN1        | 0        | 1        |
|             | IN2 or IN3 | 1        | 0        |
|             | ON         | 1        | 1        |

Diagnosis Register Bank (read only)

| Name | Addr             | 3   | 2  | 1   | 0  |
|------|------------------|-----|----|-----|----|
| DR01 | 000 <sub>B</sub> | OL1 | D1 | OL0 | D0 |
| DR23 | 001 <sub>B</sub> | OL3 | D3 | OL2 | D2 |
| DR45 | 010 <sub>B</sub> | OL5 | D5 | OL4 | D4 |
| DR67 | 011 <sub>B</sub> | OL7 | D7 | OL6 | D6 |

## 9.5 Timing Diagrams

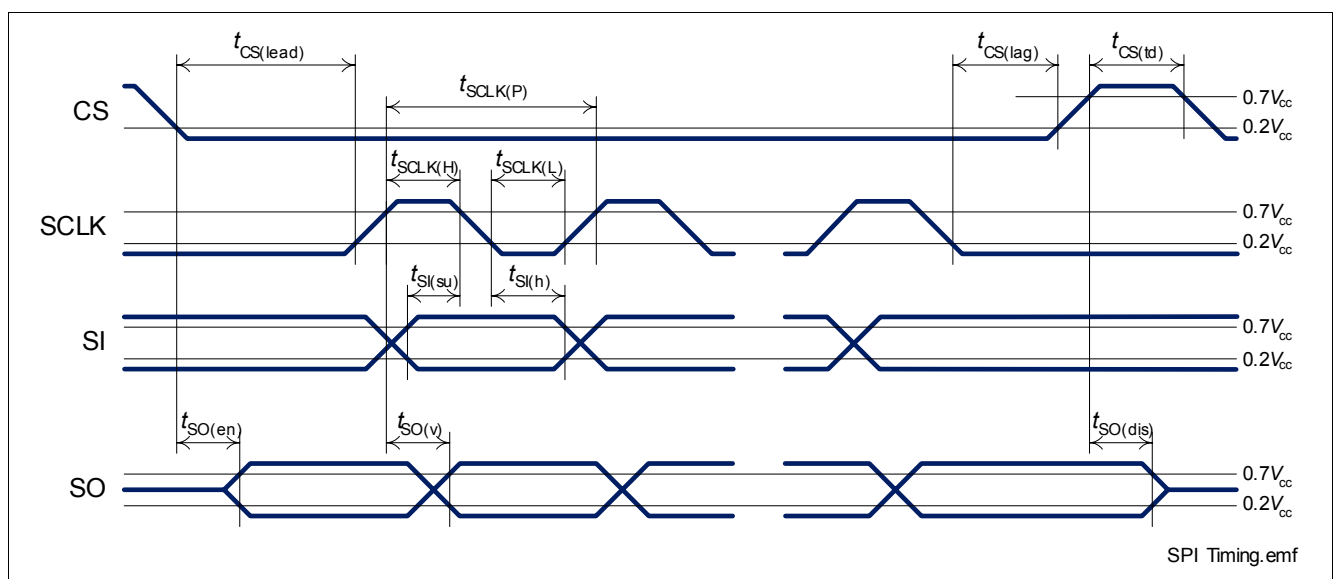


Figure 12 Timing Diagram

## 9.6 Electrical Characteristics

Unless otherwise specified:  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$

typical values:  $V_{DD} = 5.0\text{ V}$ ,  $V_{BAT} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos. | Parameter | Symbol | Limit Values |      |      | Unit | Test Conditions |
|------|-----------|--------|--------------|------|------|------|-----------------|
|      |           |        | min.         | typ. | max. |      |                 |

### Input Characteristics ( $\overline{CS}$ , SCLK, SI)

|       |   |   |                    |    |                    |               |  |
|-------|---|---|--------------------|----|--------------------|---------------|--|
| 9.6.1 | L level of pin<br>$\overline{CS}$<br>SCLK<br>SI     | $V_{CS(L)}$<br>$V_{SCLK(L)}$<br>$V_{SI(L)}$ | 0                  | –  | $0.2 \cdot V_{DD}$ | V             | –  |
| 9.6.2 | H level of pin<br>$\overline{CS}$<br>SCLK<br>SI     | $V_{CS(H)}$<br>$V_{SCLK(H)}$<br>$V_{SI(H)}$ | $0.5 \cdot V_{DD}$ | –  | $V_{DD}$           | V             | –  |
| 9.6.3 | L-input pull-up current through $\overline{CS}$     | $I_{CS(L)}$                                 | 5                  | 40 | 90                 | $\mu\text{A}$ | $V_{CS} = 0\text{ V}$<br>$V_{DD} = 5\text{ V}$                                   |
| 9.6.4 | H-input pull-up current through $\overline{CS}$     | $I_{CS(H)}$                                 | 2.5                | –  | –                  | $\mu\text{A}$ | <sup>1)</sup><br>$V_{DD} = 5\text{ V}$<br>$V_{CS} = 0.5 \cdot V_{DD}$            |
| 9.6.5 | L-input pull-down current through pin<br>SCLK<br>SI | $I_{SCLK(L)}$<br>$I_{SI(L)}$                | 1.5                | –  | –                  | $\mu\text{A}$ | <sup>1)</sup><br>$V_{DD} = 5\text{ V}$<br>$V_{SCLK} = V_{SI} = 0.2 \cdot V_{DD}$ |
| 9.6.6 | H-input pull-down current through pin<br>SCLK<br>SI | $I_{SCLK(H)}$<br>$I_{SI(H)}$                | 10                 | 40 | 80                 | $\mu\text{A}$ | <sup>1)</sup><br>$V_{DD} = 5\text{ V}$<br>$V_{SCLK} = V_{SI} = V_{DD}$           |

### Output Characteristics (SO)

|       |                                 |               |                         |   |          |               |                           |
|-------|---------------------------------|---------------|-------------------------|---|----------|---------------|---------------------------|
| 9.6.7 | L level output voltage          | $V_{SO(L)}$   | 0                       | – | 0.4      | V             | $I_{SO} = +2\text{ mA}$   |
| 9.6.8 | H level output voltage          | $V_{SO(H)}$   | $V_{DD} - 0.4\text{ V}$ | – | $V_{DD}$ |               | $I_{SO} = -1.5\text{ mA}$ |
| 9.6.9 | Output tristate leakage current | $I_{SO(OFF)}$ | -10                     | – | 10       | $\mu\text{A}$ | $V_{CS} = V_{DD}$         |

### Timings

|        |  |                |     |   |   |     |               |
|--------|--|----------------|-----|---|---|-----|---------------|
| 9.6.10 | Serial clock frequency   | $f_{SCLK}$     | 0   | – | 5 | MHz | –             |
| 9.6.11 | Serial clock period  | $t_{SCLK(P)}$  | 200 | – | – | ns  | –             |
| 9.6.12 | Serial clock high time   | $t_{SCLK(H)}$  | 50  | – | – | ns  | <sup>1)</sup> |
| 9.6.13 | Serial clock low time  | $t_{SCLK(L)}$  | 50  | – | – | ns  | <sup>1)</sup> |
| 9.6.14 | Enable lead time (falling $\overline{CS}$ to rising SCLK)                | $t_{CS(lead)}$ | 250 | – | – | ns  | <sup>1)</sup> |
| 9.6.15 | Enable lag time (falling SCLK to rising $\overline{CS}$ )                | $t_{CS(lag)}$  | 250 | – | – | ns  | <sup>1)</sup> |
| 9.6.16 | Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$ ) | $t_{CS(td)}$   | 250 | – | – | ns  | <sup>1)</sup> |
| 9.6.17 | Data setup time (required time SI to falling SCLK)                       | $t_{SI(su)}$   | 20  | – | – | ns  | <sup>1)</sup> |
| 9.6.18 | Data hold time (falling SCLK to SI)                                      | $t_{SI(h)}$    | 20  | – | – | ns  | <sup>1)</sup> |

Unless otherwise specified:  $V_{DD} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{BAT} = 9.0\text{ V to }16\text{ V}$ ,  $T_j = -40\text{ °C to }+150\text{ °C}$   
 typical values:  $V_{DD} = 5.0\text{ V}$ ,  $V_{BAT} = 13.5\text{ V}$ ,  $T_j = 25\text{ °C}$

| Pos.   | Parameter   | Symbol               | Limit Values |      |      | Unit | Test Conditions           |
|--------|---|----------------------|--------------|------|------|------|---------------------------|
|        |   |                      | min.         | typ. | max. |      |                           |
| 9.6.19 | Output enable time (falling $\overline{\text{CS}}$ to SO valid)     | $t_{\text{SO(en)}}$  | –            | –    | 200  | ns   | $C_L = 20\text{ pF}^{1)}$ |
| 9.6.20 | Output disable time (rising $\overline{\text{CS}}$ to SO tri-state) | $t_{\text{SO(dis)}}$ | –            | –    | 200  | ns   | $C_L = 20\text{ pF}^{1)}$ |
| 9.6.21 | Output data valid time with capacitive load                         | $t_{\text{SO(v)}}$   | –            | –    | 100  | ns   | $C_L = 20\text{ pF}^{1)}$ |

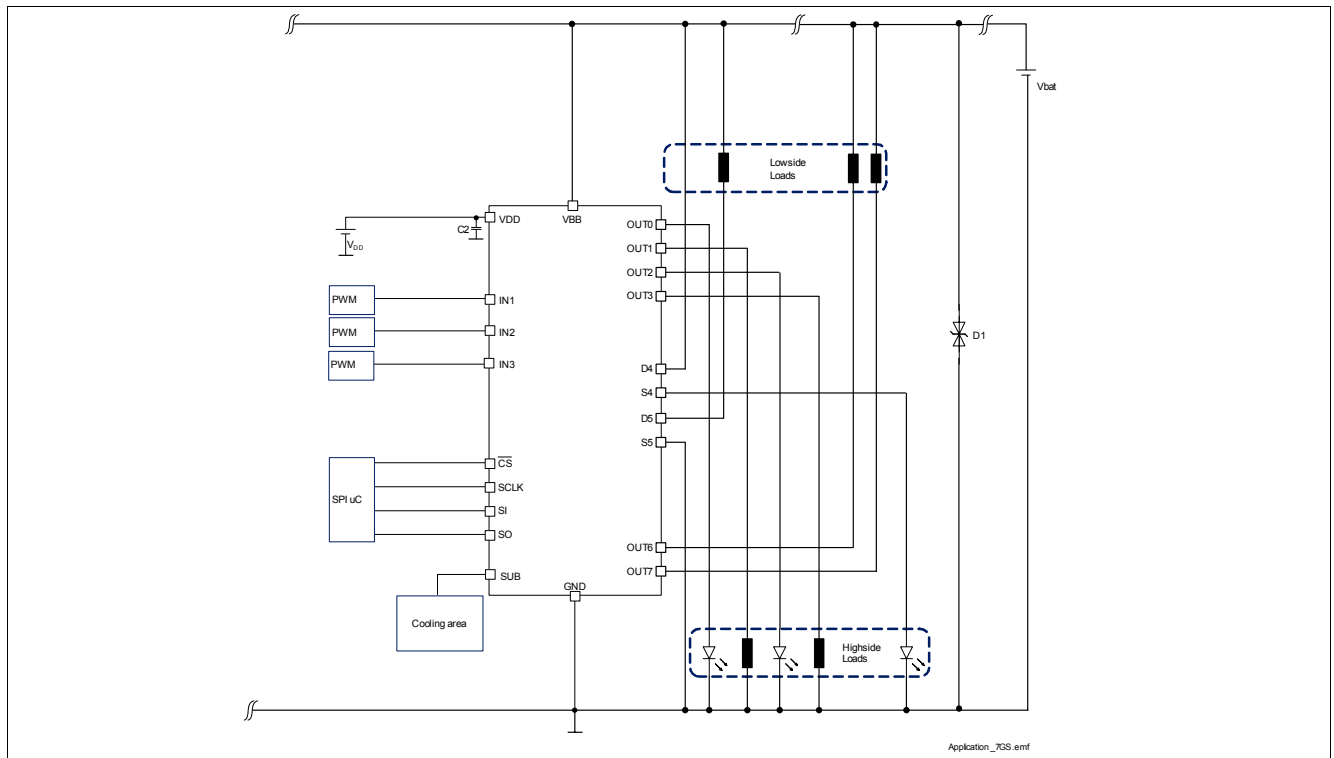
1) Not subject to production test, specified by design.



## 11 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

**Figure 14** shows a simplified application circuit. V<sub>DD</sub> need to be externally reverse polarity protected.



**Figure 14 Application Diagram**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

The circuit above shows a example of using this device in a automotive target application.

D1 is optional for loss of battery or loss of ground if no other circuit on this battery feed can limit the voltage to the max. rating of the device (-40 V) .

C2 is for EMC and to stabilize the digital driver, recommended value is 47nF.

There are no resistors to the  $\mu$ C needed due to the internal reverse polarity protection.

For further information you may contact <http://www.infineon.com/spider>

## 12 Revision History

| Revision | Date       | Changes            |
|----------|------------|--------------------|
| Rev. 1.0 | 2010-02-18 | Datasheet released |



**Edition 2010-02-18**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

**© 2008 Infineon Technologies AG  
All Rights Reserved.**

### **Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

### **Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### **Warnings**

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.