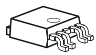
5-V Low Drop Voltage Regulator

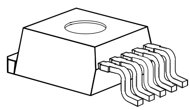
TLE 7270

Features

- Output voltage 5 V ±2%
- Ultra low current consumption: typ. 20µA
- 300 mA current capability
- Reset Feature
- Very low-drop voltage
- Short-circuit-proof
- Suitable for use in automotive electronics



P-TO252-5-1



P-TO263-5-1

Functional Description

The TLE 7270 is a monolithic integrated low-drop voltage regulator which can supply loads up to 300 mA. An input voltage up to 42 V is regulated to $V_{Q,nom}$ = 5.0 V with a precision of ±2%. Due to its integrated reset circuitry featuring a 2-step adjustable power on timing and output voltage monitoring the IC is well suited for µ-controller supplies. The sophisticated design allows to achieve stable operation even with ceramic output capacitors down to 470 nF. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions. Of course the TLE 7270 can be used also in all other applications, where a stabilized 5 V voltage is required. Due to its ultra low current consumption the TLE 7270 is dedicated for use in applications permanently connected to V_{BAT}. An integrated output sink current circuitry keeps the voltage at the Output pin Q below 5.5 V even when reverse currents are applied. Thus connected devices are protected from overvoltage damage. For applications requiring extremely low noise levels the Infineon voltage regulator family TLE 42XY and TLE 44XY is more suited than the TLE 7270. A mV-range output noise on the TLE 7270 caused by the charge pump operation is unavoidable due to the ultra low quiescent current concept.

Type	Ordering Code	Package
TLE 7270 D	Q67006-A9670	P-TO252-5-1
TLE 7270 G	on request	P-TO263-5-1

Reset

The Reset pin informs e.g. the microcontroller in case the output voltage has fallen below the lower threshold V_{RT} of typ. 4.65 V. The hysteresis is typically 100mV. Connecting the regulator to a battery voltage at first the reset signal remains LOW. When the output voltage has reached the reset threshold V_{RT} the reset output RO remains still LOW for the reset delay time t_{rd} adjustable in 2 steps via the DT Pin. Afterwards the reset output turns HIGH.

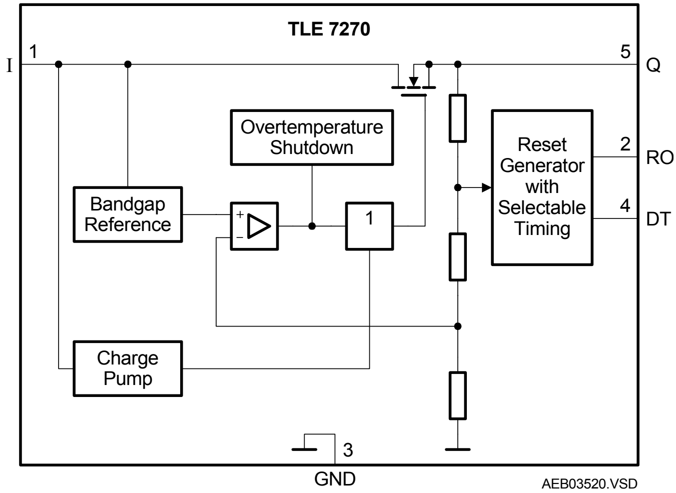


Figure 1 Block Diagram

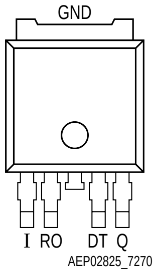


Figure 2 Pin Configuration P-TO252-5-1 (D-PAK), P-TO263-5-1 (top view)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	**Input;** block to ground directly at the IC with a ceramic capacitor.
2	RO	**Reset Output**. Open Collector Output with integrated pull-up resistor of typically 30kΩ. Optional external pull-up resistor of ≥ 10 kΩ to pin Q.
3	GND	**Ground;** Pin 3 internally connected to heatsink.
4	DT	**Delay Time;** connect to Q or GND to choose reset delay time.
5	Q	**Output;** block to ground with a ceramic capacitor, $C \geq 470$ nF.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Input I					
Voltage	V_I	-0.3	45	V	–
Current	I_I	-1	–	mA	–
Output Q					
Voltage	V_Q	-0.3	5.5	V	–
Voltage	V_Q	-0.3	6.2	V	t < 10 s[1)]
Current	I_Q	-1	–	mA	–
Reset Output RO					
Voltage	V_{RO}	-0.3	5.5	V	–
Voltage	V_{RO}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{RO}	-1	1	mA	–
Delay Time DT					
Voltage	V_{DT}	-0.3	5.5	V	–
Voltage	V_{DT}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{DT}	-1	1	mA	–
Temperature					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

1) Exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_I	5.5	42	V	–
Junction temperature	T_j	-40	150	°C	–

Note: In the operating range, the functions given in the circuit description are fulfilled.

Table 4 Thermal Resistance

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Junction case	$R_{thj\text{-}c}$	–	10[1]	K/W	–
Junction ambient	$R_{thj\text{-}a}$	–	80[1]	K/W	TO252[2]
Junction ambient	$R_{thj\text{-}a}$	–	55[1]	K/W	TO263[3]

1) Target values need to be verified
2) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm³, heat sink area 300 mm²

3) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm³, heat sink area 300 mm²

Table 5 Electrical Characteristics

V_I = 13.5 V; – 40 °C < T_j < 150 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Output Q						
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA<I_Q<300 mA; 6 V < V_I < 16 V
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA<I_Q<100 mA; 6 V < V_I < 40 V
Output current limitation	I_Q	320	–	–	mA	[1]
Output current limitation	I_Q			800	mA	V_Q =0V
Current consumption; $I_q = I_I - I_Q$	I_q	–	20	30	µA	I_Q = 0.1 mA; T_j = 25 °C
Current consumption; $I_q = I_I - I_Q$	I_q	–	–	40	µA	I_Q = 0.1 mA; $T_j \leq$ 80 °C
Drop voltage	V_{dr}	–	200	500	mV	I_Q = 200 mA $V_{dr} = V_I - V_Q$[1]
Load regulation	$\Delta V_{Q,\ lo}$	– 40	15	40	mV	I_Q = 5 mA to 250 mA
Line regulation	$\Delta V_{Q,\ li}$	– 20	5	20	mV	V_I = 10 V to 32 V; I_Q = 5 mA

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Power supply ripple rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Temperature output voltage drift	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	–
Output Capacitor	C_Q	470	–	–	nF	ESR < 3 Ω
Reset Output RO						
Reset switching threshold	V_{RT}	4.50	4.65	4.80	V	V_Q decreasing V_i = 6V
Reset output low voltage	V_{ROL}	–	0.2	0.4	V	R_{RO} = 10 kΩ; V_Q > 1 V
Internal reset pull up resistor	$R_{R,int}$	15	30	45	kΩ	
External reset pull up resistor	$R_{R,ext}$	10		∞[2]	kΩ	see Fig. 3
Reset delay time	t_{rd}	10	16	22	ms	DT connected to GND
Reset delay time	t_{rd}	80	128	176	ms	DT connected to Q
Reset reaction time	t_{rr}	–	–	12	µs	–

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

2) An external reset pull up resistor is not required.

Application Information

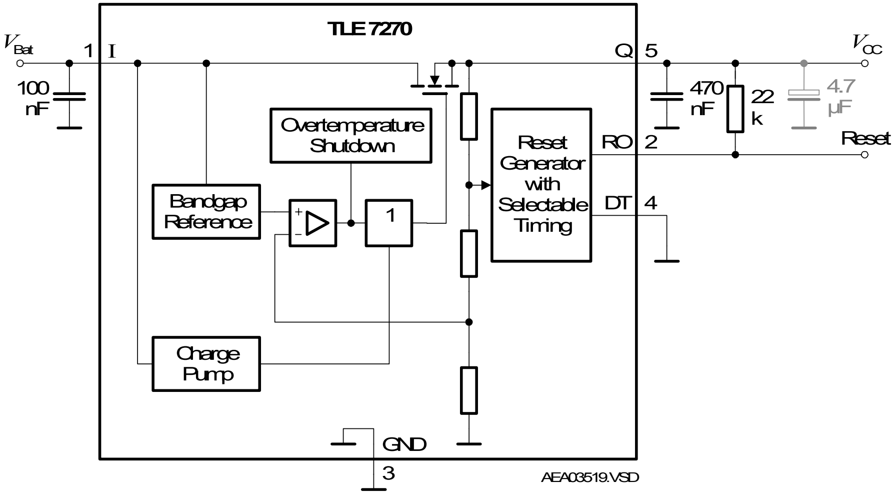


Figure 3 Application Diagram

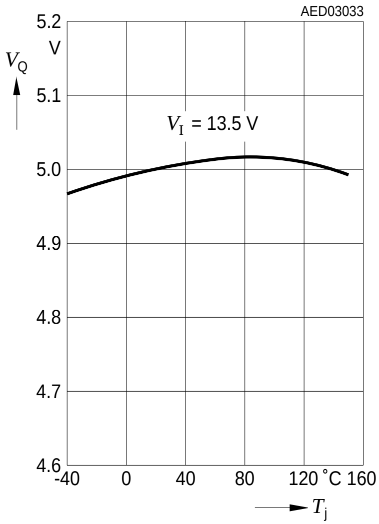
Input, Output

An input capacitor is necessary for damping line influences. A resistor of approx. 1 Ω in series with C_I, can damp the LC of the input inductivity and the input capacitor.

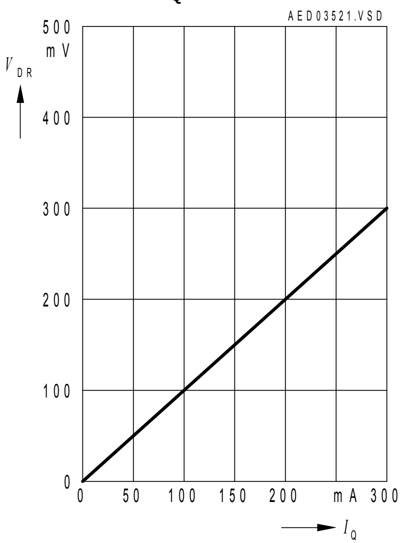
The TLE 7270 requires a ceramic output capacitor of at least 470 nF to assure stability of the regulation loop. In order to damp influences resulting from load current surges it is recommended to add an additional electrolytic capacitor of 4.7 µF to 47 µF at the output as shown in **Figure 3**.

Typical Performance Characteristics

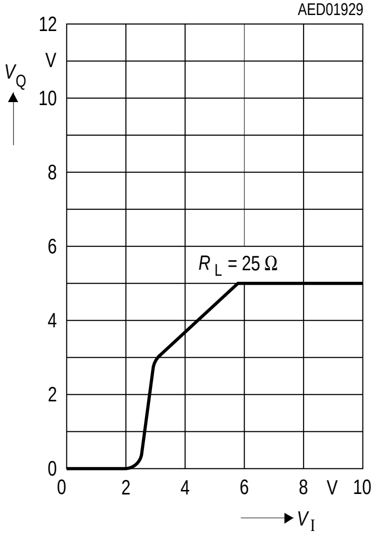
Output Voltage V_Q versus Temperature T_j



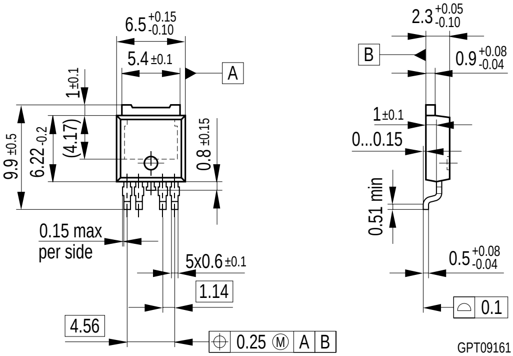
Drop Voltage V_{DR} versus Output Current I_Q



Output Voltage V_Q versus
Input Voltage V_I



Package Outlines



All metal surfaces tin plated, except area of cut.

Figure 4 **P-TO252-5-1** (Plastic Transistor Single Outline)

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Dimensions in mm

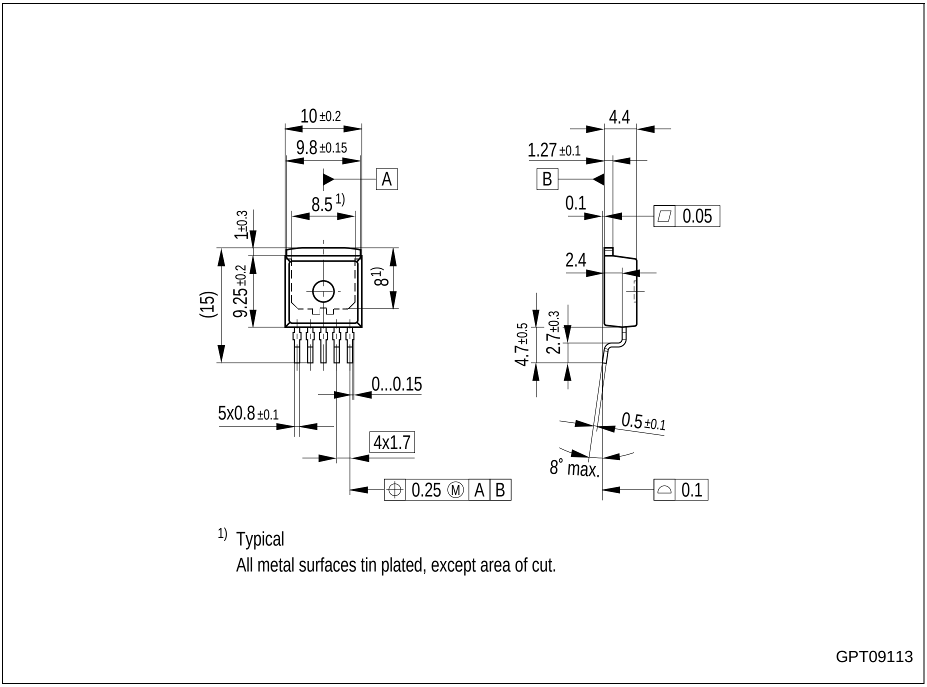

Figure 5 **P-TO263-5-1** (Plastic Transistor Single Outline)

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Dimensions in mm

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Previous Version: 1.02

Page	Subjects (major changes since last revision)
	minor text modifications