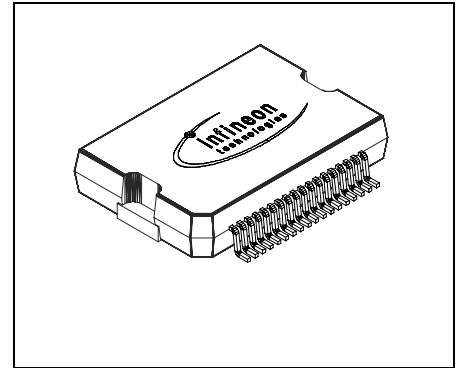**Door Module Power IC**
TLE 8201R

Data Sheet Rev. 2.0

Features

- Full bridge (150mΩ) for main doorlock motor
- Two half-bridges (400mΩ) for deadbolt and mirror position motor or mirror fold motor
- Two half-bridges (800mΩ) for mirror position
- High-side switch (100mΩ) for mirror defrost
- Four high-side switches (500mΩ) for 5W and 10W lamps
- Current sense analog output with multiplex
- All outputs with short circuit protection and diagnosis
- Over-temperature protection with warning
- Open load diagnosis for all outputs
- Charge pump-Output for n-channel MOS-FET reverse-polarity protection
- Very low current consumption in sleep mode
- Standard 16-bit SPI for control and diagnosis
- Over-and Undervoltage Lockout
- Power-SO package with full-size heatslug for excellent low thermal resistance

Type	Ordering Code	Package/Shipment
TLE 8201R	-	PG-DSO-36-27

Functional Description

The TLE 8201R is an Application Specific Standard Product for automotive door-module applications. It includes all the power stages necessary to drive the loads in a typical front door application, i.e. central lock, deadlock or mirror fold, mirror position, mirror defrost and 5W or 10W lamps, e.g for turn signal, courtesy/warning or control panel illumination. It is designed as a monolithic circuit in Infineons mixed technology SPT which combines bipolar and CMOS control circuitry with DMOS power devices.

Short circuit and over-temperature protection and a detailed diagnosis are in line with the safety requirements of automotive applications. The current sense output allows to improve the total system performance. The standard SPI interface saves microcontroller I/O lines while still giving flexible control of the power stages and a detailed diagnosis.

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1　Block Diagram

Figure 1　Block Diagram

2   Pin Configuration

2.1   Pin Assignment

cooling tab
(GND)

Left				Right
GND	1		36	**GND**
OUT5	2		35	n.c.
OUT6	3		34	**OUT4**
Vs	4		33	**Vs**
INH	5		32	**OUT7**
PWM1	6		31	**OUT7**
PWM2	7		30	**Vs**
ISO	8		29	**OUT8**
Vcc	9		28	**OUT9**
DO	10		27	CP
CLK	11		26	**Vs**
CSN	12		25	**OUT10**
DI	13		24	**OUT11**
GO	14		23	**Vs**
Vs	15		22	OUT3
OUT1	16		21	OUT2
OUT1	17		20	OUT2
GND	18		19	**GND**

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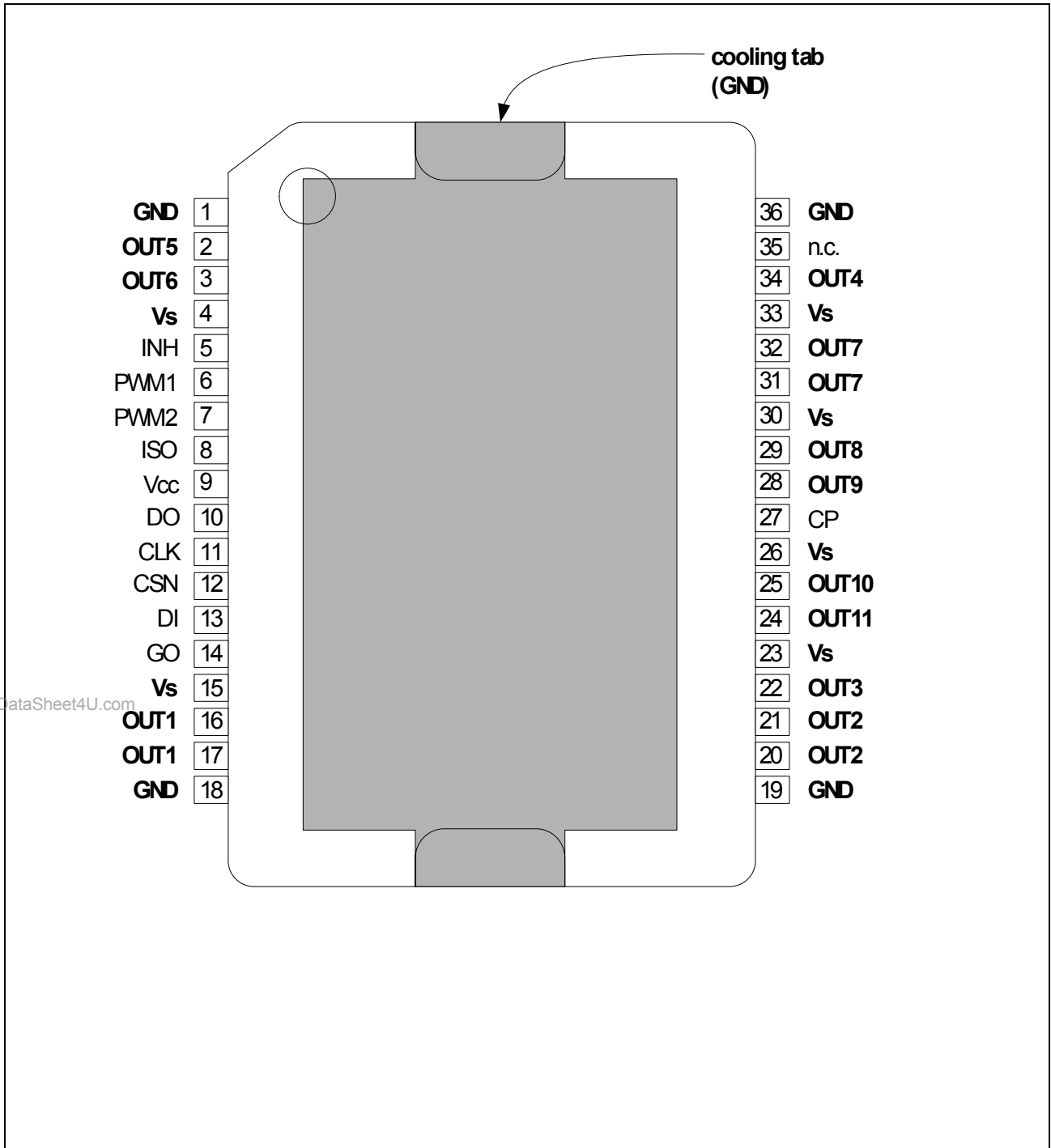
Figure 2   Pin Configuration PG-DSO-36-27

2.2 Pin Definitions and Functions

Pin	Symbol	Function
cooling tab	GND	**Cooling tab**, internally connected to GND; to reduce thermal resistance place cooling areas and thermal vias on PCB.
1, 18, 19, 36	GND	**Ground;** internally connected to cooling tab (heat slug).
2	OUT5	**Power-Output of half-bridge 5;** DMOS half-bridge
3	OUT6	**Power-Output of half-bridge 6;** DMOS half-bridge.
4, 15, 23, 26, 30, 33	Vs	**Power supply**; needs decoupling capacitors to GND. > 47μF electrolytic in parallel with 100nF ceramic is recommended. All Vs pins must be connected externally
5	INH	**Inhibit**; active low. Sets the device in sleep mode with low current consumption when left open or pulled to LOW. Has an internal pull down current source
6	PWM1	**Logic Input for direct power stage control**; direct input to control the high-side switches selected by the SPI xsel1 bits in control register CtrlReg01
7	PWM2	**Logic Input for direct power stage control**; direct input to control the switches selected by the SPI xsel2 bits in control register CtrlReg11
8	ISO	**Current sense output**; Mirrors the current of the high-side switch selected by the current sense multiplexer control bits ISx
9	Vcc	**Logic Supply Voltage**; needs decoupling capacitors to GND (pin 1). 10μF electrolytic in parallel with 10nF ceramic is recommended
10	DO	**Serial Data Output**; Transfers data to the master when the chip is selected by CSN=LOW. Data transmission is synchronized by CLK, DO state is changed on the rising edge of CLK. The most significant bit (MSB) is transferred first. The pin is tristated as long as CSN=HIGH
11	CLK	**Serial Data Clock Input;** Receives the clock signal from the master and clocks the SPI shift register. Has an internal pull down current source
12	CSN	**Serial Port Chip Select Not Input**; SPI communication is enabled by pulling CSN to LOW. CLK must be LOW during the transition of CSN. The CSN-pin has an internal pull-up current source

Pin Configuration

Pin	Symbol	Function
13	DI	**Serial Data Input**; Receives serial data from the master when the chip is selected by CSN=LOW. Data transmission is synchronized by CLK. Data are accepted on the falling edge of CLK. The LSB is transferred first. The DI-pin has an internal pull-down current source.
14	GO	**Gate Out**; Charge pump output to drive the gate of external n-channel MOS-FET for reverse polarity protection
16, 17	OUT1	**Power-Output of half-bridge 1**; DMOS half-bridge.
20, 21	OUT2	**Power-Output of half-bridge 2**; DMOS half-bridge.
22	OUT3	**Power-Output of half-bridge 3;** DMOS half-bridge
24	OUT11	**Power Output of high-side switch 11**; DMOS high-side switch
25	OUT10	**Power Output of high-side switch 10**; DMOS high-side switch
27	CP	**Charge Pump;** pin for optional external charge-pump reservoir capacitor. 3.3 nF to Vs is recommended
28	OUT9	**Power-Output of high-side switch 9;** DMOS high-side switch
29	OUT8	**Power-Output of high-side switch 8;** DMOS high-side switch
31, 32	OUT7	**Power Output of high-side switch 7**; DMOS high-side switch
34	OUT4	**Power-Output of half-bridge 4;** DMOS half-bridge
35	n.c.	**Not connected**

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
3.1.1	Supply voltage	V_S	-0.3	40	V	–
3.1.2	Logic supply Voltage	V_{CC}	-0.3	5.5	V	–
3.1.3	Logic input- and output Voltages		-0.3	5.5	V	–
3.1.4	Voltage at GO-pin	V_{GO}	-16	$V_S + 5$	V	–
3.1.5	Junction temperature	T_j	-40	150	°C	–
3.1.6	Storage temperature	T_{stg}	-50	150	°C	–
3.1.7	ESD capability of power stage output and V_S pins	V_{ESD}	–	4	kV	Human Body Model according to ANSI EOS\ESD S5.1 standard (eqv. to MIL STD 883D and JEDEC JESD22-A114)
3.1.8	ESD capability of logic pins and ISO pin	V_{ESD}	–	2	kV	

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Operating Range

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
3.2.1	Supply voltage	V_S	5	40	V	Including over-voltage lockout
3.2.2	Supply voltage	V_S	5	20	V	Functional
3.2.3	Supply voltage	V_S	8	20	V	Parameter Specification
3.2.4	Logic supply voltage	V_{CC}	4.75	5.5	V	–
3.2.5	SPI clock frequency	f_{CLK}	–	2	MHz	–
3.2.6	Junction temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the limit given at the table.

3.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
3.3.1	Junction pin	R_{thjC}	–	1.5	K/W	–
3.3.2	Junction ambient	R_{thjA}	–	50	K/W	minimal footprint

4 Block Description and Electrical Characteristics

4.1 Power Supply

4.1.1 General

The TLE 8201R has two power supply inputs: All power drivers are connected to the supply voltage V_S which is connected to the automotive 12 V board-net. The internal logic part is supplied by a separate Voltage V_{CC} = 5 V.

The advantage of this system is that information stored in the logic remains intact in the event of short-term failures in the supply voltage V_S. The system can therefore continue to operate after V_S has recovered, without having to be reprogrammed.

A rising edge on V_{CC} triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All data stored internally is deleted, and the outputs are switched to high-impedance status (tristate).

4.1.2 Sleep-Mode

The TLE 8201R can be put in a low current-consumtion mode by setting the input INH to LOW. The INH pin has an internal pull-down current source. In sleep-mode, all output transistors are turned off and the SPI is not operating. When enabling the IC by setting INH from L to H, a Power-On Reset is performed as described above.

4.1.3 Reverse Polarity

The TLE 8201R requires an external reverse polarity protection. The gate-driver (charge-pump output) for an external n-channel logic-level MOS-FET is integrated. The gate voltage is provided at pin GO which should be connected as shown in the application diagram.

4.1.4 Electrical Characteristics

Electrical Characteristics

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
Current Consumption							
4.1.1	Supply current	I_S	–	3.0	7.0	mA	–
4.1.2	Logic supply current	I_{CC}	–	5	10	mA	SPI not active

Block Description and Electrical Characteristics

Electrical Characteristics

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.1.3	Quiescent current	I_S	–	2.5	5	µA	INH = L,
4.1.4	Logic quiescent current	I_{CC}	–	0.2	1	µA	V_S = 14 V, $V_{OUT7-11}$ = 0V;
4.1.5	Total quiescent current	$I_S + I_{cc}$	–	3	6	µA	T_j < 85 °C

Charge Pump-output for Reverse-Polarity Protection FET (GO)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.1.6	Gate-Voltage	V_{GO} - V_S	5	–	8	V	I_{GO} = 50 µA
4.1.7	Setup-time	t_{GO}	–	–	1	ms	–
4.1.8	Reverse leakage current	I_{lkGO}	–	–	5	µA	V_S = 0 V V_{GO} = -14 V

4.2 Monitoring Functions

4.2.1 Power Supply Monitoring

The power supply Voltage V_S is monitored for over- and under voltage.

- **Under Voltage**
  If the supply voltage V_S drops below the switch off voltage $V_{UV\,OFF}$, all output transistors are switched off and the power supply fail bit PSF is set. The error is not latched, i.e. if V_S rises again and reaches the switch on voltage $V_{UV\,ON}$, the power stages are restarted and the error bit is reset.

- **Over Voltage**
  If the supply voltage V_S rises above the switch off voltage $V_{OV\,OFF}$, all output transistors are switched off and the power supply fail bit (bit 7 of the SPI diagnosis word) is set. The error is not latched, i.e. if V_S falls again and reaches the switch on voltage $V_{OV\,ON}$, the power stages are restarted and the error is reset.

4.2.1.1 Characteristics Power Supply Monitoring

Electrical Characteristics

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.2.1	UV-Switch-ON voltage	V_{UVON}	–	–	5.2	V	V_S increasing
4.2.2	UV-Switch-OFF voltage	V_{UVOFF}	4.0	–	5.0	V	V_S decreasing
4.2.3	UV-ON/OFF-Hysteresis	V_{UVHY}	–	0.25	–	V	V_{UVON} - V_{UVOFF}
4.2.4	OV-Switch-OFF voltage	V_{OVOFF}	21	–	25	V	V_S increasing
4.2.5	OV-Switch-ON voltage	V_{OVON}	20	–	24	V	V_S decreasing
4.2.6	OV-ON/OFF-Hysteresis	V_{OVHY}	0.5	1	–	V	V_{OVOFF} - V_{OVON}

4.2.2 Temperature Monitoring

Temperature sensors are integrated in the power stages. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds. If one or more temperature sensors reach the warning temperature, the temperature warning bit TW is set to HIGH. This bit is not latched (i.e. if the temperature falls below the warning threshold (with hysteresis), the TW bit is reset to LOW again).

If one or more temperature sensors reach the shut-down temperature, the outputs are shut down as described in the next paragraph and the temperature shut-down bit TSD is set to HIGH. The shutdown is latched (i.e. the output stages remain off and the TSD bit set high until a SRR command is sent or a power-on reset is performed).

The power-stages are subdivided into two groups for over-temperature shut-down:

• **Group1**: OUT 1, OUT 2 and OUT 3
• **Group2**: OUT 4 to 11

If one or more temperature sensors within a group reaches the shutdown threshold, all outputs within the group are switched off, while the other outputs continue normal operation.

4.2.2.1 Characteristics Temperature Monitoring

Electrical Characteristics

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.2.7	Thermal warning junction temperature[1]	T_{jW}	120	145	170	°C	–
4.2.8	Temperature warning hysteresis[1]	ΔT	–	30	–	K	–
4.2.9	Thermal shutdown junction temperature[1]	T_{jSD}	150	175	200	°C	–
4.2.10	Thermal switch-on junction temperature[1]	T_{jSO}	120	–	170	°C	–
4.2.11	Temperature shutdown hysteresis[1]	ΔT	–	30	–	K	–
4.2.12	Ratio of SD to W temperature[1]	T_{jSD} / T_{jW}	1.05	1.20	–	–	–

[1] Not subject to production test, specified by design

4.2.3 Current Sense

A current proportional to the output current that flows from the selected power output to GND is provided at the ISO (I sense out) pin. The output selection is done via the SPI. The sense current can be transformed into a voltage by an external sense resistor and provided to an A/D converter input (see section application).

4.2.3.1 Characteristics Current Sense

Electrical Characteristics

$8\ V < V_S < 20\ V$; $4.75\ V < V_{CC} < 5.25\ V$; INH = High; all outputs open;
$-40\ °C < T_j < 150\ °C$; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
HS1, HS2 (Register IS = 000, 001)							
4.2.13	Output voltage range	V_{ISO12}	0	–	3	V	$V_{CC} = 5\ V$
4.2.14	Current Sense Ratio	k_{ILIS12}	–	2000	–	–	$k_{ILIS} = I_{OUT}/I_{ISO}$ $I_{OUT} > 3\ A$
4.2.15	Current Sense accuracy	$k_{ILISacc12}$	–	–	10	%	
4.2.16	Matching	Δk_{ILIS12}	-6	1	2	%	$\Delta k_{ILIS12} = (k_{ILIS1} - k_{ILIS2}) / k_{ILIS1}$
HS3, HS4 (Register IS = 010, 011)							
4.2.17	Output voltage range	V_{ISO34}	0	–	3	V	$V_{CC} = 5\ V$
4.2.18	Current Sense Ratio	k_{ILIS34}	–	1000	–	–	$k_{ILIS} = I_{OUT}/I_{ISO}$ $I_{OUT} > 1.5\ A$
4.2.19	Current Sense accuracy	$k_{ILISacc}$	–	–	10	%	
HS7 (Register IS = 100)							
4.2.20	Output voltage range	V_{ISO7}	0	–	3	V	$V_{CC} = 5\ V$
4.2.21	Current Sense Ratio for HS7	k_{ILIS7}	–	2000	–	–	$k_{ILIS} = I_{OUT}/I_{ISO}$ $I_{OUT} > 2A$
4.2.22	Current Sense accuracy	$k_{ILISacc}$	–	–	10	%	

4.3 SPI

4.3.1 General

The SPI is used for bidirectional communication with a control unit. The TLE 8201R acts as SPI-slave and the control unit acts as SPI-master. The 16-bit control word is read via the DI serial data input. The status word appears synchronously at the DO serial data output. The communication is synchronized by the serial clock input CLK.

Standard data transfer timing is shown in **Figure 3**. The clock polarity is data valid on falling edge. CLK must be low during CSN transition. The transfer is MSB first.

The transmission cycle begins when the chip is selected with the chip-select-not (CSN) input (H to L). Then the data is clocked through the shift register. The transmission ends when the CSN input changes from L to H and the word which has been read into the shift register becomes the control word. The DO output switches then to tristate status, thereby releasing the DO bus circuit for other uses. The SPI allows to parallel multiple SPI devices by using multiple CSN lines. The SPI can also be used with other SPI-devices in a daisy-chain configuration.
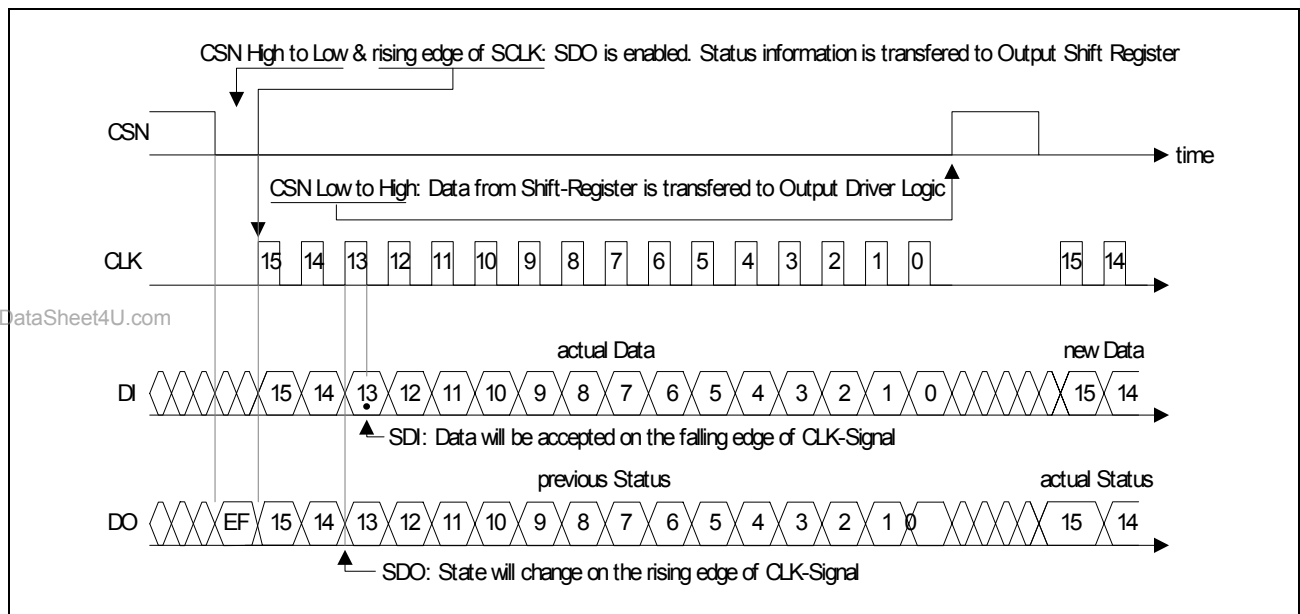
Figure 3   SPI standard data transfer timing

4.3.2 Register Address

The 16-bit SPI frame is composed of an addressable block, an address-independent block and a 2-bit address as shown in **Figure 4**.

The control word transmitted from the master to the TLE 7201R is executed at the end of the SPI transmission (CSN L -> H) and remains valid until a different control word is transmitted or a power on reset occurs. At the beginning of the SPI transmission (CSN

H ->L), the diagnostic data currently valid are latched into the SPI and transferred to the master. For Status Register address handling, please refer to **Section 4.3.4**
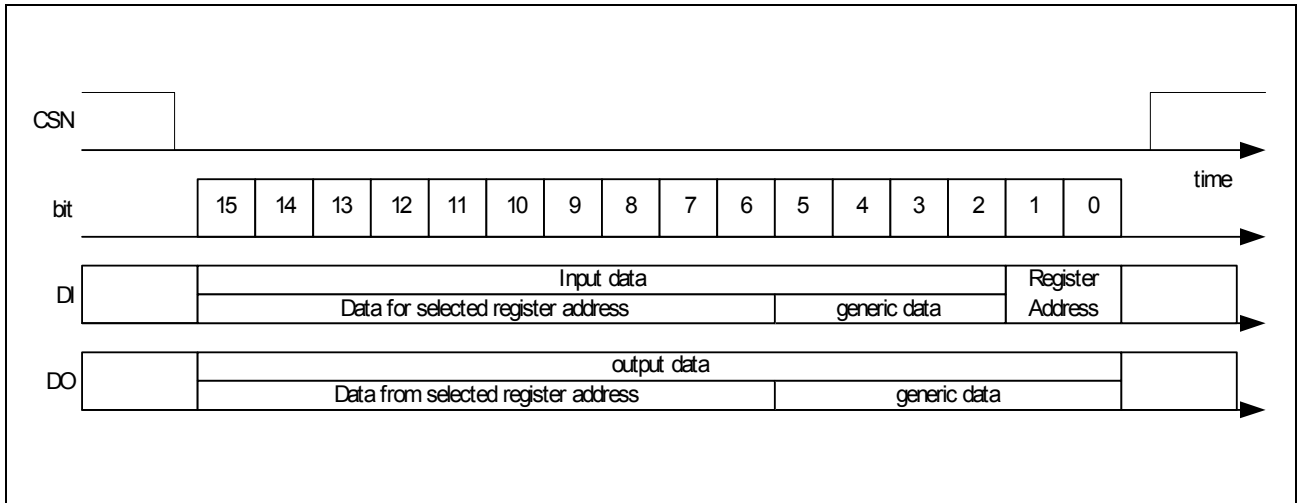

Figure 4   SPI structure

4.3.3 SPI bit definitions

4.3.3.1 Control - word

Table 1   **Input (Control) Data Register**

Bit	CtrlReg 00 Lock and Mirror heat control	CtrlReg 01 PWM1 input select	CtrlReg 10 Mirror and Lamp-driver control	CtrlReg 11 PWM2 input select
15	LS1ON	HS7sel1	LS4ON	HS7sel2
14	HS1ON	HS8sel1	HS4ON	HS8sel2
13	LS2ON	HS9sel1	LS5ON	HS9sel2
12	HS2ON	HS10sel1	HS5ON	HS10sel2
11	LS3ON	HS11sel1	LS6ON	HS11sel2
10	HS3ON	LS1sel1	HS6ON	LS1sel2
9	HS7ON	LS2sel1	HS8ON	LS2sel2
8	Testmode	LS3sel1	HS9ON	LS3sel2
7	Testmode	OpL7ON	HS10ON	OpL89ON
6	Testmode	Testmode	HS11ON	OpL1011ON
Address - independent data				
5	IS_2	IS_2	IS_2	IS_2
4	IS_1	IS_1	IS_1	IS_1
3	IS_0	IS_0	IS_0	IS_0
2	SRR	SRR	SRR	SRR
Address - bits				
1	RA_1 = 0	RA_1 = 0	RA_1 = 1	RA_1 = 1
0	RA_0 = 0	RA_0 = 1	RA_0 = 0	RA_0 = 1

Note: Testmode-bits must be set to L for normal operation

Table 2   Control bit definitions

Control Bit	Definition
LSxON	low-side switch no. x is turned ON (OFF) if this bit is set to HIGH (LOW)
HSxON	high-side switch no. x is turned ON (OFF) if this bit is set to HIGH (LOW)
xsel1	power switch x is selected to be switched by the PWM1 input.
xsel2	power switch x is selected to be switched by the PWM2 input
OpL7ON	the pull-up current for open-load detection on output 7 is switched on (off) if this bit is set to HIGH (LOW)
OpL89ON	the pull-up currents for open-load detection on outputs 8 and 9 are switched on (off) if this bit is set to HIGH (LOW)
OpL1011ON	the pull-up currents for open-load detection on outputs 10 and 11are switched on (off) if this bit is set to HIGH (LOW)

IS_x	the output for the current sense multiplexer is selected by these bits:				
	IS_2	**IS_1**	**IS_0**	**Power stage selected for current sense**
	0	0	0	HS1
	0	0	1	HS2
	0	1	0	HS3
	0	1	1	HS4
	1	0	0	HS7
	all others			no output selected ($I_{ISO} = 0$)

Control Bit	Definition
SRR	Status Register Reset. If set to high, the error bits of the selected status register are reset after transmission of the data in the next SPI frame (see <Fett>Section 4.3.4)
RA_x	Register Address, selects the control-register address for the current SPI transmission and the status-register address for the next SPI transmission

4.3.3.2 Diagnosis

Table 3 **Output (Status) Data Register**

Bit	StatReg 00 Lock and Mirror heat overload	StatReg 01 Lock and Mirror heat open load	StatReg 10 Mirror and Lamp-driver overload	StatReg 11 Mirror and Lamp-driver open load
	valid for input data RA = 00	valid for input data RA = 01	valid for input data RA = 10	valid for input data RA = 11
15	LS1OvL	LS1OpL	LS4OvL	LS4OpL
14	HS1OvL	n.c.	HS4OvL	n.c.
13	LS2OvL	LS2OpL	LS5OvL	LS5OpL
12	HS2OvL	n.c	HS5OvL	n.c.
11	LS3OvL	LS3OpL	LS6OvL	LS6OpL
10	HS3OvL	n.c.	HS6OvL	n.c.
9	HS7OvL	HS7OpL	HS8OvL	HS8OpL
8	n.c.	n.c.	HS9OvL	HS9OpL
7	n.c.	n.c.	HS10OvL	HS10OpL
6	n.c.	n.c.	HS11OvL	HS11OpL
Address - independent data				
5	PSF	PSF	PSF	PSF
4	TSD	TSD	TSD	TSD
3	TW	TW	TW	TW
Error Flags				
2	EF_11	EF_11	EF_11	EF_10
1	EF_10	EF_10	EF_01	EF_01
0	EF_01	EF_00	EF_00	EF_00

Note: n.c. bits are fixed LOW

Table 4   Status bit definitions

Status Bit	Definition
LSxOvL	Low-Side switch Over Load. Set to HIGH if low-side switch no. x is shut down due to overcurrent or over temperature
HSxOvL	High-Side switch Over Load. Set to HIGH if high-side switch no. x is shut down due to overcurrent or over temperature
LSxOpL	Low-Side switch open load. Set to HIGH if open load (undercurrent) is detected in low-side switch x
HSxOpL	High-Side switch Open Load. Set to HIGH if open load is detected in high-side switch x
PSF	Power Supply Fail. Set to HIGH if the Voltage at the Vs pin is below the Vs under-voltage threshold or above the Vs over-voltage threshold
TSD	one or more powerstages are shut down due to over temperature
TW	one or more powerstages have reached the warning temperature
EF_xy	Error Flag for StatReg xy. Set to HIGH if any bit is set to HIGH StatReg xy
n.c.	not connected. These bits may be used for test-mode purposes. They are set to fixed LOW in normal operation

4.3.4 Status Register Address selection and Reset

The SPI is using a standard shift-register concept with daisy-chain capability. Any data transmitted to the SPI will be available to the internal logic part at the end of the SPI transmission (CSN L -> H). To read a specific register, the address of the register is sent by the master to the SPI in a first SPI frame. The data that corresponds to this address is transmitted by the SPI DO during the following (second) SPI frame to the master. The default address for Status Register transmission after Power-ON Reset is 00.

The Status-Register-Reset command-bit is executed after the next SPI transmission. The three bits RA_0, RA_1 and SRR act as command to read and reset (or not reset) the addressed Status-Register. This is also explained in **Figure 5**.

The TSD status bit is not part of the adressable data but of the address independent data. When any of the status registers is reset, the TSD bit is reset, too.
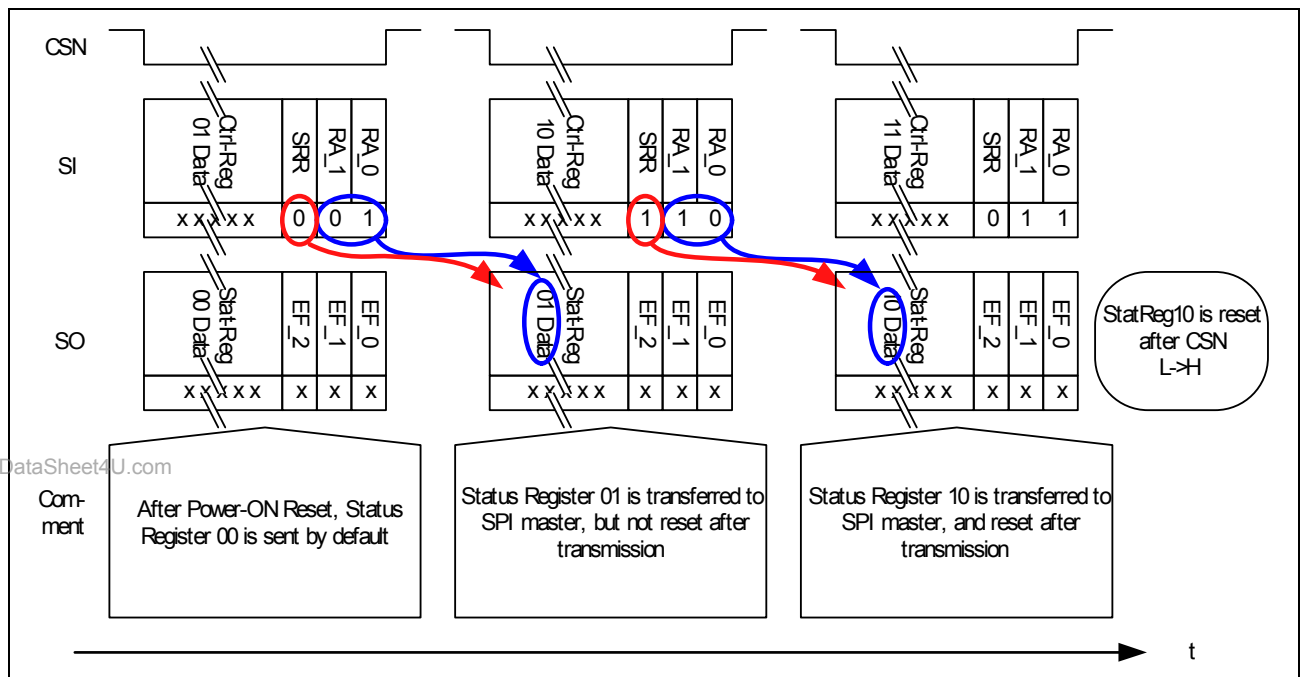
Figure 5   Status Register Addressing and Reset

4.3.4.1 Error-Flag

In addition to the 16 bits transferred from the TLE 7201R to the SPI master, an additional Error Flag (EF) is transmitted at the DO pin. The EF status is shown on the DO pin after CSN H->L, before the first rising edge at CLK, as shown in **Figure 6**.

The Error flag is set to H if any of the Status Registers contains an error message (i.e. EF = EF_00 or EF_01 or EF_10 or EF_11)
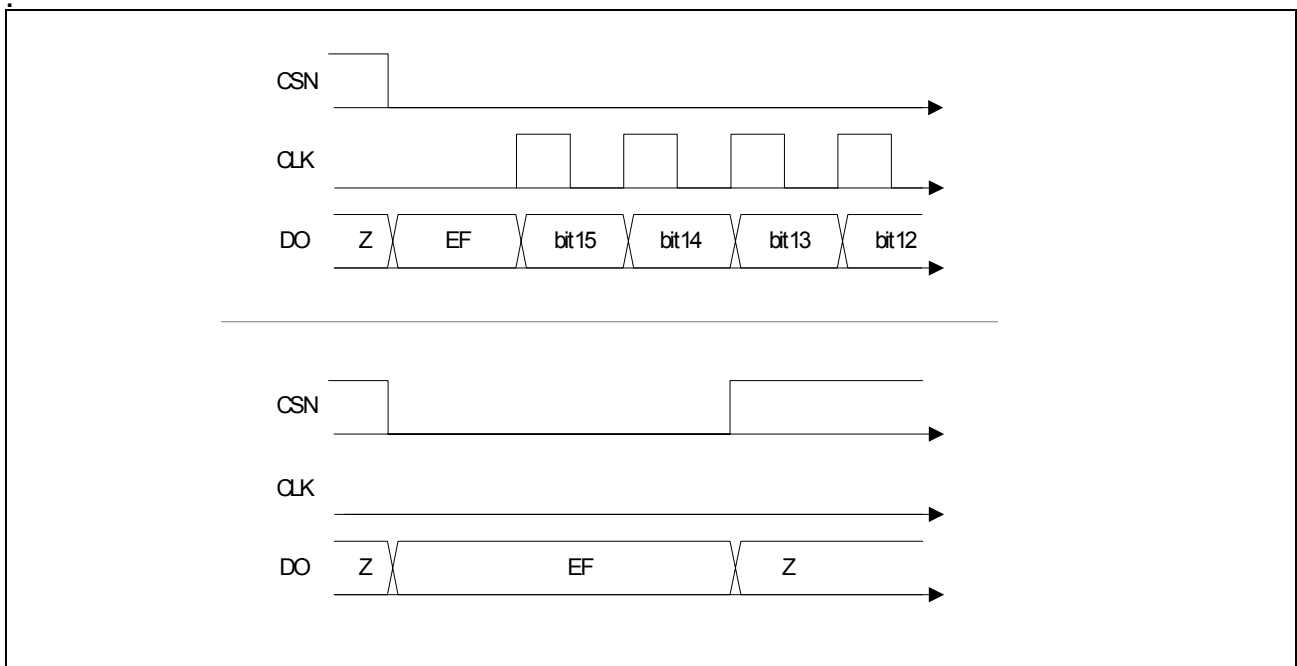
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Figure 6 **Error Flag transmission on DO during standard SPI transmission (top), or without additional SPI transmission, CLK low (bottom)**

4.3.5 Electrical Characteristics

Electrical Characteristics - SPI-timing

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.3.1	CSN lead time	t_{lead}	100	–	–	ns	1[1]
4.3.2	CSN lag time	t_{lag}	100	–	–	ns	2[1]
4.3.3	Fall time for CSN, CLK, DI, DO	t_f	–	–	25	ns	3[1]
4.3.4	Rise time for CSN, CLK, DI, DO	t_r	–	–	25	ns	4[1]

Electrical Characteristics - SPI-timing

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
4.3.5	DI data setup time	t_{SU}	40	–	–	ns	5[1]
4.3.6	DI data hold time	t_h	40	–	–	ns	6[1]
4.3.7	DI data valid time	t_v	–	–	50	ns	–[1]
4.3.8	DO data setup time	$t_{DOsetup}$	0	–	60	ns	7 and 8[1]
4.3.9	DO data hold time	t_{DOhold}	50	–	–	ns	9[1]
4.3.10	No-data-time between SPI commands	t_{nodata}	5	–	–	µs	10[1]
4.3.11	Clock frequency	f_{CL}	–	–	2	MHz	[1]
4.3.12	Duty cycle of incoming clock at CLK	–	40	–	60	%	–[1]

[1] SPI Timing is not subject to production test - specified by design. SPI functional test is performed at 5 MHz CLK frequency. Timing specified with an external load of 30pF at pin [DO].
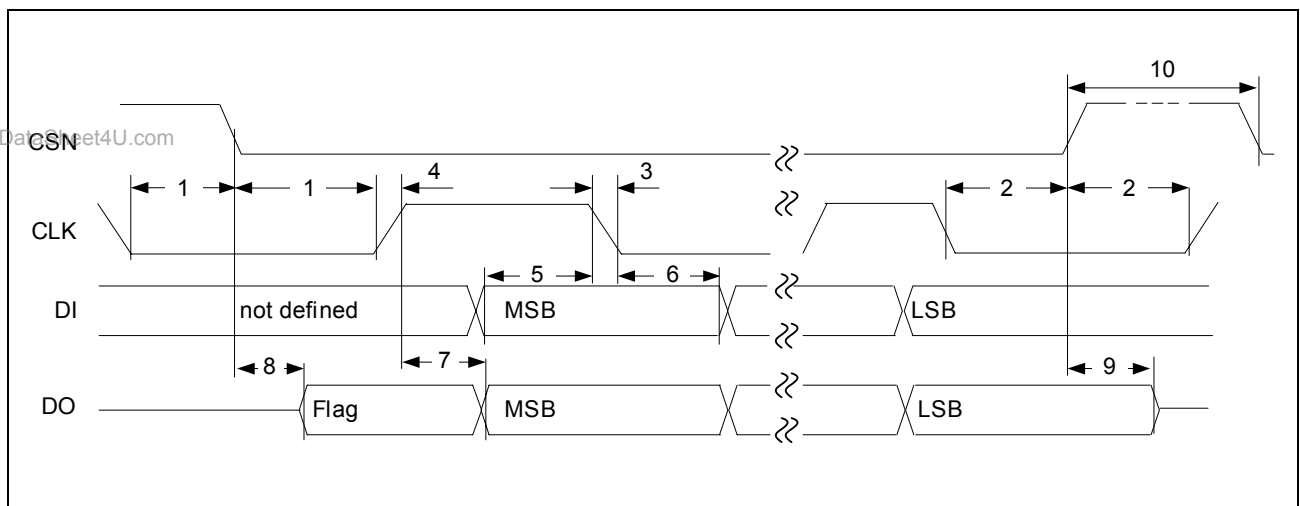

Figure 7   Timing Diagram

4.3.6   PWM inputs

The PWM inputs PWM1 and PWM2 are direct power stage control inputs that can be used to switch on and off one or more of the power transistors with a PWM signal supplied to this pin. The setting of the SPI Registers CtrlReg_01 and CtrlReg_11 defines which of the power stages will be controlled by the PWM inputs. If the selection-bits of

power Stage x, xsel1 and xsel2 are LOW, the power stage x is controlled only via the SPI control bit xON. If the selection bit xsel1 is HIGH and the control bit xON is also high, the power stage x is controlled by the PWM1 pin (xsel2 and PWM2, respectively). The behavior is shown in the pricipal schematic and truth table below. In terms of power dissipation due to switching loss, a PWM frequency below 200 Hz is recommended.
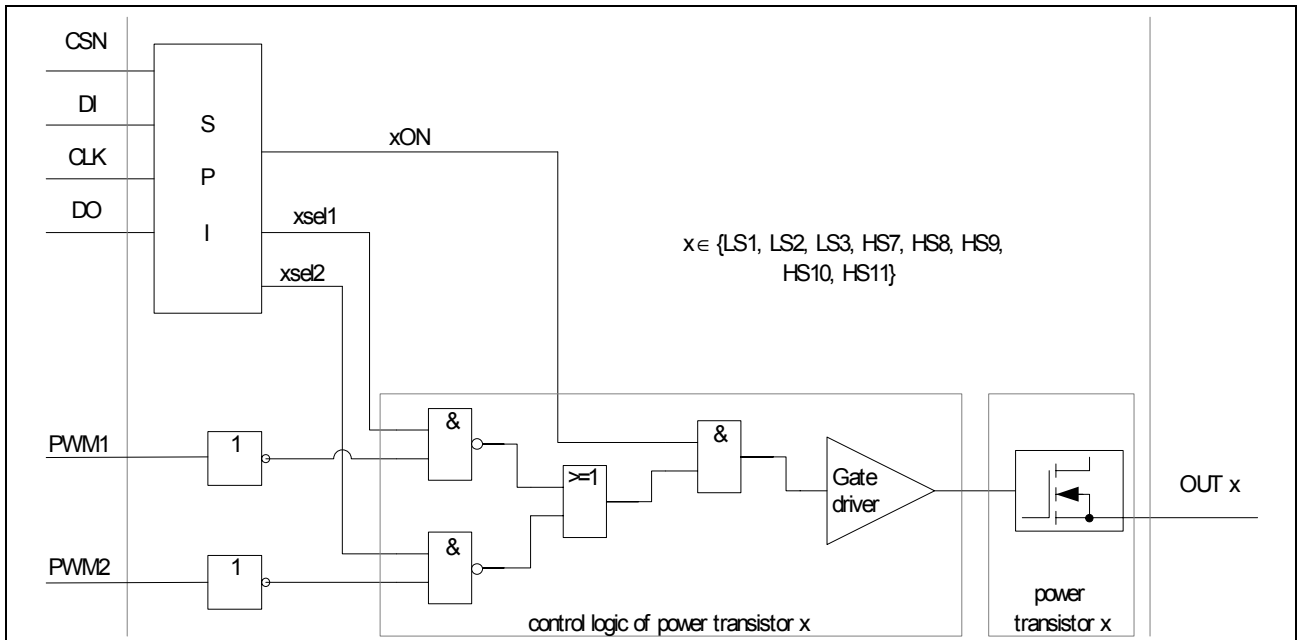

Figure 8   PWM input and SPI control registers

Truth-table for PWM inputs

xON	xsel1	xsel2	PWM1	PWM2	power stage x
0	x	x	x	x	OFF
1	0	0	x	x	ON
1	1	0	0	x	OFF
1	1	0	1	x	ON
1	0	1	x	0	OFF
1	0	1	x	1	ON
1	1	1	1	x	ON
1	1	1	x	1	ON
1	1	1	0	0	OFF

4.4 Power-Outputs 1-6 (Bridge Outputs)

4.4.1 Protection and Diagnosis

4.4.1.1 Short Circuit of Output to Ground or Vs

The low-side switches are protected against short circuit to supply and the high-side switches against short to GND.

If a switch is turned on and the current rises above the shutdown threshold I_{SD} for longer than the shutdown delay time t_{dSD}, the output transistor is turned off and the corresponding diagnosis bit is set. During the delay time, the current is limited to I_{SC} as shown in **Figure 9**.
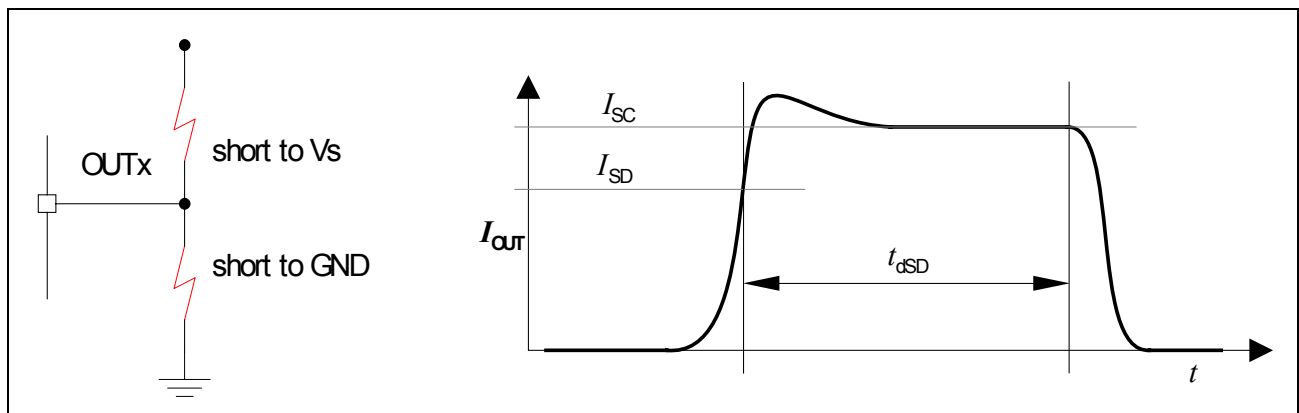
Figure 9   Short circuit protection

The delay time ia relatively short (typ. 25 µs) to limit the energy that is dissipated in the device during a short circuit. This scheme allows high peak-currents as required in motor-applications.

The output stage stays off and the error bit set until a status register reset is sent to the SPI or a power-on reset is performed.

4.4.1.2 Cross-Current

If for instance HS1 is ON and LS1 is OFF, you can turn OFF HS1 and turn ON LS1 with the same SPI command. To ensure that there is no overlap of the switching slopes that would lead to a cross current, the dead-time H to L and L to H is specified.

In the control registers, it is also possible to turn ON high- and low-side switches of the same half-bridge (e.g. LS1ON = H and HS1ON = H). To prevent a cross-current through the bridge, such a command is not executed. Instead, both switches are turned OFF and the Over-Load bit is set High for both switches (e.g. LS1OvL = H and HS1OvL = H).

4.4.1.3   Open Load

Open-load detection in ON-state is implemented in the low-side switches of the bridge outputs: When the current through the low side transistor is lower than the reference current I_{OCD} in ON-state for longer than the open-load detection delay time t_{dOC}, the according open-load diagnosis bit is set. The output transistor, however, remains ON. The open load error bit is latched and can be reset by the SPI status register reset or by a power-on reset.

As an example, if a motor is connected between outputs OUT 1 and OUT 2 with a broken wire as shown in **Figure 10**, the resulting diagnostic information is shown in **Table 5**
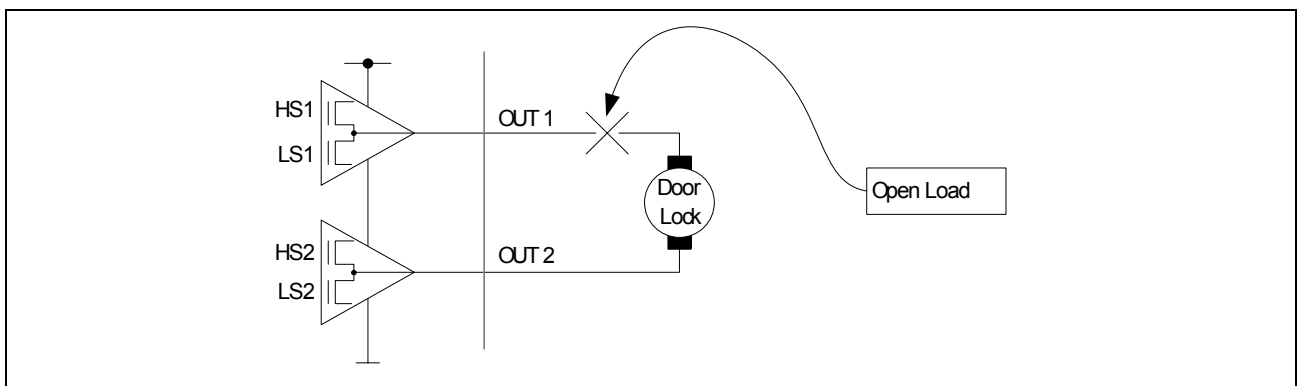
Figure 10   Open load example

Table 5   Open load diagnosis example

Control					Diagnostic information				
					motor connected		motor disconnected		Remark on Open Load Detection
LS1 ON	HS1 ON	LS2 ON	HS2 ON	motor rotation	LS1 OpL	LS2 OpL	LS1 OpL	LS2 OpL	
0	0	0	0	motor off	0	0	0	0	not detectable
1	0	0	1	clock-wise	**0**	0	**1**	0	detected
0	1	1	0	counter clock-wise	0	**0**	0	**1**	detected
0	1	0	1	brake high	0	0	0	0	not detectable
1	0	1	0	brake low	1	1	1	1	not detectable.

4.4.2 Electrical Characteristics

Electrical Characteristics OUT 1 and 2 (driver for door latch)

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
Static Drain-source ON-Resistance							
4.4.1	High- and low-side switch	R_{DSON12}	–	–	150	mΩ	I_{OUT} = 3 A; T_j = 25 °C
			–	–	260	mΩ	I_{OUT} = 3 A
Switching Times							
4.4.2	high-side ON delay-time	t_{dONH12}	–	50	100	µs	V_S = 14 V, resistive load of 10 Ω, see **Figure 11** and **Figure 12**
4.4.3	high-side OFF delay time	$t_{dOFFH12}$	–	25	50	µs	
4.4.4	low-side ON delay-time	t_{dONL12}	–	50	100	µs	
4.4.5	low-side OFF delay time	$t_{dOFFL12}$	–	25	50	µs	
4.4.6	dead-time H to L	t_{DHL12}	3	–	–	µs	t_{dONL12} - $t_{dOFFH12}$
4.4.7	dead-time L to H	t_{DLH12}	3	–	–	µs	t_{dONH12} - $t_{dOFFL12}$
Short Circuit Protection							
4.4.8	Over-current shutdown threshold	I_{SD12}	8	–	15	A	high- and low-side
4.4.9	Shutdown delay time	t_{dSD12}	10	25	50	µs	
4.4.10	Short circuit current[1]	I_{SC12}	–	20	–	A	
Open Load Detection							
4.4.11	Detection current	I_{OCD12}	40	–	200	mA	low-side
4.4.12	Delay time	t_{dOC12}	200	350	600	µs	
Leakage Current							
4.4.13	OFF-state output current	I_{QL}	–	–	25	µA	V_{OUT} = GND

[1] Not subject to production test - specified by design

Electrical Characteristics OUT3, 4 (Driver for deadbolt, mirror fold and mirror xy)

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Sym-bol	Limit Values			Unit	Conditions
			min.	typ.	max.		
Static Drain-source ON-Resistance							
4.4.14	High- and low-side switch	R_{DSON34}	–	–	0.4	Ω	I_{OUT} = ±1 A; T_j = 25 °C
			–	–	0.7	Ω	I_{OUT} = ±1 A
Switching Times							
4.4.15	high-side ON delay-time	t_{dONH34}	–	50	100	µs	V_S = 14 V, resistive load of 14 Ω, see **Figure 11** and **Figure 12**
4.4.16	high-side OFF delay time	$t_{dOFFH34}$	–	25	50	µs	
4.4.17	low-side ON delay-time	t_{dONL34}	–	50	100	µs	
4.4.18	low-side OFF delay time	$t_{dOFFL34}$	–	25	50	µs	
4.4.19	dead-time H to L	t_{DHL34}	3	–	–	µs	t_{dONL34} - $t_{dOFFH34}$
4.4.20	dead-time L to H	t_{DLH34}	3	–	–	µs	t_{dONH34} - $t_{dOFFL34}$
Short Circuit Protection							
4.4.21	Over-current shutdown threshold	I_{SD34}	3	4	8	A	high- and low-side
4.4.22	Shutdown delay time	t_{dSD34}	10	25	50	µs	
4.4.23	Short Circuit current[1]	I_{SC34}	–	6	–	A	
Open Load Detection							
4.4.24	Detection current	I_{OCD34}	12	25	40	mA	low-side
4.4.25	Delay time	t_{dOC34}	200	350	600	µs	
Leakage Current							
4.4.26	OFF-state output current	I_{QL}	–	–	10	µA	V_{OUT} = 0.2V

[1] Not subject to production test - specified by design

Electrical Characteristics OUT 5, 6
(driver for mirror x-y position)

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
Static Drain-source ON-Resistance							
4.4.27	High- and low-side switch	R_{DSON56}	–	–	0.8	Ω	I_{OUT} = ±0.5 A; T_j = 25 °C
			–	–	1.3	Ω	I_{OUT} = ±0.5 A
Switching Times							
4.4.28	high-side ON delay-time	t_{dONH56}	–	50	100	µs	V_S = 14 V, resistive load of 25 Ω, see **Figure 11** and **Figure 12**
4.4.29	high-side OFF delay time	$t_{dOFFH56}$	–	25	50	µs	
4.4.30	low-side ON delay-time	t_{dONL56}	–	50	100	µs	
4.4.31	low-side OFF delay time	$t_{dOFFL56}$	–	25	50	µs	
4.4.32	dead-time H to L	t_{DHL56}	3	–	–	µs	t_{dONL56} - $t_{dOFFH56}$
4.4.33	dead-time L to H	t_{DLH56}	3	–	–	µs	t_{dONH56} - $t_{dOFFL56}$
Short Circuit Protection							
4.4.34	Over-current shutdown threshold	I_{SD56}	1.25	1.5	2.5	A	high- and low-side
4.4.35	Shutdown delay time	t_{dSD56}	10	25	50	µs	
4.4.36	Short Circuit current[1]	I_{SC56}	–	3.0	–	A	
Open Load Detection							
4.4.37	Detection current	I_{OCD56}	12	25	40	mA	low-side
4.4.38	Delay time	t_{dOC56}	200	350	600	µs	
Leakage Current							
4.4.39	OFF-state output current	I_{QL}	–	–	10	µA	V_{OUT} = 0.2V

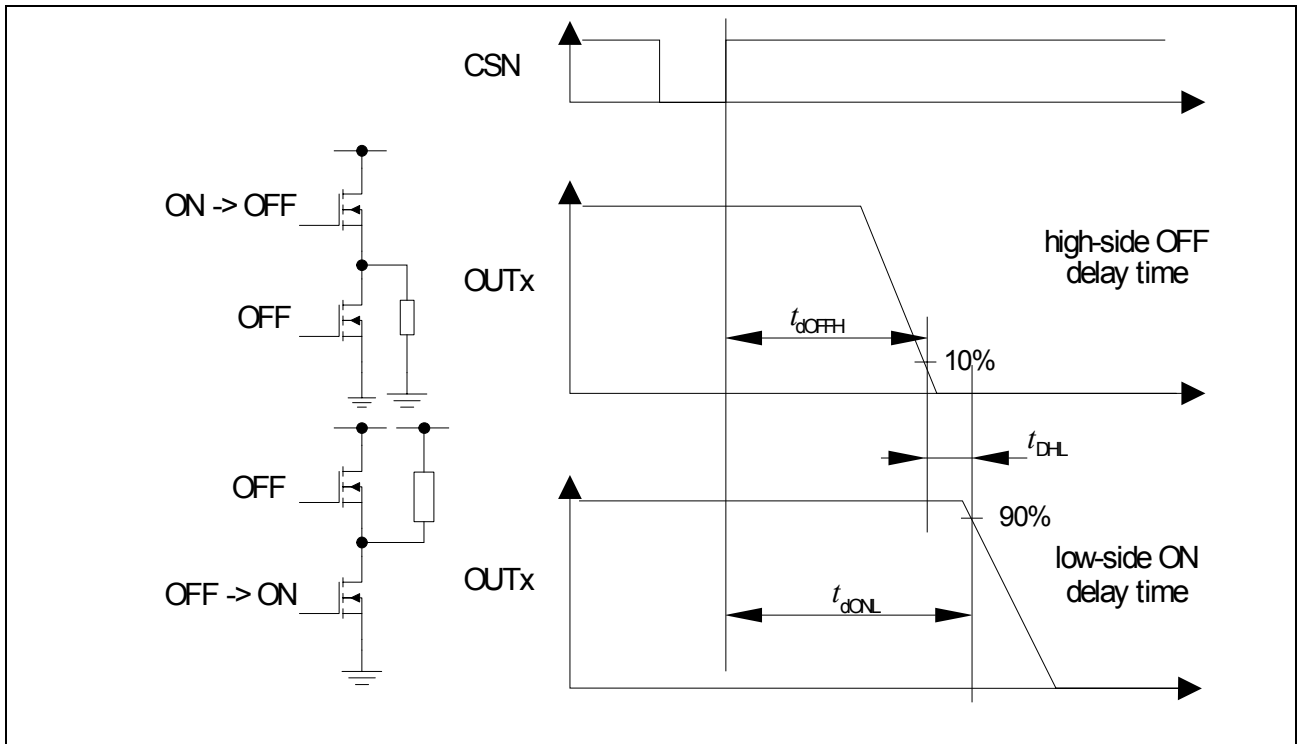[1] Not subject to production test - specified by design

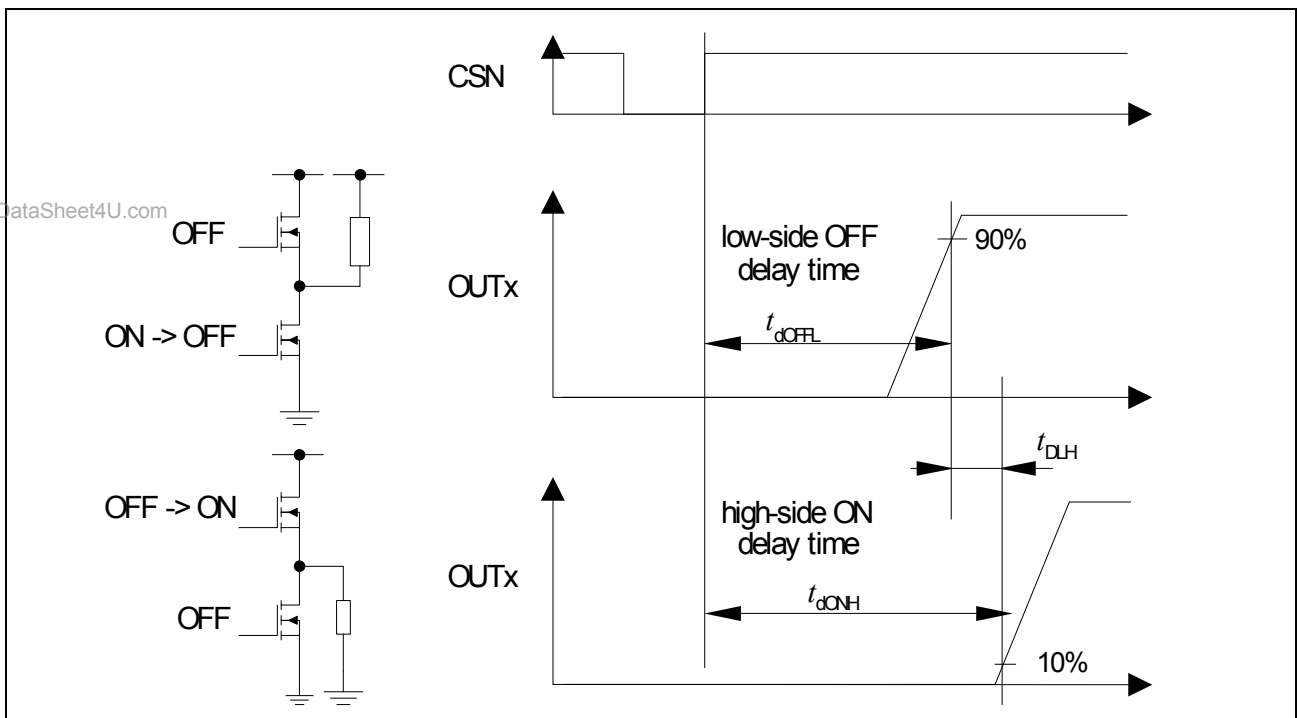**Figure 11   Timing bridge outputs high to low**

Figure 12   Timing bridge outputs low to high

4.5 Power-Output 7 (Mirror heater driver)

Output 7 is a high-side switch intended to drive ohmic loads like the heater of an exterior mirror.

4.5.1 Protection and Diagnosis

4.5.1.1 Short Circuit of Output to Ground

If the high-side switch is turned on and the current rises above the shutdown threshold I_{SD} for longer than the shutdown delay time t_{dSD}, the output transistor is turned off and the corresponding diagnosis bit is set. During the delay time, the current is limited to I_{SC} as shown in **Figure 13**.
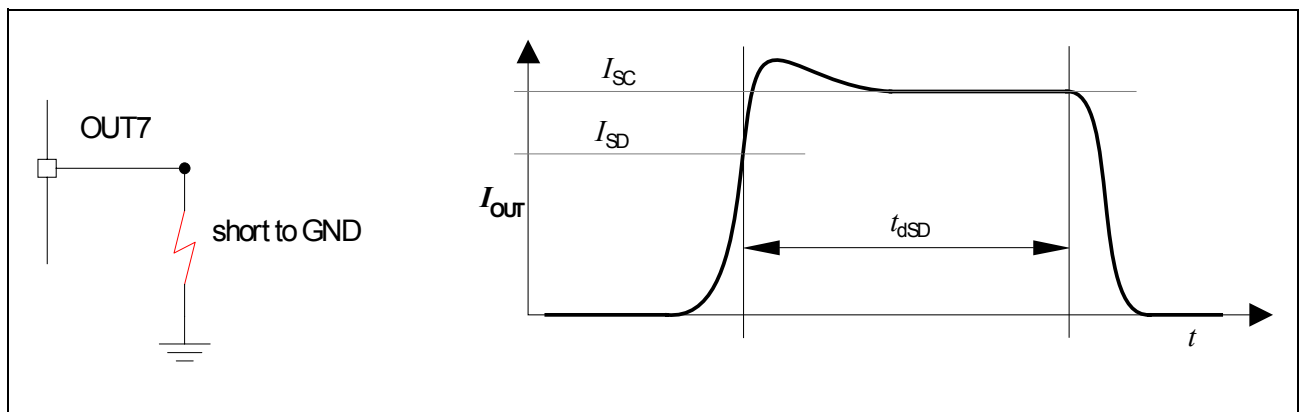
Figure 13 **Short circuit protection**

The output stage stays off and the error bit set until a status register reset is sent to the SPI or a power-on reset is performed.

4.5.1.2 Open Load

For the high-side switches, an open-load in OFF-state scheme is used as shown in **Figure 14**. The output is pulled up by a current source I_{OpL}. In OFF-state, the output voltage is monitored and compared to the threshold V_{OpL}. If the voltage rises above this threshold, the open-load signal is set to high. This is equivalent to comparing the load resistance to the value V_{OpL} / I_{OpL}. The open load error bit is latched and can be reset by the SPI status register reset or by a power-on reset.

The pull-up current can be switched on and off by the OpLxON bits. This bit should be set to LOW (i.e. pull-up current switched off) if an output is used to drive LEDs because they may emit light if biased with the pull-up current.
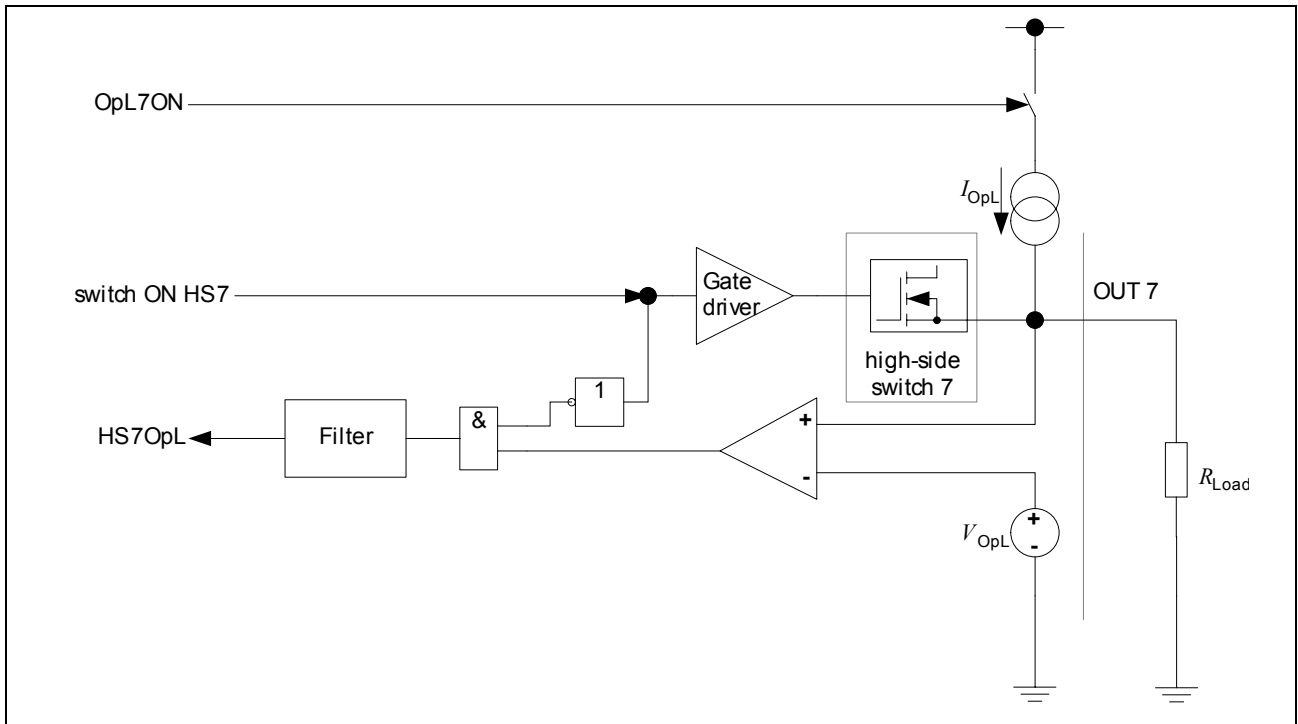
Figure 14   Open load in OFF-state scheme

4.5.2 Electrical Characteristics

Electrical Characteristics OUT 7 (mirror heater driver)

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
Static Drain-source ON-Resistance							
4.5.1	High-side switch	R_{DSON7}	–	–	100	mΩ	I_{OUT} = 2.5 A; T_j = 25 °C
			–	–	170	mΩ	I_{OUT} = 2.5 A
Switching Times							
4.5.2	Turn-ON delay time	t_{dONH7}	–	5	15	μs	V_S = 14 V, resistive load of 10 Ω, see **Figure 15**
4.5.3	Output rise-time	t_{rise7}	–	15	40	μs	
4.5.4	Turn-OFF delay time	t_{dOFFH7}	–	20	40	μs	
4.5.5	Output fall-time	t_{fall7}	–	5	10	μs	
Short Circuit Protection							
4.5.6	Over-current shutdown threshold	I_{SD7}	6.25	8	11	A	–
4.5.7	Shutdown delay time	t_{dSD7}	10	25	50	μs	–
4.5.8	Short Circuit current[1]	I_{SC7}	–	12	–	A	–
Open Load Detection							
4.5.9	Pull-up current	I_{OpL}	100	–	300	μA	V_{OUT} = 4V
4.5.10	Detection Threshold	V_{OpL}	2	–	4	V	–
4.5.11	Delay time	t_{dOC}	–	–	200	μs	–
Leakage Current							
4.5.12	OFF-state output current	I_{QL}	–	–	5	μA	V_{OUT} = GND

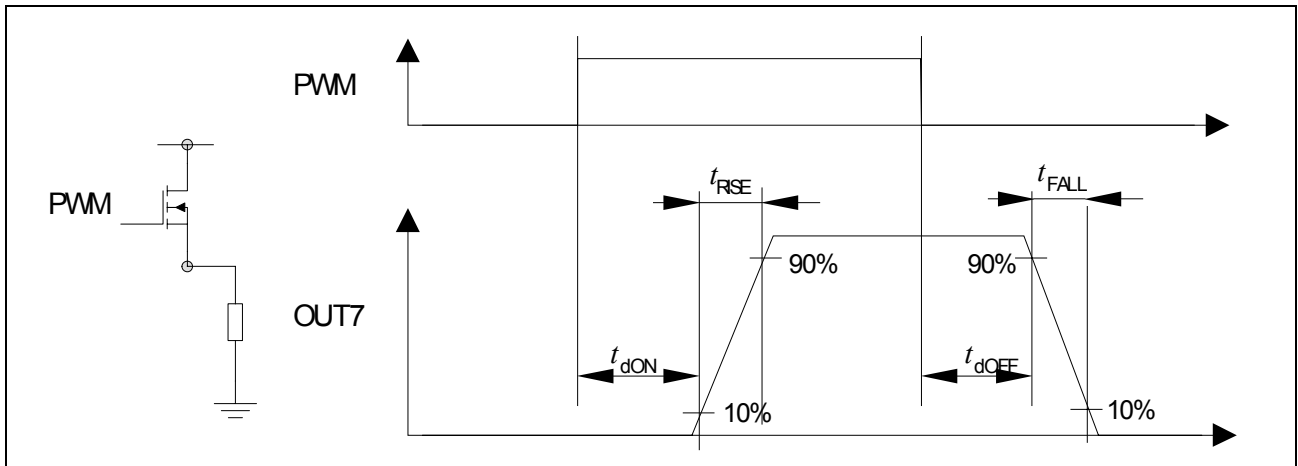[1] Not subject to production test - specified by design

Figure 15   Timing OUT 7

4.6 Power-Outputs 8 - 11 (Lamp drivers)

Outputs 8 - 11 are a high-side switches intended to drive ohmic loads 5W or 10W lamp (bulb) loads.

4.6.1 Protection and Diagnosis

4.6.1.1 Short Circuit of Output to Ground

The high-side switches are protected against short to GND.

The high-side switches Out 8 - 11 are protected against short to GND.

Short Circuit during switch-on

During switch-on of an output a current an voltage level is used to check for a short circuit. If a switch is turned on and the short circuit condition is valid after t_{dSDon8} the output transistor is turned off and the corresponding diagnosis bit is set. A short circuit condition is valid if the current rises above the shutdown threshold I_{SD8} and the voltage at the output stays below V_{SD8}. During the delay time, the current is limited to I_{SC8} as shown in **Figure 16**
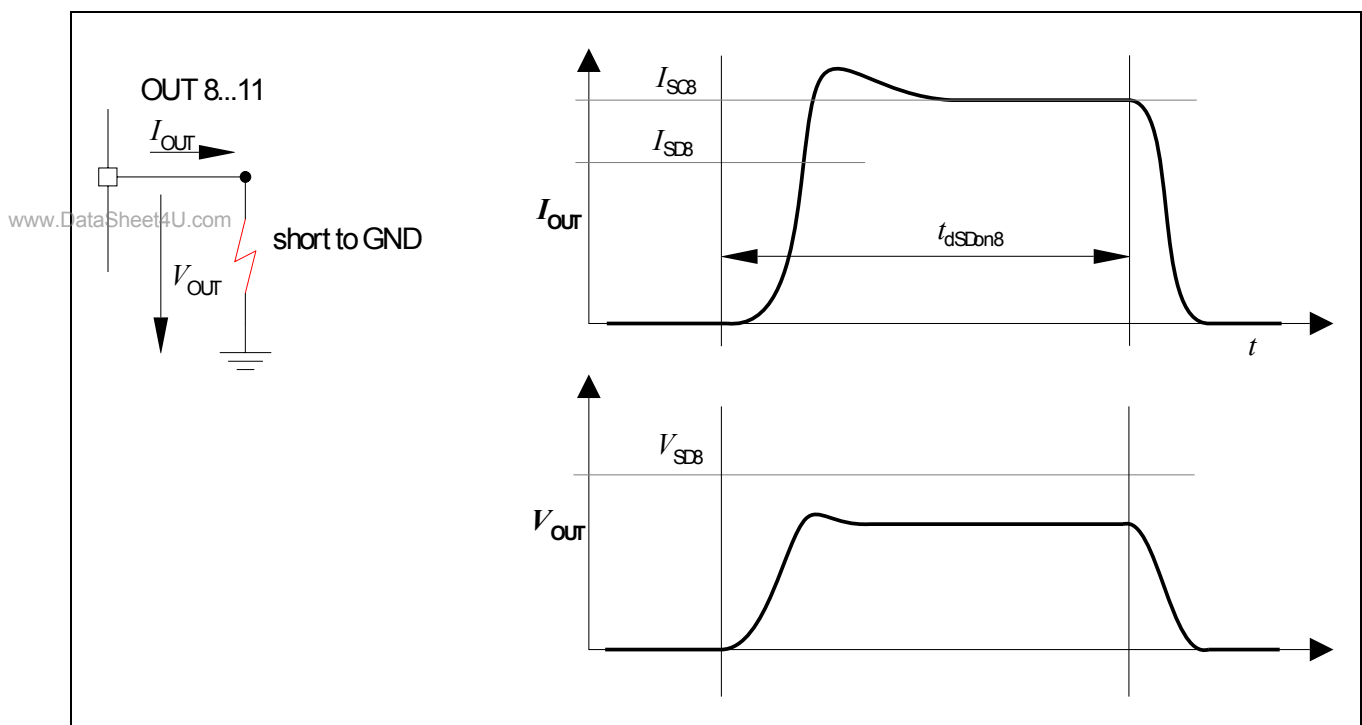

Figure 16   Short circuit protection during switch-on

Short Circuit in On-state

If a switch is already on and the current rises above the shutdown threshold I_{SD} for longer than the shutdown delay time t_{dSD} the output transistor is turned off and the corresponding diagnosis bit is set. This is independent of the voltage V_{out}. See **Figure 17**
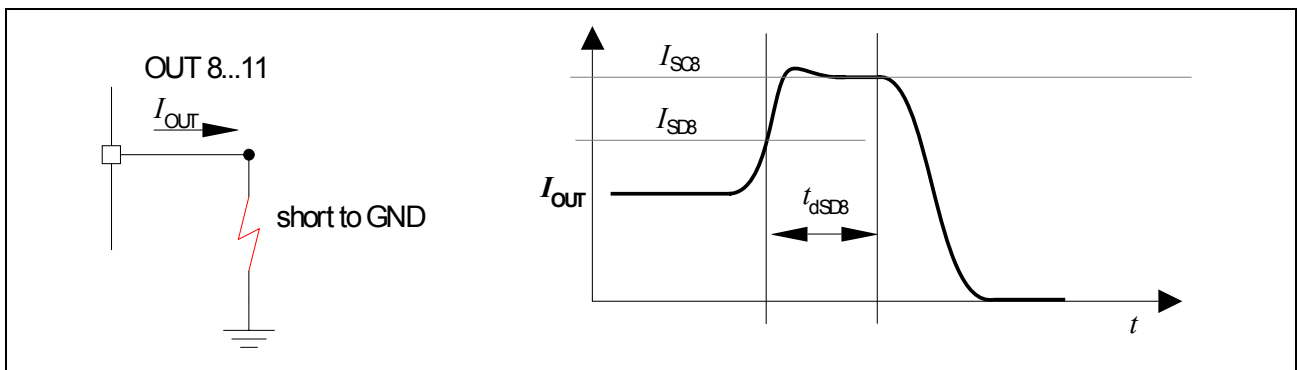

Figure 17   Short circuit protection in on-state

4.6.1.2   Open Load

For the high-side switches, an open-load in OFF-state scheme is used as shown in **Figure 18**. The output is pulled up by a current source I_{OpL}. In OFF-state, the output voltage is monitored and compared to the threshold V_{OpL}. If the voltage rises above this threshold, the open-load signal is set to high. This is equivalent to comparing the load resistance to the value V_{OpL} / I_{OpL}. The open load error bit is latched and can be reset by the SPI status register reset or by a power-on reset.

The pull-up current can be switched on and off by the OpLxON bits. This bit should be set to LOW (i.e. pull-up current switched off) if an output is used to drive LEDs because they may emit light if biased with the pull-up current.
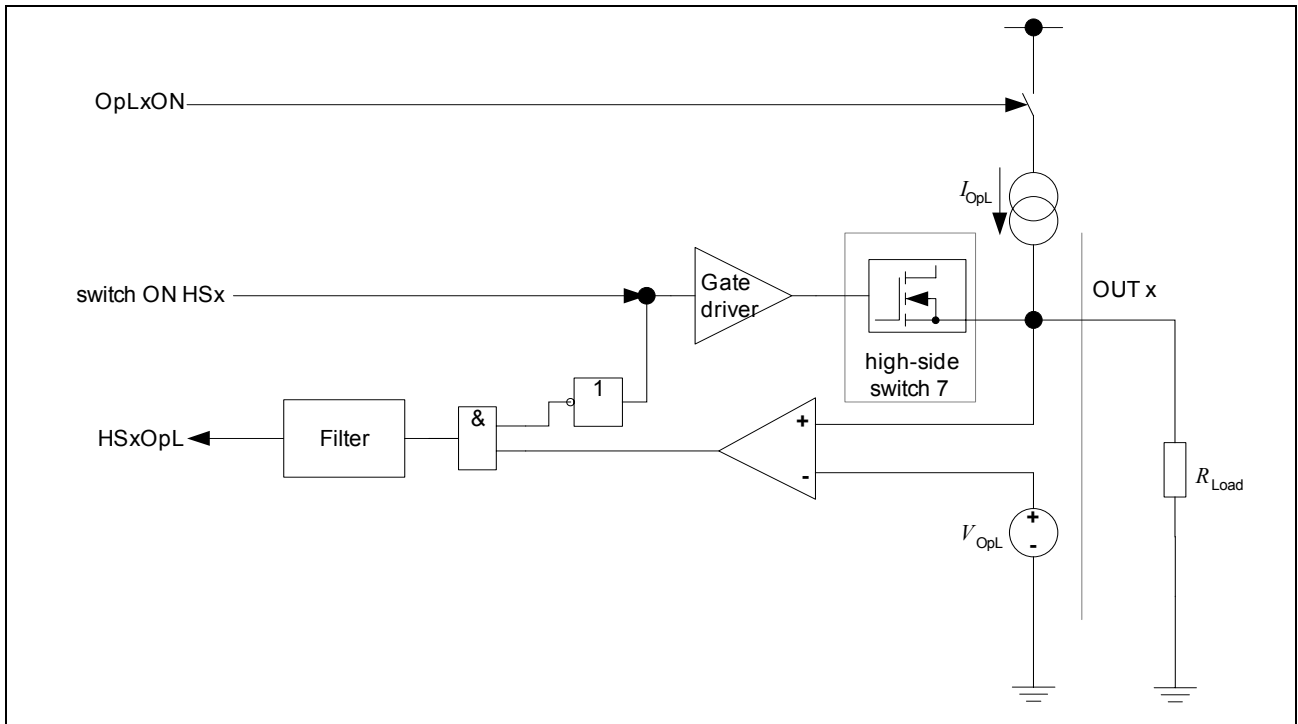
Figure 18   Open load in OFF-state scheme

4.6.2   Electrical Characteristics

Electrical Characteristics OUT 8 - 11 (Lamp drivers)

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
Static Drain-source ON-Resistance							
4.6.1	High-side switch	R_{DSON8}	–	–	0.5	Ω	I_{OUT} = +0.5 A; T_j = 25 °C
			–	–	0.8	Ω	I_{OUT} = +0.5 A
Switching Times							
4.6.2	Turn-ON delay time	t_{dONH8}	–	5	15	µs	V_S = 14 V, resistive load of 25 Ω, see **Figure 19**
4.6.3	Output rise-time	t_{rise8}	5	10	30	µs	
4.6.4	Turn-OFF delay time	t_{dOFFH8}	–	25	50	µs	
4.6.5	Output fall-time	t_{fall8}	7	15	30	µs	
Short Circuit Protection							
4.6.6	Over-current shutdown threshold	I_{SD8}	1.8	2.9	3.5	A	
4.6.7	Over-current shutdown threshold voltage	V_{SD8}	1.5	2,5	3.3	V	
4.6.8	Short circuit current[1]	I_{SC8}	-	4.2	-	A	
4.6.9	Shutdown delay time	t_{dSDon8}	125	200	350	µs	at switching-on
4.6.10	Shutdown delay time	t_{dSD8}	10	25	60	µs	in on-state
Open Load Detection							
4.6.11	Pull-up current	I_{OpL8}	100	–	250	µA	V_{OUT} = 4V
4.6.12	Detection Threshold	V_{OpL8}	2	–	4	V	–
4.6.13	Delay time	t_{dOC8}	–	–	200	µs	–
Leakage Current							
4.6.14	OFF-state output current	I_{QL}	–	–	5	µA	V_{OUT} = GND

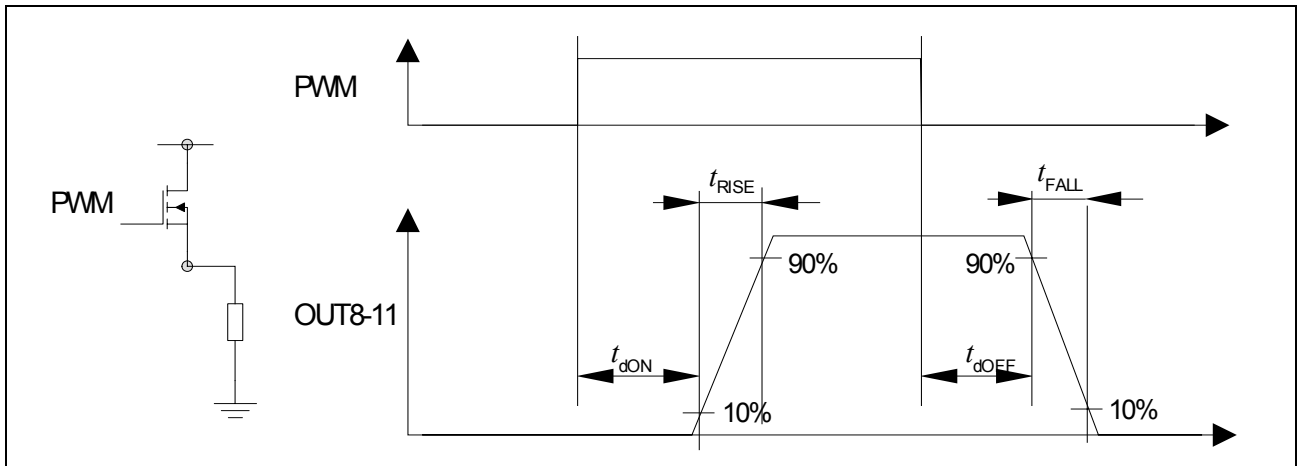[1] Not subject to production test - specified by design.

Figure 19   Timing OUT 8 - 11

4.7 Logic In- and Outputs

The threshold specifications of the logic inputs are compatible to both 5V and 3.3V standard CMOS micro controller outputs. The logic output DO is a 5V CMOS output

4.7.1 Electrical Characteristics

Electrical Characteristics Diagnostics

8 V < V_S < 20 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
-40 °C < T_j < 150 °C; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			min.	typ.	max.		
Inhibit Input							
4.7.15	H-input voltage threshold	V_{IH}	–	–	2	V	V_{IN} rising
4.7.16	L-input voltage threshold	V_{IL}	1	–	–	V	V_{IN} falling
4.7.17	Hysteresis of input voltage	V_{IHY}	100	–	600	mV	–
4.7.18	Pull down current	I_{IINH}	–	–	50	µA	V_{IINH} = 2 V
Logic Inputs DI, CLK, CSN, PWM1 and PWM2							
4.7.19	H-input voltage threshold	V_{IH}	–	–	2	V	V_{IN} rising
4.7.20	L-input voltage threshold	V_{IL}	1	–	–	V	V_{IN} falling
4.7.21	Hysteresis of input voltage	V_{IHY}	100	–	600	mV	–
4.7.22	Pull up current at pin CSN	I_{ICSN}	-50	-25	-10	µA	V_{CSN} = 1 V
4.7.23	Pull down current at pins PWM1, PWM2, DI, CLK	I_{Input}	10	25	50	µA	V_{Input} = 2 V
4.7.24	Input capacitance at pin CSN, DI, CLK, PWM1, PWM2[1]	C_I	–	10	15	pF	0 V < V_{CC} < 5.25 V
Logic Output DO							
4.7.25	H-output voltage level	V_{DOH}	V_{CC} - 1.0	V_{CC} - 0.7	–	V	I_{SDOH} = 1 mA
4.7.26	L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{SDOL} = -1.6 mA
4.7.27	Tri-state leakage current	I_{DOLK}	-10	–	10	µA	V_{CSN} = V_{CC} 0 V < V_{SDO} < V_{CC}
4.7.28	Tri-state input capacitance[1]	C_{DO}	–	10	15	pF	V_{CSN} = V_{CC} 0 V < V_{CC} < 5.25 V

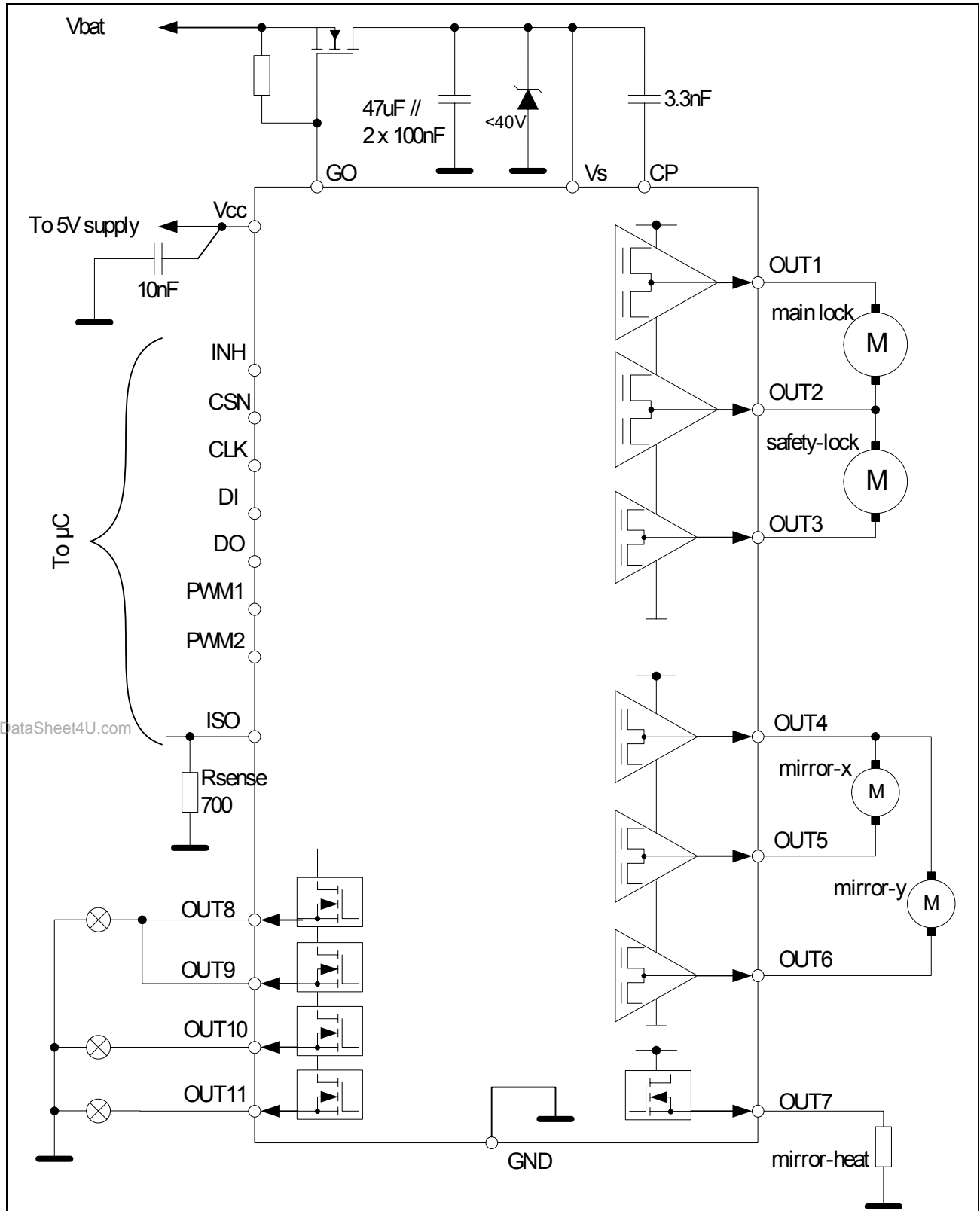[1] Not subject to production test, specified by design

5 Application Description

Figure 20   Application example with two-motor (safety-) lock
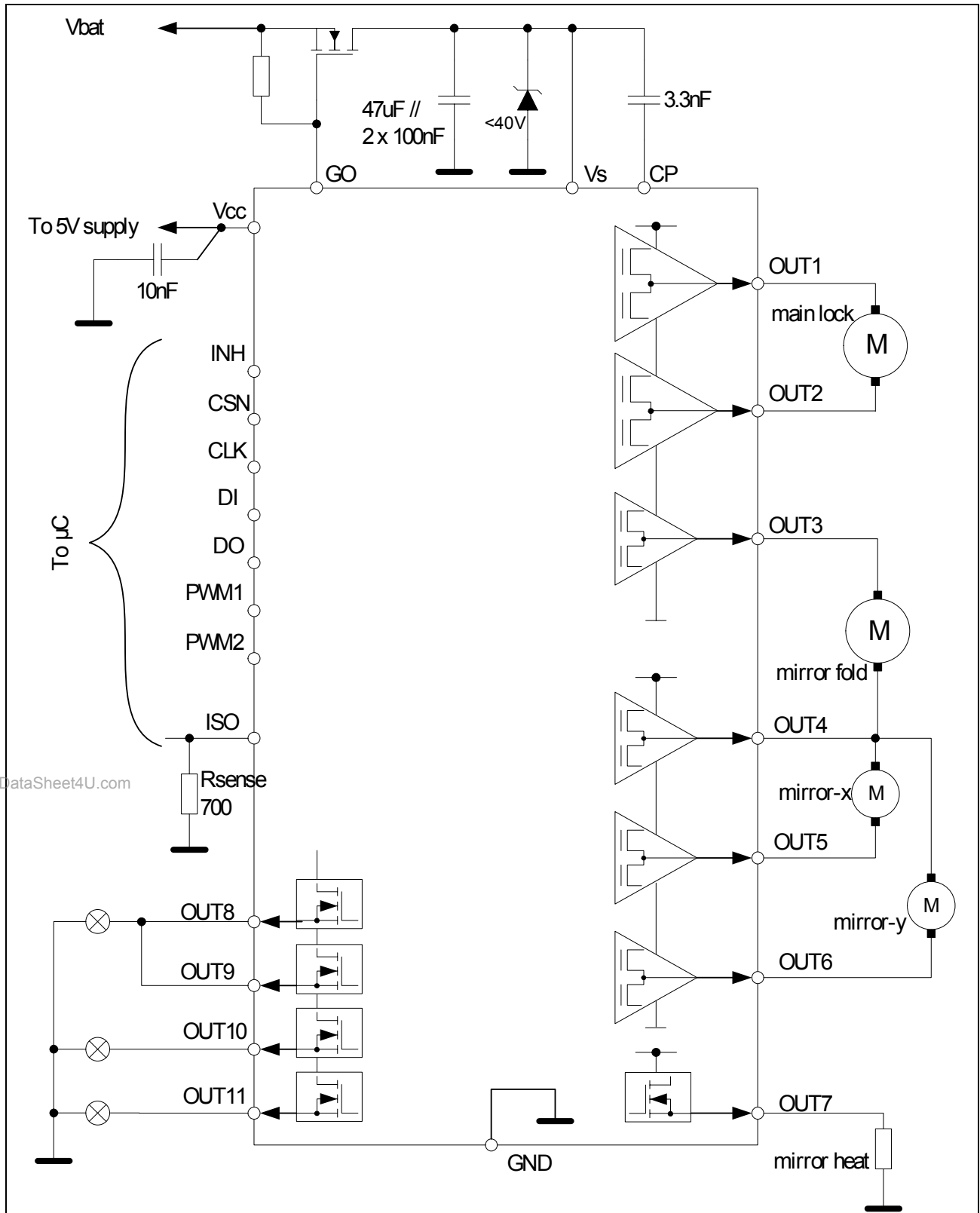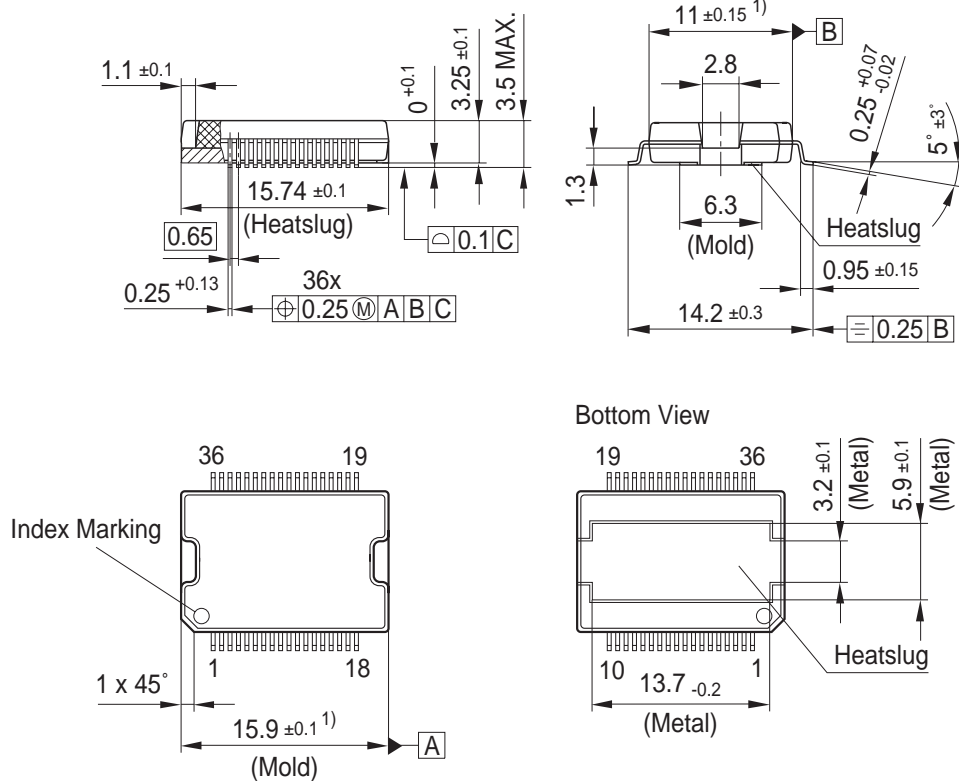
Figure 21   Application example with mirror-fold

6   Package Outlines

PG-DSO-36-27
(Plastic Dual Small Outline Package)

1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09181

You can find all of our packages, sorts of packing and others in our
Infineon Internet Page "Products": http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

Attention please!

The information given in this data sheet shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

TLE 8201R

Revision History:	2006-06-07
Previous Version:	Preliminary Data Sheet Rev. 1.0
Page	Subjects (major changes since last revision)
	No changes