TLE 8203E

Mirror Power IC

Automotive Power

Never stop thinking

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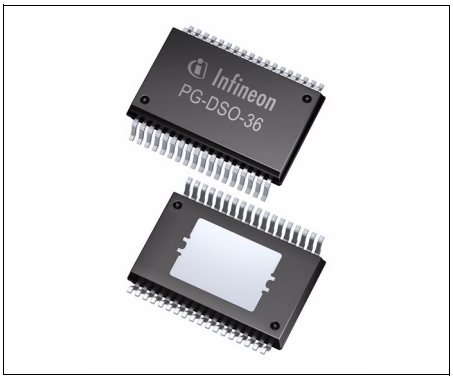
1 Overview



PG-DSO-36-50

Features

- Three half-bridges (1 x 0.7Ω ; 2 x 1.3Ω $R_{DSON(MAX)}$ @ T_J=150°C) for mirror position
- High-side switch (0.17Ω $R_{DSON(MAX)}$ @ T_J=150°C) for mirror defrost
- Two high-side switches (0.8Ω $R_{DSON(MAX)}$ @ T_J=150°C) for 5 W and 10 W lamps
- Current sense analog output with multiplexer
- All outputs with short circuit protection and diagnosis
- Over-temperature protection with warning
- Open load diagnosis for all outputs
- Charge pump-Output for n-channel MOSFET reverse-polarity protection
- Very low current consumption in sleep mode
- Standard 16-bit SPI for control and diagnosis
- Over- and Under-voltage Lockout
- DSO package with exposed pad for low thermal resistance
- Part of scalable door family products
- Green Product (RoHS compliant)
- AEC Qualified

Functional Description

The TLE 8203E is an Application Specific Standard Product for automotive mirror control applications. It includes the power stages necessary to drive mirror loads such as mirror position, mirror defrost and 5W or 10W lamp, i.e. turn signal. It is a monolithic die based on Infineon's smart mixed technology SPT which combines bipolar and CMOS control circuitry with DMOS power devices.

The short circuit and over-temperature protection and detailed diagnosis offered meet the automotive application safety requirements. The current sense output mprove system reliability and performance. The standard SPI interface saves microcontroller I/O lines while still providing flexible control of the power stages and a detailed diagnosis.

Type	Package	Marking
TLE 8203E	PG-DSO-36-50	TLE8203E

2 Block Diagram

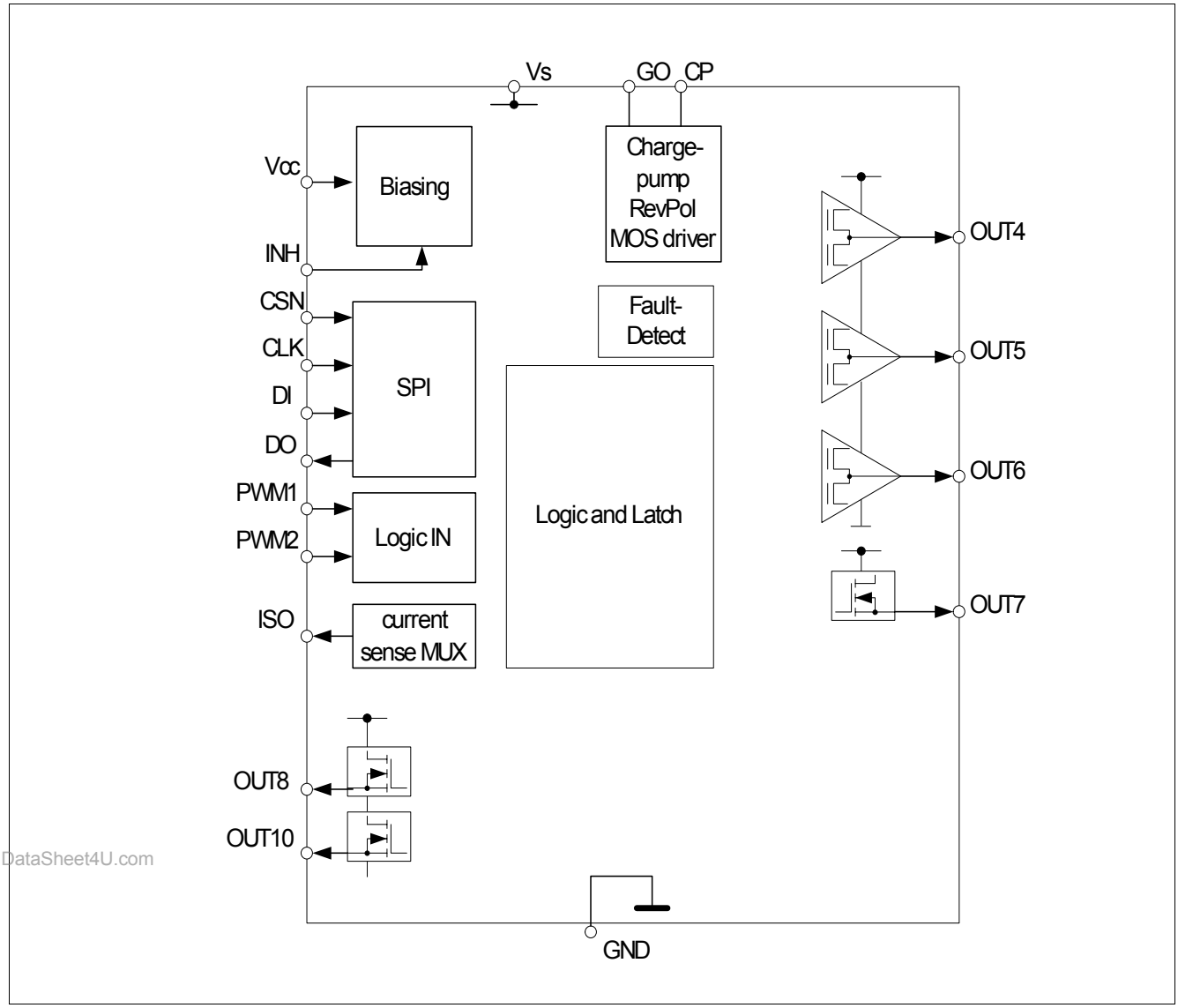


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

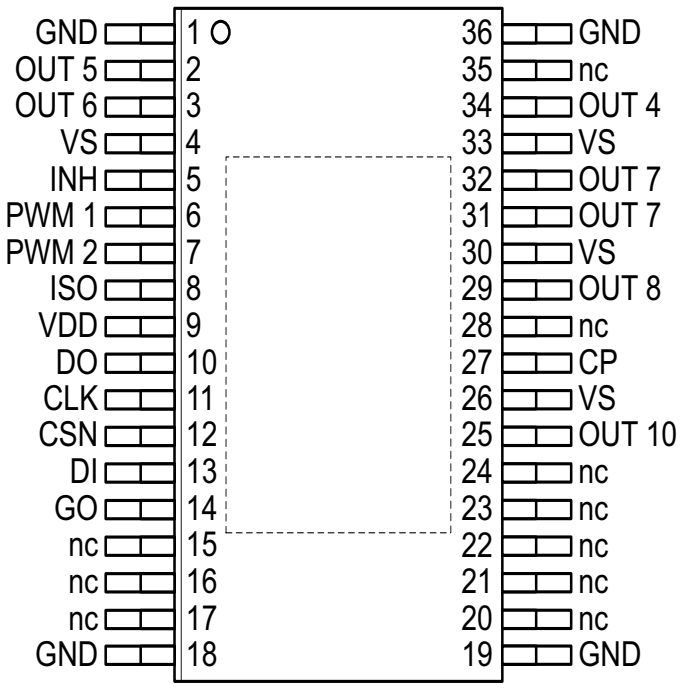


Figure 2 Pin Configuration PG-DSO-36-50

3.2 Pin Definitions and Functions

Pin	Symbol	Function
cooling tab	GND	**Cooling Tab;** internally connected to GND; To reduce thermal resistance, place cooling areas and thermal vias on PCB.
1, 18, 19, 36	GND	**Ground;** internally connected to cooling tab (exposed pad).
2	OUT5	**Power-Output of Half-Bridge output 5;** DMOS half-bridge (mirror position).
3	OUT6	**Power-Output of Half-Bridge output 6;** DMOS half-bridge (mirror position).
4, 26, 30, 33	V_S	**Power Supply;** needs decoupling capacitors to GND. > 47 µF electrolytic in parallel with 100 nF ceramic is recommended. All V_S pins must be connected externally.
5	INH	**Inhibit;** active low. Sets the device in sleep mode with low current consumption when left open or pulled to LOW. Has an internal pull-down current source.
6	PWM1	**Logic Input for Direct Power Stage Control;** direct input to control the high-side switches selected by the SPI xsel1 bits in control register CtrlReg01.
7	PWM2	**Logic Input for Direct Power Stage Control;** direct input to control the switches selected by the SPI xsel2 bits in control register CtrlReg11.

Pin	Symbol	Function
8	ISO	**Current Sense Output;** Mirrors the current of the high-side switch selected by the current sense multiplexer control bits ISx.
9	V_{DD}	**Logic Supply Voltage;** needs decoupling capacitors to GND (pin 1). 10 µF electrolytic in parallel with 10 nF ceramic is recommended.
10	DO	**Serial Data Output;** Transfers data to the master when the chip is selected by CSN = LOW. Data transmission is synchronized by CLK, DO state is changed on the rising edge of CLK. The most significant bit (MSB) is transferred first. The pin is tristated as long as CSN = HIGH.
11	CLK	**Serial Data Clock Input;** Receives the clock signal from the master and clocks the SPI shift register. Has an internal pull-down current source.
12	CSN	**Serial Port Chip Select Not Input;** SPI communication is enabled by pulling CSN to LOW. CLK must be LOW during the transition of CSN. The CSN-pin has an internal pull-up current source.
13	DI	**Serial Data Input;** Receives serial data from the master when the chip is selected by CSN = LOW. Data transmission is synchronized by CLK. Data are accepted on the falling edge of CLK. The LSB is transferred first. The DI-pin has an internal pull-down current source.
14	GO	**Gate Out;** Charge pump output to drive the gate of external n-channel MOSFET for reverse polarity protection.
15, 16	N.C	**Not Connected**
20, 21	N.C	**Not Connected**
22	N.C	**Not Connected**
24	N.C	**Not Connected**
25	OUT10	**Power-Output of High-Side Switch output 10;** DMOS high-side switch (lamp driver
27	CP	**Charge Pump;** pin for optional external charge-pump reservoir capacitor. 3.3 nF to V_S is recommended.
28	N.C	**Not Connected**
29	OUT8	**Power-Output of High-Side Switch output 8;** DMOS high-side switch (lamp driver)
31, 32	OUT7	**Power Output of High-Side Switch output 7;** DMOS high-side switch (mirror heat)
34	OUT4	**Power-Output of Half-Bridge output 4;** DMOS half-bridge (sum of mirror position).
35	N.C.	**Not Connected**

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]
T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-0.3	40	V	–
4.1.2	Logic supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.3	Logic input- and output voltages		-0.3	5.5	V	–
4.1.4	Voltage at GO-pin	V_{GO}	-16	V_S + 5	V	–
Temperatures						
4.1.5	Junction Temperature	T_j	-40	150	°C	–
4.1.6	Storage Temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
4.1.7	ESD capability of power stage output and V_S pins vers. GND	V_{ESD}	–	4	kV	2)
4.1.8	ESD capability of logic pins and ISO pin vers. GND	V_{ESD}	–	2	kV	2)

1) Not subject to production test, specified by design.
2) Human Body Model according to JEDEC EIA/JESD22-A114-B (1.5kΩ, 100 pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Operating Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage range for normal operation	V_S	8	20	V	–
4.2.2	Extended supply voltage range for operation	$V_{S(ext)}$	5	40	V	(Limit Values Deviations possible)
4.2.3	Logic supply voltage range for normal operation	V_{DD}	4.75	5.25	V	–
4.2.4	Extended logic supply voltage range for operation	$V_{DD(ext)}$	4.75	5.5	V	(Limit Values Deviations possible)
4.2.5	SPI clock frequency	f_{CLK}	–	2	MHz	–
4.2.6	Junction temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thjC}	–	5	–	K/W	1)
4.3.2	Junction to Ambient	R_{thjA}	–	25	–	K/W	1) 2)

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer

5 Monitoring Functions

5.1 Power Supply Monitoring

The power supply Voltage V_S is monitored for over- and under-voltage.

- **Under Voltage**
  If the supply voltage V_S drops below the switch off voltage $V_{UV\ OFF}$, all output transistors are switched off and the power supply fail bit PSF is set. The error is not latched, i.e. if V_S rises again and reaches the switch on voltage $V_{UV\ ON}$, the power stages are restarted and the error bit is reset.
- **Over Voltage**
  If the supply voltage V_S rises above the switch off voltage $V_{OV\ OFF}$, all output transistors are switched off and the power supply fail bit (bit 7 of the SPI diagnosis word) is set. The error is not latched, i.e. if V_S falls again and reaches the switch on voltage $V_{OV\ ON}$, the power stages are restarted and the error is reset.

5.1.1 Characteristics Power Supply Monitoring

Electrical Characteristics: Power Supply Monitoring

T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	UV-Switch-ON voltage	V_{UVON}	–	–	5.2	V	V_S increasing
5.1.2	UV-Switch-OFF voltage	V_{UVOFF}	4.0	–	5.0	V	V_S decreasing
5.1.3	UV-ON/OFF-Hysteresis	V_{UVHY}	–	0.25	–	V	V_{UVON} - V_{UVOFF}
5.1.4	OV-Switch-OFF voltage	V_{OVOFF}	21	–	25	V	V_S increasing
5.1.5	OV-Switch-ON voltage	V_{OVON}	20	–	24	V	V_S decreasing
5.1.6	OV-ON/OFF-Hysteresis	V_{OVHY}	0.5	1	–	V	V_{OVOFF} - V_{OVON}

5.2 Temperature Monitoring

Temperature sensors are integrated in the power stages. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds. If one or more temperature sensors reach the warning temperature, the temperature warning bit TW is set to HIGH. This bit is not latched (i.e. if the temperature falls below the warning threshold (with hysteresis), the TW bit is reset to LOW again).

If one or more temperature sensors reach the shut-down temperature, the outputs are shut down as described in the next paragraph and the temperature shut-down bit TSD is set to HIGH. The shutdown is latched (i.e. the output stages remain off and the TSD bit set high until a SRR command is sent or a power-on reset is performed).

If one or more temperature sensors reaches the shutdown threshold, all outputs are switched off.

5.2.1 Characteristics Temperature Monitoring

Electrical Characteristics: Temperature Monitoring

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Thermal warning junction temperature[1)]	T_{jW}	120	145	170	°C	–
5.2.2	Temperature warning hysteresis[1)]	ΔT_{jW}	–	30	–	K	–
5.2.3	Thermal shutdown junction temperature[1)]	T_{jSD}	150	175	200	°C	–
5.2.4	Thermal switch-on junction temperature[1)]	T_{jSO}	120	–	170	°C	–
5.2.5	Temperature shutdown hysteresis[1)]	ΔT_{jSD}	–	30	–	K	–
5.2.6	Ratio of SD to W temperature[1)]	T_{jSD}/T_{jW}	1.05	1.20	–	–	–

1) Not subject to production test, specified by design.

5.3 Current Sense

A current proportional to the output current that flows from the selected power output to GND is provided at the ISO (I sense out) pin. The output selection is done via the SPI. The sense current can be transformed into a voltage by an external sense resistor and provided to an A/D converter input (see **Chapter 12**).

5.3.1 Characteristics Current Sense

Electrical Characteristics: Current Sense

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
HS4 (Register IS = 011)							
5.3.1	Output voltage range	V_{ISO4}	0	–	3	V	V_{DD} = 5 V
5.3.2	Current sense ratio	k_{ILIS4}	–	1000	–	–	$k_{ILIS} = I_{OUT}/I_{ISO}$; I_{OUT} > 1.5 A
5.3.3	Current sense accuracy	$k_{ILISacc4}$	–	–	10	%	
HS7 (Register IS = 100)							
5.3.4	Output voltage range	V_{ISO7}	0	–	3	V	V_{DD} = 5 V
5.3.5	Current Sense Ratio for HS7	k_{ILIS7}	–	2000	–	–	$k_{ILIS} = I_{OUT}/I_{ISO}$; I_{OUT} > 2 A
5.3.6	Current Sense accuracy	$k_{ILISacc7}$	–	–	10	%	

6 Power Supply

6.1 General

The TLE 8203E has two power domains: All power drivers are connected to the supply voltage V_S which is connected to the automotive 12 V board-net. The internal logic part is supplied by a separate Voltage V_{DD} = 5 V.

The advantage of this system is that information stored in the logic remains intact in the event of short-term failures in the supply voltage V_S. The system can therefore continue to operate after V_S has recovered, without having to be reprogrammed.

A rising edge on V_{DD} triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All data stored internally is deleted, and the outputs are switched to high-impedance status (tristate).

6.2 Sleep-Mode

The TLE 8203E can be put in a low current-consumption mode by setting the input INH to LOW. The INH pin has an internal pull-down current source. In sleep-mode, all output transistors are turned off and the SPI is not operating. When enabling the IC by setting INH from L to H, a Power-On Reset is performed as described above.

6.3 Reverse Polarity

The TLE 8203E requires an external reverse polarity protection. The gate-driver (charge-pump output) for an external n-channel logic-level MOSFET is integrated. The gate voltage is provided at pin GO which should be connected as shown in the application diagram.

6.4 Electrical Characteristics

Electrical Characteristics: Power Supply

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Current Consumption							
6.4.1	Supply current	I_S	–	1.0	7.0	mA	–
6.4.2	Logic supply current	I_{DD}	–	2.5	10	mA	SPI not active
6.4.3	Supply quiescent current	I_{S_Q}	–	2.5	5	µA	INH = L; V_S = 14 V; V_{OUTX} = 0 V; T_j < 85 °C
6.4.4	Logic quiescent current	I_{DD_Q}	–	0.2	1	µA	
6.4.5	Total quiescent current	I_{S_Q} + I_{DD_Q}	–	3	6	µA	
Charge Pump-output for Reverse-Polarity Protection FET (GO)							
6.4.6	Gate-Voltage	V_{GO} - V_S	5	–	8	V	I_{GO} = 50 µA
6.4.7	Setup-time	t_{GO}	–	–	1	ms	–
6.4.8	Reverse leakage current	I_{lkGO}	–	–	5	µA	V_S = 0 V; V_{GO} = -14 V

7 SPI

7.1 General

The SPI is used for bidirectional communication with a control unit. The TLE 8203E acts as SPI-slave and the control unit acts as SPI-master. The 16-bit control word is read via the DI serial data input. The status word appears synchronously at the DO serial data output. The communication is synchronized by the serial clock input CLK.

Standard data transfer timing is shown in **Figure 3**. The clock polarity is data valid on falling edge. CLK must be low during CSN transition. The transfer is MSB first.

The transmission cycle begins when the chip is selected with the chip-select-not (CSN) input (H to L). Then the data is clocked through the shift register. The transmission ends when the CSN input changes from L to H and the word which has been read into the shift register becomes the control word. The DO output switches then to tristate status, thereby releasing the DO bus circuit for other uses. The SPI allows to parallel multiple SPI devices by using multiple CSN lines. The SPI can also be used with other SPI-devices in a daisy-chain configuration.

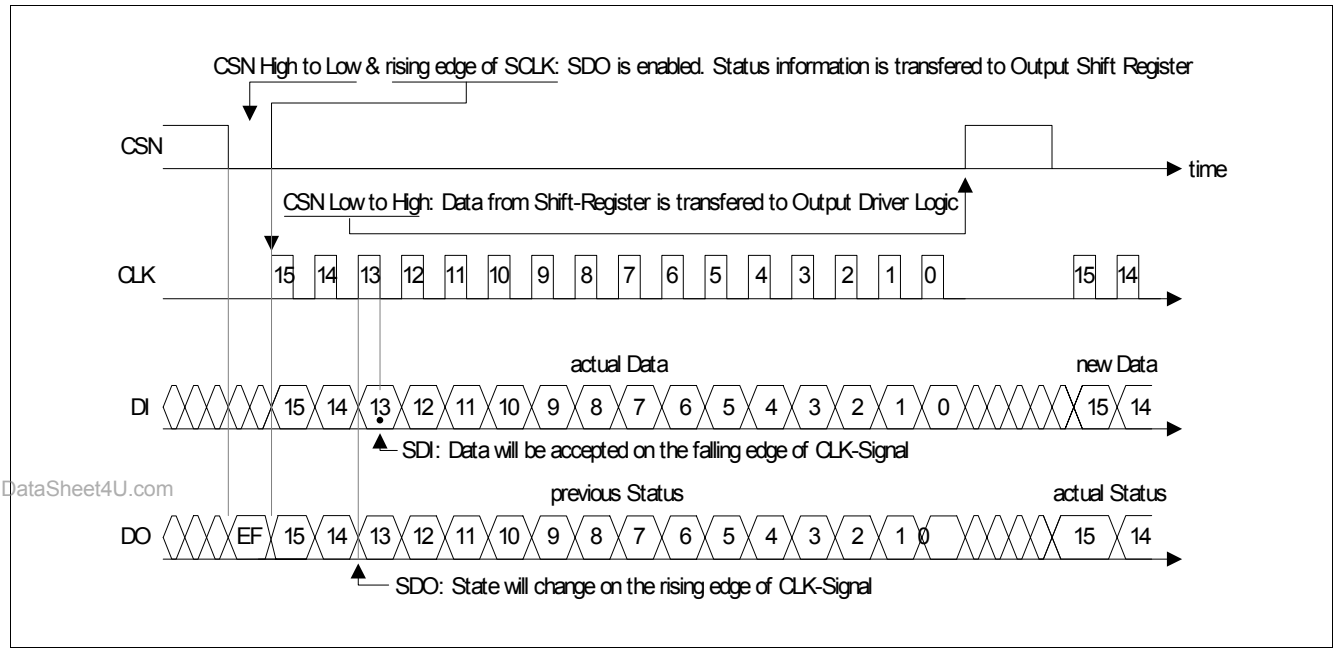


Figure 3 SPI Standard Data Transfer Timing

7.2 Register Address

The 16-bit SPI frame is composed of an addressable block, an address-independent block and a 2-bit address as shown in **Figure 4**.

The control word transmitted from the master to the TLE 8203E is executed at the end of the SPI transmission (CSN L -> H) and remains valid until a different control word is transmitted or a power on reset occurs. At the beginning of the SPI transmission (CSN H -> L), the diagnostic data currently valid are latched into the SPI and transferred to the master. For Status Register address handling, please refer to **Section 7.4**.

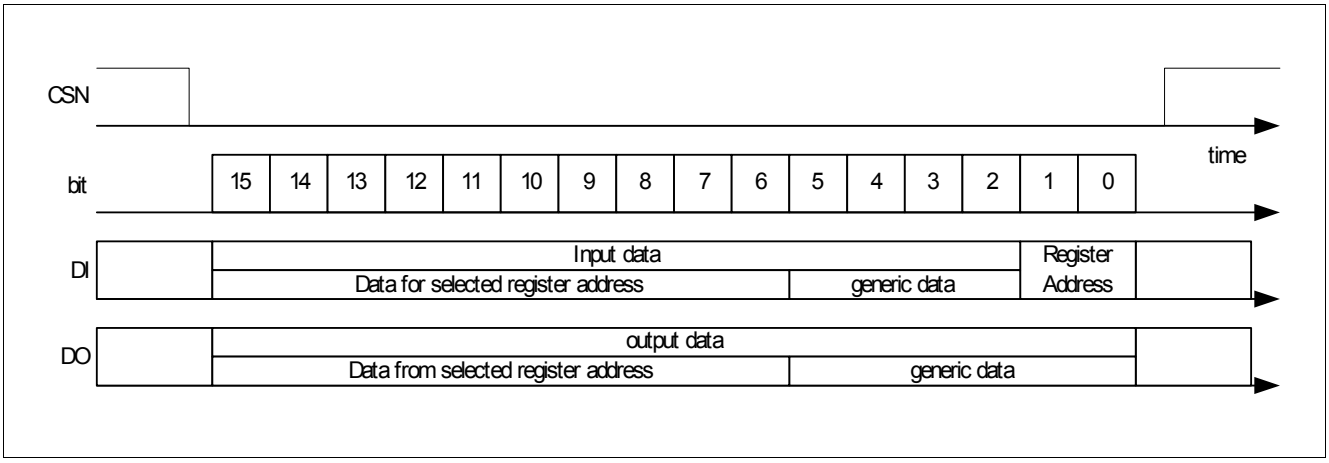


Figure 4 SPI Structure

7.3 SPI Bit Definitions

7.3.1 Control - Word

Table 1 Input (Control) Data Register

Bit	CtrlReg 00 Mirror Heat Control	CtrlReg 01 PWM1 Input Select	CtrlReg 10 Mirror and Lamp-driver Control	CtrlReg 11 PWM2 Input Select
15	x	HS7sel1	LS4ON	HS7sel2
14	x	HS8sel1	HS4ON	HS8sel2
13	x	x	LS5ON	x
12	x	HS10sel1	HS5ON	HS10sel2
11	x	x	LS6ON	x
10	x	x	HS6ON	x
9	HS7ON	x	HS8ON	x
8	Testmode = 0	x	x	x
7	Testmode = 0	OpL7ON	HS10ON	OpL8ON
6	Testmode = 0	Testmode = 0	x	OpL10ON
Address - Independent Data				
5	IS_2	IS_2	IS_2	IS_2
4	IS_1	IS_1	IS_1	IS_1
3	IS_0	IS_0	IS_0	IS_0
2	SRR	SRR	SRR	SRR
Address - Bits				
1	RA_1 = 0	RA_1 = 0	RA_1 = 1	RA_1 = 1
0	RA_0 = 0	RA_0 = 1	RA_0 = 0	RA_0 = 1

Note: Testmode is entered when the Testmode bits are set to High. Otherwise set to Low for normal operation.

Table 2 Control Bit Definitions

Control Bit	Definition			
LSxON	Low-side switch no. x is turned ON (OFF) if this bit is set to HIGH (LOW).			
HSxON	High-side switch no. x is turned ON (OFF) if this bit is set to HIGH (LOW).			
xsel1	Power switch x is selected to be switched by the PWM1 input.			
xsel2	Power switch x is selected to be switched by the PWM2 input			
OpLxON	The pull-up current for open-load detection on output 4, 5 and 6 are switched on (off) if this bit is set to HIGH (LOW).			
IS_x	The output for the current sense multiplexer is selected by these bits:			
	IS_2	**IS_1**	**IS_0**	**Power stage selected for current sense**
	0	0	0	x
	0	0	1	x
	0	1	0	x
	0	1	1	HS4
	1	0	0	HS7
	all others			no output selected (I_{ISO} = 0)
SRR	Status Register Reset. If set to high, the error bits of the selected status register are reset after transmission of the data in the next SPI frame (see **Chapter 7.4**).			
RA_x	Register Address, selects the control-register address for the current SPI transmission and the status-register address for the next SPI transmission.			

7.3.2 Diagnosis

Table 3 Output (Status) Data Register

Bit	StatReg 00 Lock and Mirror Heat Overload	StatReg 01 Lock and Mirror Heat Open Load	StatReg 10 Mirror and Lamp-driver Overload	StatReg 11 Mirror and Lamp-driver Open Load
	valid for input data RA = 00	valid for input data RA = 01	valid for input data RA = 10	valid for input data RA = 11
15	x	x	LS4OvL	LS4OpL
14	x	x	HS4OvL	x
13	x	x	LS5OvL	LS5OpL
12	x	x	HS5OvL	x
11	x	x	LS6OvL	LS6OpL
10	x	x	HS6OvL	x
9	HS7OvL	HS7OpL	HS8OvL	HS8OpL
8	x	x	x	x
7	x	x	HS10OvL	HS10OpL
6	x	x	x	x
Address - Independent Data				
5	PSF	PSF	PSF	PSF
4	TSD	TSD	TSD	TSD
3	TW	TW	TW	TW
Error Flags				

Table 3 Output (Status) Data Register (cont'd)

Bit	StatReg 00 Lock and Mirror Heat Overload	StatReg 01 Lock and Mirror Heat Open Load	StatReg 10 Mirror and Lamp-driver Overload	StatReg 11 Mirror and Lamp-driver Open Load
2	EF_11	EF_11	EF_11	EF_10
1	EF_10	EF_10	EF_01	EF_01
0	EF_01	EF_00	EF_00	EF_00

Note: x-bits are set to low

Table 4 Status Bit Definitions

Status Bit	Definition
LSxOvL	Low-Side switch Over Load. Set to HIGH if low-side switch no. x is shut down due to overcurrent or overtemperature or crosscurrent.
HSxOvL	High-Side switch Over Load. Set to HIGH if high-side switch no. x is shut down due to overcurrent or overtemperature or crosscurrent.
LSxOpL	Low-Side switch open load. Set to HIGH if open load (undercurrent) is detected in low-side switch x.
HSxOpL	High-Side switch Open Load. Set to HIGH if open load is detected in high-side switch x.
PSF	Power Supply Fail. Set to HIGH if the Voltage at the V_S pin is below the V_S undervoltage threshold or above the V_S overvoltage threshold.
TSD	All powerstages are shut down due to overtemperature.
TW	One or more powerstages have reached the warning temperature.
EF_xy	Error Flag for StatReg xy. Set to HIGH if any bit is set to HIGH StatReg xy.
N.C.	Not connected. These bits may be used for test-mode purposes. They are set to fixed LOW in normal operation.

7.4 Status Register Address Selection and Reset

The SPI is using a standard shift-register concept with daisy-chain capability. Any data transmitted to the SPI will be available to the internal logic part at the end of the SPI transmission (CSN L -> H). To read a specific register, the address of the register is sent by the master to the SPI in a first SPI frame. The data that corresponds to this address is transmitted by the SPI DO during the following (second) SPI frame to the master. The default address for Status Register transmission after Power-ON Reset is 00.

The Status-Register-Reset command-bit is executed after the next SPI transmission. The three bits RA_0, RA_1 and SRR act as command to read and reset (or not reset) the addressed Status-Register. This is also explained in **Figure 5**.

The TSD status bit is not part of the addressable data but of the address independent data. When any of the status registers is reset, the TSD bit is reset, too.

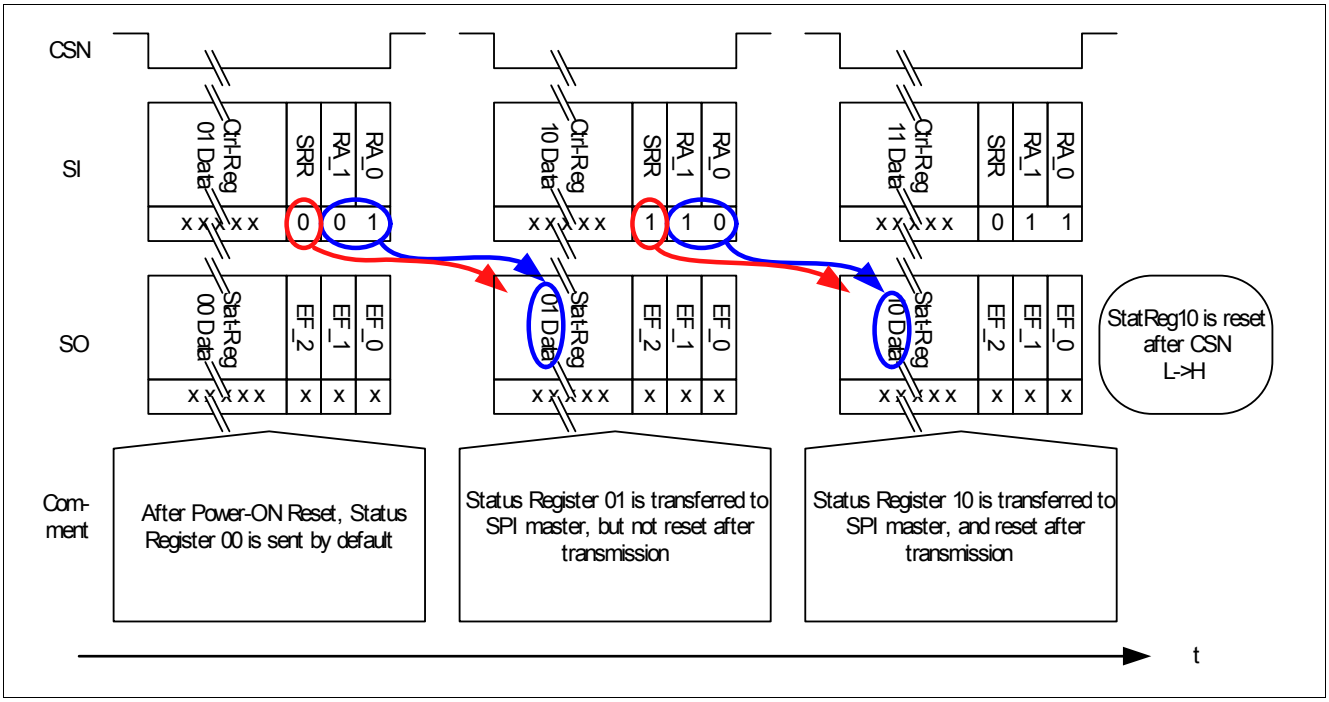


Figure 5 Status Register Addressing and Reset

7.4.1 Error-Flag

In addition to the 16 bits transferred from the TLE 8203E to the SPI master, an additional Error Flag (EF) is transmitted at the DO pin. The EF status is shown on the DO pin after CSN H -> L, before the first rising edge at CLK, as shown in **Figure 6**.

The Error flag is set to H if any of the Status Registers contains an error message (i.e. EF = EF_00 or EF_01 or EF_10 or EF_11).

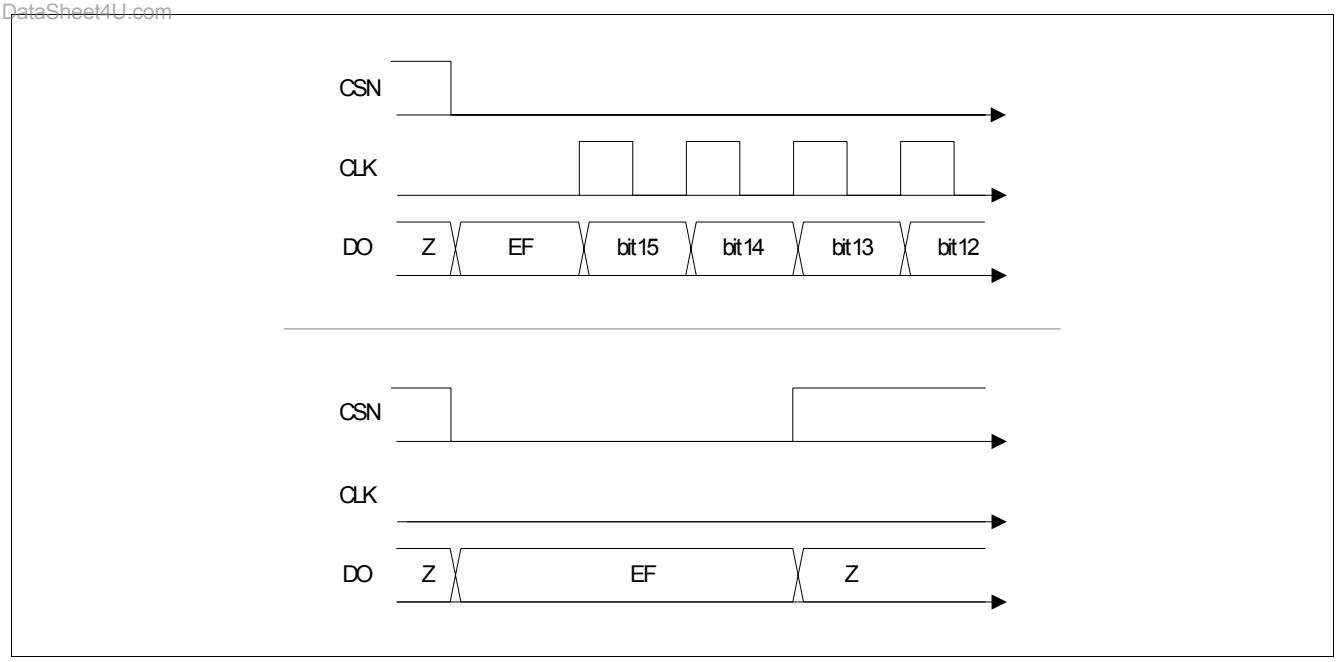


Figure 6 Error Flag Transmission on DO during Standard SPI Transmission (top), or without Additional SPI Transmission, CLK Low (bottom)

7.5 Electrical Characteristics

Electrical Characteristics: SPI-Timing

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.5.1	CSN lead time	t_{lead}	100	–	–	ns	1)
7.5.2	CSN lag time	t_{lag}	100	–	–	ns	1)
7.5.3	Fall time for CSN, CLK, DI, DO	t_f	–	–	25	ns	1)
7.5.4	Rise time for CSN, CLK, DI, DO	t_r	–	–	25	ns	1)
7.5.5	DI data setup time	t_{SU}	40	–	–	ns	1)
7.5.6	DI data hold time	t_h	40	–	–	ns	1)
7.5.7	DI data valid time	t_v	–	–	50	ns	1)
7.5.8	DO data setup time	$t_{DOsetup}$	0	–	60	ns	1)
7.5.9	DO data hold time	t_{DOhold}	50	–	–	ns	1)
7.5.10	No-data-time between SPI commands	t_{nodata}	5	–	–	µs	1)
7.5.11	Clock frequency	f_{CL}	–	–	2	MHz	1)
7.5.12	Duty cycle of incoming clock at CLK	–	40	–	60	%	1)

1) SPI Timing is not subject to production test - specified by design. SPI functional test is performed at 5 MHz CLK frequency. Timing specified with an external load of 30 pF at pin [DO].

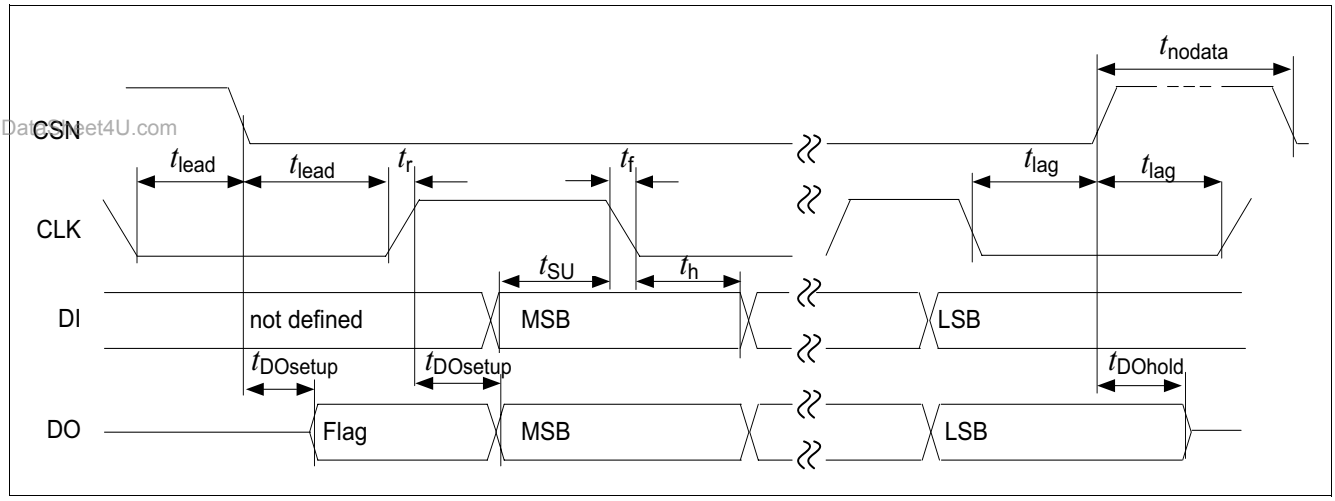


Figure 7 Timing Diagram

7.6 PWM Inputs

The PWM inputs PWM1 and PWM2 are direct power stage control inputs that can be used to switch on and off one or more of the power transistors with a PWM signal supplied to this pin. The setting of the SPI Registers CtrlReg_01 and CtrlReg_11 defines which of the power stages will be controlled by the PWM inputs. If the selection-bits of power Stage x, xsel1 and xsel2 are LOW, the power stage x is controlled only via the SPI control bit xON. If the selection bit xsel1 is HIGH and the control bit xON is also high, the power stage x is controlled by the PWM1 pin (xsel2 and PWM2, respectively). The behavior is shown in the principal schematic and in **Table 5** below. In terms of power dissipation due to switching loss, a PWM frequency below 200 Hz is recommended.

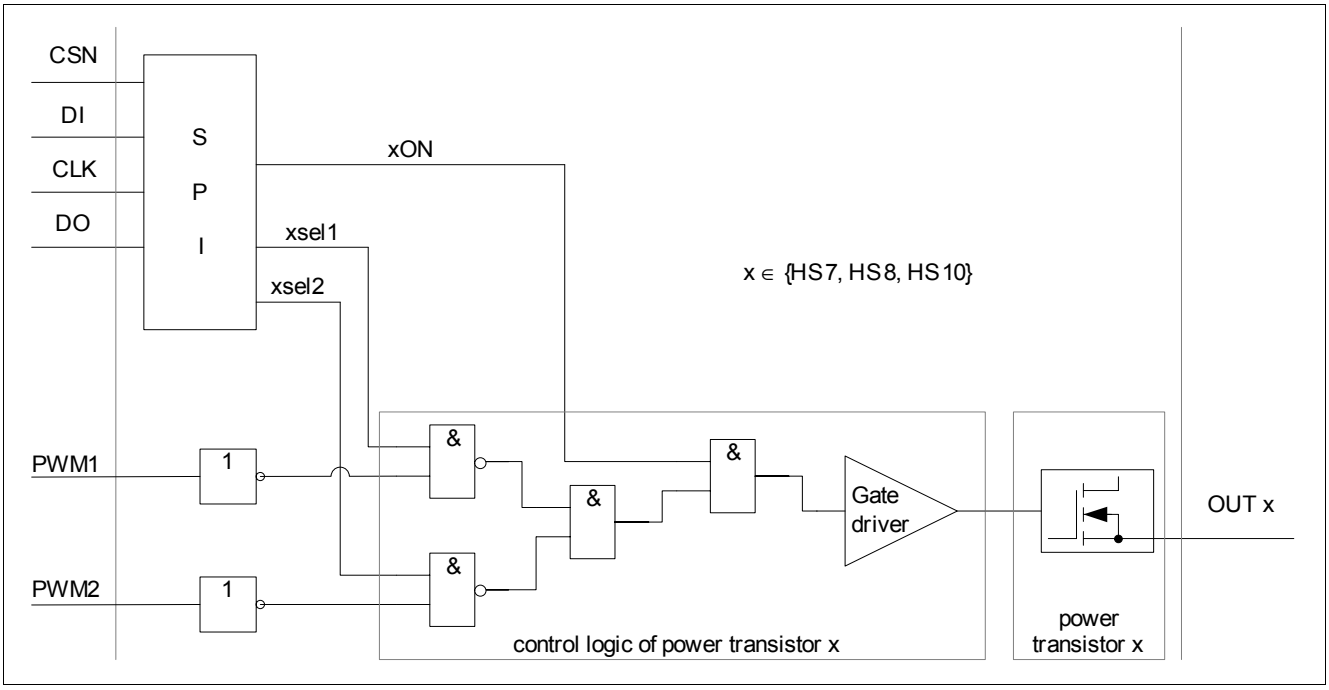


Figure 8 PWM Input and SPI Control Registers

Table 5 Truth Table for PWM Inputs

xON	xsel1	xsel2	PWM1	PWM2	Power Stage x
0	x	x	x	x	OFF
1	0	0	x	x	ON
1	1	0	0	x	OFF
1	1	0	1	x	ON
1	0	1	x	0	OFF
1	0	1	x	1	ON
1	1	1	1	x	ON
1	1	1	x	1	ON
1	1	1	0	0	OFF

8 Power-Outputs 4-6 (Bridge Outputs)

8.1 Protection and Diagnosis

8.1.1 Short Circuit of Output to Ground or V_s

The low-side switches are protected against short circuit to supply and the high-side switches against short to GND.

If a switch is turned on and the current rises above the shutdown threshold I_{SD} for longer than the shutdown delay time t_{dSD}, the output transistor is turned off and the corresponding diagnosis bit is set. During the delay time, the current is limited to I_{SC} as shown in **Figure 9**.

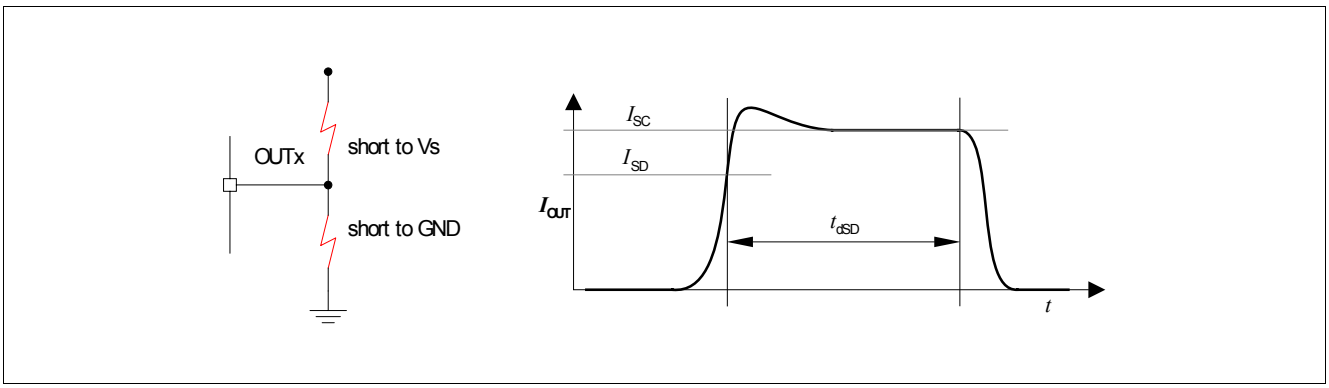


Figure 9 Short Circuit Protection

The delay time is relatively short (typ. 25 µs) to limit the energy that is dissipated in the device during a short circuit. This scheme allows high peak-currents as required in motor-applications.

The output stage stays off and the error bit set until a status register reset is sent to the SPI or a power-on reset is performed.

8.1.2 Cross-Current

If for instance HS4 is ON and LS4 is OFF, you can turn OFF HS4 and turn ON LS4 with the same SPI command. To ensure that there is no overlap of the switching slopes that would lead to a cross current, the dead-time H to L and L to H is specified.

In the control registers, it is also possible to turn ON high- and low-side switches of the same half-bridge (e.g. LS4ON = H and HS4ON = H). To prevent a cross-current through the bridge, such a command is not executed. Instead, both switches are turned OFF and the Over-Load bit is set High for both switches (e.g. LS4OvL = H and HS4OvL = H).

8.1.3 Open Load

Open-load detection in ON-state is implemented in the low-side switches of the bridge outputs: When the current through the low side transistor is lower than the reference current I_{OCD} in ON-state for longer than the open-load detection delay time t_{dOC}, the according open-load diagnosis bit is set. The output transistor, however, remains ON. The open load error bit is latched and can be reset by the SPI status register reset or by a power-on reset.

As an example, if a motor is connected between outputs OUT 4 and OUT 5 with a broken wire as shown in **Figure 10**, the resulting diagnostic information is shown in **Table 6**.

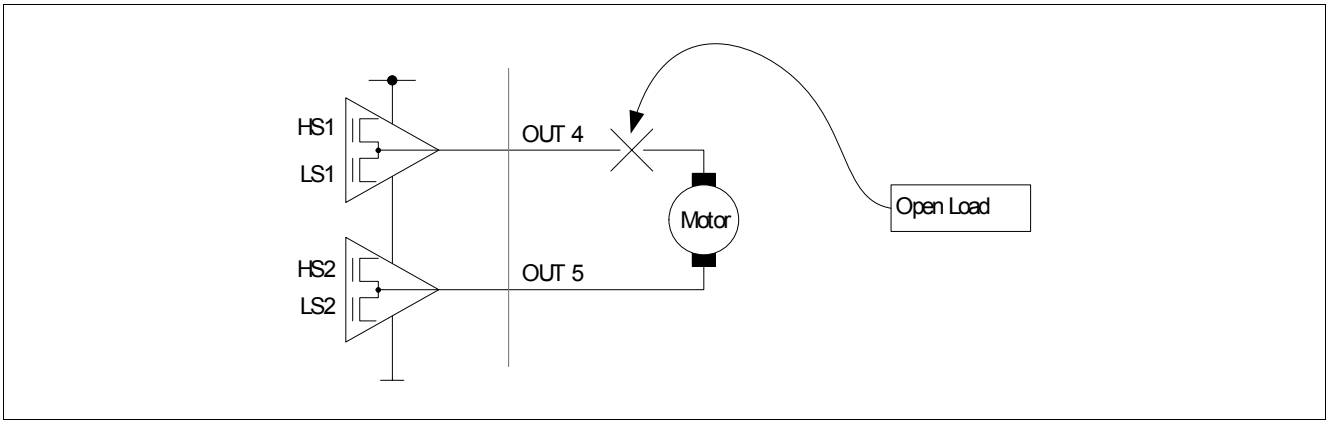


Figure 10 Open Load Example

Table 6 Open Load Diagnosis Example

Control					Diagnostic Information				
					Motor Connected		Motor Disconnected		Remark on Open Load Detection
LS4 ON	HS4 ON	LS5 ON	HS5 ON	Motor Rotation	LS4 OpL	LS5 OpL	LS4 OpL	LS5 OpL	
0	0	0	0	motor off	0	0	0	0	not detectable
1	0	0	1	clock-wise	0	0	1	0	detected
0	1	1	0	counter clock-wise	0	0	0	1	detected
0	1	0	1	brake high	0	0	0	0	not detectable
1	0	1	0	brake low	1	1	1	1	not detectable

8.2 Electrical Characteristics

Electrical Characteristics: OUT4 (Driver for mirror xy and halfbridge for fold)

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Static Drain-Source ON-Resistance							
8.2.1	High- and low-side switch	R_{DSON4}	–	0.3	–	Ω	I_{OUT} = ±1 A; T_j = 25 °C
			–	0.4	0.7	Ω	I_{OUT} = ±1 A T_j = 150 °C
Switching Times							
8.2.2	High-side ON delay-time	t_{dONH4}	–	50	100	µs	V_S = 14 V; resistive load of 14 Ω, see Figure 11 and Figure 12
8.2.3	High-side OFF delay time	t_{dOFFH4}	–	25	50	µs	
8.2.4	Low-side ON delay-time	t_{dONL4}	–	50	100	µs	
8.2.5	Low-side OFF delay time	t_{dOFFL4}	–	25	50	µs	
8.2.6	Dead-time H to L	t_{DHL4}	3	–	–	µs	t_{dONL4} - t_{dOFFH4}

Electrical Characteristics: OUT4 (Driver for mirror xy and halfbridge for fold) (cont'd)

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.2.7	Dead-time L to H	t_{DLH4}	3	–	–	µs	t_{dONH4} - t_{dOFFL4}
Short Circuit Protection							
8.2.8	Over-current shutdown threshold	I_{SD4}	3	4	8	A	high- and low-side
8.2.9	Shutdown delay time	t_{dSD4}	10	25	50	µs	
8.2.10	Short Circuit current[1)]	I_{SC4}	–	6	–	A	
Open Load Detection							
8.2.11	Detection current	I_{OCD4}	12	25	45	mA	low-side
8.2.12	Delay time	t_{dOC4}	200	350	600	µs	
Leakage Current							
8.2.13	OFF-state output current	$I_{OUT4\_leakage}$	–	–	10	µA	V_{OUT} = 0.2 V

1) Not subject to production test - specified by design.

Electrical Characteristics: OUT 5, 6 (driver for mirror x-y position)

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Static Drain-Source ON-Resistance							
8.2.14	High- and low-side switch	R_{DSON56}	–	0.5	–	Ω	I_{OUT} = ±0.5 A; T_j = 25 °C
			–	0.8	1.3	Ω	I_{OUT} = ±0.5 A T_j = 150 °C
Switching Times							
8.2.15	High-side ON delay time	t_{dONH56}	–	50	100	µs	V_S = 14 V; resistive load of 25 Ω, see Figure 11 and Figure 12
8.2.16	High-side OFF delay time	$t_{dOFFH56}$	–	25	50	µs	
8.2.17	Low-side ON delay time	t_{dONL56}	–	50	100	µs	
8.2.18	Low-side OFF delay time	$t_{dOFFL56}$	–	25	50	µs	
8.2.19	Dead-time H to L	t_{DHL56}	3	–	–	µs	t_{dONL56} - $t_{dOFFH56}$
8.2.20	Dead-time L to H	t_{DLH56}	3	–	–	µs	t_{dONH56} - $t_{dOFFL56}$
Short Circuit Protection							
8.2.21	Over-current shutdown threshold	I_{SD56}	1.25	1.5	3.0	A	high- and low-side
8.2.22	Shutdown delay time	t_{dSD56}	10	25	50	µs	
8.2.23	Short Circuit current[1)]	I_{SC56}	–	3.0	–	A	
Open Load Detection							
8.2.24	Detection current	I_{OCD56}	12	25	40	mA	low-side
8.2.25	Delay time	t_{dOC56}	200	350	600	µs	

Electrical Characteristics: OUT 5, 6 (driver for mirror x-y position) (cont'd)

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Leakage Current							
8.2.26	OFF-state output current	$I_{OUT56\_leakage}$	–	–	10	µA	V_{OUT} = 0.2 V

1) Not subject to production test - specified by design.

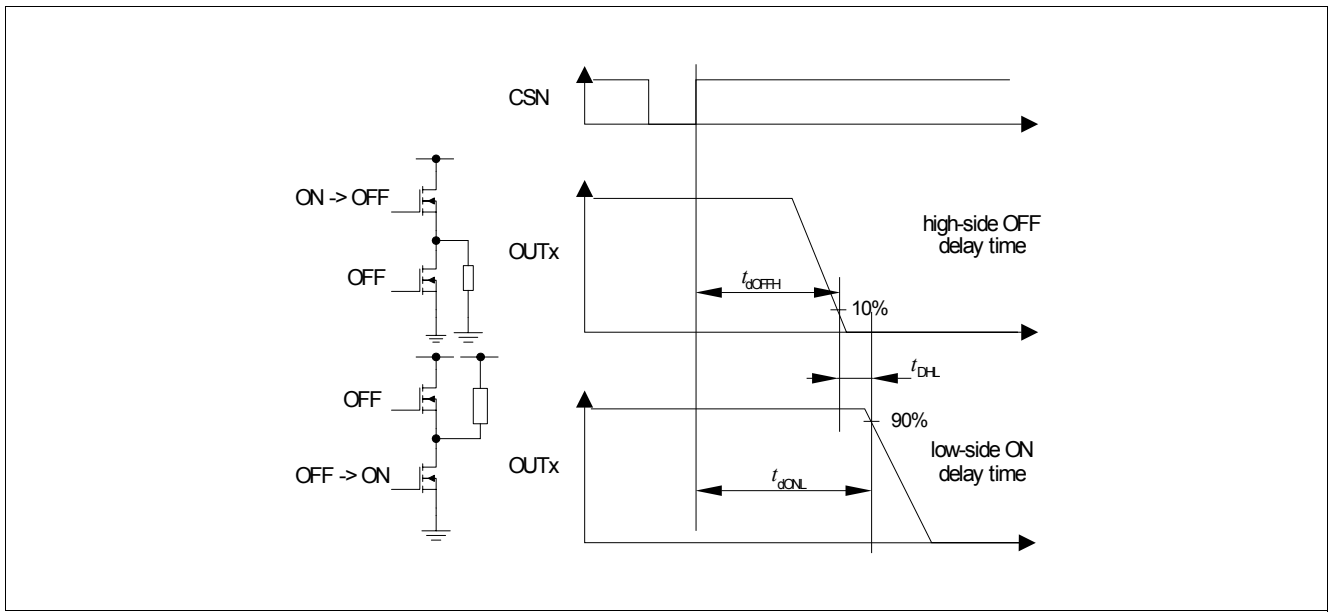


Figure 11 Timing Bridge Outputs High to Low

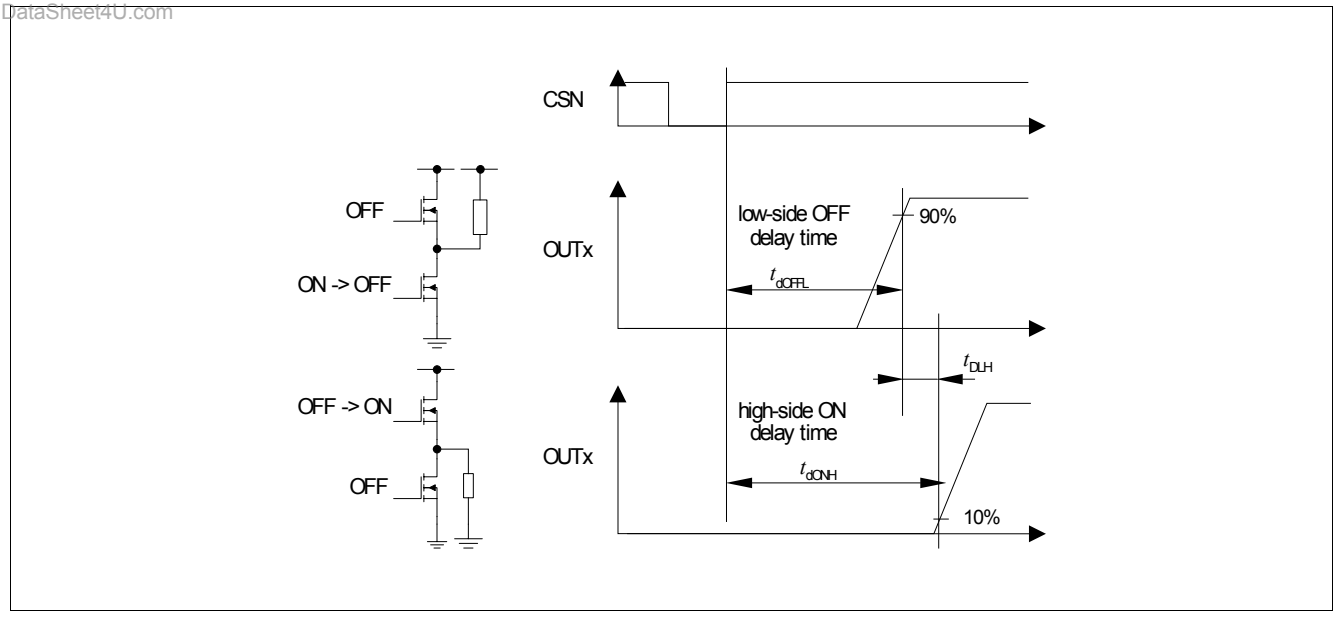


Figure 12 Timing Bridge Outputs Low to High

9 Power-Output 7 (Mirror Heater Driver)

Output 7 is a high-side switch intended to drive ohmic loads like the heater of an exterior mirror.

9.1 Protection and Diagnosis

9.1.1 Short Circuit of Output to Ground

If the high-side switch is turned on and the current rises above the shutdown threshold I_{SD} for longer than the shutdown delay time t_{dSD}, the output transistor is turned off and the corresponding diagnosis bit is set. During the delay time, the current is limited to I_{SC} as shown in **Figure 13**.

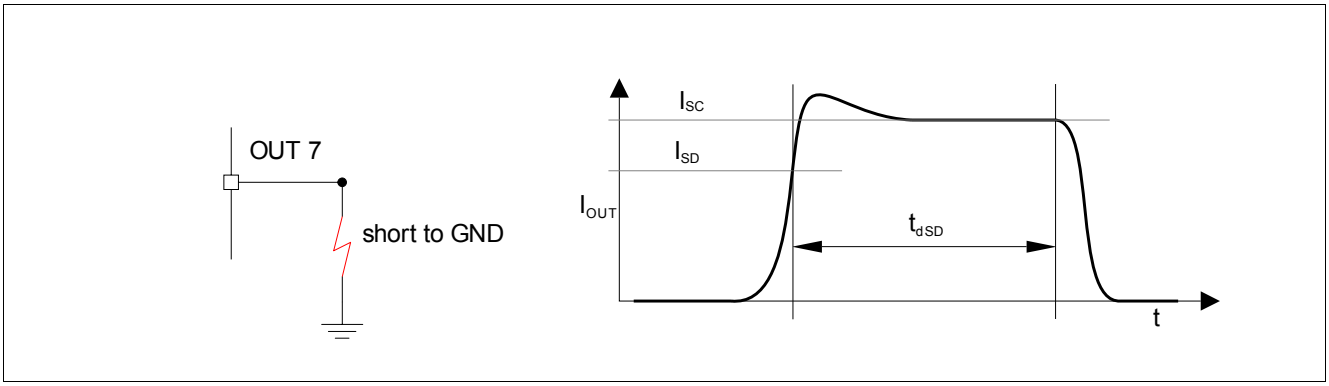


Figure 13 Short Circuit Protection

The output stage stays off and the error bit set until a status register reset is sent to the SPI or a power-on reset is performed.

9.1.2 Open Load

For the high-side switches, an open-load in OFF-state scheme is used as shown in **Figure 10**. The output is pulled up by a current source I_{OpL}. In OFF-state, the output voltage is monitored and compared to the threshold V_{OpL}. If the voltage rises above this threshold, the open-load signal is set to high. This is equivalent to comparing the load resistance to the value V_{OpL} / I_{OpL}. The open load error bit is latched and can be reset by the SPI status register reset or by a power-on reset.

The pull-up current can be switched on and off by the OpLxON bits. This bit should be set to LOW (i.e. pull-up current switched off) if an output is used to drive LEDs because they may emit light if biased with the pull-up current.

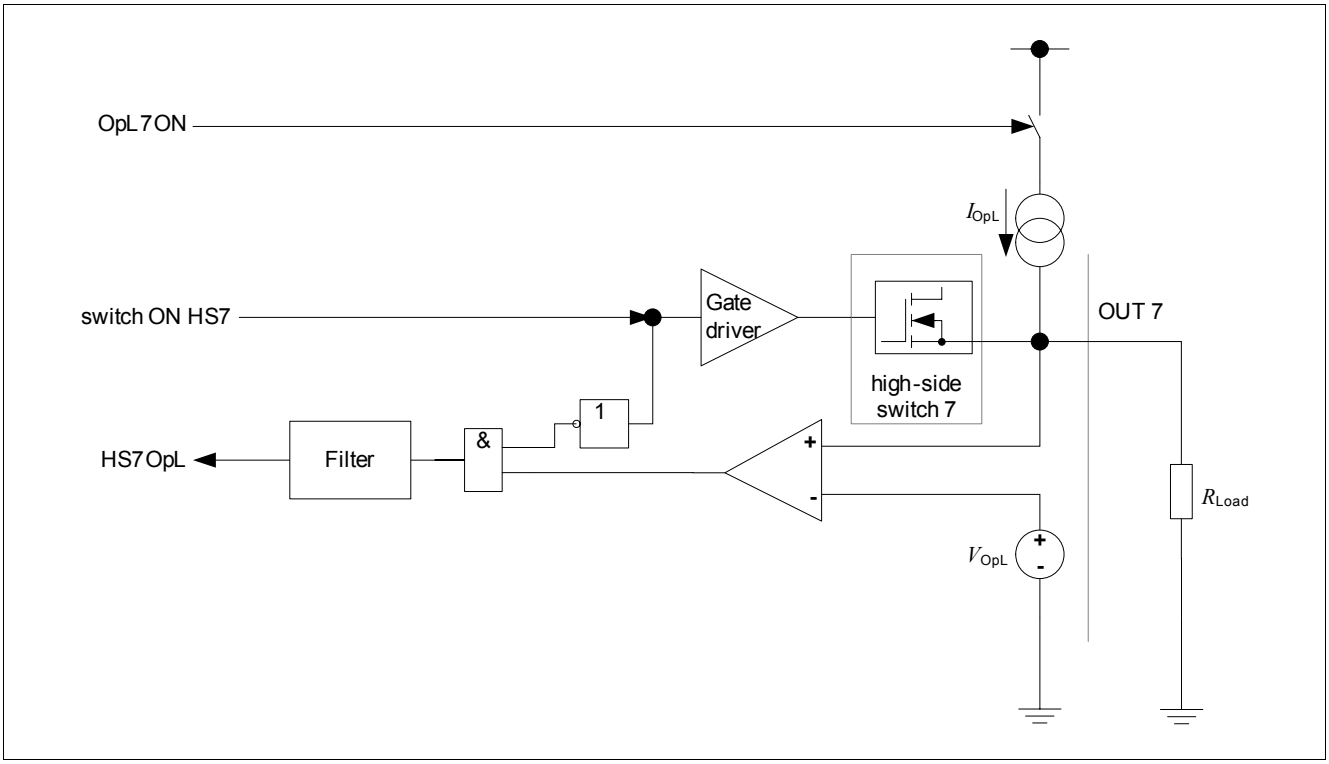


Figure 14 Open Load in OFF-state Scheme

9.2 Electrical Characteristics

Electrical Characteristics: OUT 7(mirror heater driver)

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Static Drain-source ON-Resistance							
9.2.1	High-side switch	R_{DSON7}	–	0.07	–	Ω	I_{OUT} = 2.5 A; T_j = 25 °C
			–	0.1	0.17	Ω	I_{OUT} = 2.5 A T_j = 150 °C
Switching Times							
9.2.2	Turn-ON delay time	t_{dONH7}	–	5	15	µs	V_S = 14 V; resistive load of 10 Ω, see Figure 15
9.2.3	Output rise-time	t_{rise7}	–	15	40	µs	
9.2.4	Turn-OFF delay time	t_{dOFFH7}	–	20	40	µs	
9.2.5	Output fall-time	t_{fall7}	–	5	10	µs	
Short Circuit Protection							
9.2.6	Over-current shutdown threshold	I_{SD7}	6.25	8	11	A	–
9.2.7	Shutdown delay time	t_{dSD7}	10	25	50	µs	–
9.2.8	Short Circuit current[1)]	I_{SC7}	–	12	–	A	–
Open Load Detection							
9.2.9	Pull-up current	I_{OpL7}	100	–	300	µA	V_{OUT} = 4 V

Electrical Characteristics: OUT 7(mirror heater driver) (cont'd)

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.2.10	Detection Threshold	V_{OpL7}	2	–	4	V	–
9.2.11	Delay time	t_{dOC7}	–	–	200	µs	–
Leakage Current							
9.2.12	OFF-state output current	$I_{OUT7\_leakage}$	–	–	5	µA	V_{OUT} = GND

1) Not subject to production test - specified by design.

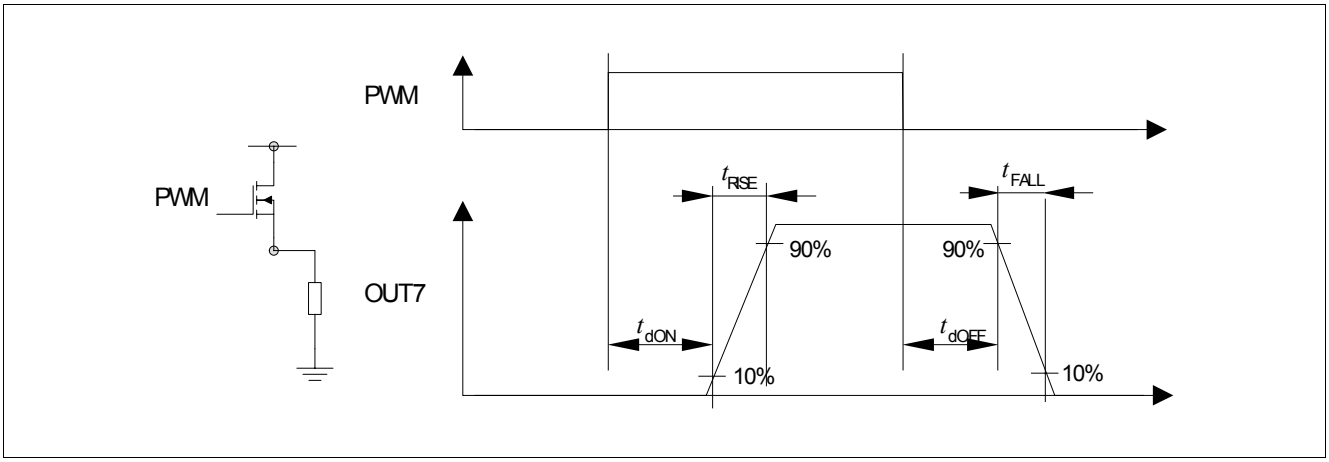


Figure 15 Timing OUT 7

10 Power-Outputs 8 and 10 (Lamp drivers)

Outputs 8 and 10 are a high-side switches intended to drive ohmic loads 5 W or 10 W lamp (bulb) loads.

10.1 Protection and Diagnosis

10.1.1 Short Circuit of Output to Ground

The high-side switches Out 8 and 10 are protected against short to GND.

Short Circuit during Switch-on

During switch-on of an output a current and voltage level is used to check for a short circuit. If a switch is turned on and the short circuit condition is valid after t_{dSDon8} the output transistor is turned off and the corresponding diagnosis bit is set. A short circuit condition is valid if the current rises above the shutdown threshold I_{SD8} and the voltage at the output stays below V_{SD8}. During the delay time, the current is limited to I_{SC8} as shown in **Figure 16**

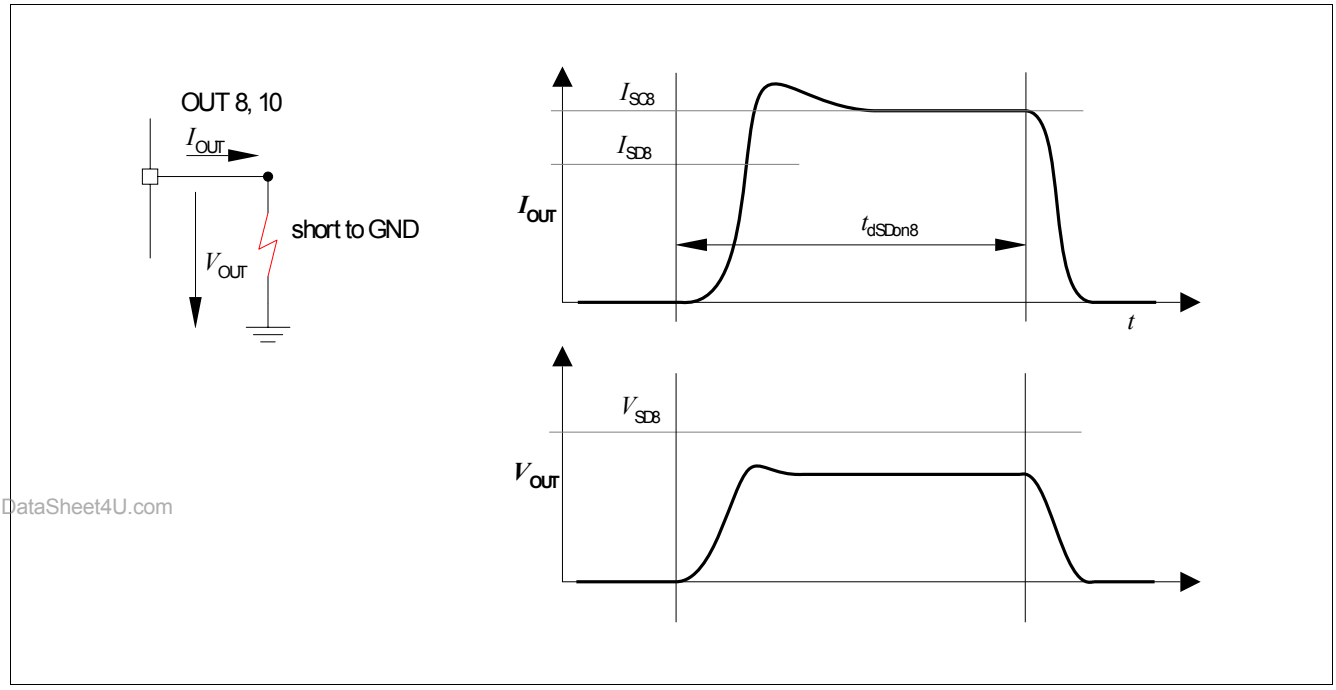


Figure 16 Short Circuit Protection during Switch-on

Short Circuit in On-state

If a switch is already on and the current rises above the shutdown threshold I_{SD} for longer than the shutdown delay time t_{dSD} the output transistor is turned off and the corresponding diagnosis bit is set. This is independent of the voltage V_{out}. See **Figure 17**.

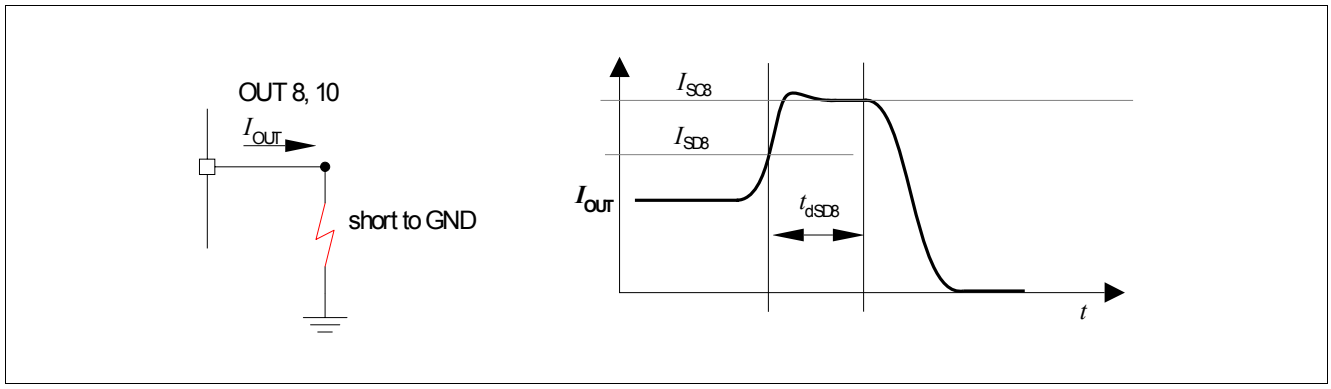


Figure 17 Short Circuit Protection in On-state

10.1.2 Open Load

For the high-side switches, an open-load in OFF-state scheme is used as shown in **Figure 18**. The output is pulled up by a current source I_{OpL}. In OFF-state, the output voltage is monitored and compared to the threshold V_{OpL}. If the voltage rises above this threshold, the open-load signal is set to high. This is equivalent to comparing the load resistance to the value V_{OpL} / I_{OpL}. The open load error bit is latched and can be reset by the SPI status register reset or by a power-on reset.

The pull-up current can be switched on and off by the OpLxON bits. This bit should be set to LOW (i.e. pull-up current switched off) if an output is used to drive LEDs because they may emit light if biased with the pull-up current.

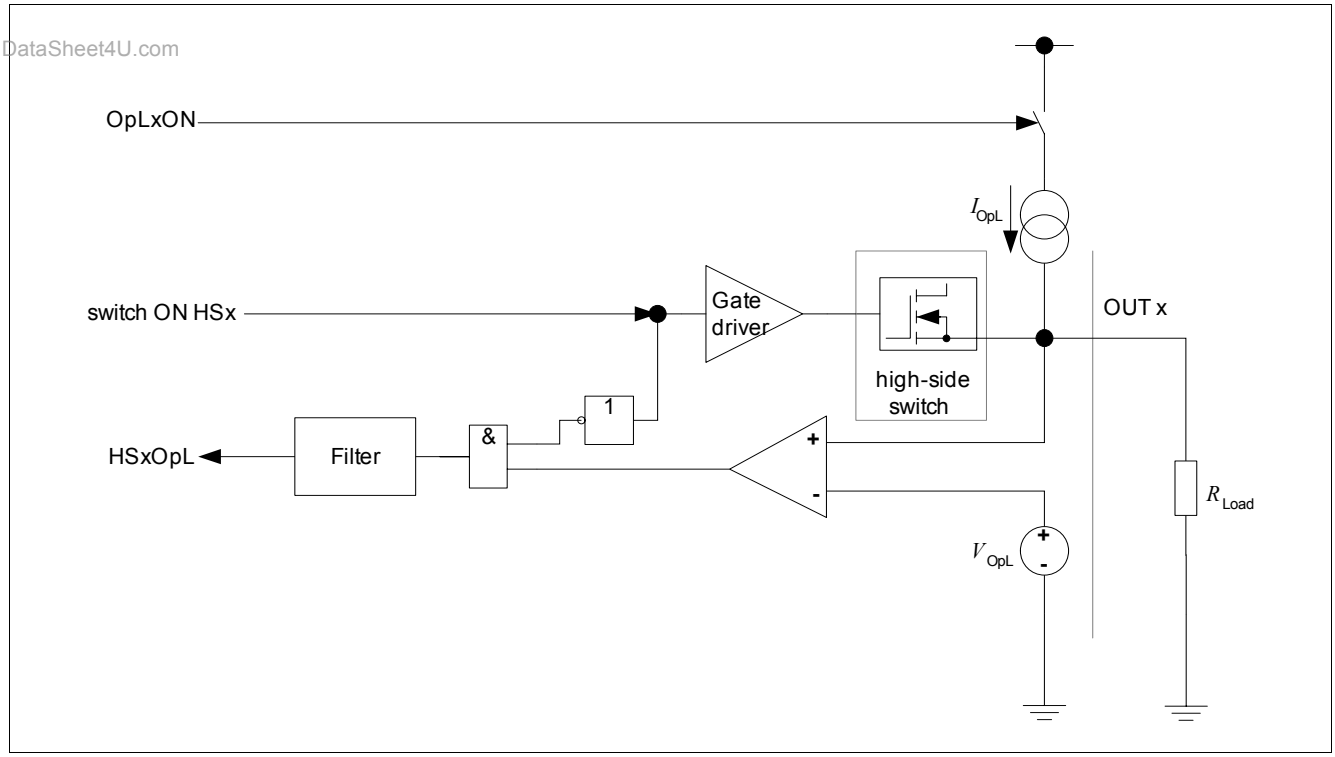


Figure 18 Open Load in OFF-state Scheme

10.2 Electrical Characteristics

Electrical Characteristics: OUT 8, 10 (Lamp drivers)

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Static Drain-Source ON-Resistance							
10.2.1	High-side switch	$R_{DSON8,10}$	–	0.4	–	Ω	I_{OUT} = +0.5 A; T_j = 25 °C
			–	0.5	0.8	Ω	I_{OUT} = +0.5 A T_j = 150 °C
Switching Times							
10.2.2	Turn-ON delay time	$t_{dONH8,10}$	–	5	15	µs	V_S = 14 V; resistive load of 25 Ω, see Figure 15
10.2.3	Output rise-time	$t_{rise8,10}$	5	10	30	µs	
10.2.4	Turn-OFF delay time	$t_{dOFFH8,10}$	–	25	50	µs	
10.2.5	Output fall-time	$t_{fall8,10}$	7	15	30	µs	
Short Circuit Protection							
10.2.6	Over-current shutdown threshold	$I_{SD8,10}$	1.8	2.9	3.5	A	–
10.2.7	Over-current shutdown threshold voltage	$V_{SD8,10}$	1.5	2.5	3.3	V	–
10.2.8	Short circuit current[1)]	$I_{SC8,10}$	–	4.2	–	A	–
10.2.9	Shutdown delay time	$t_{dSDon8,10}$	125	200	350	µs	at switching-on
10.2.10	Shutdown delay time	$t_{dSD8,10}$	10	25	60	µs	in on-state
Open Load Detection							
10.2.11	Pull-up current	$I_{OpL8,10}$	100	–	250	µA	V_{OUT} = 4 V
10.2.12	Detection Threshold	$V_{OpL8,10}$	2	–	4	V	–
10.2.13	Delay time	$t_{dOC8,10}$	–	–	200	µs	–
Leakage Current							
10.2.14	OFF-state output current	$I_{OUT810\_leakage}$	–	–	5	µA	V_{OUT} = GND

1) Not subject to production test - specified by design.

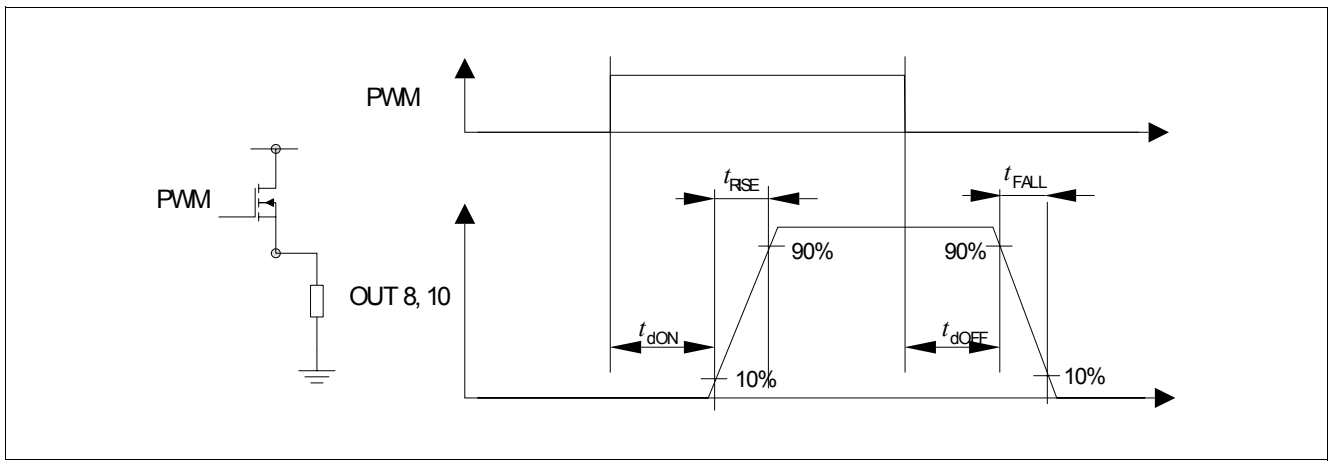


Figure 19 Timing OUT 8, 10

11 Logic In- and Outputs

The threshold specifications of the logic inputs are compatible to both 5 V and 3.3 V standard CMOS micro controller outputs. The logic output DO is a 5 V CMOS output.

11.1 Electrical Characteristics

Electrical Characteristics: Diagnostics

V_S = 8 V to 20 V; V_{DD} = 4.75 V to 5.25 V, T_j = -40 °C to +150 °C; INH = High; all outputs open, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Inhibit Input							
11.1.1	H-input voltage threshold	V_{IH}	–	–	2	V	V_{IN} rising
11.1.2	L-input voltage threshold	V_{IL}	1	–	–	V	V_{IN} falling
11.1.3	Hysteresis of input voltage	V_{IHY}	100	–	600	mV	–
11.1.4	Pull-down current	I_{IINH}	–	–	50	µA	V_{IINH} = 2 V
Logic Inputs DI, CLK, CSN, PWM1 and PWM2							
11.1.5	H-input voltage threshold	V_{IH}	–	–	2	V	V_{IN} rising
11.1.6	L-input voltage threshold	V_{IL}	1	–	–	V	V_{IN} falling
11.1.7	Hysteresis of input voltage	V_{IHY}	100	–	600	mV	–
11.1.8	Pull-up current at pin CSN	I_{ICSN}	-50	-25	-10	µA	V_{CSN} = 1 V
11.1.9	Pull-down current at pins PWM1, PWM2, DI, CLK	I_{Input}	10	25	50	µA	V_{Input} = 2 V
11.1.10	Input capacitance at pin CSN, DI, CLK, PWM1, PWM2[1)]	C_I	–	10	15	pF	0 V < V_{DD} < 5.25 V
Logic Output DO							
11.1.11	H-output voltage level	V_{DOH}	V_{DD} - 1.0	V_{DD} - 0.7	–	V	I_{SDOH} = 1 mA
11.1.12	L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{SDOL} = -1.6 mA
11.1.13	Tri-state leakage current	I_{DOLK}	-10	–	10	µA	V_{CSN} = V_{DD}; 0 V < V_{SDO} < V_{DD}
11.1.14	Tri-state input capacitance[1)]	C_{DO}	–	10	15	pF	V_{CSN} = V_{DD}; 0 V < V_{DD} < 5.25 V

1) Not subject to production test, specified by design.

12 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

12.1 Application Diagram

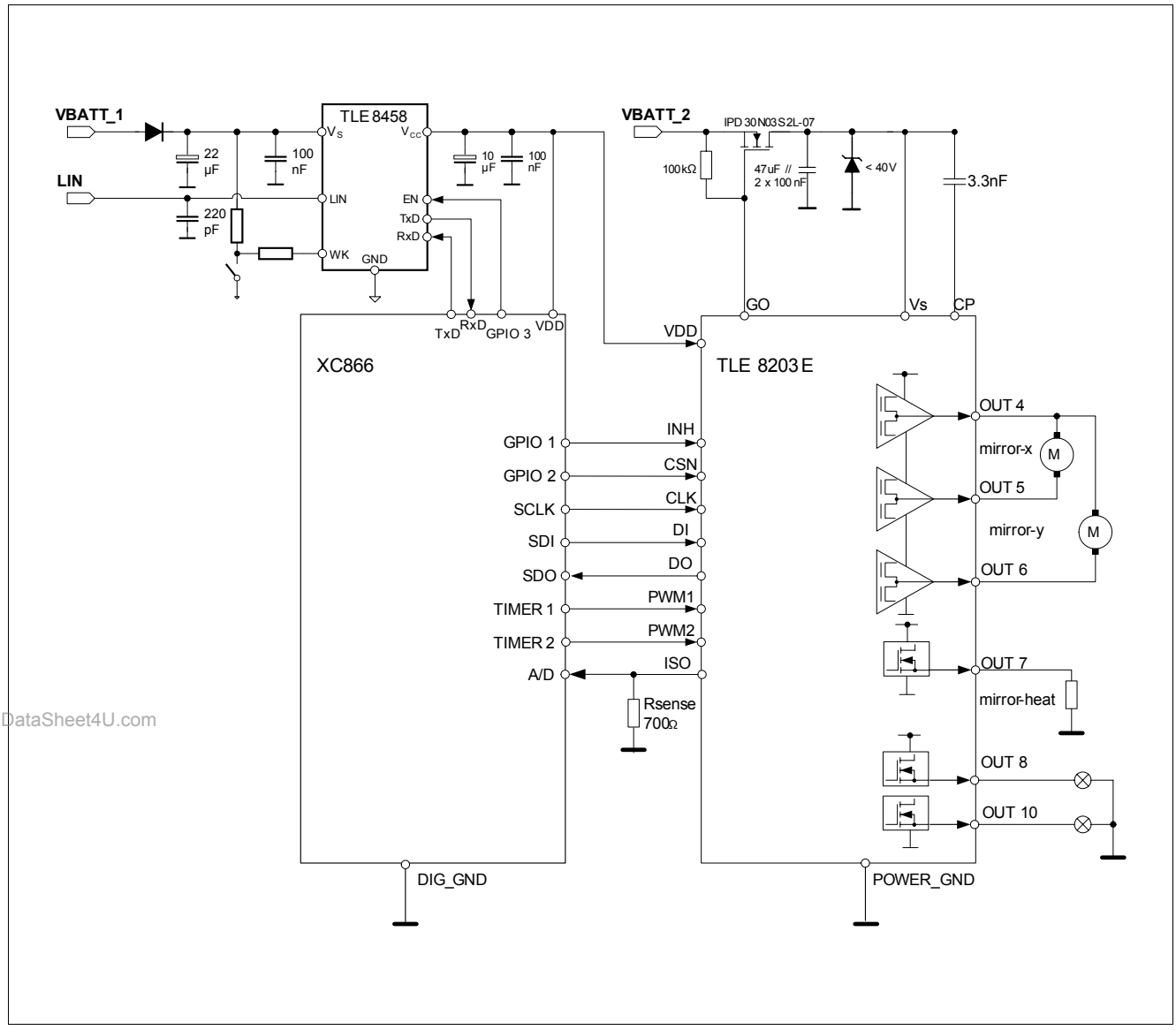
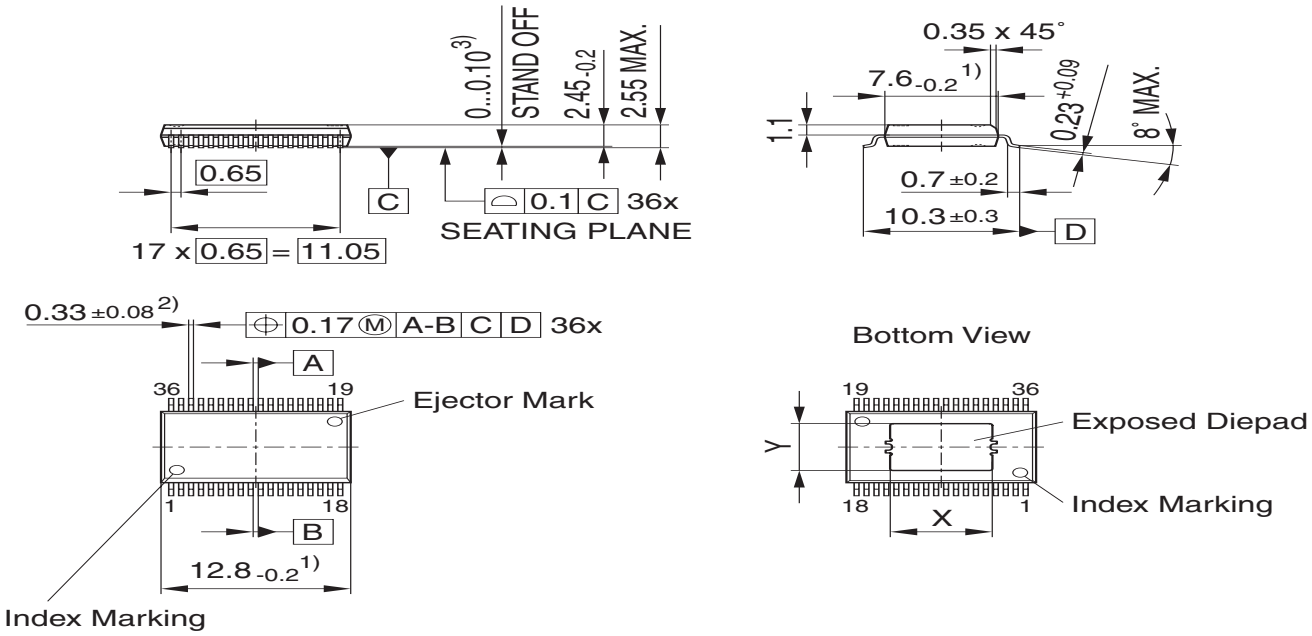


Figure 20 Application Example for Mirror Control

13 Package Outlines



Exposed Diepad Dimensions			
Package	Leadframe	X	Y
PG-DSO-36-24, -41, -42	A6901-C001	7	5.1
PG-DSO-36-38	A6901-C003	7	5.1
PG-DSO-36-38	A6901-C007	5.2	4.6
PG-DSO-36-50	A6901-C008	6.0	5.4

1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side
3) Distance from leads bottom (= seating plane) to exposed diepad

PG-DSO-36-24, -38, -41, -42, -50-PO V09

Figure 21 PG-DSO-36-50 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

14 Revision History

0.9

Version	Date	Changes
1.0	03.02.09	Final Data Sheet Release

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Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.