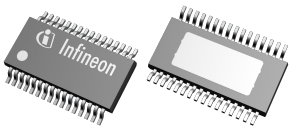
MOTIX™ Bridge

Features



- Integrated half-bridges and high-side switches
  - Overcurrent detection
  - Open load detection
  - High-side current sense
  - PWM input for half-bridges (up to 25 kHz)
  - Integrated PWM generators with phase shift for high-side switches
  - Control of capacitive loads for high-side switches
- Electrochromic mirror control
- Driver for external MOSFET for heater function
- 5 V / 3.3 V regulator with short circuit protection for off-board supply
- 32-bit SPI interface for control and diagnostic
- Overtemperature warning and protection
- Over- and under-voltage lockout
- Watchdog

Potential applications

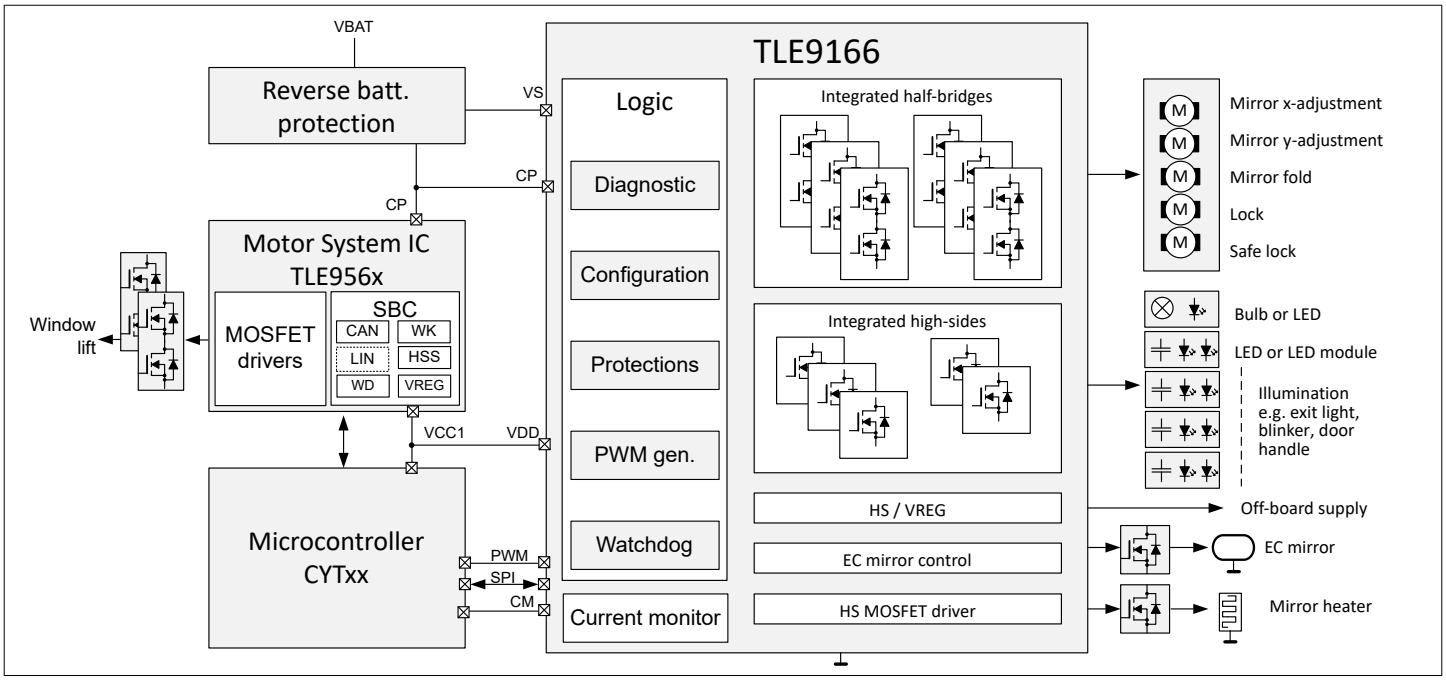
Door zone applications

Product validation

Product validation according to AEC-Q100, Grade 1. Qualified for automotive applications.

Description

The device is optimized for automotive door zone modules to control mirror functions such as mirror positioning, folding and heating, including electrochromic mirror functions. It also integrates half-bridges to control door locks and safe locks, as well as high-sides for LED control.



Product type	Package	Marking
TLE9166EQ	PG-TSDSO-32	TLE9166EQ

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1 Block diagram

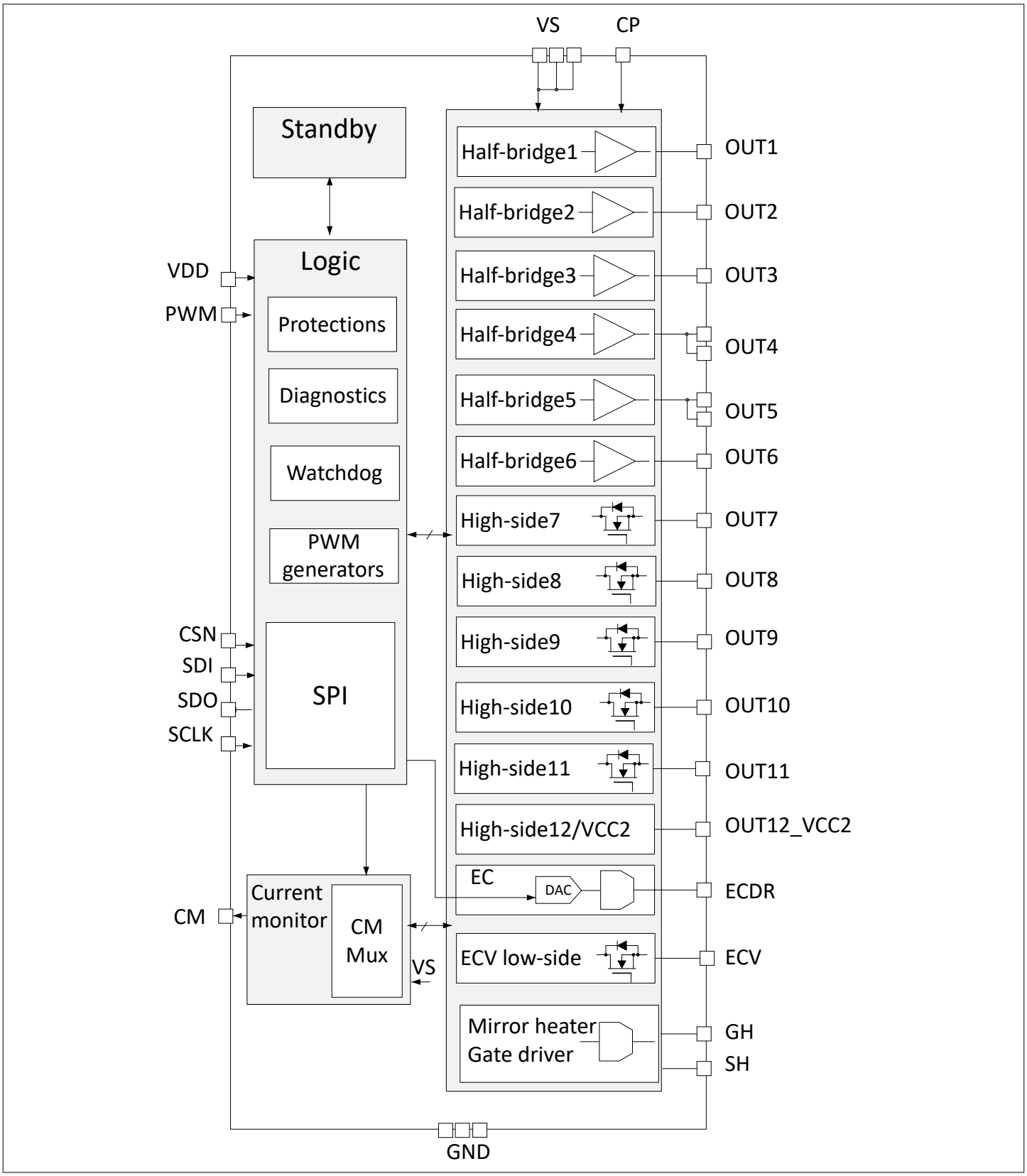


Figure 1 Block diagram TLE9166

1.1 Voltage and current definition

Chapter 1.1 shows terms used in this datasheet, with associated convention for positive values.
When OUT12_VCC2 is configured as voltage regulator, then the current flowing out of the pin is considered positive.

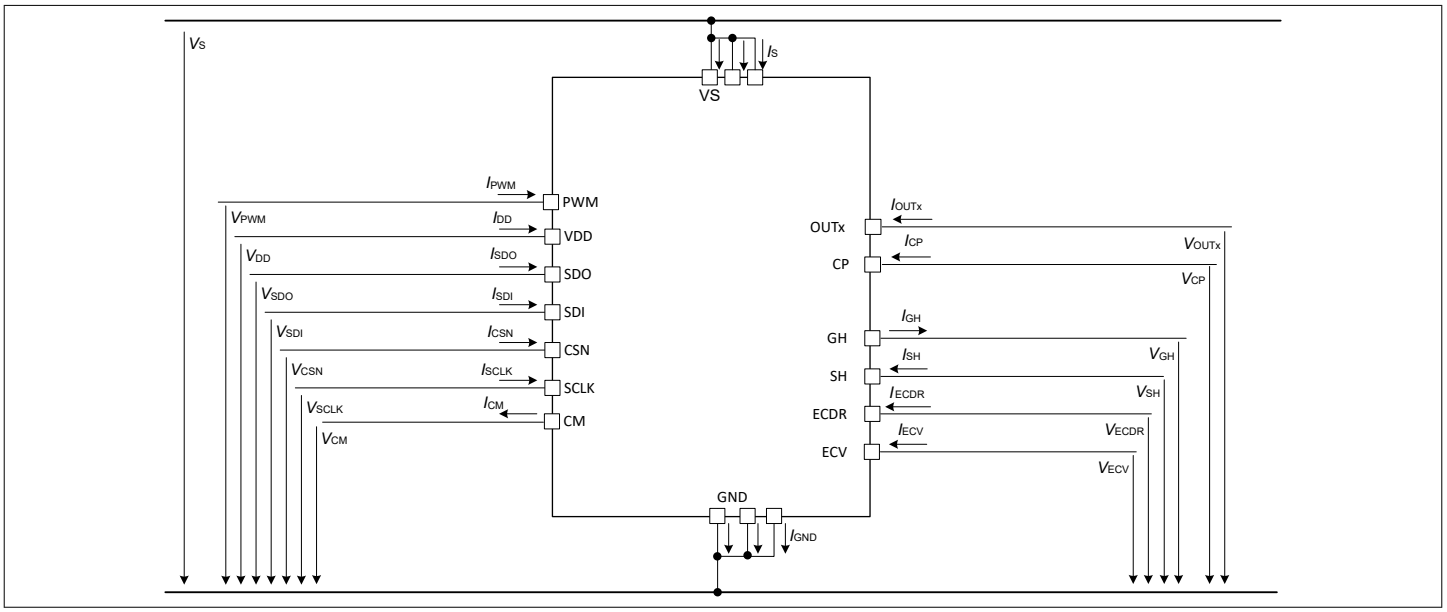


Figure 2 Voltage and current definition

2 Pin configuration

2.1 Pin assignment

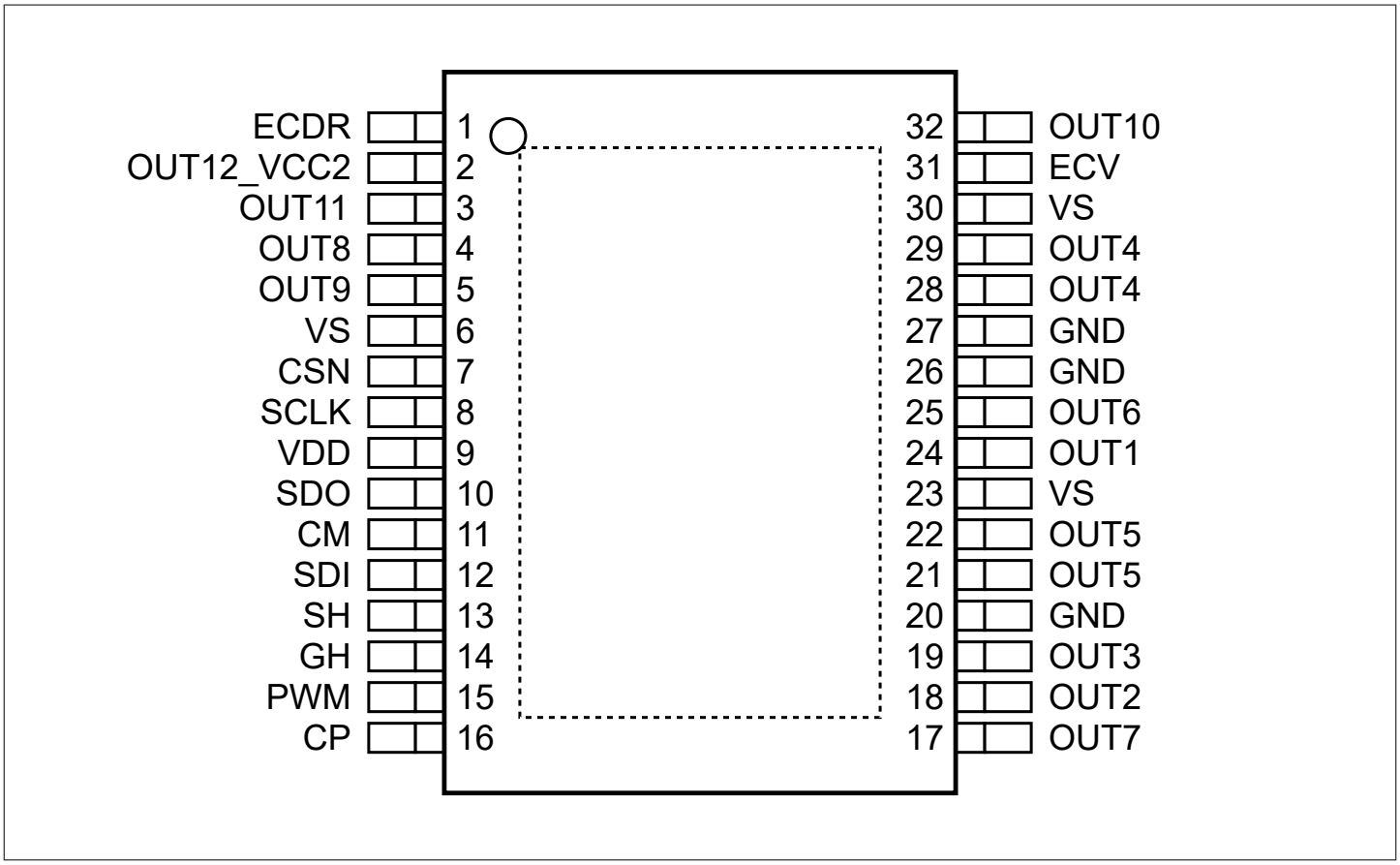


Figure 3 Pin configuration

2.2 Pin definitions and functions

Table 1 Pin definition and functions

Pin	Symbol	Function
1	ECDR	MOSFET driver for electrochromic mirror
2	OUT12_VCC2	Output 12 Configurable as high-side or as VCC2 (LDO)
3	OUT11	Output 11 (high-side)
4	OUT8	Output 8 (high-side)
5	OUT9	Output 9 (high-side)
6	VS	Main voltage supply for the integrated high-sides and half-bridges All VS pins must be connected externally
7	CSN	Chip select not input with internal pull-up
8	SCLK	Serial clock input with internal pull-down

(table continues...)

Table 1 (continued) Pin definition and functions

Pin	Symbol	Function
9	VDD	VDD supply Power supply for digital circuits. To be connected to the microcontroller supply.
10	SDO	Serial data output
11	CM	Current monitor High-side current sensing and VS monitoring
12	SDI	Serial data input with internal pull-down
13	SH	Connection to the source of the MOSFET for heater function
14	GH	Connection to the gate of the MOSFET for heater function
15	PWM	PWM input
16	CP	Charge pump input
17	OUT7	Output 7 (high-side)
18	OUT2	Half-bridge output 2
19	OUT3	Half-bridge output 3
20	GND	Ground All GND pins must be connected externally
21-22	OUT5	Half-bridge output 5 All OUT5 pins must be connected externally
23	VS	Main voltage supply for the integrated high-sides and half-bridges. All VS pins must be connected externally
24	OUT1	Half-bridge output 1
25	OUT6	Half-bridge output 6
26-27	GND	Ground All GND pins must be connected externally
28-29	OUT4	Half-bridge output 4 All OUT4 pins must be connected externally
30	VS	Main voltage supply for the integrated high-sides and half-bridges. All VS pins must be connected externally
31	ECV	Input for the measurement of the electrochromic mirror voltage. This pin is also connected to a low-side driver for a fast discharge
32	OUT10	Output 10 (high-side)
	EP	Exposed Pad; For cooling purpose only - not usable as electrical ground. Electrical ground must be provided by the GND pins [1)]

The exposed die pad at the bottom of the package allows better heat dissipation from the device via the PCB.

The exposed pad (EP) must be either left open or connected to GND. It is recommended to connect EP to GND for a better thermal performance.

3 General product characteristics

Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3.1 Absolute maximum ratings

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V	–	P_GEN_01_01
Logic supply voltage	V_{DD}	-0.2	–	5.5	V	–	P_GEN_01_02
Charge pump voltage	V_{CP}	-0.3	–	Min(V_S+ 17; 52)	V	–	P_GEN_01_03
Static output voltage	V_{OUTx}	-0.3	–	V_S + 0.3	V	–	P_GEN_01_04
Dynamic half-bridge slew rate	$V_{OUTx\_SR\_MAX}$	-20	–	20	V/µs	Slew rate applied to OUT1 to OUT6	P_GEN_01_05
SDI, CSN	V_{SDI},V_{CSN}	-0.3	–	V_S + 0.3 V	V	–	P_GEN_01_07
SDO, CM, SCLK	V_{SDO}, V_{CM}, V_{SCLK}	-0.3	–	V_{DD}+0.3	V	–	P_GEN_01_08
ECDR voltage	V_{ECDR}	-0.3	–	V_S+0.3	V	–	P_GEN_01_09
ECV voltage	V_{ECV}	-0.3	–	V_S+0.3	V	–	P_GEN_01_10
VECDR - VECV	V_{EC_DIFF}	-0.3	–	V_S	V	V_{ECDR}-V_{ECV}	P_GEN_01_31
VSH voltage	V_{SH}	-6	–	V_S +0.3	V	–	P_GEN_01_11
VGH voltage	V_{GH}	-6	–	V_{CP} + 0.3	V	–	P_GEN_01_12
VGH-VSH	V_{GS}	-0.3	–	12	V	–	P_GEN_01_13
VSH - VCP	V_{SH} - V_{CP}	–	–	0.6	V		P_GEN_01_29
PWM	V_{PWM}	-0.3	–	V_{CP}	V	–	P_GEN_01_30
Currents							
Cumulated VS current	I_{VS}	-10	–	10	A	Cumulated DC current for all 3 VS pins [1)]	P_GEN_01_14

(table continues...)

Table 2 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cumulated GND current	I_{GND}	-12	–	12	A	Cumulated DC current for all 3 GND pins 1)	P_GEN_01_15
Output current, OUT1,6	$I_{OUT1,6}$	-5	–	5	A	2)	P_GEN_01_16
Output current OUT2,3	$I_{OUT2,3}$	-1.1	–	1.1	A	2)	P_GEN_01_17
Output current OUT4	I_{OUT4}	-7	–	7	A	2)	P_GEN_01_18
Output current OUT5	I_{OUT5}	-8	–	8	A	2)	P_GEN_01_19
Output current OUT7	I_{OUT7}	-3	–	3	A	2)	P_GEN_01_21
Output current OUT8-12, ECV	$I_{OUT8-12}$	-1.1	–	1.1	A	2)	P_GEN_01_22
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_GEN_01_24
Storage temperature	T_{stg}	-50	–	150	°C	–	P_GEN_01_25
ESD robustness							
ESD robustness all pins (HBM)	V_{ESD_HBM}	-2	–	2	kV	3)	P_GEN_01_26
ESD robustness all pins (CDM)	V_{ESD_CDM1}	-500	–	500	V	4)	P_GEN_01_27
ESD robustness corner pins (CDM)	V_{ESD_CDM2}	-750	–	750	V	4)	P_GEN_01_28

1) Absolute maximum DC current through the bond wires, without considerations for maximum power or other limits.
2) Absolute maximum DC current through the bond wires, without considerations for maximum power or other limits.
3) Human body model (HBM) robustness according to AEC - Q100-002
4) Charged device model (CDM) robustness according to AEC - Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard

3.2 Functional range

Table 3 shows the device functional range.

***Note**: For $V_{UV\_OFF} \le V_S \le 5.5$ V, $20 \le V_S \le 40$ V and $V_{DD\_POFFR} \le V_{DD} \le 3$ V:*

- *The device is operating*
- *Parameter deviations are possible*
- *For $V_S \ge V_{OV\_OFF}$ the outputs are deactivated*

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VS voltage range for normal operation	$V_{S(nor)}$	5.5	–	20	V	–	P_GEN_02_01
Charge pump voltage range for normal operation	V_{CP}	V_S+7.5	–	V_S+17	V	–	P_GEN_02_02
Logic supply voltage range for normal operation	V_{DD}	3.0	–	5.5	V	–	P_GEN_02_03
Logic input voltages (SDI, SCLK, CSN, EN, PWM)	V_{SDI}, V_{SCLK}, V_{CSN}, V_{EN},V_{PWM}	-0.3	–	5.5	V	–	P_GEN_02_04
Junction temperature	T_j	-40	–	150	°C	–	P_GEN_02_05

3.3 Thermal resistance

Table 4 Thermal resistance

Parameter	Symbol	Typ. value	Unit	Note or condition	P-Number
Junction to ambient (2s2p)	R_{thjA}	23	K/W	1)	P_GEN_03_01
Junction to case	R_{thjC}	3	K/W	–	P_GEN_03_02

Specified R_{thJA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 2s2p board with 6 cm^2 cooling area; The product (chip and package) was simulated on a 76.2 x 114.3 x 1.5 mm board with two inner copper layers (70 / 35 / 35 / 70 µm Cu). T_a = 85°C.

4 Supply and operation modes

4.1 Supplies

The device has three supply inputs:

- The VS pin supplies the half-bridges and the high-side drivers
- The VDD pin supplies the device logic, including the SPI interface and the I/O buffers
- The CP pin is the charge pump input, used the control the integrated high-sides

***Note**: The microcontroller can measure a voltage proportional to V_S at the CM pin. Refer to Chapter 5.5.1.*

4.2 Overvoltage and undervoltage

The device monitors V_S, V_{DD} and V_{CP}:

- V_S is monitored for under- and over-voltage conditions (UV and OV)
- V_{DD} and V_{CP} are monitored for under-voltage conditions

4.2.1 VS undervoltage

A V_S undervoltage is detected if $V_S < V_{SUV\_OFF}$ for t = t_{FVSUV}.

The failure reaction is:

- All output stages are latched off
- The V_S undervoltage status bit is set and latched

A clear command to the register containing the V_S undervoltage status bit:

- Clears V_S undervoltage status bit
- Enables the outputs according to the control registers

4.2.2 VS overvoltage

If V_S rises above V_{OV_OFF} for t = t_{FVSOV}:

- All output stages are switched off
- The V_S overvoltage bit is set and latched

A clear command to the register containing the V_S overvoltage status bit:

- Clears the V_S overvoltage status bit
- Enables the outputs according to the control registers

4.2.3 VDD undervoltage

A V_{DD} undervoltage is detected if $V_{DD} < V_{DD\_POFFR}$.

If a V_{DD} undervoltage is detected:

- The SPI Interface does not operate
- The digital block is deactivated
- The output stages are off

4.2.4 Charge pump undervoltage

If V_{CP} drops below V_{CPUV} for t = t_{FCPUV}, then:

- All output stages are switched off
- The charge pump undervoltage (CPUV) bit is set and latched

A clear command to the register containing the charge pump undervoltage bit:

- Clears the charge pump undervoltage bit
- Enables the outputs according to the control registers

4.3 Operation modes

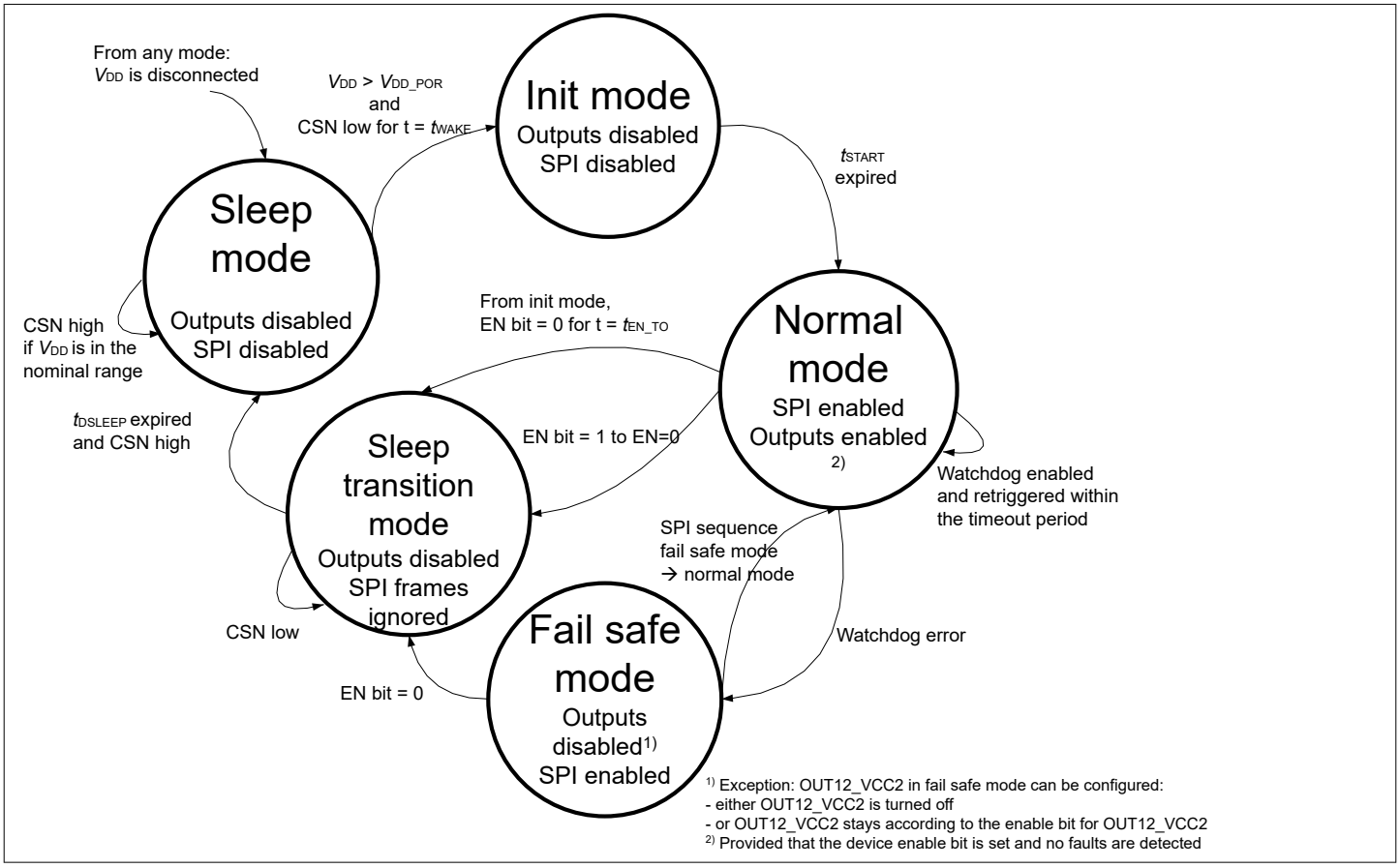


Figure 4 State diagram with mode transitions

4.3.1 Mode description

4.3.1.1 Sleep mode

The device has the lowest current consumption in sleep mode.

In sleep mode:

- The outputs are off
- The SPI communication is disabled
- The current consumption is reduced to $I_{SQ} + I_{DD\_Q}$

The device stays in sleep mode:

- if CSN is high while V_{DD} is in the nominal range
- if V_{DD} is disconnected, independently from V_{CSN}

4.3.1.2 Init mode

The init mode is a transition mode from sleep mode to normal mode. In this mode, the device is initialized.

In init mode:

- The outputs are off

- The content of the registers are reset to their default value
- The SPI communication is disabled

4.3.1.3 Normal mode

The normal mode is the standard operation mode of the device.

In normal mode, the SPI communication is enabled and the outputs follow the content of the control registers, provided that:

- The device enable bit is set
- And no failure is detected

Before the device enable bit is set, the SPI write[1)] and clear commands are ignored. No configuration change[1)] and no clear of a status register are possible.

[1)] with the exception of a SPI frame to set the device enable bit,

The following conditions must be fulfilled to stay in normal mode:

- After the transition from init mode to normal mode, the device enable bit must be set within t_{EN_TO}
- And if the watchdog is enabled, then the watchdog must be retriggered within the watchdog period (t_{WDPER})

***Attention**: OUT12_VCC2 can be configured as high-side, or 5 V / 3.3 V voltage regulator according to* Table 30 *only:*

- ***Within t_{EN_TO} after the transition from init to normal mode***
- ***With the first SPI write command. This SPI write command must set the device enable bit.***

The configuration of OUT12_VCC2 is frozen at the first SPI write command setting the device enable bit.

4.3.1.4 Fail safe mode

The purpose of the fail safe mode is to disable the outputs in case of watchdog failure.

In fail safe mode:

- All outputs are disabled with the exception of OUT12_VCC2
- The SPI communication is enabled
- The fail safe status bit is set until the device receives the SPI sequence to return to normal mode
- All control bits stay to their default value regardless of the SPI write commands with the exception of:
  - The device enable bit
  - The configuration bits for OUT12_VCC2 as high-side or 5 V/ 3.3 V regulator
  - The OUT12_VCC2 enable bit
  - The control bit for the setting of OUT12_VCC2 in fail safe mode
- An SPI write command to change the value of a control bit causes an SPI error[1)]

[1)] Exceptions: The value of the device enable bit can be changed without SPI error detection.

Clearing a status register in fail safe mode is allowed and does not set the SPI error bit.

Table 5 OUT12_VCC2 in fail safe mode

SPI configuration	OUT12_VCC2
Setting1	Off (default)
Setting2	According to the enable bit for OUT12_VCC2

***Note**: When:*

- *OUT12_VCC2 is configured as high-side switch*
- *and OUT12_VCC2 is configured to follow the enable bit for OUT12_VCC2*
- *and the enable bit for OUT12_VCC2 is set*

Then the CCM mode and the PWM mode for OUT12_VCC2 are disabled since these control bits are reset to their default value in fail safe mode.

Refer to the user manual for the description of the sequence to recover from fail safe mode to normal mode.

4.3.1.5 Sleep transition mode

The purpose of this mode is to prepare the device before entering the sleep mode.

The device stays in sleep transition mode for t_{DSLEEP}.

During the sleep transition mode:

- The outputs are turned off
- The device does not accept SPI read or write commands

4.3.2 Mode transitions

Transition from sleep mode to init mode

From sleep mode, the device enters init mode when CSN is low for t = t_{WAKE}.

Transition from init mode to normal mode

After staying in init mode for initialization during t = t_{START}, the device goes automatically to normal mode.

Transition from normal mode to fail safe mode

The device goes from normal mode to fail safe mode in case of watchdog error.

Transition from normal mode to sleep transition mode

The device goes to sleep transition mode in the following cases:

- The device enters normal mode from init mode with the device enable bit reset for t = t_{EN_TO}
- The device is in normal mode with the device enable bit set. Then the device enable bit is reset.

Transition from fail safe mode to sleep transition mode

The device goes to sleep transition mode when:

1. The device is in fail safe mode
2. Then the device enable bit reset

Transition from fail safe mode to normal mode

The device goes from fail safe mode to normal mode when the dedicated SPI sequence is received. Refer to the user manual.

Transition from sleep transition mode to sleep mode

The device goes to sleep mode after t = t_{DSLEEP} if CSN is high.

The device stays in sleep transition mode as long as CSN is low.

Transition from any mode to sleep mode by disconnecting V_{DD}

The device goes in sleep mode when V_{DD} is disconnected.

The device stays in sleep mode independently from V_{CSN} level if V_{DD} is disconnected.

4.4 Timeout watchdog

The timeout watchdog monitors the communication with the microcontroller and the integrity of the SPI bus.

The watchdog is configurable by SPI:

- The watchdog is enabled by default after power-on reset and starts at the transition from init mode to normal mode
- The watchdog can be disabled by a dedicated SPI sequence
- The watchdog can be re-enabled by bit configuration
- The watchdog period is selectable by bit configuration (Table 6)

Table 6 Selectable watchdog period

Parameter	Symbol	Nominal value	Unit	Default	Tolerance
Watchdog period	t_{WDPER}	50 250	ms	50	t_{OSC1_TOL}

The watchdog must be retriggered within the configured period (t_{WDPER}) to stay in normal mode.

A new watchdog period starts when the watchdog is retriggered.

Refer to the user manual for the description of the watchdog retrigger and for the SPI sequence to disable the watchdog.

Monitoring the watchdog timer

The watchdog monitoring bits (refer to the user manual) report the relative position of the watchdog timer in relation to the watchdog period.

This allows the detection of a potential latent failure associated to a frozen watchdog timer.

The microcontroller can monitor the incrementation of the watchdog counter to verify that the watchdog timer is not frozen.

Table 7 Monitoring of the watchdog timer

Watchdog monitoring bits	Position of the watchdog timer
00_B	Between [0%, 25%[of t_{WDPER}
01_B	Between [25%, 50%[of t_{WDPER}
10_B	Between [50%, 75%[of t_{WDPER}
11_B	Between [75%, 100%[of t_{WDPER}

If the watchdog is not retriggered within t_{WDPER} then:

- The device goes in fail safe mode (Refer to Chapter 4.3.1.4)
- The fail safe bit is set

4.5 Temperature monitoring

Several temperature sensors are integrated in the power stages to detect and report thermal warning and thermal shutdown conditions.

The thermal sensors are arranged in clusters according to Table 8.

Table 8 Thermal clusters

Cluster 1	Cluster 2	Cluster 3	Cluster 4	Cluster 5	Cluster 6
OUT1 + OUT6	OUT2 + OUT3	OUT4 + OUT5	OUT7	OUT8+OUT9+OUT 11	OUT10, ECV LS, OUT12_VCC2

4.5.1 Thermal warning

A temperature warning is detected for a given thermal cluster if the temperature of the corresponding thermal sensor exceeds T_{jW} for t = t_{FTW}.

The device reaction is:

- The temperature warning status bit is set and latched
- The thermal warning event is reported in the global status byte
- The state of the outputs belonging to the impacted thermal cluster remains unchanged

The thermal warning bit is cleared when a clear command to the register containing the thermal warning bit is received.

4.5.2 Thermal shutdown

A thermal shutdown (TSD) is detected for a given thermal cluster if the temperature of the corresponding sensor exceeds T_{jSD} for t = t_{FTSD}.

In this case the device reaction is:

- The thermal shutdown bit of the thermal cluster is set and latched
- The thermal shutdown event is reported in the global status byte
- The outputs of the thermal cluster are latched off

After a thermal shutdown event, the deactivated outputs are re-enabled (according to the control registers) if the thermal shutdown status bit is cleared.

4.6 Electrical characteristics

Electrical characteristics, V_S =5.5 V to 20 V, V_{DD} = 3.0 V to 5.5 V, V_{CP} = V_S+ 7.5 V to V_S+ 17 V, T_j = -40°C to +150°C, I_{OUTx} = 0 A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Table 9 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply quiescent current	I_{SQ}	–	2.4	5	µA	-40°C ≤ T_j ≤ 85°C; V_S = V_{CP}	P_SUP_01_01
Logic supply quiescent current	I_{DD_Q}	–	1.8	5	µA	-40°C ≤ T_j ≤ 85°C	P_SUP_01_03
Supply current	I_S	–	3.5	5	mA	Outputs off	P_SUP_01_05
Logic supply current	I_{DD}	–	3.5	6	mA	–	P_SUP_01_06

(table continues...)

Table 9 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CP current	I_{CP}	–	–	3	mA	OUT12 HS; OUT1-12 on; OUT2,4,6 20kHz PWM with active freewheeling; Mirror heater on	P_SUP_01_07
VCC2 supply current	I_{VCC2}	–	2.5	3	mA	OUT12_VCC2 configured as 3.3 V / 5 V regulator VCC2 on, no load	P_SUP_01_33
VSUV filter time	t_{FVSUV}	4	7	12	µs	–	P_SUP_01_09
VSOV filter time	t_{FVSOV}	4	7	12	µs	–	P_SUP_01_10
TW filter time	t_{FTW}	4	7	12	µs	–	P_SUP_01_11
TSD filter time	t_{FTSD}	4	7	12	µs	–	P_SUP_01_12
CPUV filter time	t_{FCPUV}	51	64	77	µs	–	P_SUP_01_13
Undervoltage switch-on voltage threshold	V_{UV_ON}	4.25	–	5.25	V	V_S increasing	P_SUP_01_14
Undervoltage switch-off voltage threshold	V_{UV_OFF}	4	–	5	V	V_S decreasing	P_SUP_01_15
Undervoltage switch-on/off hysteresis	V_{UV_HY}	0.10	0.25	0.40	V	V_{UV_ON} - V_{UV_OFF}	P_SUP_01_16
Overvoltage switch-off voltage threshold	V_{OV_OFF}	20	–	22.5	V	V_S increasing	P_SUP_01_17
Overvoltage switch-on voltage threshold	V_{OV_ON}	19	–	21.5	V	V_S decreasing	P_SUP_01_18
Overvoltage switch-on/off hysteresis	V_{OV_HY}	0.7	1	1.3	V	V_{OV_OFF} - V_{OV_ON}	P_SUP_01_19
VDD power on reset	V_{DD_POR}	2.5	2.7	2.9	V	V_{DD} increasing	P_SUP_01_20
VDD power off reset	V_{DD_POFFR}	2.4	2.6	2.8	V	V_{DD} decreasing	P_SUP_01_21
VDD power on/off hysteresis	$V_{DD\_POR\_HY}$	30	–	–	mV	V_{DD_POR} - V_{DD_POFFR}	P_SUP_01_22
Wake-up time	t_{WAKE}	–	–	150	µs	–	P_SUP_01_23

(table continues...)

Table 9 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Start time	t_{START}	400	500	600	µs	–	P_SUP_01_24
Enable timeout	t_{EN_TO}	32	40	48	ms	–	P_SUP_01_25
Sleep time delay	t_{DSLEEP}	80	100	120	µs	–	P_SUP_01_26
Thermal warning junction temperature	T_{jW}	145	160	175	°C	–	P_SUP_01_27
Thermal shutdown junction temperature	T_{jSD}	185	200	215	°C	–	P_SUP_01_28
Thermal comparator hysteresis	T_{jHYS}	5	10	15	°C	–	P_SUP_01_29
CPUV threshold	V_{CPUV}	V_S + 5.5	V_S + 6	V_S + 7	V	–	P_SUP_01_30
Oscillator 1 tolerance	t_{OSC1_TOL}	-20%	–	+20%	–	–	P_SUP_01_31

5 Integrated power outputs

This chapter describes the features related to the integrated power outputs:

- OUT1 to OUT6: Integrated half-bridges
- OUT7 to OUT11: Integrated high-side switches
- OUT12_VCC2: Configurable output as high-side switch or as 5 V / 3.3 V voltage regulator
- ECV: Integrated low-side

In this chapter the active MOSFET designates the MOSFET defined according to Table 10:

- Setting2: The low-side MOSFET is the active MOSFET
- Setting3: The high-side MOSFET is the active MOSFET

***Note**: This chapter is applicable when OUT12_VCC2 is configured as high-side. Refer to Table 30 and to Chapter 4.3.1.3 for the configuration.*

***Note**: The device monitors I_{OUTx} for diagnostic and protection purposes.*
For activated high-side switches: I_{OUTx} can be monitored only if the current flows out of OUTx. Otherwise I_{OUTx} is considered equal to 0.
For activated low-side switches: I_{OUTx} can be monitored only if the current flows into OUTx. Otherwise I_{OUTx} is considered equal to 0.

5.1 Integrated half-bridges

OUT1 to OUT6 consist of integrated high-side and low-side switches, optimized for inductive loads.

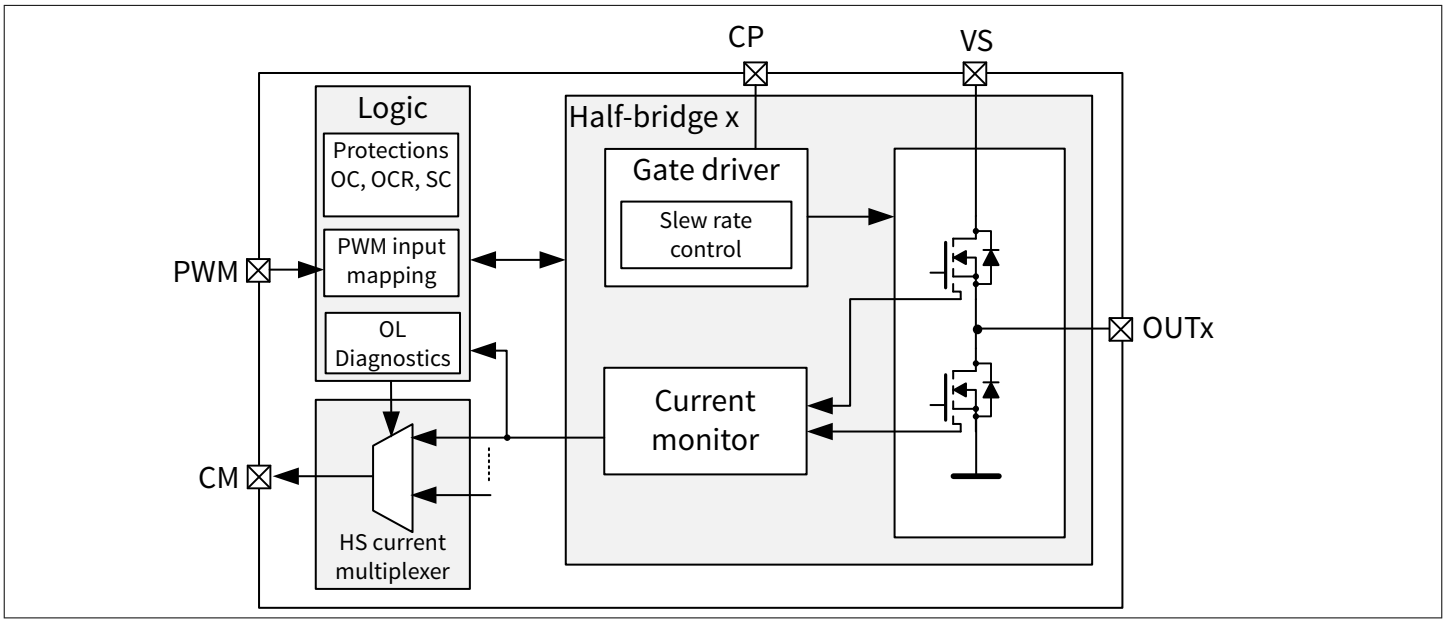


Figure 5

The MOSFETs of the half-bridge are controlled by SPI according to Table 10.

Table 10 Half-bridge control by SPI

SPI Configuration	HSx	LSx	Comment
Setting1	OFF	OFF	Default configuration
Setting2	OFF	ON	–
Setting3	ON	OFF	–

5.1.1 Cross-current protection

The integrated half-bridges have a cross-current protection to avoid cross-conduction.

A cross-current protection time (t_{CCPx}) is applied when a high-side or a low-side must be activated, while the opposite MOSFET of the same half-bridge is already on.

1. During t_{CCPx}, the MOSFET which was previously on, is turned off
2. After t_{CCPx}, the MOSFET to be activated is then turned on

The cross-current protection time is available with or without PWM operation.

t_{CCP1} or t_{CCP2} are selected according to Table 11.

5.1.2 Half-bridges in PWM operation

The half-bridges can operate with a PWM frequency up to 25 kHz.

The PWM control of OUT1 to OUT6 by the PWM input is enabled by SPI according to Table 11.

The active MOSFET designates the MOSFET selected according to Table 10. The freewheeling MOSFET is the opposite MOSFET of the same half-bridge.

Table 11 PWM enable for half-bridges

SPI configuration	Half-bridge configuration	Overcurrent and open load blank time	Slew rate	Cross-current protection time
Setting1	No PWM operation (default)	No OC detection: t_{BLK_OCOL1} Once OC is detected: t_{BLK_OCOL3}	No OC detection: S_{R1} Once OC is detected:S_{R2}	No OC detection: t_{CCP1} Once OC is detected: t_{CCP2}
Setting2	The signal at the PWM input pin is applied to the active MOSFET	t_{BLK_OCOL2}	S_{R2}	t_{CCP2}

The half-bridges can be individually configured with passive or active freewheeling according to Table 12.

Table 12 Freewheeling configuration in PWM operation

SPI configuration	Freewheeling
Setting 1	Passive freewheeling (default)
Setting 2	Active freewheeling

In passive freewheeling mode:

- The active MOSFET follows the PWM pin
- The freewheeling MOSFET stays off
- No cross-current protection is applied

In active freewheeling mode:

- At the rising edge at the PWM pin
  1. The freewheeling MOSFET is turned off during t_{CCP2}
  2. After t_{CCP2}, the PWM MOSFET is turned on
- At the falling edge at the PWM pin:
  - The active MOSFET is turned off during t_{CCP2}
  - After t_{CCP2}, the freewheeling MOSFET is turned on

5.2 Integrated high-side switches OUT7-OUT12

The high-sides OUT7 to OUT12 are intended to control:

- Resistive loads such as LEDs
- Capacitive loads with the constant current mode (CCM)

controlling inductive loads with these outputs requires an external freewheeling diode between GND and the corresponding outputs.

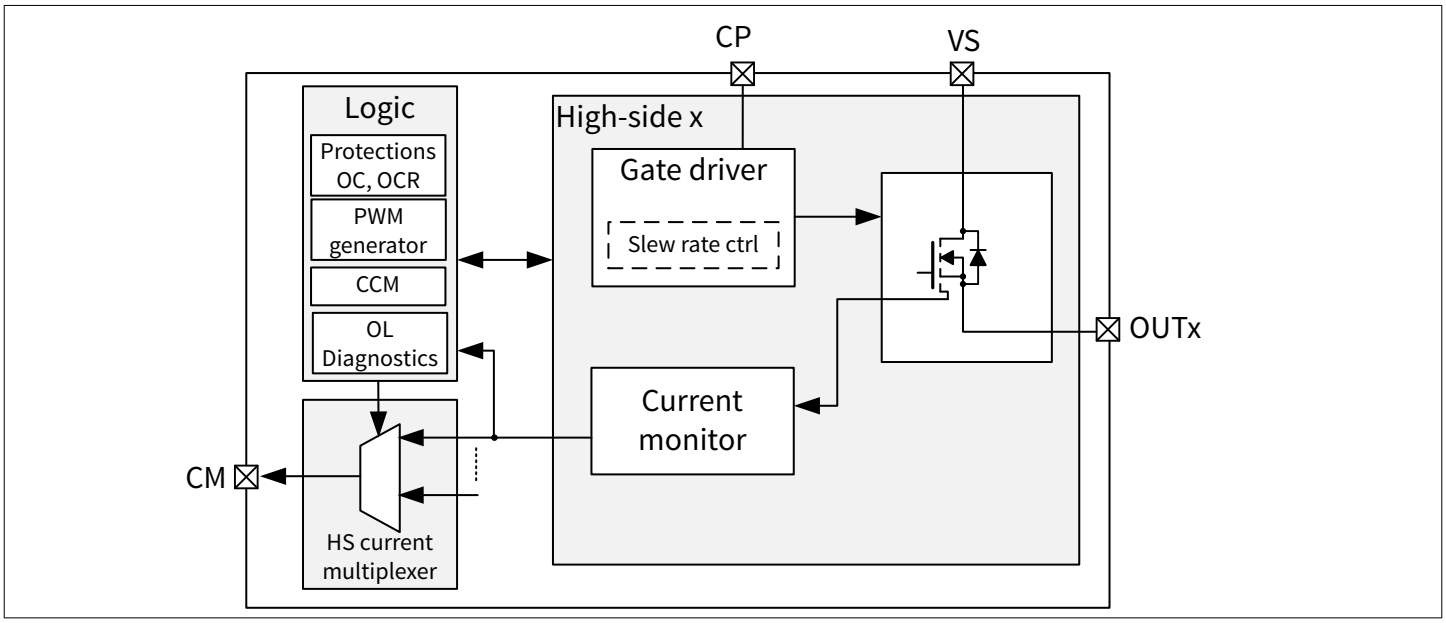


Figure 6 Block diagram of a high-side switch – OUT7 to OUT11

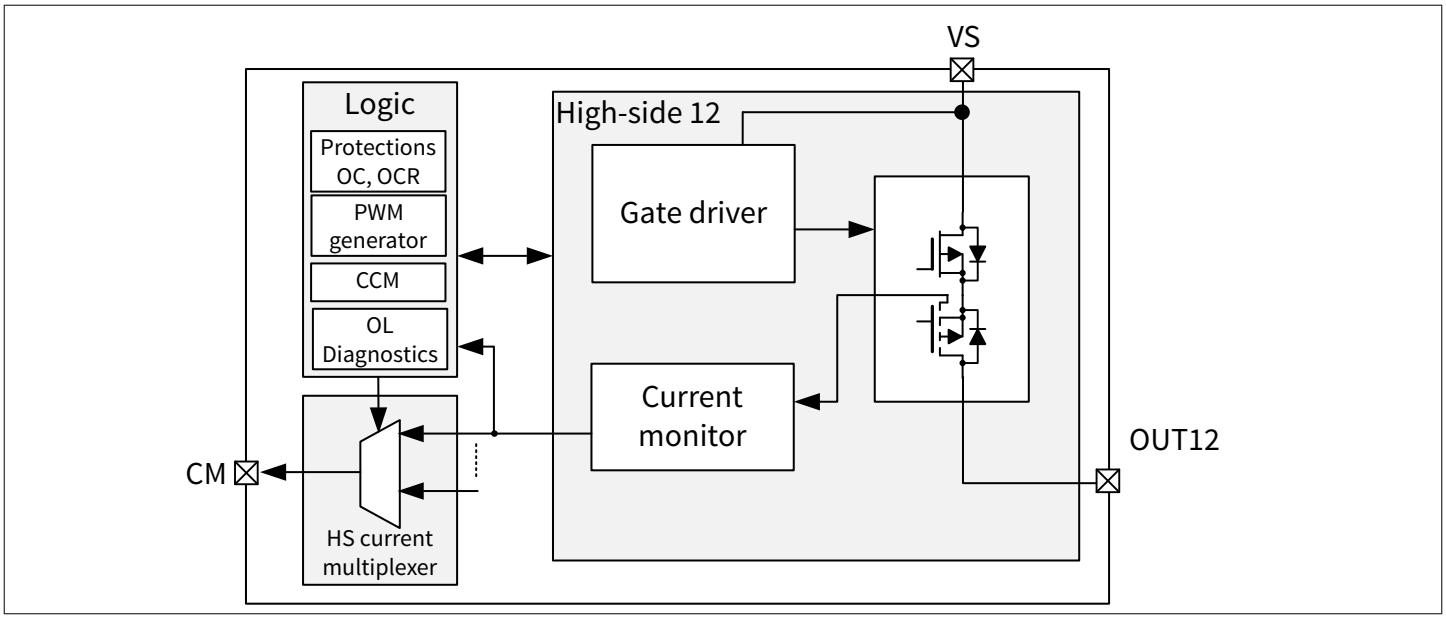


Figure 7 Block diagram of OUT12_VCC2 configured as high-side switch

OUT7 to OUT12 have an individual enable bit to control the high-side switch. Refer to Table 13:

Table 13 Turn-on of OUT7-OUT12

SPI configuration	Output state
Setting1	OUTx is off (default)
Setting2	OUTx is on

5.2.1 PWM operation

OUT7 to OUT12 can be mapped to one of the internal PWM generators PWM1 to PWM6.
The duty cycle of each PWM generator is configurable by SPI with a 10-bit resolution.

Table 14 PWM mapping for OUT7 to OUT12

SPI configuration	PWM mapping
Setting1	No PWM (default)
Setting2	High-side mapped to PWM1
Setting3	High-side mapped to PWM2
Setting4	High-side mapped to PWM3
Setting5	High-side mapped to PWM4
Setting6	High-side mapped to PWM5
Setting7	High-side mapped to PWM6

Table 15 Internal PWM frequency selection

Parameter	Symbol	Nominal value	Unit	Default	Tolerance
PWMx frequency	F_{PWM}	100 200 320 400	Hz	100	t_{OSC1_TOL}

An individual phase shift can be applied to each PWM generator according to Table 16:

Table 16 PWM generator phase shift

Parameter	Nominal range	Unit	Step width	Default
Phase shift	0 to 315	°	45	0

5.2.2 Constant current mode

OUT7 to OUT12 can be individually configured by SPI in constant current mode (CCM) to drive capacitive loads according to Table 17:

Table 17 Activation of the constant current mode

SPI configuration	Constant current mode selection
Setting1	Constant current mode disabled (default) Output in $R_{DS(ON)}$ mode
Setting2	Constant current mode 1 (CCM1) enabled

(table continues...)

Table 17 (continued) Activation of the constant current mode

SPI configuration	Constant current mode selection
Setting3	Constant current mode 2 (CCM2) enabled
Setting4	Constant current mode 3 (CCM3) enabled

CCM1 is selected for OUTx:

1. A control signal to activate OUTx is received
2. $|I_{OUTx}|$ is limited to I_{CCM1} for t = t_{BLK_OCOL} + t_{CCM1}
3. After t_{CCM1}, OUTx switches to $R_{DS(ON)}$ mode

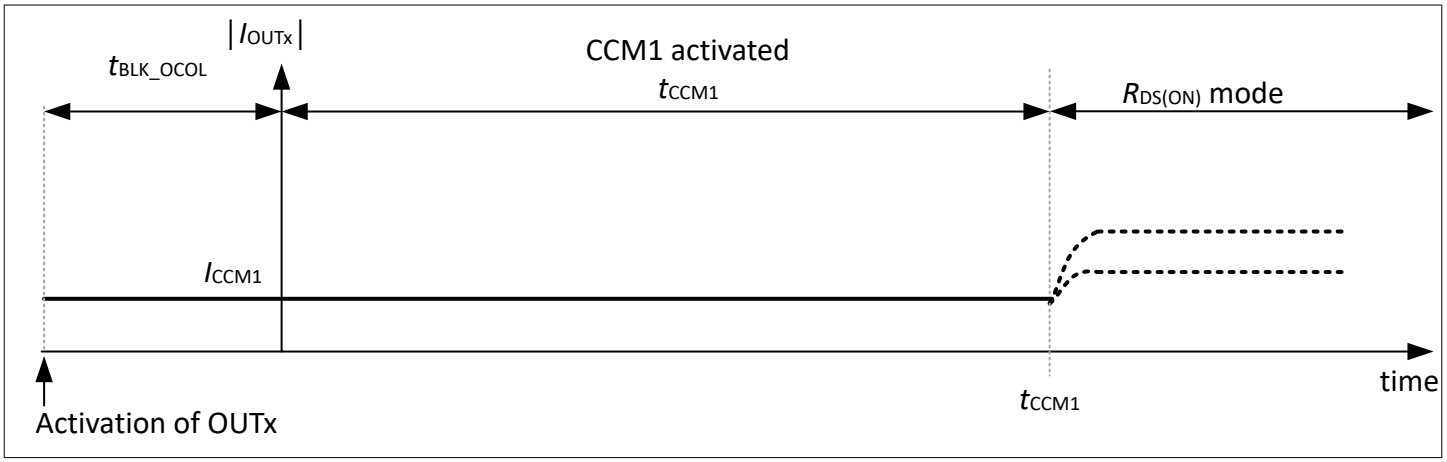


Figure 8 CCM1

CCM2 is selected for OUTx:

1. A control signal to activate OUTx is received
2. For t = t_{BLK_OCOL} $|I_{OUTx}|$ is limited to I_{CCM1}
3. Then CCM2 is activated for t = t_{CCM2}:
   - **a.** If $V_{OUTx} \le V_{OUT\_LOW}$ for t = t_{FVOUT_LOW}, then $|I_{OUTx}|$ is limited to I_{CCM1}
   - **b.** If $V_{OUTx} \ge V_{OUT\_LOW}$ for t = t_{FVOUT_LOW}, then $|I_{OUTx}|$ is limited to I_{CCM2}
4. After t_{CCM2}, OUTx switches to $R_{DS(ON)}$ mode

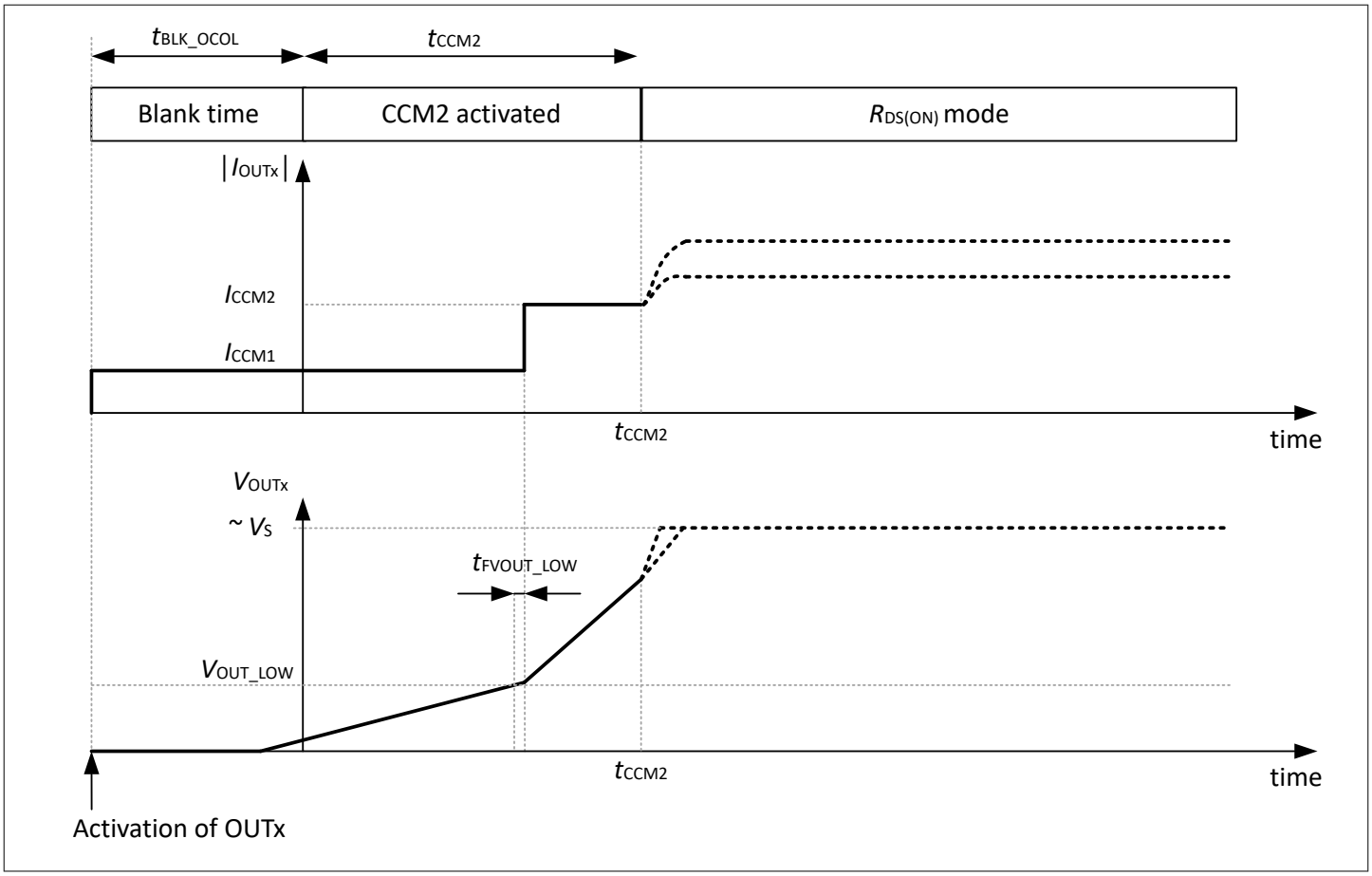


Figure 9 CCM2

CCM3 is selected for OUTx:

1. A control signal to activate OUTx is received
2. For t = t_{BLK_OCOL}, $|I_{OUTx}|$ is limited to I_{CCM2}
3. Then CCM3 is activated for t_{CCM3}:
   - **a.** If $V_{OUTx} \leq V_{OUT\_LOW}$ for t = t_{FVOUT_LOW}, then $|I_{OUTx}|$ is limited to I_{CCM2}
   - **b.** If $V_{OUTx} \geq V_{OUT\_LOW}$ for t = t_{FVOUT_LOW}, then $|I_{OUTx}|$ is limited to I_{CCM3}
4. At t = t_{CCM3}, OUTx switches to $R_{DS(ON)}$ mode

During t_{CCM3}, the overcurrent detection is deactivated.

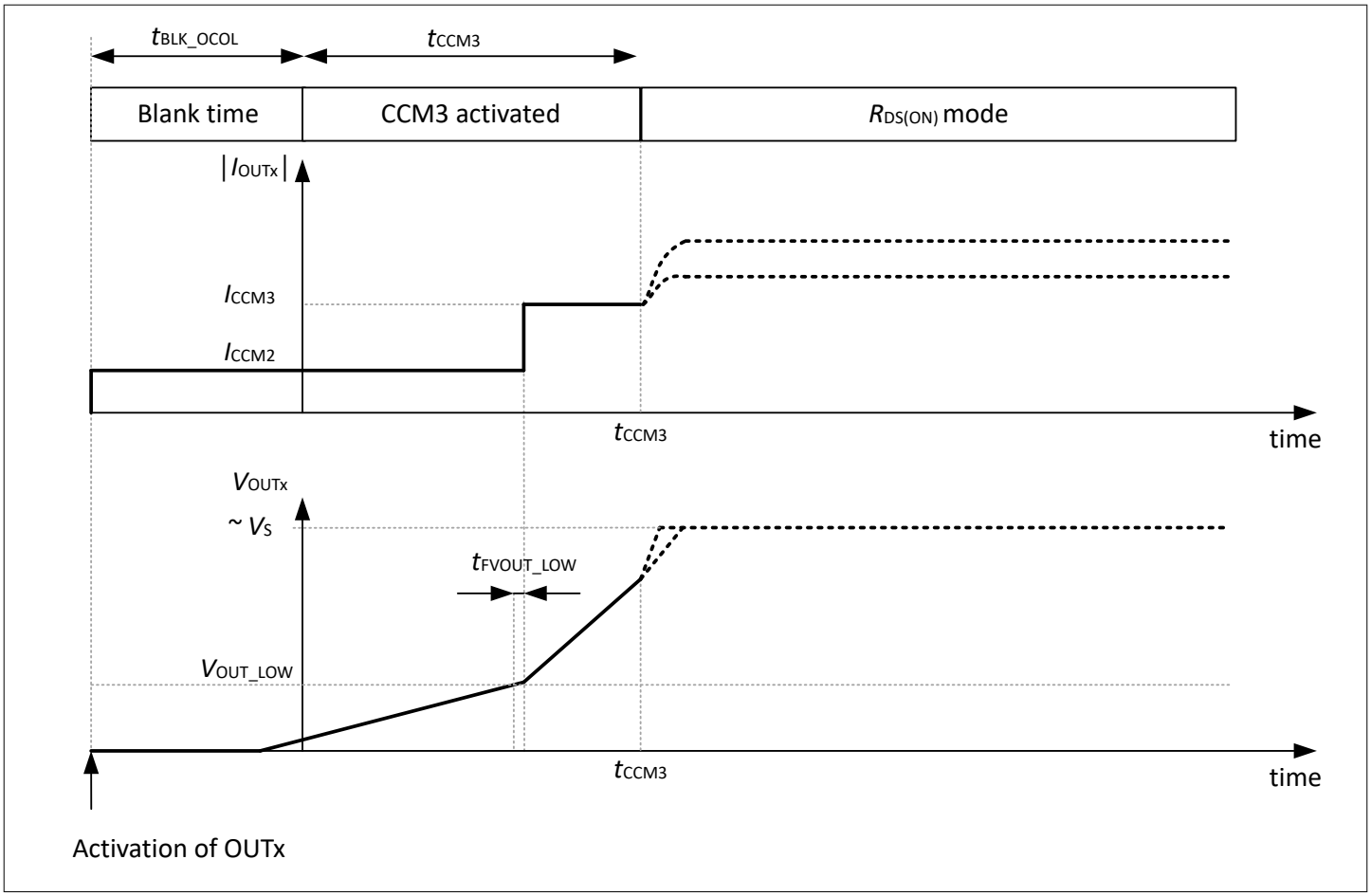


Figure 10 CCM3

If the CCM is disabled by SPI before the end of the respective t_{CCMx}, then the CCM mode is deactivated and the output switches to $R_{DS(ON)}$ mode.

If CCM is enabled or changed by SPI while the output is already in $R_{DS(ON)}$ mode, then the new CCM is applied at the next activation of the output.

For the respective CCM mode, if $V_{OUT} < V_{OUT\_LOW}$ at t = t_{CCMx} , x = 1 to 3, then:

- The output is turned off
- The overcurrent bit is set

5.2.3 Configurability of OUT7

OUT7 can be configured to control:

- Incandescent bulbs up to 10W in low $R_{DS(ON)}$ mode in combination with the overcurrent recovery feature (Chapter 5.4.3)
- LEDs in high $R_{DS(ON)}$ mode thanks to the low open load detection threshold

The electrical characteristics of OUT7 are configurable according to Table 18, Table 20 and Table 19.

Table 18 OUT7 RDS(ON), open load, and overcurrent thresholds

SPI configuration	R_{ON}	Open load	Overcurrent	Current limitation	Note
Setting1: Low $R_{DS(ON)}$	$R_{DS(ON)\_OUT7\_1}$	$I_{OL\_OUT7\_1}$	$I_{OC\_OUT7\_1}$	Configurable Table 20	Default
Setting2: High $R_{DS(ON)}$	$R_{DS(ON)\_OUT7\_2}$	$I_{OL\_OUT7\_2}$	$I_{OC\_OUT7\_2}$	$I_{LIM\_OUT7\_2}$	–

Table 19 OUT7 slew rate and overcurrent/open load blank time

Configured $R_{DS(ON)}$	Configured slew rate	Overcurrent recovery	Overcurrent OUT7 status bit	Applied slew rate	OC/OL blank time
Low	Don't care	Don't care	0	S_{R1}	t_{BLK_OCOL1}
Low	Low	Enabled	1	S_{R1}	t_{BLK_OCOL1}
Low	High	Enabled	1	S_{R2}	t_{BLK_OCOL2}
High	Not applicable	Not applicable	0	S_{R1}	t_{BLK_OCOL1}

Table 20 OUT7 current limitation in low RDS(ON) mode

SPI configuration	I_{LIM}	Note
Setting1	$I_{LIM\_OUT7\_11}$	–
Setting2	$I_{LIM\_OUT7\_12}$	Default

***Note**: Even if the overcurrent recovery feature is enabled by SPI, S_{R1} and t_{BLK_OCOL1} are applied in any configuration as long as no overcurrent is detected.*

5.3 Integrated ECV low-side

The ECV low-side (ECV LS) is configurable according to Table 21:

- To control non-inductive loads in low-side configuration
- To control inductive loads in half-bridge configuration, when associated to OUT10
- To allow a fast discharge of the ECV pin to GND for an electrochromic mirror

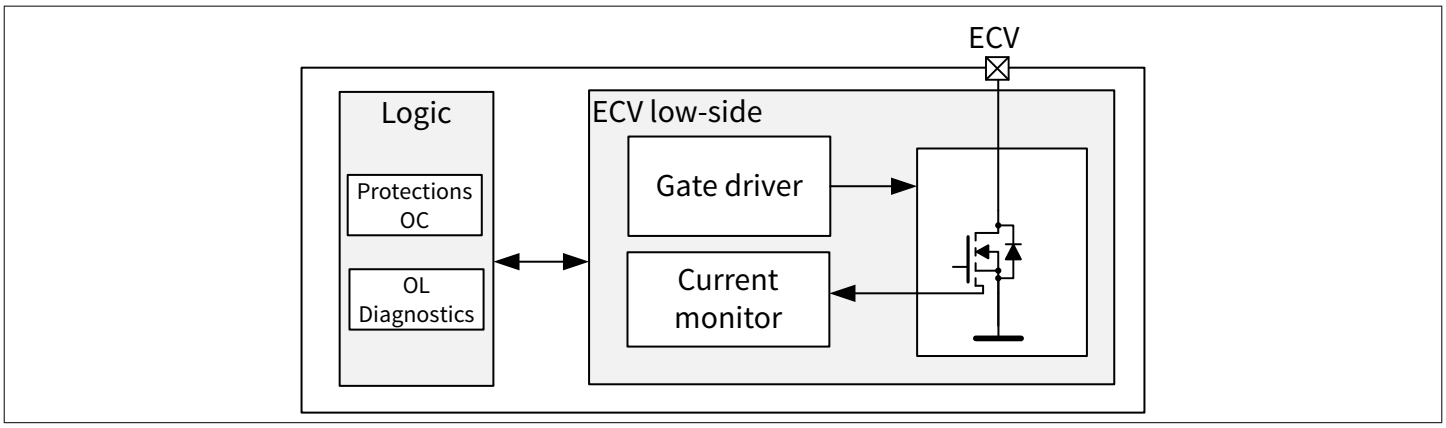


Figure 11 Block diagram of the ECV low-side

Table 21 Configuration of ECV low-side and EC regulation

SPI Configuration	EC regulation	ECV low-side	Remarks
Setting1	Disabled	Standalone low-side switch (default)	The ECV low-side follows its enable bit
Setting2	Disabled	ECV low-side and OUT10 are configured in half-bridge mode	ECV low-side and OUT10 follow their respective enable bit A cross-current protection is implemented

(table continues...)

Table 21 (continued) Configuration of ECV low-side and EC regulation

SPI Configuration	EC regulation	ECV low-side	Remarks
Setting3	Enabled	If the ECV LS control bit is set, the ECV low-side is activated depending on V_{ECV}	Refer to Chapter 7
Setting4	Enabled	If the ECV LS control bit is set, ECV low-side is activated independently from V_{ECV}	Refer to Chapter 7

5.3.1 OUT10 and ECV low-side in half-bridge configuration

In half-bridge configuration, a cross-current protection time is applied when OUT10 or ECV low-side must be activated, while the opposite MOSFET of the half-bridge is already on.

1. During t_{CCP1}, the MOSFET which was previously on, is turned off
2. After t_{CCP1}, the MOSFET to be activated is then turned on

In half-bridge configuration, if the enable bits of ECV low-side and of OUT10 are both set, then:

- both outputs are turned off
- the input error bit is set and latched

ECV low-side and OUT10 stay off until the input error bit is cleared.

The bit setting for OUT10 CCM and PWM are ignored:

- CCM mode is disabled
- OUT10 is not controlled by any PWM generator

5.4 Protections

The overcurrent detection is available for each activated output. The device reaction upon an overcurrent detection depends on the output and on the register configuration.

OUT1 to OUT6 have the following protections:

- Overcurrent latch-off. Refer to Chapter 5.4.2.
- Overcurrent recovery with short circuit detection. Refer to Chapter 5.4.3.1.
- Overcurrent recovery with short circuit detection and half-bridge pairing when PWM is disabled. Refer to Chapter 5.4.3.1.

OU7 in low $R_{DS(ON)}$ mode has the following protections:

- Overcurrent latch-off. Refer to Chapter 5.4.2.
- Overcurrent recovery with short circuit detection. Refer to Chapter 5.4.3.2.

OUT7 in high $R_{DS(ON)}$ and OUT8 to OUT12 have the overcurrent latch-off protection. Refer to Chapter 5.4.2.

The overcurrent thresholds of OUT1,5,6 are configurable according to Table 22.

Table 22 Configurable overcurrent thresholds

Parameter	Symbol	Nominal value high side / low side	Unit	Default
Overcurrent threshold OUT1,6	$I_{OC\_OUT1,6\_HS}$ / $I_{OC\_OUT1,6\_LS}$	-2 / 2 -3 / 3 -4 / 4	A	-2 / 2
Overcurrent threshold OUT5	$I_{OC\_OUT5\_HS}$ / $I_{OC\_OUT5\_LS}$	-4 / 4 -6 / 6 -7.5 / 7.5	A	-4 / 4

5.4.1 Overcurrent detection

The overcurrent detection is ignored:

- For any output: At the activation of the output during any t_{BLK_OCOLx}
- For half-bridges when OCR and pairing are enabled: During t_{BLK_OCOL3} (refer to Chapter 5.4.3.1.3)

After t_{BLK_OCOLx}, an overcurrent is detected:

- For an activated high-side: If $|I_{OUT}| \geq |I_{OC}|$ for t = t_{FOC}
- For an activated low-side: If $I_{OUT} \geq I_{OC}$ for t = t_{FOC}
- For the ECV low-side: If $I_{ECV} \geq I_{OC\_ECV\_LS}$ for t = t_{FOC}

5.4.2 Overcurrent latch-off

The overcurrent latch-off function is available for every integrated high-side and low-side. When an overcurrent condition is detected:

- The overcurrent status bit of the impacted MOSFET is set and latched
- The impacted half-bridge is latched off for OUT1 to OUT6
- The impacted MOSFET is latched off for OUT7 to OUT12

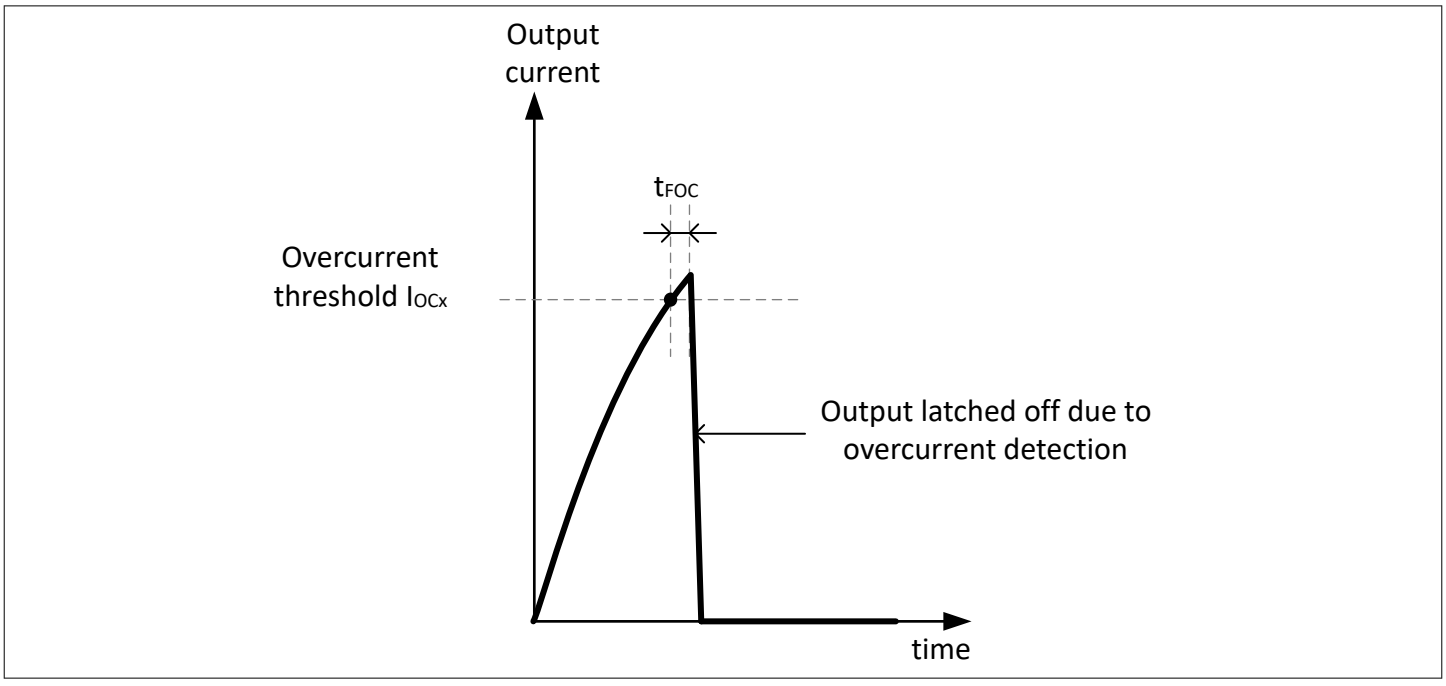


Figure 12 Overcurrent latch-off

After an overcurrent latch-off, the output is re-enabled (according to the control registers) when the overcurrent status bit is cleared.

5.4.3 Overcurrent recovery

The overcurrent recovery (OCR) mode enables the control of loads with an inrush current higher than the overcurrent detection threshold. It is recommended to minimize the operation in OCR conditions for reliability reasons, especially in short circuit conditions.

The OCR is available and individually configurable for OUT1 to OUT6 and OUT7 in low $R_{DS(ON)}$ mode.

t_{OCR} is configurable according to Table 23.

Table 23 Settings of overcurrent recovery time

Overcurrent recovery time	Symbol	Nominal value	Unit	Default	Tolerance
Integrated half-bridges	t_{OCR}	0 24 32 48	µs	0	t_{OSC1_TOL}
OUT7 in low $R_{DS(ON)}$ mode	t_{OCR}	0 3 6 9	µs	0	t_{OSC1_TOL}

t_{OCR_OFF} is configurable according to Table 24.

Table 24 Settings of OCR off-time

Parameter	Symbol	Nominal value	Unit	Default	Tolerance
Half-bridges OCR off-time	t_{OCR_OFF}	200 300 400 600	µs	200	t_{OSC1_TOL}
OUT7 in low $R_{DS(ON)}$ OCR off-time	t_{OCR_OFF}	100 200 400 600	µs	200	t_{OSC1_TOL}

5.4.3.1 Overcurrent recovery for half-bridges

Refer to Table 11 for the applicable slew rate and OC/OL blank time t_{BLK_OCOLx} for half-bridges during OCR operation.

When OCR is enabled, the short circuit detection is also enabled.

For clarify reasons:

- Chapter 5.4.3.1.1 shows first the device behavior when the short circuit detection is not triggered.
- Chapter 5.4.3.1.2 shows the device behavior when the short circuit detection is triggered.

***Note**: When OCR is enabled, it is recommended to set t_{OCR} of the half-bridges to 0.*
Extending the on-time by t_{OCR} for an inductive load (e.g. mirror adjustment, mirror fold or door lock) for up to 48 µs does not increase significantly the average current of the load.
However, extending the on-time during an overload increases the stress applied to the output.

5.4.3.1.1 OCR for half-bridges with disabled PWM

When an overcurrent is detected:

1. The output stays on for t = t_{OCR}
2. Then the output is turned off for t = t_{OCR_OFF}
3. After t = t_{OCR_OFF}:
   - The output is turned on
   - t_{BLK_OCOL3} is applied

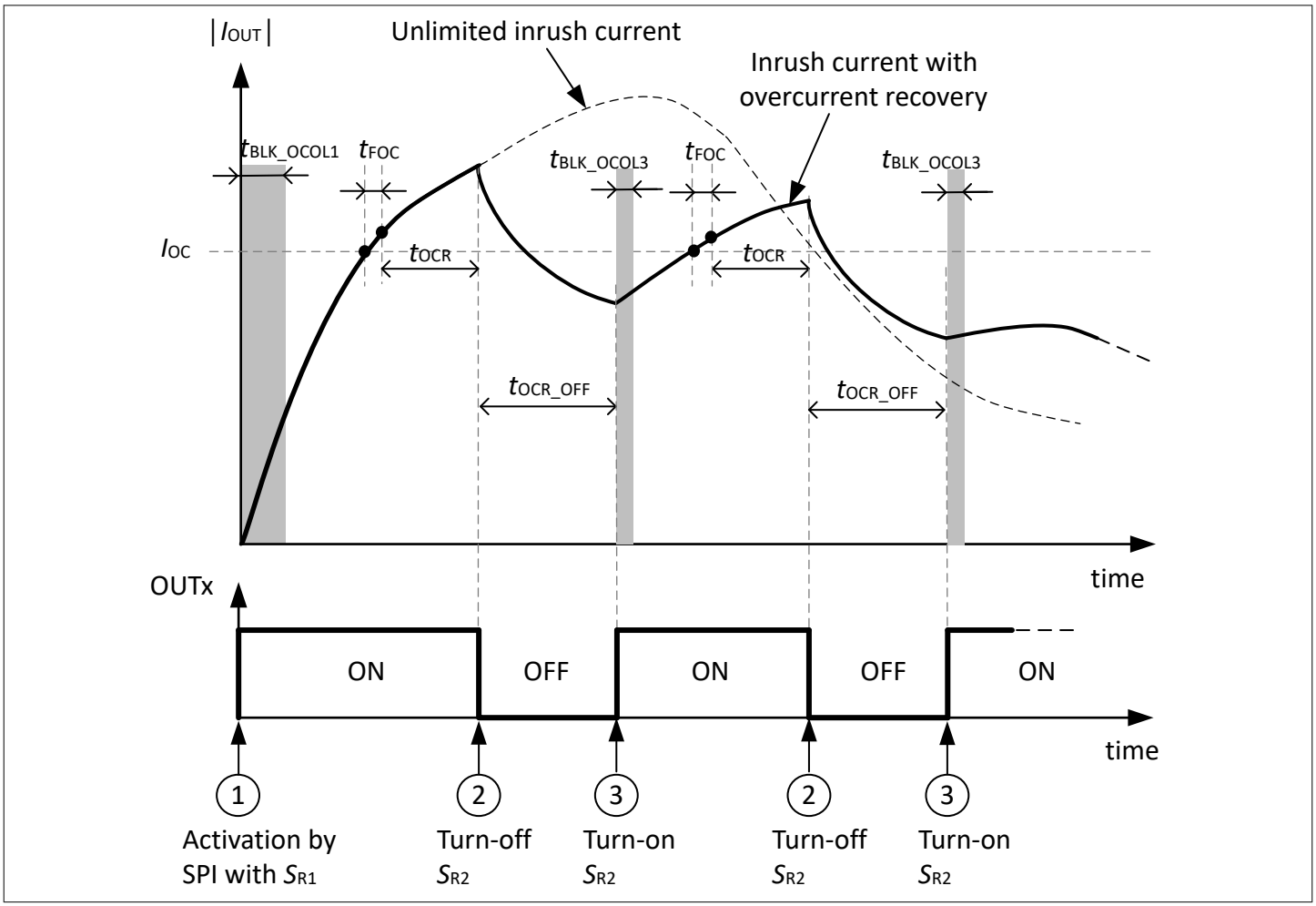


Figure 13 OCR for a half-bridge with disabled PWM

5.4.3.1.2 OCR for half-bridges with disabled PWM and with short circuit detection

When the OCR is enabled, an additional short circuit (SC) threshold and a SC detection are implemented for OUT1 to OUT6.

The short circuit detection is ignored:

- At the activation of the output during any t_{BLK_OCOLx}
- And during t_{BLK_OCOL3} when OCR and pairing are enabled (refer to Chapter 5.4.3.1.3)

After t_{BLK_OCOLx}:

- For an activated high-side: If $|I_{OUT}| \geq |I_{SC}|$ for t = t_{FSC}, then a SC pulse is detected at the high-side
- For an activated low-side: If $I_{OUT} \geq I_{SC}$ for t = t_{FSC}, then a SC pulse is detected at the low-side

For the active MOSFET, it is possible to disable or enable by SPI the SC counter (OUTx_SC_CFG). The configuration bit is applied to all half-bridges.

SC counter disabled

If the SC counter is disabled, then at the first SC pulse (Figure 14):

- The SC status bit is set
- The half-bridge is latched off until the SC status bit is cleared

SC counter enabled

If the SC counter is enabled (Figure 15), then:

- At the first SC pulse, the active MOSFET is turned off for t = t_{OCR_OFF}
- At the end of t_{OCR_OFF}:
  - The active MOSFET is turned on
  - t_{BLK_OCOL3} is applied
- At the second **consecutive** SC pulse:
  - The SC status bit is set
  - The half-bridge is latched off until the SC status bit is cleared

The SC counter is reset after the first SC pulse:

- If $|I_{OUT}| \leq |I_{SC}|$ while:
  - The active MOSFET is on
  - And the active MOSFET is outside of its OC/OL blank time
- If the output is deactivated by SPI

Note: The short circuit detection of the active MOSFET is enabled even during t_{OCR}.

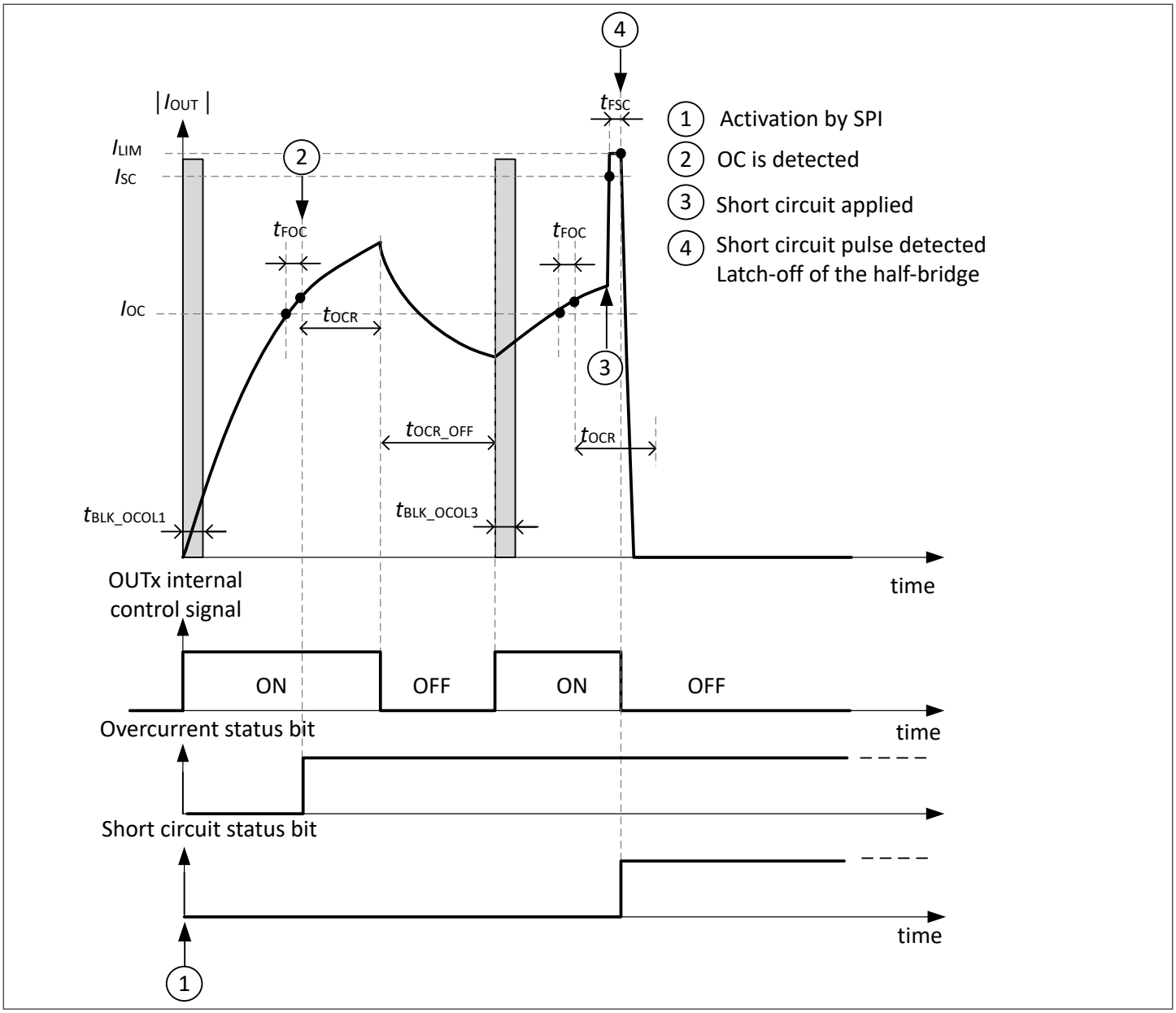


Figure 14 Short circuit detection on the active MOSFET, OCR enabled, SC counter disabled

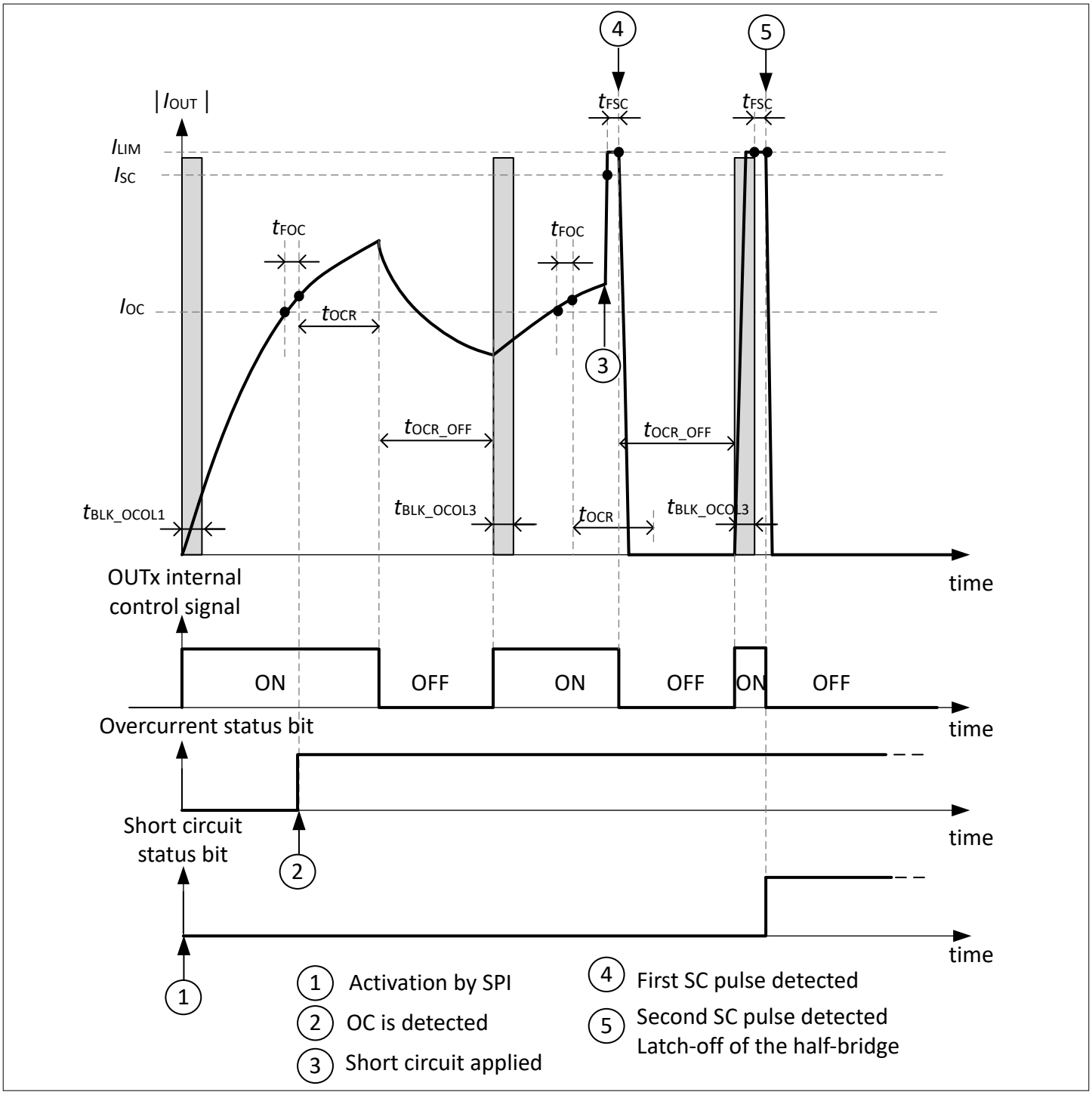


Figure 15 Short circuit detection on the active MOSFET, OCR enabled, SC counter enabled

5.4.3.1.3 OCR for half-bridges with disabled PWM, with short circuit detection and pairing

When the PWM control is disabled and the OCR is enabled, it is possible to enable the pairing of half-bridges, distributed in two groups. Refer to Table 25 and to Table 26.

OUT1 and OUT5 are defined as master outputs for each group, while the other outputs are defined as slave outputs.

The pairing feature enables the paired outputs to control DC motors with parallel capacitors up to 1 µF in overcurrent recovery mode.

When the pairing is enabled, the turn-on and the turn-off of one MOSFET can (depending on the conditions)

- Force a blank time t_{BLK_OCOL3} of an another paired half-bridge
- Mask the OC detection of an another paired half-bridge

These measures avoid an overcurrent or short circuit detection caused by:

- The charge of the motor capacitor
- The ringing due to the stray inductances in combination with the motor capacitor

Note: This feature is available only when the PWM mode is disabled for all outputs of a paring group.

Table 25 OUT1 – Pairing configurations

Configuration	Paired outputs
Setting1	No pairing (default)
Setting2	OUT1 paired with OUT2
Setting3	OUT1 paired with OUT3
Setting4	OUT1 paired with OUT2 and OUT3
Setting5	OUT1 paired with OUT6
Setting6	OUT1 paired with OUT2 and OUT6
Setting7	OUT1 paired with OUT3 and OUT3
Setting8	OUT1 paired with OUT2, OUT3 and OUT6

Table 26 OUT5 – Pairing configurations

Configuration	Paired outputs
Setting1	No pairing (default)
Setting2	OUT5 paired with OUT4
Setting3	OUT5 paired with OUT6
Setting4	OUT5 paired with OUT4 and OUT6

Pairing OUT6 to OUT1 and OUT5 is considered as an incorrect configuration. In this case, the paired error bit is set and latched until:

1. The pairing configuration is correct
2. And a clear command for the paired error bit is received

The pairing of all half-bridges is ignored until the paired error bit is cleared.

The pairing of a group of outputs is ignored if:

- At least one of the paired outputs is in PWM mode
- At least one of the paired outputs has its OCR disabled

5.4.3.1.4 OCR and SC detection for half-bridges with enabled PWM and passive FW

When an overcurrent for the active MOSFET is detected:

1. The output stays on if the PWM signal is high and $t < t_{OCR}$
2. Output reactivation:
   - Case 1: If the PWM signal stays high until the end of t_{OCR_OFF}, then the output is turned on at the end of t_{OCR_OFF}
   - Case 2: If the PWM signal goes low before the end of t_{OCR_OFF}, then the output is turned on at the PWM rising edge

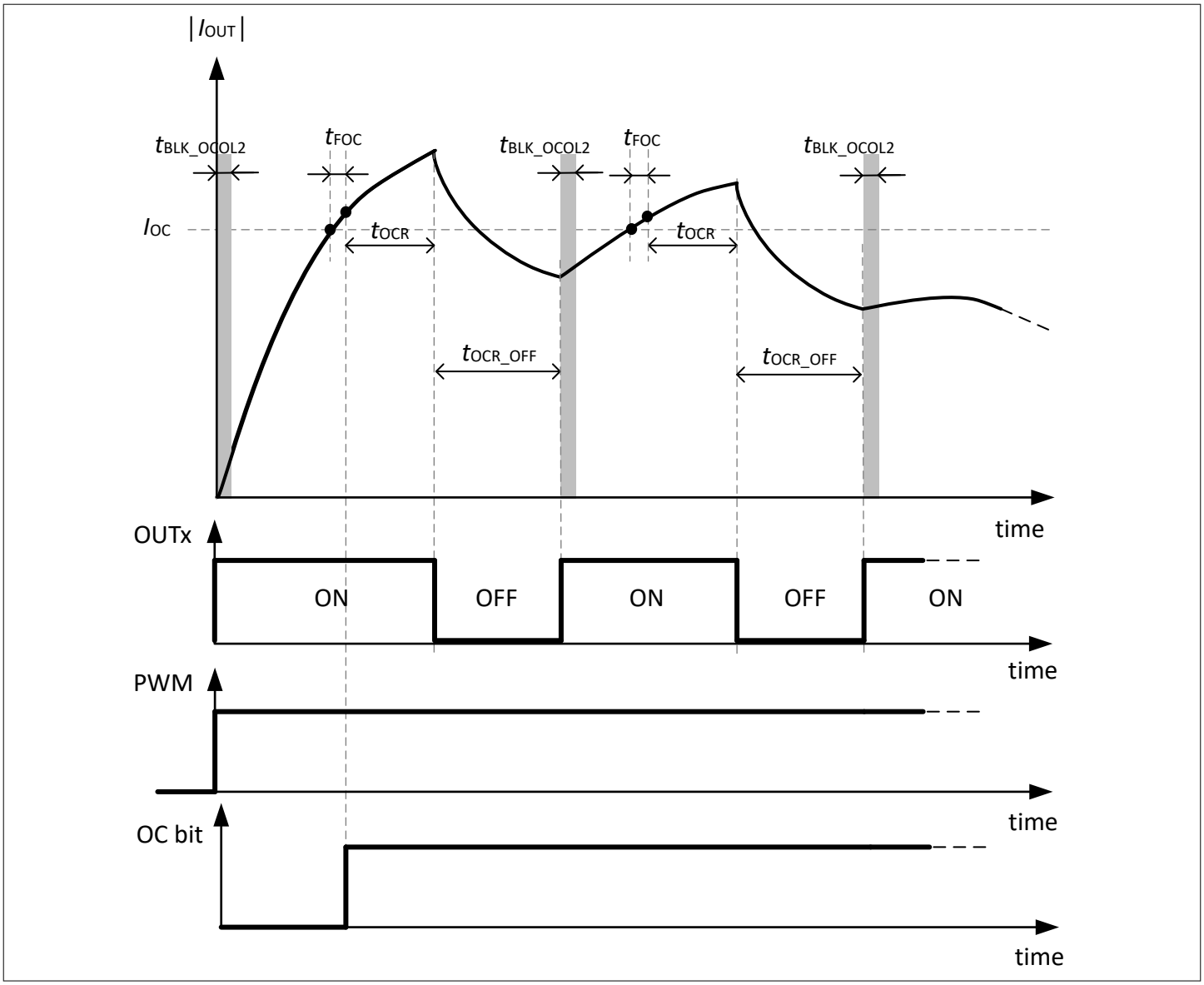


Figure 16 **OCR for a half-bridge with enabled PWM and passive freewheeling - The PWM signal stays high until the end to t_{OCR_OFF}**

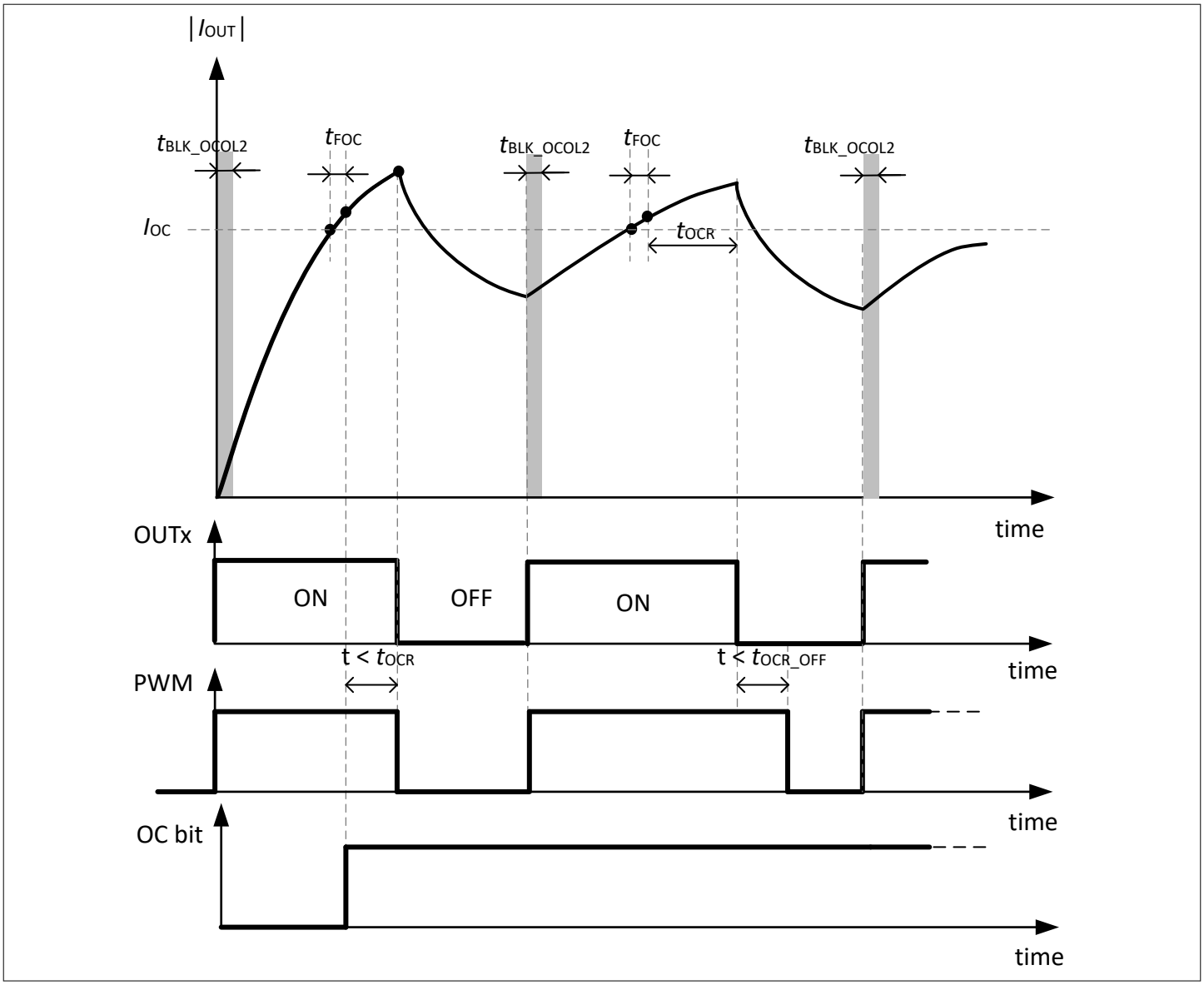


Figure 17 **OCR for a half-bridge with enabled PWM and passive freewheeling - The PWM signal goes low before the end of t_{OCR_OFF}**

SC detection for the active MOSFET with SC counter disabled

If the SC counter is disabled, then at the first SC pulse

- The SC status bit is set
- The half-bridge is latched off until the SC status bit is cleared

SC detection for the active MOSFET with SC counter enabled

If the SC counter is enabled, then:

- At the first SC pulse:
  - The active MOSFET is turned off:
    - For $t = t_{OCR\_OFF}$ if the PWM signal stays high during t_{OCR_OFF}
    - Until a rising of the PWM signal if the PWM signal goes low before the end t_{OCR_OFF}

- At the second **consecutive** SC pulse:
  - The SC status bit is set
  - The half-bridge is latched off until the SC status bit is cleared
- The SC counter is reset after the first SC pulse:
  - If $|I_{OUT}| \leq |I_{SC}|$ while:
    - The active MOSFET is on
    - And the active MOSFET is outside of its OC/OL blank time
  - If the output is deactivated by SPI

Notes:

- The short circuit detection of the active MOSFET is enabled even during t_{OCR}
- If the half-bridge is in PWM mode, then a rising or falling edge of the PWM input does not reset the SC counter

5.4.3.1.5 OCR and SC detection for half-bridges with enabled PWM and active FW

OC and SC detection for the FW MOSFET

If an OC is detected for the FW MOSFET, then the FW MOSFET is latched off.

If a SC pulse is detected for the FW MOSFET, then the complete half-bridge is latched off, independently from the SC counter.

OC and SC detection for the active MOSFET

The behavior of the active MOSFET in case of OC and SC with active FW enabled is the same as with FW disabled, except for an additional reset condition of the SC counter.

When the SC counter is enabled, the SC counter is also reset with an activation of the FW MOSFET.

Important: Because the SC counter is reset if the FW MOSFET is activated, it is highly recommended either to configure the half-bridge in PWM:

- With active FW enabled and SC counter disabled
- With active FW disabled and SC counter enabled

A short circuit of the active MOSFET may not be detected due to the repetitive reset of the SC counter if:

- Active FW is enabled
- **And** SC counter is enabled

When an overcurrent status bit of the active MOSFET is set, the impacted half-bridge is controlled in passive freewheeling, even if active freewheeling is configured.

5.4.3.2 Overcurrent recovery for OUT7 in low RDS(ON) mode

The slew rate and t_{BLK_OCOLx} of OUT7 in low $R_{DS(ON)}$ mode during OCR are configurable according to Table 19.

When an overcurrent is detected:

1. OUT7 stays on:
   - For t = t_{OCR} if the PWM is disabled
   - For t = t_{OCR} if the PWM is enabled and the PWM signal is high
   - Until the PWM signal is low if the PWM signal goes low before the expiration of t_{OCR}
2. Then OUT7 is turned off for t = t_{OCR_OFF}
3. OUT7 is turned back on:
   - With disabled PWM: at t = t_{OCR_OFF}
   - With enabled PWM: when the PWM signal is high and after the end of t_{OCR_OFF}

5.4.3.2.1 Short circuit detection for OUT7 in low RDS(ON) mode

The device implements a short circuit detection of OUT7 in low $R_{DS(ON)}$ mode when the OCR is activated.
A short circuit is detected if $V_{OUT7} < V_{OUT7\_SC}$ at the end of t_{OCR} for two consecutive cycles.
OUT7 is latched off and the short circuit status bit for OUT7 is set until a clear command to the corresponding status register is received.

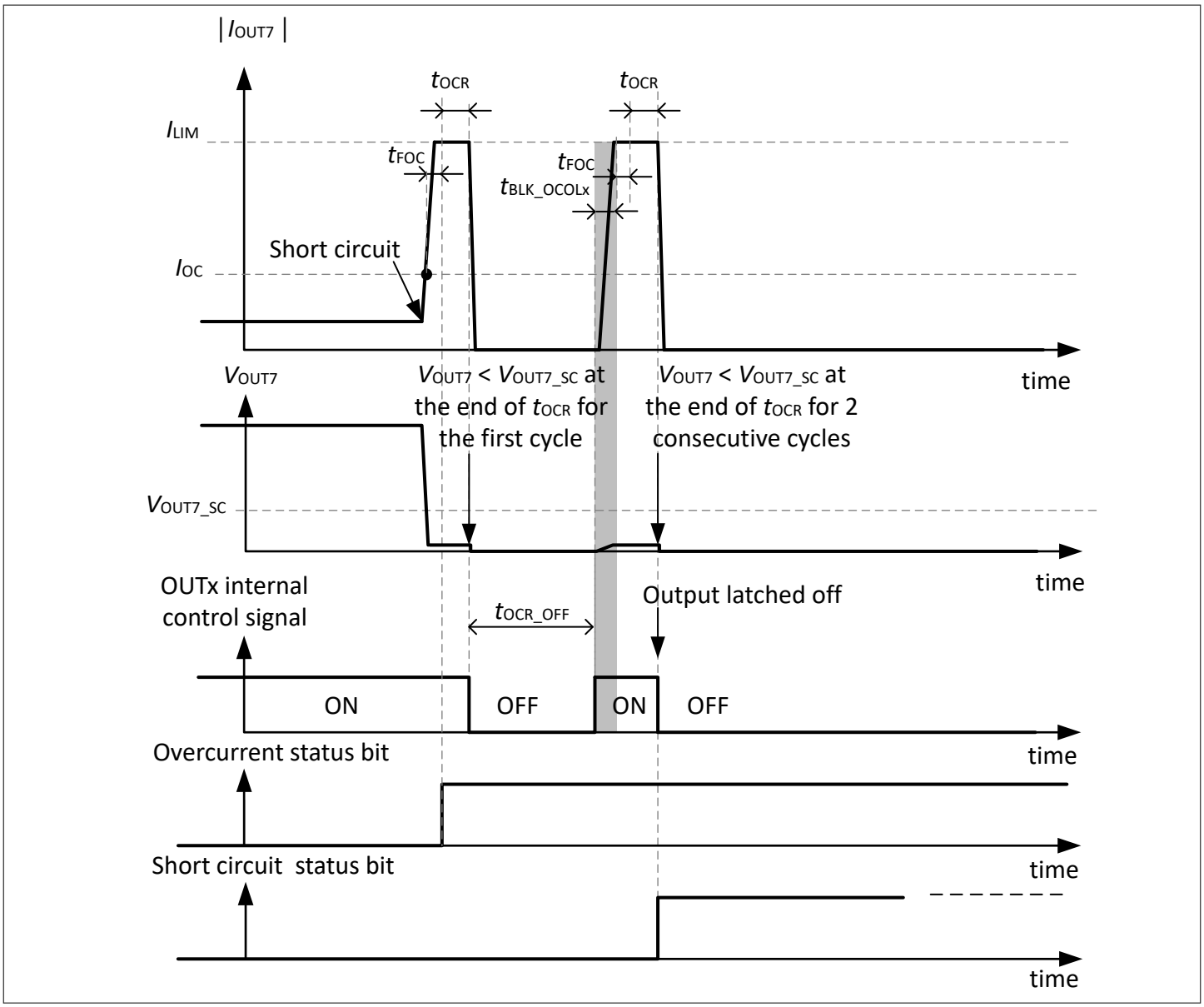


Figure 18 Short circuit detection of OUT7 in low *R*DS(ON)

The short circuit counter is reset if one of these conditions is met:

- If OC is detected: $V_{OUT7} \geq V_{OUT7\_SC}$ at the end of t_{OCR}
- OUT7 is turned off by SPI
- If the PWM mode is activated: At the turn-off of the OUT7 by the PWM generator

5.5 Diagnostics

5.5.1 Current monitor

The CM (current monitor) pin provides an image of the current through the high-sides, flowing out of OUTx, or an image of V_S according to Table 27.

Table 27 CM selection

SPI configuration	CM output	Note
Setting1	CM in high-impedance	Default
Settingx+1, x=1 to 12	$I_{CM} = I_{CM\_OFFSET} + \lvert I_{OUTx} \rvert / d_{KILIS}$	I_{OUTx} flows out of the high-side
Setting14	$V_{CM} = 0.2 \times V_S$	Tolerance: $V_{S\_RATIO\_TOL}$
Setting15	$V_{CM} = 0.13 \times V_S$	Tolerance: $V_{S\_RATIO\_TOL}$

The VS ratio is configurable by SPI:

Table 28 Configurable VS ratio

Parameter	Symbol	Nominal value	Unit	Default	Tolerance	Note
V_S ratio at CM pin	V_{S_RATIO}	0.200 0.130	–	0.200	$V_{S\_RATIO\_TOL}$	V_S selected at CM pin

5.5.2 Open load detection

The open load detection monitors the current in each activated output stage, including the ECV low-side.

The open load detection is ignored:

- For any output: At the activation of the output during any t_{BLK_OCOLx}
- For half-bridges when OCR and pairing are enabled: During t_{BLK_OCOL3} (refer to Chapter 5.4.3.1.3)

t_{BLK_OCOL1} and the slew rate S_{R1} are applicable to:

- OUT8-OUT12
- ECV LS

Refer to Table 11 for the applicable t_{BLK_OCOLx} of OUT1 to OUT6.

Refer to Table 19 for the applicable t_{BLK_OCOLx} of OUT7.

After t_{BLK_OCOLx}:

- For an activated high-side of OUT1 to OUT6: If $\lvert I_{OUT} \rvert \leq \lvert I_{OL} \rvert$ for t = t_{FOL1}, then an open load is detected at the high-side
- For an activated low-side of OUT1 to OUT6: If $I_{OUT} \leq I_{OL}$ for t = t_{FOL1}, then an open load is detected at the low-side
- For an activated high-side of OUT7 to OUT12: If $\lvert I_{OUT} \rvert \leq \lvert I_{OL} \rvert$ for t = t_{FOL2}, then an open load is detected at the high-side
- For the ECV low-side: If $I_{ECV} \leq I_{OL}$ for t = t_{FOL2}, then an open load is detected at the ECV low-side

If an open load is detected:

- The corresponding open load status bit is set and latched, until a clear command to the corresponding status register is received
- The state of the output remains unchanged

5.6 Electrical characteristics

Electrical characteristics, V_S =5.5 V to 20 V, V_{DD} = 3.0 V to 5.5 V, V_{CP} = V_S+ 7.5 V to V_S+ 17 V, T_j = -40°C to +150°C; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Table 29 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Drain-source on-resistance							
RDS(ON) OUT1,6 HS/LS	$R_{DS(ON)\_OUT1,6}$	–	280	330	mΩ	I_{OUT} = ±1.5 A; T_j = 25 °C	P_OUT_01_01
RDS(ON) OUT1,6 HS/LS	$R_{DS(ON)\_OUT1,6}$	–	450	550	mΩ	I_{OUT} = ±1.5 A; T_j = 150 °C	P_OUT_01_02
RDS(ON) OUT2,3 HS/LS	$R_{DS(ON)\_OUT2,3}$	–	1200	1600	mΩ	I_{OUT} = ±0.4 A; T_j = 25 °C	P_OUT_01_05
RDS(ON) OUT2,3 HS/LS	$R_{DS(ON)\_OUT2,3}$	–	2000	2400	mΩ	I_{OUT} = ±0.4 A; T_j = 150 °C	P_OUT_01_06
RDS(ON) OUT4 HS/LS	$R_{DS(ON)\_OUT4}$	–	135	160	mΩ	I_{OUT} = ±3 A; T_j = 25 °C	P_OUT_01_07
RDS(ON) OUT4 HS/LS	$R_{DS(ON)\_OUT4}$	–	210	250	mΩ	I_{OUT} = ±3 A; T_j = 150 °C	P_OUT_01_08
RDS(ON) OUT5 HS/LS	$R_{DS(ON)\_OUT5}$	–	135	160	mΩ	I_{OUT} = ±3 A; T_j = 25 °C	P_OUT_01_09
RDS(ON) OUT5 HS/LS	$R_{DS(ON)\_OUT5}$	–	200	250	mΩ	I_{OUT} = ±3 A; T_j = 150°C	P_OUT_01_10
RDS(ON) OUT7 Low RDS(ON)	$R_{DS(ON)\_OUT7\_1}$	–	280	350	mΩ	I_{OUT} = -0.9 A; T_j = 25 °C; Low $R_{DS(ON)}$	P_OUT_01_11
RDS(ON) OUT7 Low RDS(ON)	$R_{DS(ON)\_OUT7\_1}$	–	440	550	mΩ	I_{OUT} = -0.9 A; T_j = 150 °C; Low $R_{DS(ON)}$	P_OUT_01_12
RDS(ON) OUT7 High RDS(ON)	$R_{DS(ON)\_OUT7\_2}$	–	1.2	1.6	Ω	I_{OUT} = -0.2 A ;T_j = 25 °C; High $R_{DS(ON)}$	P_OUT_01_13
RDS(ON) OUT7 High RDS(ON)	$R_{DS(ON)\_OUT7\_2}$	–	2	2.4	Ω	I_{OUT} = -0.2 A; T_j = 150 °C; High $R_{DS(ON)}$	P_OUT_01_14
RDS(ON) OUT8,9,10	$R_{DS(ON)\_OUT8\text{-}10}$	–	1.2	1.6	Ω	I_{OUT} = -0.4 A; T_j = 25 °C	P_OUT_01_15
RDS(ON) OUT8,9,10	$R_{DS(ON)\_OUT8,9,10}$	–	2	2.4	Ω	I_{OUT} = -0.4 A; T_j = 150 °C	P_OUT_01_16
RDS(ON) OUT11	$R_{DS(ON)\_OUT11}$	–	2.2	2.8	Ω	I_{OUT} = -60 mA T_j = 25°C	P_OUT_01_17
RDS(ON) OUT11	$R_{DS(ON)\_OUT11}$	–	3.5	4.5	Ω	I_{OUT} = -60 mA T_j = 150 °C	P_OUT_01_18
RDS(ON) OUT12	$R_{DS(ON)\_OUT12}$	–	5	7	Ω	I_{OUT} = -60 mA; T_j = 25°C; OUT12 in HS mode	P_OUT_01_19

(table continues...)

Table 29 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RDS(ON) OUT12	$R_{DS(ON)\_OUT12}$	–	7.4	12	Ω	I_{OUT} = -60 mA; T_j = 150 °C; OUT12 in HS mode	P_OUT_01_20
RDS(ON) ECV LS	$R_{DS(ON)\_ECV\_LS}$	–	1.2	1.6	Ω	I_{OUT} = 0.4 A; T_j = 25 °C	P_OUT_01_21
RDS(ON) ECV LS	$R_{DS(ON)\_ECV\_LS}$	–	2	2.4	Ω	I_{OUT} = 0.4 A; T_j = 150 °C	P_OUT_01_22
Freewheeling forward diode voltage							
Freewheeling forward diode voltage	V_f	–	0.8	1	V	$I_{OUT1,6}$ =± 1.5 A; $I_{OUT2,3}$ = ± 0.4 A; $I_{OUT4,5}$ = ± 3 A; T_j = 150 °C	P_OUT_02_01
Current monitor CM							
CM leakage current	I_{CML}	–	–	1	µA	CM deactivated	P_OUT_03_01
VCM functional range	V_{CM}	0	–	V_{DD} -1 V	V	–	P_OUT_03_02
CM current capability	I_{CM_MAX}	6	–	–	mA	–	P_OUT_03_03
High-side current monitor (HSx selected to CM pin)							
CM offset OUT1,6	$I_{CM(offset)\_OUT1,6}$	-10	–	10	µA	$\lvert I_{OUT1,6} \rvert \geq 0.3$ A	P_OUT_04_01
CM offset OUT2,3	$I_{CM(offset)\_OUT2,3}$	-10	–	10	µA	$\lvert I_{OUT2,3} \rvert \geq 0.07$ A	P_OUT_04_02
CM offset OUT4,5	$I_{CM(offset)\_OUT4,5}$	-18	–	18	µA	$\lvert I_{OUT4,5} \rvert \geq 0.5$ A	P_OUT_04_03
CM offset OUT7 low Rds(on)	$I_{CM(offset)\_OUT7L}$	-18	–	18	µA	$\lvert I_{OUT7} \rvert \geq 0.3$ A	P_OUT_04_15
CM Offset OUT7 high Rds(on)	$I_{CM(offset)\_OUT7H}$	-10	–	10	µA	OUT7 in high $R_{DS(ON)}$ $\lvert I_{OUT7} \rvert \geq 0.07$ A	P_OUT_04_05
CM Offset OUT8-10	$I_{CM(offset)\_OUT8-10}$	-10	–	10	µA	$\lvert I_{OUT8,9,10} \rvert \geq 0.07$ A	P_OUT_04_06
CM Offset OUT11-12	$I_{CM(offset)\_OUT11-12}$	-9	–	9	µA	OUT12 in HS mode $\lvert I_{OUT11,12} \rvert \geq 0.02$ A	P_OUT_04_07
Differential CM ratio OUT1,6 low current	$dK_{ILIS\_OUT1,6A}$	9850	10800	11950	–	0.3 A ≤ $\lvert I_{OUT1,6} \rvert \leq 1$ A	P_OUT_04_08
Differential CM ratio OUT1,6 high current	$dK_{ILIS\_OUT1,6B}$	10000	10800	11500	–	$\lvert I_{OUT1,6} \rvert \geq 1$ A	P_OUT_04_16
Differential CM ratio OUT2,3	$dK_{ILIS\_OUT2,3}$	2050	2250	2450	–	$\lvert I_{OUT2,3} \rvert \geq 0.07$ A	P_OUT_04_10
Differential CM ratio OUT4	dK_{ILIS_OUT4}	9400	10200	11000	–	$\lvert I_{OUT4} \rvert \geq 0.5$ A	P_OUT_04_17
Differential CM ratio OUT5	dK_{ILIS_OUT5}	9800	10600	11400	–	$\lvert I_{OUT5} \rvert \geq 0.5$ A	P_OUT_04_18

(table continues...)

Table 29 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Differential CM ratio OUT7 Low Rds(on) low current	dK_{ILIS_OUT7LA}	10400	12200	13500	–	OUT7 in low $R_{DS(ON)}$ 0.3 A ≤ $\lvert I_{OUT7} \rvert$ ≤ 1 A	P_OUT_04_22
Differential CM ratio OUT7 Low Rds(on) high current	dK_{ILIS_OUT7LB}	10800	12200	13500	–	OUT7 in low $R_{DS(ON)}$ $\lvert I_{OUT7} \rvert$ > 1 A	P_OUT_04_19
Differential CM ratio OUT7 high Rds(on)	dK_{ILIS_OUT7H}	1950	2140	2330	–	OUT7 in low $R_{DS(ON)}$ $\lvert I_{OUT7} \rvert$ ≥ 0.07 A	P_OUT_04_20
Differential CM ratio OUT8,9,10	$dK_{ILIS\_OUT8,9,10}$	1970	2200	2430	–	$\lvert I_{OUT8,9,10} \rvert$ ≥ 0.07 A	P_OUT_04_21
Differential CM ratio OUT11,12	$dK_{ILIS\_OUT11,12}$	840	1070	1300	–	OUT12 in HS mode $\lvert I_{OUT8,9,10} \rvert$ ≥ 0.02 A	P_OUT_04_12
VS selected to CM pin							
VS ratio tolerance	$V_{S\_RATIO\_TOL}$	-2 %	–	2%	–	–	P_OUT_05_01
Overcurrent, short circuit detection and current limitation							
OC filter time	t_{FOC}	5	7	9	µs	–	P_OUT_06_01
OC/OL blank time 1	t_{BLK_OCOL1}	50	65	80	µs	–	P_OUT_06_02
OC/OL blank time 2	t_{BLK_OCOL2}	3	5	7	µs	–	P_OUT_06_03
OC/OL blank time 3 OUT1-6	$t_{BLK\_OCOL3\_OUT1\_6}$	18	24	30	µs	OUT1, OUT6	P_OUT_06_20
OC/OL blank time 3 OUT2-3	$t_{BLK\_OCOL3\_OUT2\_3}$	60	80	100	µs	OUT2, OUT3	P_OUT_06_21
OC/OL blank time 3 OUT4-5	$t_{BLK\_OCOL3\_OUT4\_5}$	10	14	18	µs	OUT4, OUT5	P_OUT_06_22
OC thres. HS/LS OUT1,6	$\lvert I_{OC\_OUT1,6\_1} \rvert$	1.5	2	2.7	A	2 A nom. configured	P_OUT_06_04
OC thres.HS/LS OUT1,6	$\lvert I_{OC\_OUT1,6\_2} \rvert$	2.2	3	3.6	A	3 A nom. configured	P_OUT_06_05
OC thres.HS/LS OUT1,6	$\lvert I_{OC\_OUT1,6\_3} \rvert$	3	4	4.6	A	4 A nom. configured	P_OUT_06_06
OC thres.HS/LS OUT2,3	$\lvert I_{OC\_OUT2,3} \rvert$	0.5	0.75	1	A	–	P_OUT_06_10
OC thres.HS/LS OUT4	$\lvert I_{OC\_OUT4} \rvert$	7	7.5	8.8	A	–	P_OUT_06_11

(table continues...)

Table 29 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OC thres.HS/LS OUT5	$\lvert I_{OC\_OUT5\_1} \rvert$	3.4	4	4.9	A	4 A nom. configured	P_OUT_06_12
OC thres.HS/LS OUT5	$\lvert I_{OC\_OUT5\_2} \rvert$	5.1	6	7.5	A	6 A nom. configured	P_OUT_06_13
OC thres.HS/LS OUT5	$\lvert I_{OC\_OUT5\_3} \rvert$	7	7.5	9.6	A	7.5 A nom. configured	P_OUT_06_14
OC thres.OUT7 low RDS(ON)	$I_{OC\_OUT7\_1}$	-2.8	-2.3	-1.8	A	OUT7 in low $R_{DS(ON)}$	P_OUT_06_15
OC thres.OUT7 high RDS(ON)	$I_{OC\_OUT7\_2}$	-0.65	-0.5	-0.35	A	OUT7 in high $R_{DS(ON)}$	P_OUT_06_16
OC thres. OUT8-10	$I_{OC\_OUT8\text{-}10}$	-1	–	-0.5	A	–	P_OUT_06_17
OC thres. OUT11-12	$I_{OC\_OUT11,12}$	-0.5	–	-0.25	A	OUT12 in HS mode	P_OUT_06_18
OC thres. ECV LS	I_{OC_ECVLS}	0.5	–	1	A	–	P_OUT_06_19
Short circuit detection							
Short circuit filter time	t_{FSC}	3	5	7	µs	–	P_OUT_07_01
$\lvert$ISC_OUT1,6$\rvert$ - $\lvert$IOC_OUT1,6_3$\rvert$	$\lvert I_{SC\_OUT1,6} \rvert$ - $\lvert I_{OC\ OUT1,6\_3} \rvert$	500	800	–	mA	–	P_OUT_07_02
$\lvert$ISC_OUT2,3$\rvert$ - $\lvert$IOC_OUT2,3$\rvert$	$\lvert I_{SC\_OUT2,3} \rvert$ - $\lvert I_{OC\ OUT2,3} \rvert$	100	175	–	mA	–	P_OUT_07_04
$\lvert$ISC_OUT4$\rvert$ - $\lvert$IOC_OUT4$\rvert$	$\lvert I_{SC\_OUT4} \rvert$ - $\lvert I_{OC\ OUT4} \rvert$	0.8	1.5	–	A	–	P_OUT_07_05
$\lvert$ISC_OUT5$\rvert$ - $\lvert$IOC_OUT5$\rvert$	$\lvert I_{SC\_OUT5} \rvert$ - $\lvert I_{OC\ OUT5\_3} \rvert$	0.9	1.5	–	A	–	P_OUT_07_06
VOUT7_SC	V_{OUT7_SC}	1.6	2	2.4	V		P_OUT_07_07
Current limitation							
ILIM - ISC OUT1-6	$I_{LIM} - I_{SC}$	0	–	–	A	–	P_OUT_07_01
ILIM11 OUT7 low RDS(ON)	$I_{LIM\_OUT7\_11}$	2.1	3	3.7	A	OUT7 in low $R_{DS(ON)}$	P_OUT_07_03
ILIM12 OUT7 low RDS(ON)	$I_{LIM\_OUT7\_12}$	3.2	4	4.8	A	OUT7 in low $R_{DS(ON)}$	P_OUT_07_04
ILIM11 - IOC OUT7 low RDS(ON)	$I_{LIM\_OUT7\_11} - I_{OC\_OUT7\_1}$	0	_	_	A	OUT7 in low $R_{DS(ON)}$	P_OUT_07_07
ILIM - IOC OUT7 high RDS(ON)	$I_{LIM\_OUT7\_2} - I_{OC\_OUT7\_2}$	0	–	–	A	OUT7 in high $R_{DS(ON)}$	P_OUT_07_05
ILIM - IOC OUT8-12	$I_{LIM\_OUT8\text{-}12} - I_{OC\_OUT8\text{-}12}$	0	–	–	A	OUT12 in HS mode	P_OUT_07_06

(table continues...)

Table 29 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Constant current mode CCM							
ICCM1 OUT7-10	$I_{CCM1\_OUT7\text{-}10}$	20	90	170	mA	OUT7 in high or low $R_{DS(ON)}$	P_OUT_08_01
ICCM2 OUT7-10	$I_{CCM2\_OUT7\text{-}10}$	50	250	380	mA	OUT7 in high or low $R_{DS(ON)}$	P_OUT_08_02
ICCM3 OUT7 low RDS(ON)	$I_{CCM3\_OUT7\_1}$	0.8	2	2.5	A	OUT7 in low $R_{DS(ON)}$	P_OUT_08_03
ICCM3 OUT7 high RDS(ON)	$I_{CCM3\_OUT7\_2}$	0.3	0.5	0.65	A	OUT7 in high $R_{DS(ON)}$	P_OUT_08_04
ICCM3 OUT8-10	$I_{CCM3\_OUT8\text{-}10}$	0.25	0.5	0.75	A	–	P_OUT_08_05
ICCM1 OUT11-12	$I_{CCM1\_OUT11\text{-}12}$	15	50	75	mA	OUT12 in HS mode	P_OUT_08_06
ICCM2 OUT11-12	$I_{CCM2\_OUT11\text{-}12}$	50	100	150	mA	OUT12 in HS mode	P_OUT_08_07
ICCM3 OUT11-12	$I_{CCM3\_OUT11,12}$	0.1	–	0.5	A	OUT12 in HS mode	P_OUT_08_08
CCM time 1 OUT7-12	$t_{CCM1\_OUT7\text{-}10}$	16	20	24	ms	OUT7 in high or low $R_{DS(ON)}$ OUT12 in HS mode	P_OUT_08_09
CCM time 2 OUT7-12	$t_{CCM2\_OUT7\text{-}10}$	4	5	6	ms	OUT7 in high or low $R_{DS(ON)}$ OUT12 in HS mode	P_OUT_08_10
CCM time 3 OUT7-12	t_{CCM3}	32	36	40	µs	OUT7 in high or low $R_{DS(ON)}$ OUT12 in HS mode	P_OUT_08_11
CCM LOW VOUT	V_{OUT_LOW}	4	4.7	5.5	V	–	P_OUT_08_12
VOUT_LOW filter time	t_{FVOUT_LOW}	1	2	3	µs	–	P_OUT_08_13
Open load detection							
OL thres.HS/LS OUT1,6	$\lvert I_{OL\_OUT1,6} \rvert$	6	30	80	mA	–	P_OUT_09_01
OL thres.HS/LS OUT2,3	$\lvert I_{OL\_OUT2,3} \rvert$	6	20	35	mA	–	P_OUT_09_03
OL thres.HS/LS OUT4,5	$\lvert I_{OL\_HS4,5} \rvert$	50	–	300	mA	–	P_OUT_09_05
OL thres.OUT7 low RDS(ON)	$I_{OL\_OUT7\_1}$	-80	–	-3	mA	OUT7 in low $R_{DS(ON)}$	P_OUT_09_05
OL thres.OUT7 high RDS(ON)	$I_{OL\_OUT7\_2}$	-10	–	-2	mA	OUT7 in high $R_{DS(ON)}$	P_OUT_09_07
OL thresh. OUT8-10	$I_{OL\_OUT8\text{-}10}$	-12	–	-1	mA	–	P_OUT_09_08

(table continues...)

Table 29 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OL thresh. OUT11,12	$I_{OL\_OUT11,12}$	-4	–	-0.2	mA	OUT12 in HS mode	P_OUT_09_09
OL thres.ECV LS	I_{OLD_ECVLS}	6	20	30	mA	–	P_OUT_09_10
OL filter time for OUT1 to OUT6	t_{FOL1}	0.8	1	1.2	ms	Valid for OUT1 to OUT6	P_OUT_09_11
OL filter time OUT7-12, ECVLS	t_{FOL2}	150	200	250	µs	Valid for OUT7-12, ECVLS	P_OUT_09_12
OUTx leakage current							
OUT1-6, HS off-state leakage	$I_{L(OFF)\_HS}$	-70	–	70	µA	V_{OUT} = 0 V; V_S = 13.5 V; T_J = 85°C; Sleep mode and normal mode OUT1 to OUT6	P_OUT_10_01
OUT1-6, LS off-state leakage	$I_{L(OFF)\_LS}$	-70	–	70	µA	OUT1 to OUT6; V_{OUT} = V_S = 13.5 V; T_J = 85°C; Sleep mode and normal mode	P_OUT_10_03
OUT7-12 HS off-state leakage	$I_{L(OFF)\_HS}$	-5	–	5	µA	OUT7 to OUT12; V_{OUT} = 0 V; V_S = 13.5 V; T_J = 85°C; Sleep mode and normal mode	P_OUT_10_05
ECV LS off-state leakage normal	$I_{L(OFF)\_ECVLS\_Normal}$	-5	–	5	µA	ECV low-side; V_{ECV_LS} < 6 V; V_S = 13.5 V; T_J = 85°C; normal mode	P_OUT_10_07
ECV low-side leakage current sleep	$I_{L(OFF)\_ECVLS\_Sleep}$	0	–	700	µA	ECV low-side; V_{ECV_LS} < 6 V; V_S = 13.5 V; T_J = 150°C; sleep mode	P_OUT_10_09
OUTx switching times							
Turn-on delay time OUT1-6 SR1	t_{DON}	–	30	80	µs	1) 2) Slew rate S_{R1}, V_S = 13.5 V	P_OUT_11_01
Turn-on delay time OUT1-6 SR2	t_{DON}	–	1.5	2	µs	1) 3) Slew rate S_{R2}, V_S = 13.5 V	P_OUT_11_03
Turn-on delay time OUT7 SR1	t_{DON}	–	30	80	µs	1) 2) Slew rate S_{R1}, OUT7 in high or low $R_{DS(ON)}$, V_S = 13.5 V	P_OUT_11_05
Turn-on delay time OUT7 SR2	t_{DON}	–	2.2	5.5	µs	1) 2) Slew rate S_{R2}, OUT7 in low $R_{DS(ON)}$, V_S = 13.5 V	P_OUT_11_06

(table continues...)

Table 29 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Turn-on delay time OUT2,3,8-12	t_{DON}	–	30	80	µs	1) 2) OUT12 in HS mode, V_S = 13.5 V	P_OUT_11_07
Turn-on delay time ECV LS	t_{DON}	–	30	80	µs	1) 2) V_S = 13.5 V	P_OUT_11_08
Turn-off delay time OUT1-6 SR1	t_{DOFF}	–	60	180	µs	1) 4) Slew rate S_{R1}, V_S = 13.5 V	P_OUT_11_09
Turn-off delay time OUT1-6 SR2	t_{DOFF}	–	3	6	µs	1) 5) Slew rate S_{R2}, V_S = 13.5 V	P_OUT_11_11
Turn-off delay time OUT7 SR1	t_{DOFF}	–	60	160	µs	1) 4) Slew rate S_{R1}, V_S = 13.5 V	P_OUT_11_18
Turn-off delay time OUT7 SR2	t_{DOFF}	–	5	8.5	µs	1) Slew rate S_{R2}, V_S = 13.5 V	P_OUT_11_19
Turn-off delay time OUT8-12	t_{DOFF}	–	60	160	µs	1) 2) OUT12 in HS mode, V_S = 13.5 V	P_OUT_11_13
Cross current protection time	t_{CCP1}	120	150	180	µs	1)) Slew rate S_{R1} or latch-off	P_OUT_11_14
Cross current protection time	t_{CCP2}	5.5	7	8.4	µs	1)) Slew rate S_{R2}	P_OUT_11_15
Slew rate 1	S_{R1}	0.12	0.5	1.4	V/µs	6) V_S = 13.5 V	P_OUT_11_16
Slew rate 2	S_{R2}	5	10	20	V/µs	6) V_S = 13.5 V	P_OUT_11_17

1) Resistive load
2) For high-sides from V_{CSN} = 50% V_{DD} to V_{OUT} = 20% V_S, for low-sides V_{CSN} = 50% V_{DD} to V_{OUT} = 80% V_S
3) For high-sides from V_{PWM} = 50% V_{DD} to V_{OUT} = 20% V_S, for low-sides from V_{PWM} = 50% V_{DD} to V_{OUT} = 80% V_S
4) For high-sides from V_{CSN} = 50% V_{DD} to V_{OUT} = 80% V_S, for low-sides from V_{CSN} = 50% V_{DD} to V_{OUT} = 20% V_S
5) For high-sides from V_{PWM} = 50% V_{DD} to V_{OUT} = 80% V_S, for low-sides from V_{PWM} = 50% V_{DD} to V_{OUT} = 20% V_S
6) V_{OUT} from 20%-80% V_S and 80%-20% V_S

6 VCC2 voltage regulator

The output OUT12_VCC2 can be configured as a voltage regulator according to Table 30 for example for an off-board sensor supply.

This section describes the operation as voltage regulator.

Refer to Chapter 4.3.1.3 for the conditions for the setting of OUT12_VCC2 as high-side, 3.3 V or 5 V voltage regulator.

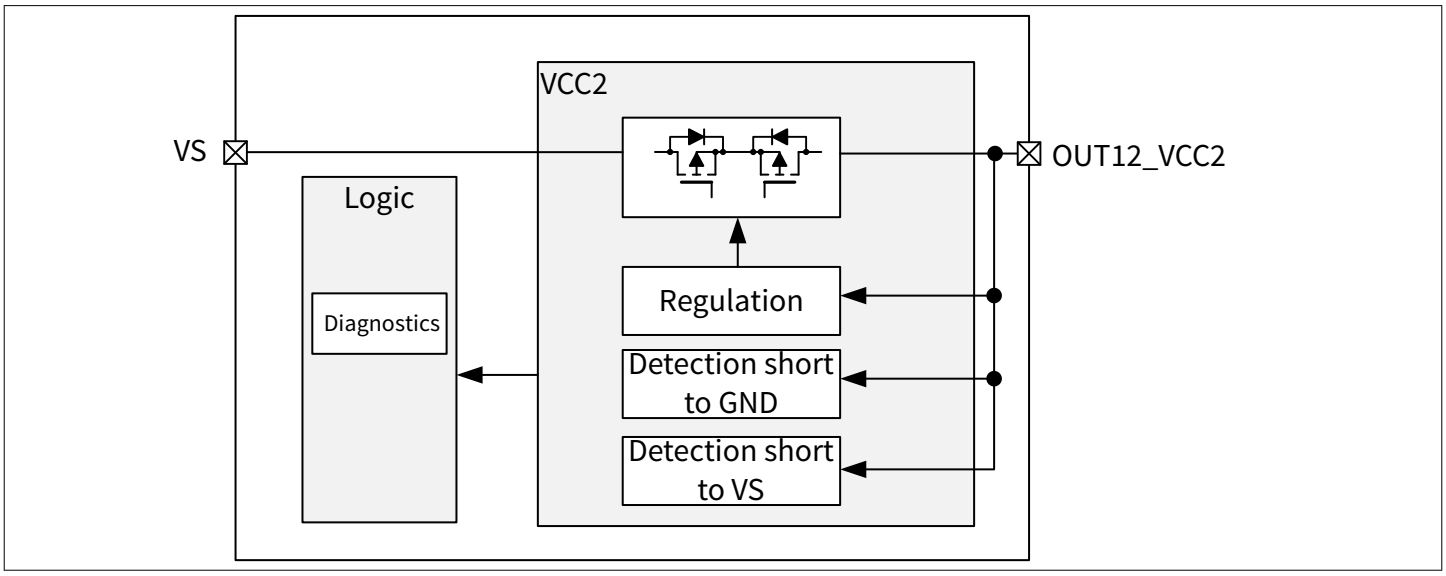


Figure 19 Block diagram of the voltage regulator VCC2

Table 30 OUT12_VCC2 settings - High-side / voltage regulator

SPI configuration	OUT12_VCC2
Setting1	Voltage regulator V_{CC2_V33} (default)
Setting2	Voltage regulator V_{CC2_V5}
Setting3	High-side

The voltage regulator VCC2 has a configurable nominal voltage of V_{CC2_V33} or V_{CC2_V5} and delivers currents up to I_{VCC2_LIM}.

VCC2 can be switched on and switched off via SPI in normal mode by the enable bit for OUT12_VCC2 (Refer to Table 13) and is protected against short-circuits to the battery.

An external output capacitor with low ESR is required at the VCC2 pin for stability and buffering transient load currents.

The regulator stability is specified for external capacitor values of C_{VCC2} with a maximum ESR of R_{CVCC2_ESR}.

VCC2 short circuit detection to GND

The short circuit detection to GND has a blank time $t_{BLKVCC2\_SC\_GND}$ starting at the activation of VCC2.

A short circuit to GND is detected if $V_{OUT12\_VCC2} \leq V_{VCC2\_SC\_GND}$ at t = $t_{FVCC2\_SC\_GND}$ after $t_{BLKVCC2\_SC\_GND}$.

The failure reaction is:

- The status bit for VCC2 short-circuit to GND is set
- VCC2 is latched off, until the status bit is cleared

VCC2 Short-circuit detection to the VS

A VCC2 short circuit to VS is detected if $V_{CC2} > V_{CC2\_SCVS\_R}$ for t = t_{FVCC2_SCVS}.

If a short-circuit to VS is detected, then:

- VCC2 is turned off
- The VCC2 short circuit to VS status bit is set and latched.

$V_{CC2\_SCVS\_R}$ and $V_{CC2\_SCVS\_F}$ depend on the configured nominal V_{CC2} voltage.

VCC2 is turned back on if V_{CC2} falls below $V_{CC2\_SCVS\_F}$ for t = t_{FVCC2_SCVS} independently from the status bit.

6.1 Electrical characteristics

Electrical characteristics, V_S =5.5 V to 20 V, V_{DD} = 3.0 V to 5.5 V, V_{CP} = V_S+ 7.5 V to VS+ 17 V, T_j = -40°C to +150°C; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Table 31 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VCC2 output voltage V33	V_{CC2_V33}	3.23	3.3	3.37	V	$V_S \geq 5.5$ V; 10 µA ≤ I_{VCC2} ≤ 30 mA Incl. line and load regulation V_{CC2_V33} configured	P_REG_1_01
VCC2 output voltage V5	V_{CC2_V5}	4.9	5	5.1	V	$V_S \geq 5.5$ V; 10 µA ≤ I_{VCC2} ≤ 30 mA Incl. line and load regulation V_{CC2_V5} configured	P_REG_1_02
VCC2 drop voltage V5	V_{CC2_DR}	–	–	0.4	V	V_S = 5.25 V; I_{VCC2} = 20 mA; VCC2 5 V configured	P_REG_1_03
VCC2 output current limitation	I_{VCC2_LIM}	50	–	150	mA	–	P_REG_1_04
VCC2 buffer capacitor	C_{VCC2}	0.47	1	10	µF	–	P_REG_1_05
VCC2 buffer cap. ESR	C_{VCC2_ESR}	–	–	1	Ω	–	P_REG_1_06
VCC2 short circuit to GND	$V_{CC2\_SC\_GND}$	1.5	2	2.5	V	–	P_REG_1_07
VCC2 short circuit to GND filter time	$t_{FVCC2\_SC\_GND}$	1.6	2	2.4	ms	–	P_REG_1_08
VCC2 short to GND blank time	$t_{BLKVCC2\_SC\_GND}$	1.6	2	2.4	ms		P_REG_1_09
VCC2 short to VS, rising V5	$V_{CC2\_SCVS\_R\_V5}$	5.6	5.8	6	V	V_{CC2_V5} configured	P_REG_1_10

(table continues...)

Table 31 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VCC2 short to VS, falling V5	$V_{CC2\_SCVS\_F\_V5}$	5.45	5.65	5.85	V	V_{CC2_V5} configured	P_REG_1_11
VCC2 short to VS, rising V33	$V_{CC2\_SCVS\_R\_V33}$	3.7	3.85	4	V	V_{CC2_V33} configured	P_REG_1_12
VCC2 short to VS, falling V33	$V_{CC2\_SCVS\_F\_V33}$	3.6	3.75	3.9	V	V_{CC2_V33} configured	P_REG_1_13
VCC2 short to VS filter time	t_{FVCC2_SCVS}	51	64	80	µs	–	P_REG_1_14

7 Electrochromic mirror control

This section describes the control of the electrochromic mirror (EC) including the integrated low-side between ECV and GND for fast discharge.

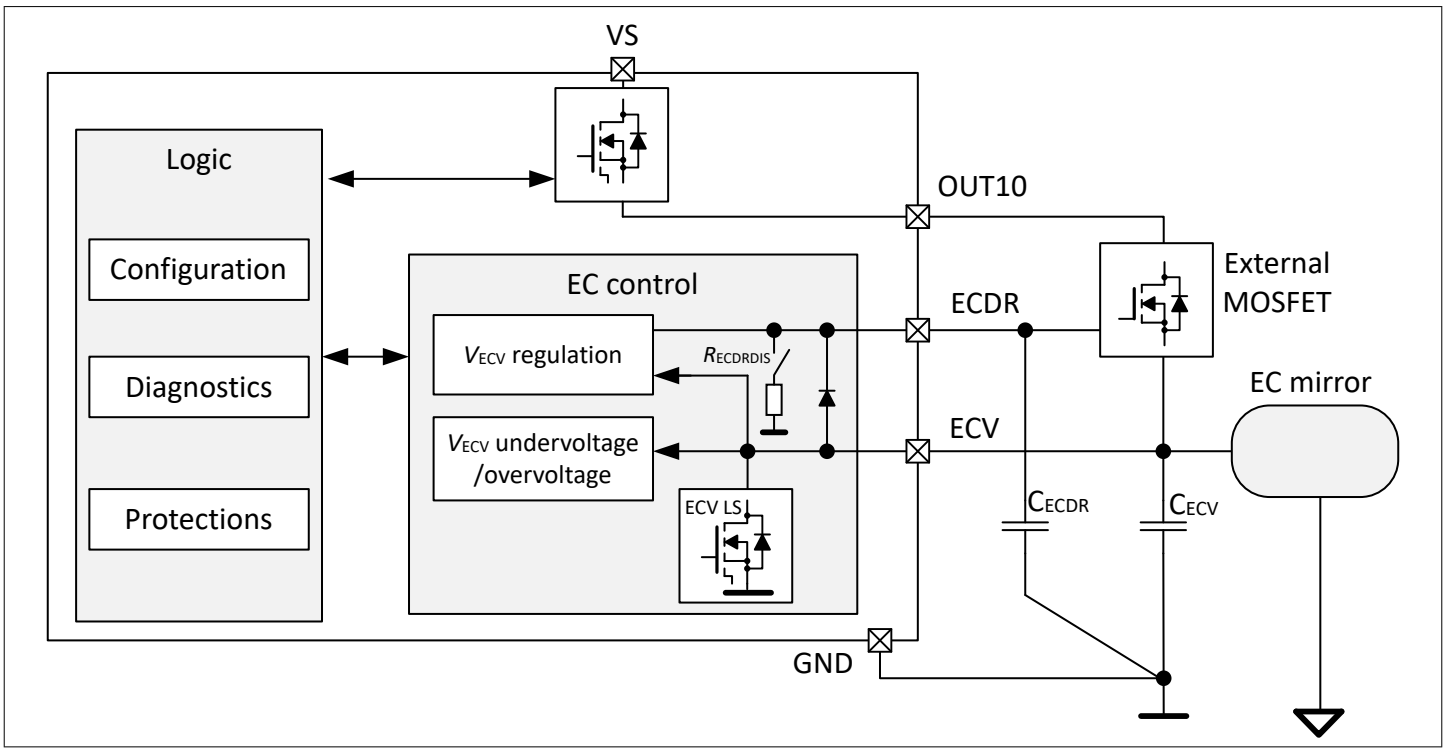


Figure 20 Driver for electrochromic mirror

The ECDR pin controls the gate of an external n-channel MOSFET to regulate the voltage at the ECV pin with a feedback loop.

The drain of the external MOSFET is supplied by OUT10.

The regulation of V_{ECV} is activated and deactivated by bit configuration. Refer to Table 21.

7.1 Deactivated EC control

Conditions	$R_{ECDRDIS}$
ECV is configured as standalone low-side, ECV low-side is enabled	Disconnected
ECV is configured as standalone low-side, ECV low-side is disabled	Connected
ECV and OUT10 are configured as half-bridge	Disconnected

7.2 Activated EC control

When the EC control mode is enabled:

- OUT10 is enabled, independently from the OUT10 control bit
- The PWM control of OUT10 is disabled, independently from the OUT10 control bit
- The CCM setting is disabled, independently from the OUT10 control bit

The target voltage for V_{ECV}, noted V_{TARGET}, is configured by SPI according to Table 32.

Setting	Configuration parameter	Symbol	Nominal range	Unit	Step width	Default	Note
Setting1	Target V_{ECV}	V_{TARGET}	0 to V_{TARGET_MAX1}	V	V_{TARGET_MAX1} / 63	0	–
Setting2	Target V_{ECV}	V_{TARGET}	0 to V_{TARGET_MAX2}	V	V_{TARGET_MAX1} / 63	0	V_{TARGET} is clamped to V_{TARGET_MAX2}

The status of the voltage control loop is reported to the microcontroller:

- The ECV overvoltage bit is set if V_{ECV} - V_{TARGET} > | dV_{ECV_OV} | for t = t_{EC_UVOV}
- The ECV undervoltage bit is set if V_{TARGET} - V_{ECV} > dV_{ECV_UV} for t = t_{EC_UVOV}

The capacitance of the EC mirror can be significant, depending on its size. Therefore, the ECV low-side between ECV and GND allows a fast discharge.

The ECV low-side can be activated for a fast discharge of the EC mirror. Two configurations are possible when the EC control is enabled (Refer to Table 21):

1. If the ECV low-side enable bit is set, then the ECV low-side is activated until V_{ECV} - V_{TARGET} < | dV_{ECV_OV} |.
2. If the ECV low-side enable bit is set, then the ECV low-side is activated independently from V_{ECV}.

***Note**:* *Note: It is not recommended to use the first setting of the fast discharge: the ECV low-side is activated until V_{ECV} - V_{TARGET} < | dV_{ECV_OV} |. This setting leads to repetitive activations and deactivations of the ECV low-side due to the behavior of the electrochromic mirror.*

Table 32 shows the reaction of the EC regulation in case of failure.

Table 32 Behavior of EC control in fault conditions

Failure	EC control	ECV LS	$R_{ECDRDIS}$	OUT10	V_{target}
OUT10 OC bit	On	As configured	On	Off	0 V
OUT10 TSD bit	Off	Off	On	Off	–
VS OV bit	Off	Off	On	Off	–
VS UV bit	Off	Off	On	Off	–
Charge pump UV bit	Off	Off	On	Off	–
Fail safe mode	Off	Off	On	Off	–
V_{DD} UV	Off	Off	On	Off	–

The EC regulation is re-enabled according to the control registers when the status bit related to the detected failure is cleared.

7.3 Electrical characteristics

Electrical characteristics, V_S =5.5 V to 20 V, V_{DD} = 3.0 V to 5.5 V, V_{CP} = V_S+ 7.5 V to V_S + 17 V, T_j = -40°C to +150°C; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Table 33 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Maximum target voltage	V_{TARGET_MAX1}	1.4	1.5	1.6	V	–	P_ECM_1_01
Maximum target voltage	V_{TARGET_MAX2}	1.12	1.2	1.28	V	–	P_ECM_1_02
Differential non linearity	DNL	-1	–	1	LSB	–	P_ECM_1_03
Voltage difference between VTARGET and VECV	dV_{ECV}	-5% - 1LSB	–	+5% + 1LSB	mV	$dV_{ECV} = V_{TARGET} - V_{ECV}$; $\lvert I_{ECDRV} \rvert < 1$ µA	P_ECM_1_04
VECV undervoltage	dV_{ECV_UV}	80	120	140	mV	$dV_{ECV\_UV} = V_{TARGET} - V_{ECV}$ setting ECV UV bit	P_ECM_1_05
VECV overvoltage	dV_{ECV_OV}	-160	-120	-80	mV	$dV_{ECV\_OV} = V_{TARGET} - V_{ECV}$ setting ECV OV bit	P_ECM_1_06
Pull-down resistance ECDR in fast discharge mode or when EC mode is off	$R_{ECDRDIS}$	6.5	10	13.5	kΩ	V_{ECDR} = 0.7 V; EC on and V_{TARGET} = 0V; EC off	P_ECM_1_07
Undervoltage/ overvoltage filter time to status bit set	t_{EC_UVOV}	24	32	40	µs	–	P_ECM_1_09
ECDR max. output voltage	$V_{ECDRmin\_high}$	4.7	–	6.8	V	I_{ECDR} = -10µA	P_ECM_1_10
ECDR max. output voltage	$V_{ECDRmax\_low}$	0	–	0.7	V	I_{ECDR} = 10 µA	P_ECM_1_11
ECDR source current	$I_{ECDR\_source1}$	-100	-50	-10	µA	Low gm ; $V_{TARGET} > V_{ECV}$ + 500 mV; V_{ECDR} = 3.5 V	P_ECM_1_12
ECDR sink current	I_{ECDR_sink1}	10	50	100	µA	Low gm; $V_{TARGET} < V_{ECV}$ - 500 mV, V_{ECDR} = 1 V; V_{TARGET} = 0 V; V_{ECV} = 0.5 V	P_ECM_1_13
ECDR source current	$I_{ECDR\_source2}$	-200	-100	-20	µA	High gm; $V_{TARGET} > V_{ECV}$ + 500 mV; V_{ECDR} = 3.5V	P_ECM_1_14

(table continues...)

Table 33 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ECDR sink current	I_{ECDR_sink2}	20	100	200	µA	High gm; $V_{TARGET} < V_{ECV}$ - 500 mV, V_{ECDR} = 1 V; V_{TARGET} = 0 V; V_{ECV} = 0.5 V	P_ECM_1_15

8 High-side MOSFET driver for mirror heater

This section describes the high-side MOSFET driver for resistive loads such as a mirror heater.

The high-side MOSFET driver is intended to control a n-channel MOSFET for resistive loads such as a mirror heater. This MOSFET driver has the following protection and diagnostic features:

- Short circuit detection to GND in on-state through the monitoring of drain-source voltage of the external MOSFET (V_S - V_{SH})
- Detection of open load conditions and short circuit to VS in off-state

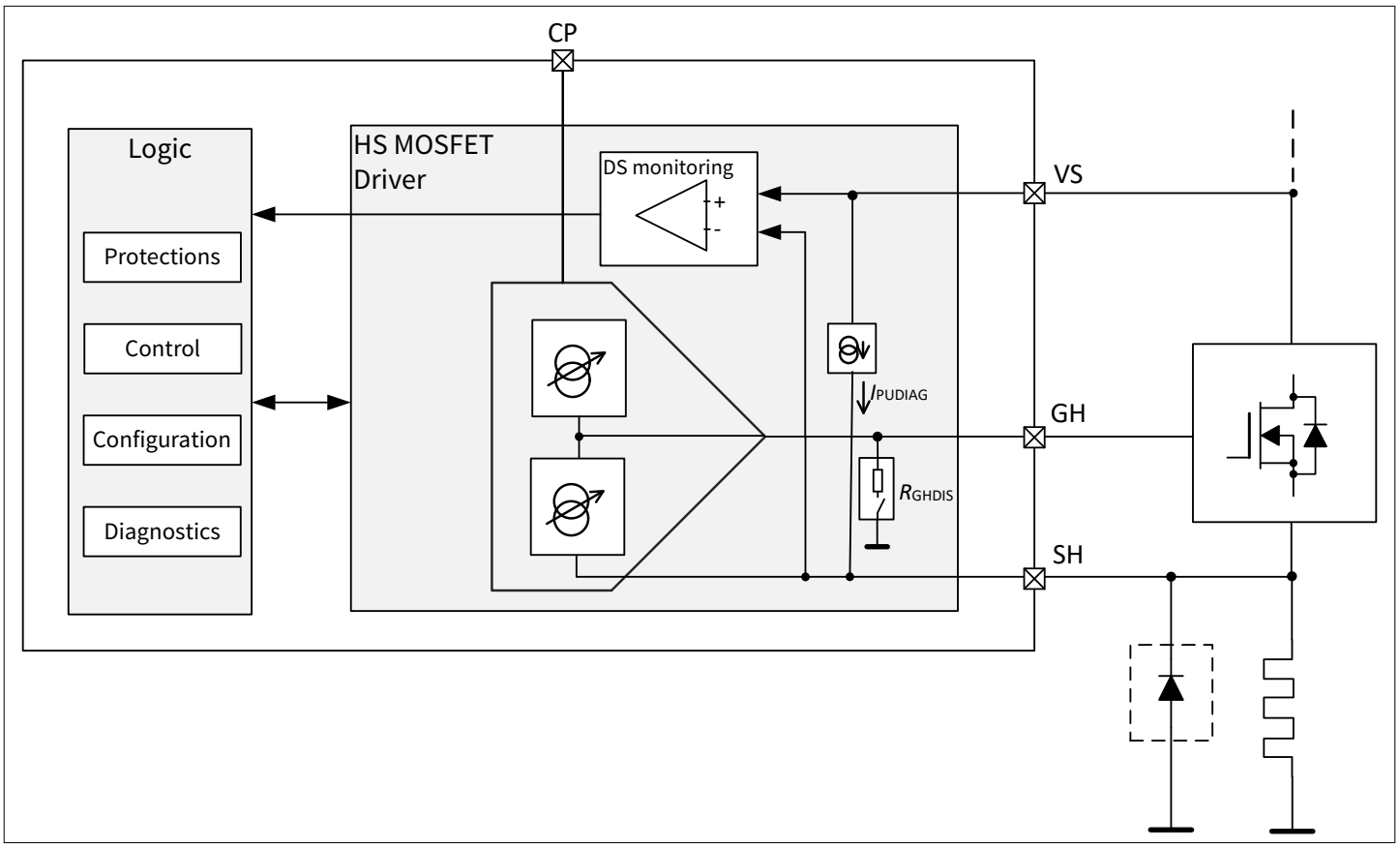


Figure 21 Block diagram of the high-side MOSFET driver

8.1 MOSFET control

The MOSFET driver consists of a current source and a current sink to drive a n-channel MOSFET in high-side configuration.

The high-side MOSFET is activated and deactivated by SPI according to Table 34:

Table 34 Activation of the heater MOSFET

Settings	Configuration	Comments
Setting1	Passive off (default)	The MOSFET gate is discharged to GND through the R_{GHDIS}
Setting2	Active off	The MOSFET gate is actively discharged by the MOSFET driver
Setting3	Active on	The MOSFET gate is charged by the MOSFET driver

When the MOSFET driver is configured as active on:

1. First, the gate of the MOSFET is charged with I_{CHG} during t_{VDS_BLK}
2. After t_{VDS_BLK}, the gate of the MOSFET is kept on with I_{HOLD}

I_{HOLD} is selectabled by SPI: 5 mA nom. (default) or I_{HOLD} = 12.5 mA nom.

When the MOSFET driver is configured as active off:

1. First, the gate of the MOSFET is discharged with I_{DCHG} during $t_{VDS\_BLK\_OFF}$
2. After $t_{VDS\_BLK\_OFF}$, the gate of the MOSFET is kept off with $-I_{HOLD}$

Table 35 Configuration of the charge and discharge currents

SPI configuration	Symbol	Nominal value I_{CHG}	Nominal value I_{DCHG}	Unit	Default	Tolerance
MOSFET driver charge and discharge currents	I_{CHG} , I_{DCHG}	0.5	-0.5	mA	2 / -2	I_{GH_TOL1}
		1	-1			I_{GH_TOL1}
		1.5	-1.5			I_{GH_TOL1}
		2	-2			I_{GH_TOL1}
		2.5	-2.5			I_{GH_TOL1}
		3	-3			I_{GH_TOL1}
		4	-4			I_{GH_TOL1}
		5	-5			I_{GH_TOL2}
		7	-7			I_{GH_TOL2}
		10	-10			I_{GH_TOL2}
		12.5	-12.5			I_{GH_TOL2}

8.2 Drain-source overvoltage

The drain-source of the external MOSFET is monitored to detect an overcurrent condition, for example caused by a short circuit of SH to GND.

The overcurrent for the external MOSFET results in a drain-source overvoltage (DS OV), which is used for the failure detection.

A blank time t_{VDS_BLK} is applied when the device receives the SPI frame to turn on the external MOSFET.

During t_{VDS_BLK}, the drain-source monitoring of the MOSFET is deactivated.

t_{VDS_BLK} is intended to avoid a wrong detection of a DS OV condition during the turn-on phase of the MOSFET.

A DS OV event is detected when the external MOSFET is on and $V_S - V_{SH} > V_{DSOV\_TH}$ for $t = t_{FVDS}$.

The drain-source overvoltage threshold (V_{DSOV_TH}) is configurable according to Table 36.

Table 36 Table drain-source overvoltage threshold

Configuration parameter	Symbol	Nominal value	Unit	Default	Tolerance
DS OV threshold	V_{DSOV_TH}	0.10	V	0.2	V_{DSOVTH_TOL1}
		0.15			V_{DSOVTH_TOL1}
		0.2			V_{DSOVTH_TOL2}
		0.25			V_{DSOVTH_TOL2}
		0.3			V_{DSOVTH_TOL2}
		0.35			V_{DSOVTH_TOL2}
		0.4			V_{DSOVTH_TOL2}
		0.5			V_{DSOVTH_TOL2}
		2			V_{DSOVTH_TOL2}

If a drain-source overvoltage event is detected, the fault reaction is:

- The drain-source overvoltage bit is set and latched
- The gate of the external MOSFET is discharged:
  1. With I_{DCHG} during $t_{VDS\_BLK\_OFF}$
  2. With $-I_{HOLD}$ after $t_{VDS\_BLK\_OFF}$

Attention: ***A decrease of the MOSFET current in combination with stray inductances result in a negative V_{SH}. The application must ensure that the absolute maximum rating of the SH pin is not exceeded, especially in case of the a short circuit with stray inductances. If the application cannot ensure that the absolute maximum ratings of the SH pin are respected, then it is recommended to use a freewheeling diode.***

t_{VDS_BLK} and $t_{VDS\_BLK\_OFF}$ are configurable by SPI according to Table 37:

Table 37 Settings of the blank times

Parameter	Symbol	Nominal value	Unit	Default	Tolerance
DS OV blank time on/off	t_{VDS_BLK} / $t_{VDS\_BLK\_OFF}$	8 / 37 50 / 124	µs	8 / 37	t_{OSC1_TOL}

Clearing the drain-source overvoltage status bits re-enables the external MOSFET (according to the control register).

8.3 Off-state diagnostic

The detection of an open load or a short circuit of SH to VS is realized by the microcontroller while the MOSFET driver is in **active off mode** by monitoring V_{SH} (refer to Table 38).

In active off mode, the pull-up diagnostic current is activated.

Table 38 VSH status bit

V_{SH} status bit	Diagnostic
0	$V_S - V_{SH} > V_{DSOV\_TH}$
1	$V_S - V_{SH} < V_{DSOV\_TH}$

8.4 Electrical characteristics

Electrical characteristics, V_S =5.5 V to 20 V, V_{DD} = 3.0 V to 5.5 V, $V_{CP} = V_S$+ 7.5 V to V_S+ 17 V, T_j = -40°C to +150°C; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Table 39 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High VGS level	V_{GS_H}	9.3	11	11.8	V	$V_{GS\_H} = V_{GH} - V_{SH}$; ext. MOSFET on; $V_{CP} \geq V_S$ +12 V	P_MH_1_01
High VGS level	V_{GS_H}	5	–	–	V	$V_{GH} - V_{SH}$; ext. MOSFET on; $V_{CP} = V_S$ +7.5 V	P_MH_1_02

(table continues...)

Table 39 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VDS OV filter time	t_{FVDS}	3.2	4	4.8	µs	–	P_MH_1_04
VDS OV tolerance	V_{DSOVTH_TOL1}	-30%	–	30%	–	–	P_MH_1_05
VDS OV tolerance	V_{DSOVTH_TOL2}	-20%	–	20%	–	–	P_MH_1_06
Passive GH discharge	R_{GHDIS}	10	20	30	kΩ	–	P_MH_1_08
Pull-up diagnostic current	I_{PUDIAG}	-500	-400	-270	µA	V_{DSOV_TH} = 2 V	P_MH_1_09
IGH tolerance 1	I_{GH_TOL1}	-30	–	30	%	–	P_MH_1_10
IGH tolerance 2	I_{GH_TOL2}	-20	–	20	%	–	P_MH_1_11

9 Serial peripheral interface (SPI)

The device has an SPI interface for the configuration and the diagnostics. This section describes the SPI protocol.

9.1 Functional description

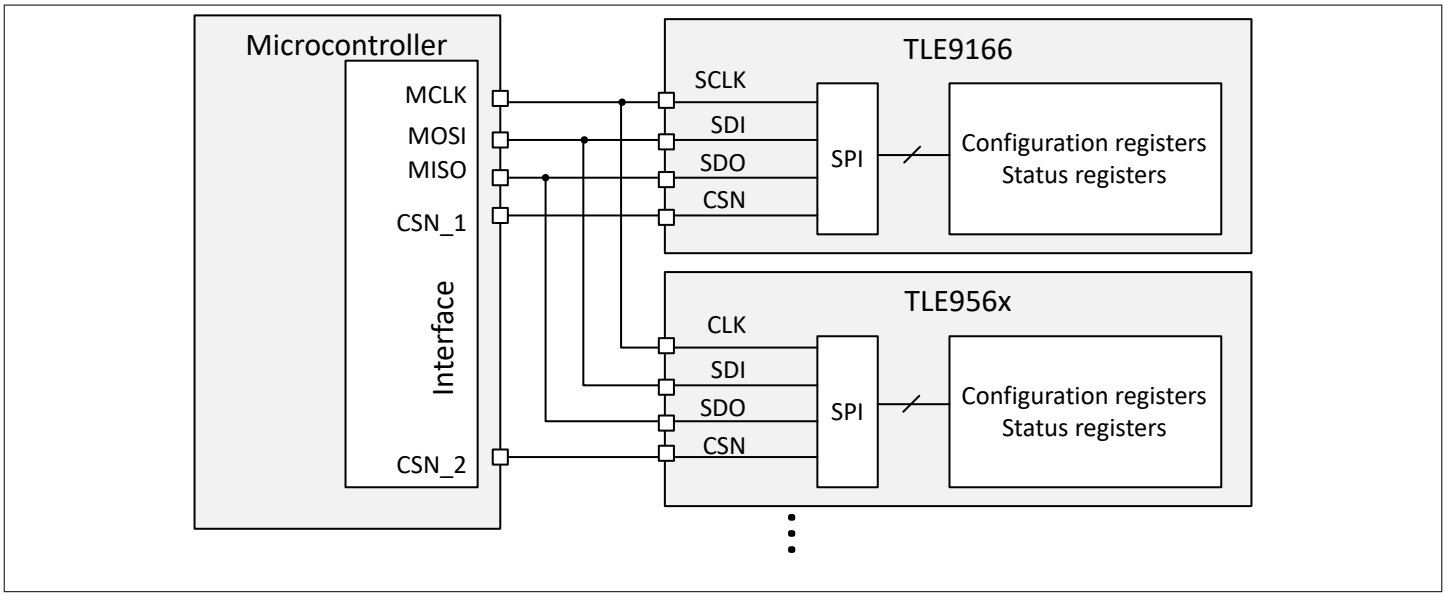


Figure 22 Simplified block diagram: SPI

The input control frame read at the SDI pin is synchronized with the clock signal provided by the microcontroller at the SCLK pin. The output frame of the actual command appears synchronously at the SDO pin (in-frame response).

The SDI data is shifted into the input register with every SCLK falling edge.

The SDO data is shifted out at every SCLK rising edge.

The SPI protocol of the device is not daisy chain capable.

An SPI frame starts by pulling CSN to low and ends by pulling CSN to high.

At the CSN rising edge:

- SDO is set to high impedance
- The received frame at the SDI pin is interpreted during t_{SET}

Therefore, incoming SPI frames are accepted only if CSN is high for t > t_{CSNH} between two SPI frames.

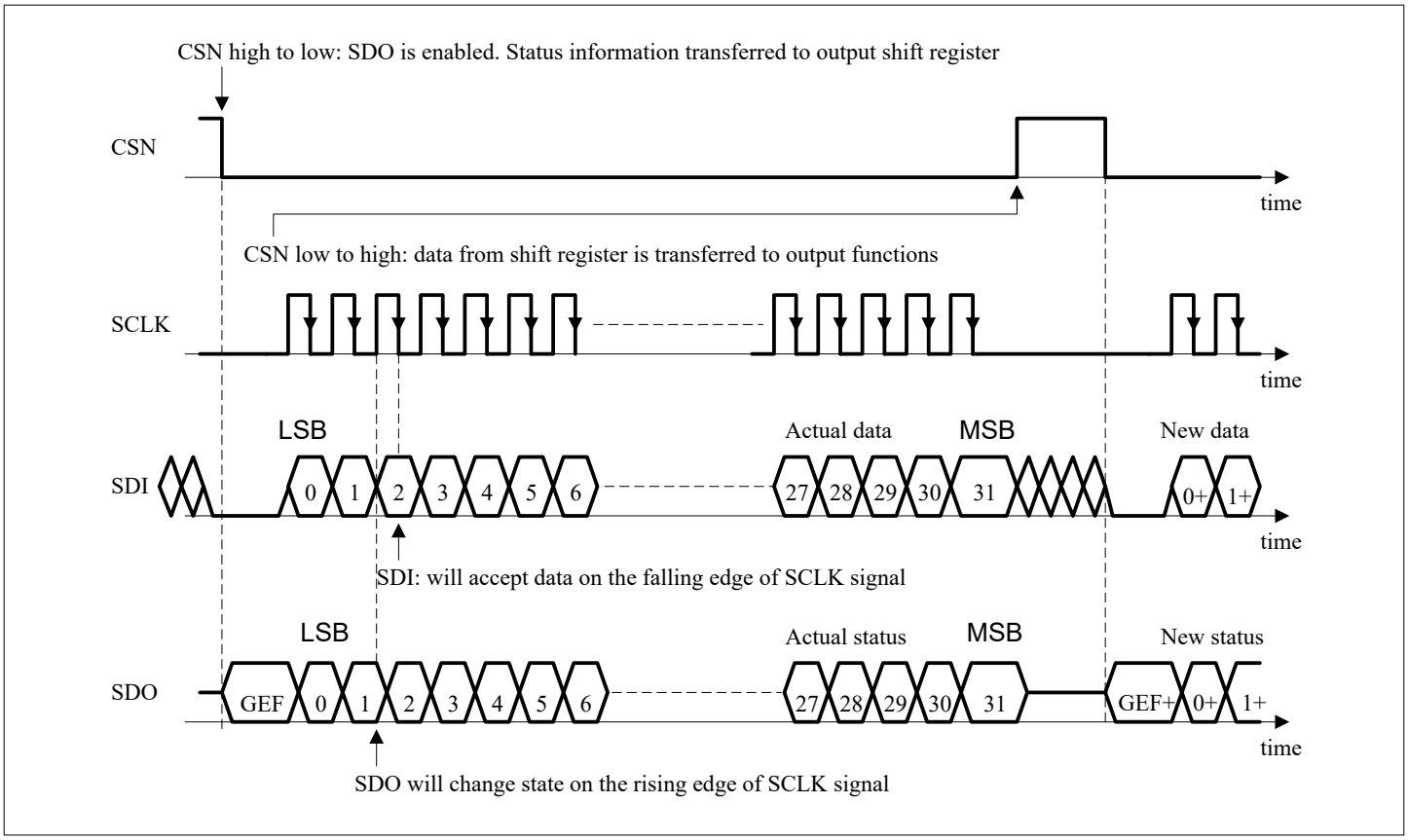


Figure 23 SPI data transfer timing

The SPI has the following characteristics:

- Clock polarity is 0 (first edge = rising edge, second edge = falling edge)
- Clock phase is 1 (shifting data on first edge, sampling data on second edge)

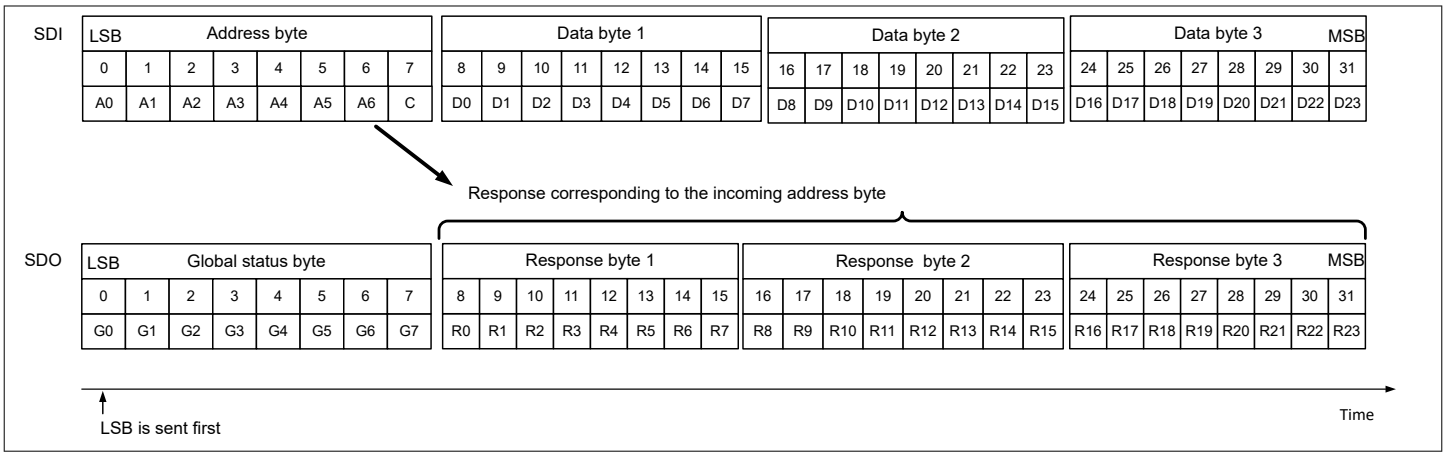


Figure 24 Content of an SPI frame

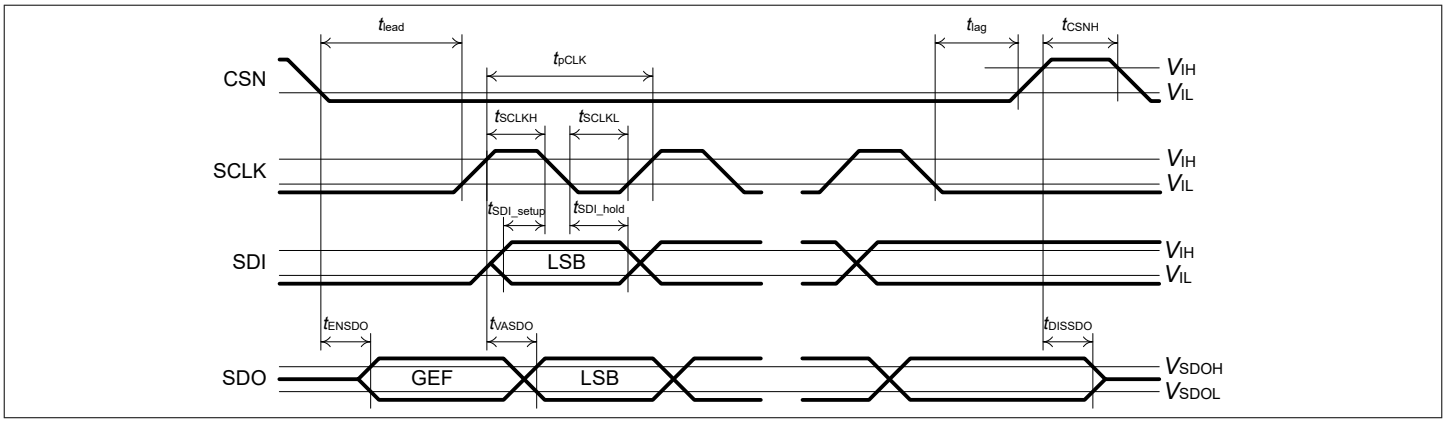


Figure 25 SPI data timing

9.1.1 SPI protocol

SPI communications consist of 32-bit frames. The less significant bit (LSB) is sent first.

9.1.1.1 SDI frame format

A SDI frame consists of:

1. One address byte with: 7 bits for the address followed by 1 command bit "C"
2. Followed by the data byte 1
3. Followed by the data byte 2
4. Followed by the data byte 3

The address byte specifies the target register and the type of command:

- Address of the target register: A[6:0]
- Type of command for **control registers**:
  - "C" = 0: Read only
  - "C" = 1: Write
- Type of command for **status registers**:
  - "C" = 0: Read only
  - "C" = 1: Clear

A clear command clears the complete status register.

9.1.1.2 SDO frame format

The SPI protocol supports an in-frame response: The content of the addressed register is shifted out at SDO within the same SPI frame.

The SDO transmits:

1. The global status byte
2. Followed by the response byte 1
3. Followed by the response byte 2
4. Followed by the response byte 3

9.1.2 Global error flag

The global error flag (GEF bit), allows a fast reporting to the microcontroller:

- In case of a failure condition
- If the device comes from a power-on reset

The GEF (Figure 23) is reported on SDO between the CSN falling edge after t_{ENSDO} and the first SCLK rising edge.

GEF = (HBE) or (PAIRE) or (TSD) or (TW) or (NOT(NPOR)) or (SUPE) or (LE) or (FS) or (SPIE) if MASKOL = MASKTW = 0

- if MASKOL = 1: OL is not reported in GEF
- if MASKTW = 1: TW is not reported in GEF

9.1.3 Global status byte

This global status byte (GSB) provides an overview of the device status while the microcontroller sends the address byte.

The SDO shifts out the GSB (Figure 24) during the first eight SCLK cycles. The GSB reports the following failures:

- G0: Always read as 0
- G1 (INE): Input error
- G2 (TE): Thermal error
- G3 (NPOR): Negated power on reset
- G4 (SUPE) : Supply error
- G5 (LE): Load error
- G6 (FS): Fail safe
- G7 (SPIE): SPI protocol error

The following table shows how failures are reported by GSB and GEF:

Table 40 Failure reported in the global status byte and global error flag

Type of error	Bits of of the GSB	Global error flag
Half-bridge configuration error (HBE) for ECV low-side and OUT10 is detected	INE = 1	1
Pairing error (PAIRE) is detected	INE = 1	1
Thermal shutdown	TE = 1	1
Thermal warning	TE = 1	1 if MASKTW = 0 0 if MASKTW = 1
Power-on reset	**NPOR = 0**	1
Supply error	SUPE = 1	1
Open load	LE =1	1 if MASKOL = 0 0 if MASKOL = 1
Overcurrent	LE = 1	1
Fail safe	FS = 1	1
SPI protocol error	SPIE = 1	1
No error and no power-on reset	TW = 0 TSD = 0 **NPOR = 1** SUPE = 0 LE = 0 FS = 0 SPIE = 0	0

The default value (after power-on reset) of NPOR is 0, therefore the default value of GEF is 1.

INE bit

The input error bit is an or-combination:

- Of the half-bridge configuration error bit for ECV low-side and OUT10
- With the pairing error bit between OUT1 to OUT6

INE = (HBE) or (PAIRE)

TE bit

The thermal error bit bit (TE) is an or-combination of the thermal shutdown and of the thermal warning status bits.
TE = (TSD) OR (TW).

NPOR bit

After a power-on reset, NPOR = 0 until a clear command to the general status register (GENSTAT1) is received.

SUPE bit

The SUPE bit is an or-combination of the VS undervoltage, VS overvoltage and charge pump status bits.

LE bit

If MASKOL = 0: LE = (or-combination of the bits in the overload status register) or (or-combination of the bits in the open load status register). If MASKOL = 1: LE = or-combination of the bits in the overload status register

FS bit

FS indicates an operation in fail safe mode.

9.1.4 SPI protocol error detection

The microcontroller can supervise the data integrity received by the SDI pin by monitoring the SPI error bit (SPIE).

An SPI protocol error is reported if one of the following conditions is detected:

- The number of SCLK clock pulses received when CSN is low is neither 0 nor 32
- The microcontroller sends an SPI command to an unused address
- The microcontroller sends a clear command to address 0x7F
- A clock polarity error is detected: The incoming clock signal was high during CSN rising or falling edges
- An SPI write command to change the value of a control bit in fail safe mode, with the exception of the device enable bit

If an SPI protocol error is detected during a given frame, the microcontroller can read the SPI error bit in the next SPI communication

SPIE is automatically reset when a valid SPI command is received.

For a correct SPI communication:

- SCLK must be low for a minimum t_{BEF} before CSN falling edge and t_{lead} after CSN falling edge
- SCLK must be low for a minimum t_{lag} before CSN rising edge and t_{BEH} after CSN rising edge

9.2 Electrical characteristics

Electrical characteristics, V_S =5.5 V to 20 V, V_{DD} = 3.0 V to 5.5 V, V_{CP} = V_S+ 7.5 V to V_S+ 17 V, T_j = -40°C to +150°C; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Table 41 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI Interface							
Maximum SPI frequency	$f_{SPI,max}$	–	–	6	MHz	–	P_SPI_1_01
SDI, SCLK, CSN and PWM							
High input voltage threshold	V_{IH}	–	–	0.75 x V_{DD}	V	–	P_SPI_1_02
Low input voltage threshold	V_{IL}	0.25 x V_{DD}	–	–	V	–	P_SPI_1_03
Hysteresis of input voltage	V_{IHY}	100	–	–	mV	–	P_SPI_1_04
Pull-up resistor at pin CSN	R_{PU_CSN}	20	40	80	kΩ	V_{CSN} = 0.75 x V_{DD}	P_SPI_1_05
Pull-down resistor at pin SDI, SCLK and PWM	R_{PD_SDI}, R_{PD_SCLK}, R_{PD_PWM}	20	40	80	kΩ	V_{SDI} = V_{SCLK} = V_{PWM} = 0.25 x V_{DD}	P_SPI_1_06
Input capacitance at pin CSN, SDI or SCLK	C_I	–	–	15	pF	V_{CSN} = V_{SDI} = V_{SCLK} = V_{DD}	P_SPI_1_07
SDO							
High output voltage level	V_{SDOH}	0.8 x V_{DD}	–	–	V	I_{SDOH} = -2 mA	P_SPI_2_01
Low output voltage level	V_{SDOL}	–	–	0.2 x V_{DD}	V	I_{SDOL} = 2 mA	P_SPI_2_02
Tri-state Leakage Current	I_{SDOLK}	-10	–	10	µA	V_{CSN} = V_{DD} 0 V < V_{SDO} < V_{DD}	P_SPI_2_03
Tri-state input capacitance	C_{SDO}	–	–	15	pF	–	P_SPI_2_04
SDI timing							
SCLK period	t_{pCLK}	160	–	–	ns	–	P_SPI_3_01
SCLK high time	t_{SCLKH}	70	–	–	ns	–	P_SPI_3_02
SCLK low time	t_{SCLKL}	70	–	–	ns	–	P_SPI_3_03
SCLK low before CSN Low	t_{BEF}	70	–	–	ns	–	P_SPI_3_04
CSN setup time	t_{lead}	160	–	–	ns	–	P_SPI_3_05
SCLK setup time	t_{lag}	160	–	–	ns	–	P_SPI_3_06
SCLK low after CSN high	t_{BEH}	70	–	–	ns	–	P_SPI_3_07

(table continues...)

Table 41 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SDI setup time	t_{SDI_setup}	60	–	–	ns	–	P_SPI_3_08
SDI hold time	t_{SDI_hold}	40	–	–	ns	–	P_SPI_3_09
Input signal rise time at pin SDI, SCLK, CSN	t_{rIN}	–	–	20	ns	–	P_SPI_3_10
Input signal fall time at pin SDI, SCLK, CSN	t_{fIN}	–	–	20	ns	–	P_SPI_3_11
Minimum CSN high time	t_{CSNH}	3	–	–	µs	–	P_SPI_3_12
SDO timing							
SDO rise time	t_{rSDO}	–	30	40	ns	C_{load} = 25 pF V_{SDO} < 0.2 x V_{DD} to V_{SDO} > 0.8 x V_{DD}	P_SPI_4_01
SDO fall time	t_{fSDO}	–	30	40	ns	C_{load} = 25 pF, V_{SDO} < 0.8 x V_{DD} to V_{SDO} > 0.2 x V_{DD}	P_SPI_4_02
SDO enable time after CSN falling edge	t_{ENSDO}	–	–	90	ns	Low impedance	P_SPI_4_03
SDO disable time after CSN rising edge	t_{DISSDO}	–	–	90	ns	High impedance	P_SPI_4_04
Duty cycle of incoming clock at SCLK	$duty_{SCLK}$	45	–	55	%	–	P_SPI_4_05
SDO valid time	t_{VASDO}	–	–	45	ns	V_{SDO} < 0.2 x V_{DD} V_{SDO} > 0.8 x V_{DD} C_{load} = 25 pF	P_SPI_4_06

10 Application information

The following simplified application examples are given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the real application.

10.1 Application diagram

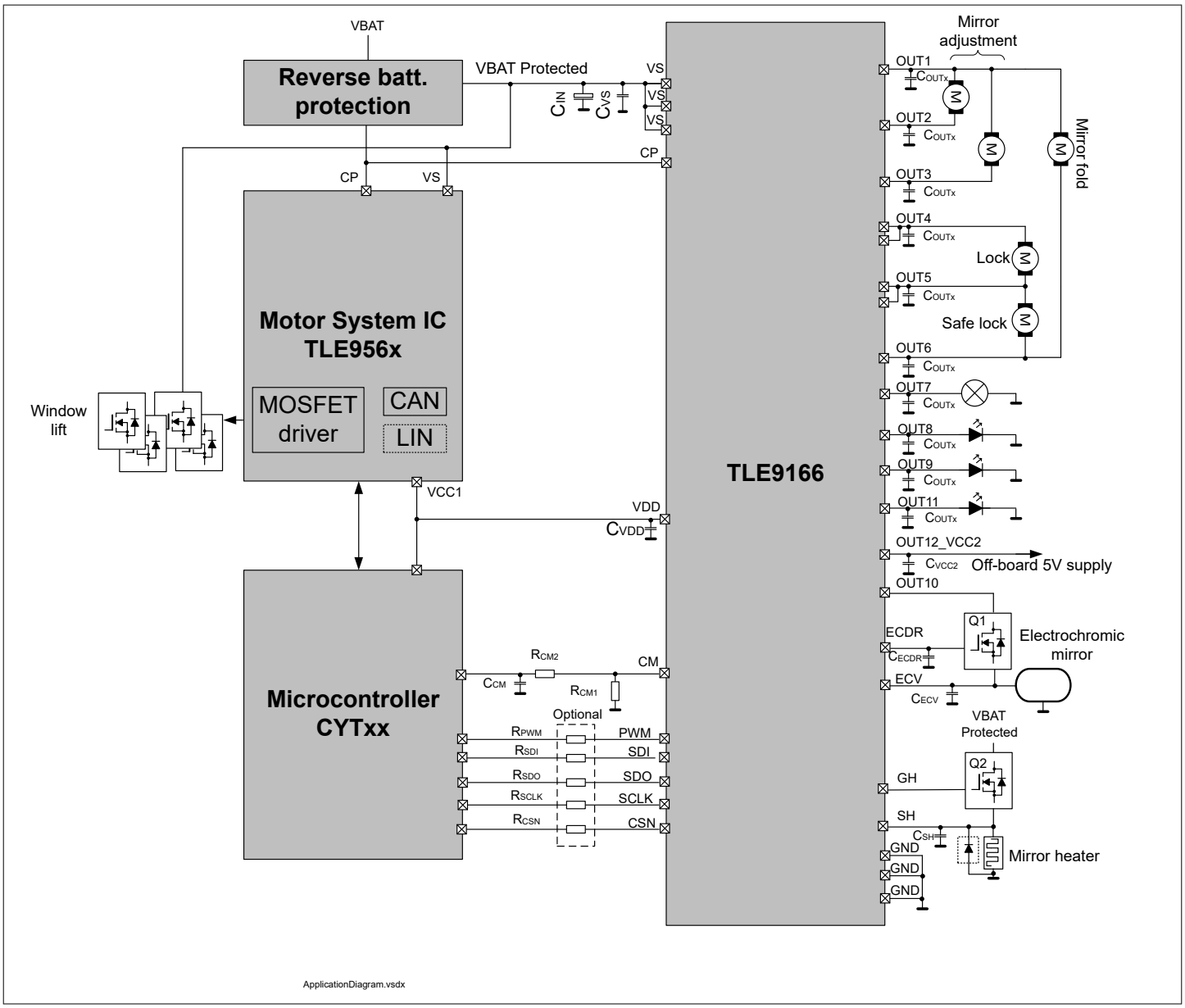


Figure 26 Simplified application diagram

Table 42 Bill of material

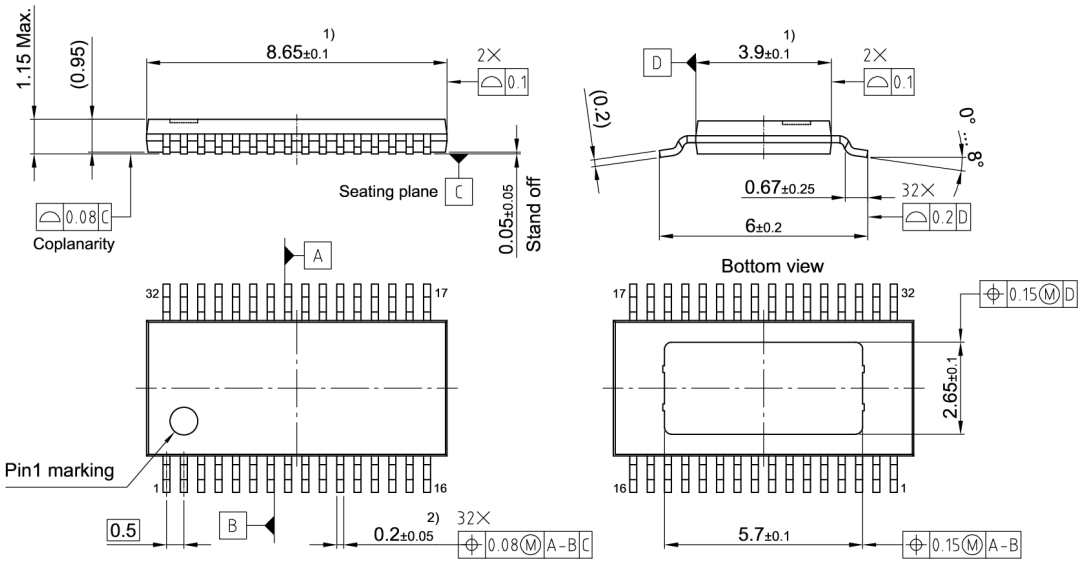
Reference	Nominal value	Purpose / comment
Capacitors		
C_{OUTx}	22 nF, 50 V	ESD protection as required by the application
C_{SH}	Ceramic	To be placed close to the connector

(table continues...)

Table 42 (continued) Bill of material

Reference	Nominal value	Purpose / comment
C_{ECV}	220 nF, 50 V Ceramic	Stability of EC control To be placed close to Q1
C_{ECDR}	4.7 nF, 50V Ceramic	Stability of EC control To be placed close to Q1
C_{VCC2}	2.2 µF, 16V Ceramic	Blocking capacitor. Min. 470 nF for stability. Required if OUT12_VCC2 is configured as voltage regulator.
C_{VS}	100 nF, 50 V Ceramic	Filter capacitor for high frequency noise
C_{IN}	Electrolytic capacitor. To be dimensioned according to the motors	Buffer capacitor for motor supply The value depends on the motors characteristics
C_{VDD}	100 nF, 16 V Ceramic	Filter capacitor for high frequency noise
C_{CM}	10 nF, 16V	Builds a low pass filter together with R_{CM2}
Resistors		
R_{CM1}	1 kΩ to 10 kΩ	For current monitoring
R_{CM2}	1 kΩ	Builds a low pass filter together with C_{CM}
R_{CSN} R_{PWM}	1 kΩ	Decoupling resistor Optional
R_{SDI}, R_{SDO}, R_{SCLK}	330 Ω	Decoupling resistors and for emission purpose Optional
Diode		
D_1	–	A free-wheeling diode between SH and GND is recommended if V_{SH} violates the device absolute maximum rating of the SH pin, for example during the fast turn-off of the external MOSFET in combination with cable stray inductances. The worst case can occur in short circuit condition with stray inductances.

11 Package outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊕]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 27 Package outline PG-TSDSO-32

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e. lead-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

12 Revision history

Document version	Date of release	Description of changes
Rev. 1.01	2025-02-17	• Document confidentiality updated
Rev. 1.00	2024-09-12	• First release

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