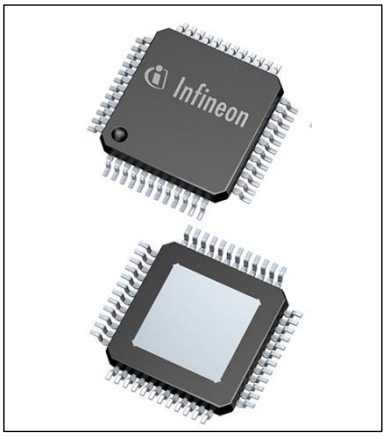
TLE9241QU

Transmission IO IC



Features

- Four input interfaces for two-wire Hall Effect position sensors
  - Short to supply protection
  - Overtemperature protection
  - Sensor state status available by SPI
- Four input interfaces for two-wire Hall Effect speed sensors
  - Digital output for speed and direction sensing
  - Further features set see position sensors above
- Two high-side gate drive channels
  - Short circuit protection
  - Programmable overcurrent threshold
  - Output state status available by SPI
- A high-side gate drive channel for driving n-channel MOSFETs in anti-serial configuration
  - Reverse polarity protected power switch
- Integrated charge pump
- 16 bit SPI interface
- Green Product (RoHS-compliant)

Potential applications

- Automatic Transmission Control Modules
- Powertrain Control Modules

Product validation

- Qualified for automotive applications
- Product validation according to AEC-Q100

Description

The TLE9241QU is an integrated circuit (IC) intended for use in automatic transmission control modules. Two gate drive outputs are included for controlling a reverse polarity protected high-side switch typically used to switch off power to the control module while the module is in a sleep state. Two high-side gate drive channels are also included for controlling two “safety” switches. These switches are typically used to provide power to the transmission solenoids. The device also provides interfaces for eight two-wire Hall Effect sensors, four of which can be used with position sensors and four which can be used with either position or speed sensors.

Type	Package	Marking
TLE9241QU	PG-TQFP-48	TLE9241QU

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1 Block diagram

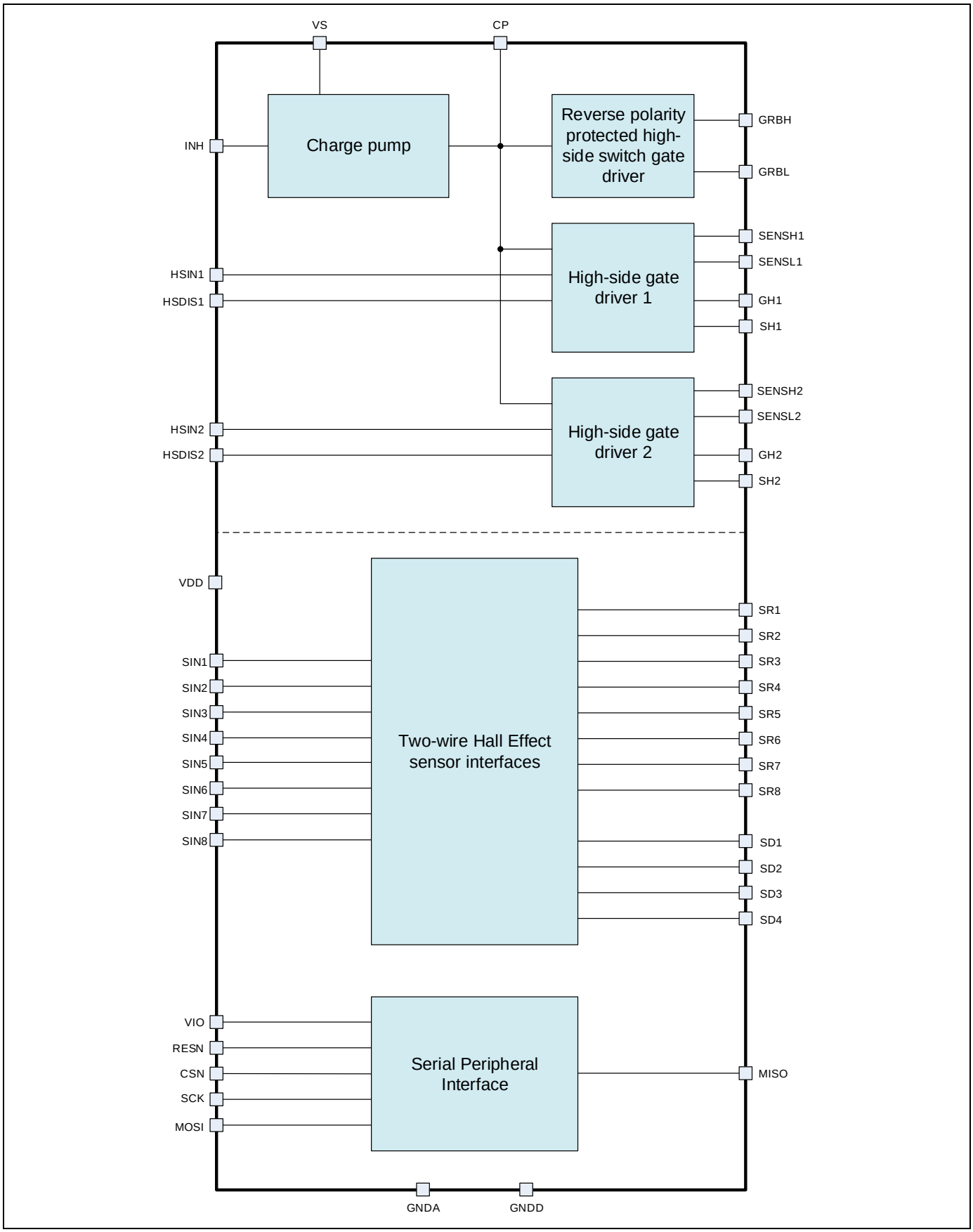

Figure 1 Block diagram

2 Pin configuration

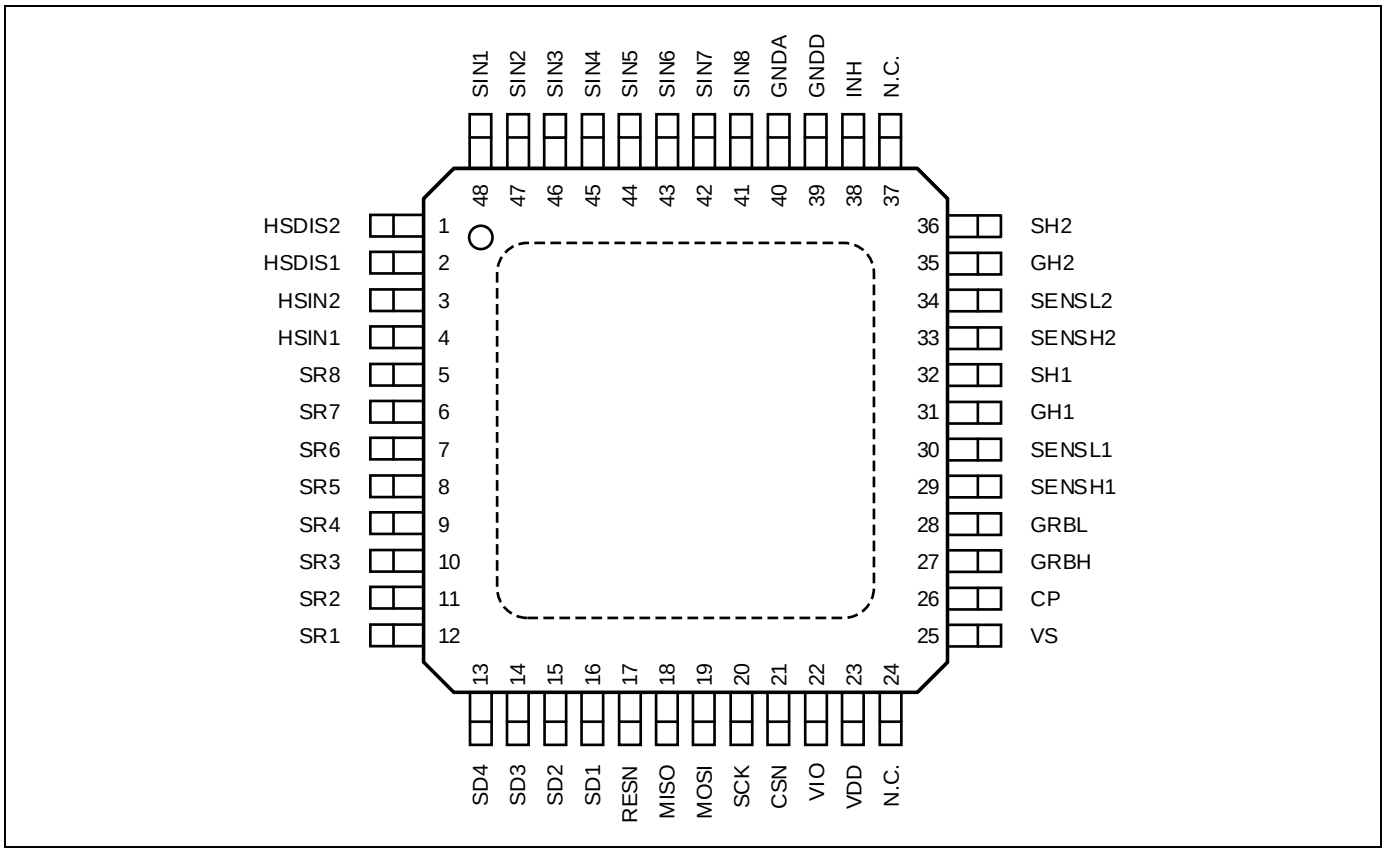

Figure 2 Pin configuration

2.1 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Pin Name	Function
1	HSDIS2	High-side disable pin channel 2
2	HSDIS1	High-side disable pin channel 1
3	HSIN2	High-side control input channel 2
4	HSIN1	High-side control input channel 1
5	SR8	Hall effect speed sensor analogue output channel 8
6	SR7	Hall effect speed sensor analogue output channel 7
7	SR6	Hall effect speed sensor analogue output channel 6
8	SR5	Hall effect speed sensor analogue output channel 5
9	SR4	Hall effect speed sensor analogue output channel 4
10	SR3	Hall effect speed sensor analogue output channel 3
11	SR2	Hall effect speed sensor analogue output channel 2
12	SR1	Hall effect speed sensor analogue output channel 1
13	SD4	Hall effect speed sensor digital output channel 4
14	SD3	Hall effect speed sensor digital output channel 3
15	SD2	Hall effect speed sensor digital output channel 2
16	SD1	Hall effect speed sensor digital output channel 1
17	RESN	Reset input (low active)
18	MISO	SPI master in slave out
19	MOSI	SPI master out slave in
20	SCK	SPI serial clock
21	CSN	SPI chip select (low active)
22	VIO	IO supply voltage. External connection to V_{IO}
23	VDD	5 V supply Input. External connection to V_{DD}
24	N.C.	Not connected
25	VS	Supply input (reverse protected battery connection). External connection to V_S
26	CP	Charge pump capacitor connection
27	GRBH	Power switch gate high
28	GRBL	Power switch gate low
29	SENSH1	Overcurrent sense resistor connection high channel 1
30	SENSL1	Overcurrent sense resistor connection low channel 1
31	GH1	Gate of external high-side FET channel 1
32	SH1	Source of external high-side FET channel 1
33	SENSH2	Overcurrent sense resistor connection high channel 2
34	SENSL2	Overcurrent sense resistor connection low channel 2
35	GH2	Gate of external high-side FET channel 2
36	SH2	Source of external high-side FET channel 2
37	N.C.	Not connected
38	INH	Inhibit input (LOW = inhibit, HIGH = device enabled)
39	GNDD	Digital Ground
40	GNDA	Analogue Ground
41	SIN8	Hall effect sensor input channel 8
42	SIN7	Hall effect sensor input channel 7
43	SIN6	Hall effect sensor input channel 6
44	SIN5	Hall effect sensor input channel 5
45	SIN4	Hall effect sensor input channel 4

Pin configuration

Pin	Pin Name	Function
46	SIN3	Hall effect sensor input channel 3
47	SIN2	Hall effect sensor input channel 2
48	SIN1	Hall effect sensor input channel 1

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

All voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage							
VS supply voltage	V_S	-0.3		40	V		P_3.1.1
VDD, VIO supply voltage	V_{DD}, V_{IO}	-0.3		5.5	V		P_3.1.2
Voltage range GRBH pin	V_{GRBH}	-14		55	V		P_3.1.3
Voltage range GRBL, CP, GHx pin	V_{GRBL}, V_{CP}, V_{GHX}	-0.3		55	V		P_3.1.4
Voltage range INH pin	V_{INH}	-0.3		40	V		P_3.1.5
Voltage range SENSHx, SENSLx, SHx	V_{SENSHX}, V_{SENSLX}, V_{SHX}	-5.5		40	V		P_3.1.6
Difference SENSHx-SENSLx	V_{SENS_DIFF}	-0.3		5.5	V		P_3.1.7
Voltage range at HSINx, HSDISx, CSN, SCK, MOSI, RESN	V_{DIG_IN}	-0.3		V_{DD} + 0.3	V		P_3.1.8
Voltage range MISO pin	V_{MISO}	-0.3		V_{IO} + 0.3	V		P_3.1.9
Voltage range at SINx	V_{SINX}	-0.3		40	V		P_3.1.10
Voltage range at SRx	V_{SRX}	-0.3		5.5	V		P_3.1.11
Voltage range at SDx	V_{SDX}	-0.3		V_{DD} + 0.3	V		P_3.1.12
Ground voltage offset GNDA vs. GNDD	V_{GNDA}	-0.3		0.3	V		P_3.1.13
Temperature							
Junction temperature	T_j	-40		150	°C		P_3.1.14
ESD							
ESD susceptibility HBM, pins VS and SINx vs. GND	$V_{ESD,HBM,VS}$; $V_{ESD,HBM,SINX}$	-4		4	kV	HBM [2)]	P_3.1.15
ESD susceptibility HBM, all pins	$V_{ESD,HBM}$	-2		2	kV	HBM [2) 3)]	P_3.1.16
ESD susceptibility CDM, corner pins	$V_{ESD,CDM,1;12;13;24;25;36;37;48}$	-750		750	V	CDM [4)]	P_3.1.17
ESD susceptibility CDM, all pins	$V_{ESD,CDM}$	-500		500	V	CDM [4)]	P_3.1.18

[1)] Not subject to production test, specified by design.
[2)] Human Body Model "HBM" AEC Q100-002
[3)] Pin SENSH1: +/- 1.5 kV
[4)] Charged Device Model "CDM" AEC Q100-011

Notes:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VS supply voltage range	V_S	5.5		40	V		P_3.2.1
VDD supply voltage range	V_{DD}	4.75	5	5.25	V		P_3.2.2
VIO supply voltage range	V_{IO}	3.1		5.25	V		P_3.2.3

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Electrical characteristics

Table 4 Electrical characteristics

V_S = 5.5 V to 40 V, V_{DD} = 4.75 V to 5.25 V, V_{IO} = 3.1 V to 5.25 V, T_j = -40°C to +150°C, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Central functions							
VDD supply current	I_{DD}		7.5	10.0	mA	[2]	P_3.2.4
VIO supply current	I_{IO}			0.5	mA		P_3.2.5
VS supply current	I_S		4	6	mA	[2]	P_3.2.6
VS quiescent current	I_{S1}			10	µA	INH = LOW, V_S < 13 V, T_j < 50°C [1]	P_3.2.7
VS quiescent current	I_{S2}			15	µA	INH = LOW, V_S < 13 V, T_j < 150°C	P_3.2.7a
VDD undervoltage reset threshold	V_{DDUV}	3.0		3.5	V		P_3.2.8
Charge pump undervoltage threshold vs. VS	V_{CPUV_rise}	7.0		9.0	V	V_{CP} rising	P_3.2.9
Charge pump undervoltage threshold vs. VS	V_{CPUV_fall}	5.5		6.8	V	V_{CP} falling	P_3.2.9a
Charge pump undervoltage hysteresis	V_{CPUV_hyst}	1		3	V		P_3.2.16
Charge pump output current VCP = 9 V	I_{CP9_low}	40			µA	V_S = 5.5 V [1]	P_3.2.12
Charge pump output current VCP = 10 V	I_{CP10_nom}	40			µA	V_S = 12.0 V [1]	P_3.2.12a
Charge pump output current VCP = 0 V	I_{CP0_low}	300			µA	V_S = 5.5 V [1]	P_3.2.12b
Charge pump output current VCP = 0 V	I_{CP0_nom}	300			µA	V_S = 12.0 V [1]	P_3.2.12c
Charge pump overvoltage clamp vs. VS	V_{CL_CP}		11	15	V	I_{CP} = 1 mA	P_3.2.10
Charge pump frequency	f_{CP}		16.0		MHz	[1]	P_3.2.11
Overtemperature shutdown threshold	T_{SD}	160	175	190	°C		P_3.2.13
Main oscillator frequency	f_{OSC}		8.25		MHz		P_3.2.14
Digital input pins							
Low level input voltage HSINx, HSDISx, RESN, CSN, MOSI, SCK	V_{IL}			0.8	V		P_3.2.17
High level input voltage HSINx, HSDISx, RESN, CSN, MOSI, SCK	V_{IH}	2.0			V		P_3.2.18
Hysteresis voltage HSINx, HSDISx, RESN, CSN, MOSI, SCK	V_{HYS}	75	150		mV	[1]	P_3.2.19
HSIN1, HSIN2, RESN, MOSI, SCK pull down current	I_{PD}	30	50	70	µA		P_3.2.20
HSDIS1, HSDIS2, CSN pull up current	I_{PU}	-70	-50	-30	µA		P_3.2.21

[1] Not subject to production test, specified by design.

[2] During discharge of an inductive load, i.e. SH1/2 < 0 V: I_{DD} < 15 mA; I_S < 20 mA.

4 Reverse polarity protected high-side switch gate driver

The device includes two gate drive outputs for controlling external MOSFETs for reverse battery protection and system power supply.

The device includes a charge pump for driving the gates of the external MOSFETs.

The state of the reverse protected power switch gate drive outputs are controlled by the input pin INH.

If the power switch is in the “off” state, the gate drive outputs GRBL is driven to ground potential. The gate drive output GRBH will remain near the battery voltage.

4.1 Electrical characteristics

Table 5 Electrical characteristics

V_S = 5.5 V to 40 V, V_{DD} = 4.75 V to 5.25 V, V_{IO} = 3.1 V to 5.25 V, T_j = -40°C to +150°C, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reverse protected switch							
Low level input voltage INH	V_{IL_INH}			1.0	V		P_4.1.1
High level input voltage INH	V_{IH_INH}	3.0			V		P_4.1.2
Input hysteresis INH	V_{HYS_INH}	75	150		mV		P_4.1.3
INH pull down resistor to GND	R_{PD_INH}	0.5	1.25	2.0	MΩ	V_{INH} = 1.0 V	P_4.1.4
Power switch activation time	T_{ON_PS}			15	ms	time until ext. MOSFET is switched on after INH signal assertion [1) 2)]	P_4.1.5
Power switch de-activation time	T_{OFF_PS}			15	ms	time until ext. MOSFET is switched off after INH signal de-assertion	P_4.1.6
High level output voltage GRBH vs. VS	V_{OH_GRBH1}	6.75		15	V	V_S = 5.5 V, I_{GRBH} < 40 µA	P_4.1.7
High level output voltage GRBH vs. VS	V_{OH_GRBH2}	8		15	V	V_S > 12 V, I_{GRBH} < 40 µA	P_4.1.8
Low level output voltage GRBH vs. VS	V_{OL_GRBH}	-2		1	V		P_4.1.9
Low level output voltage GRBL	V_{OL_GRBL}	-2		1	V		P_4.1.10
DC output current GRBx	I_{GRBX}		25		µA		P_4.1.11
Overvoltage clamp GRBH to VS	V_{CL_GRBH}	-21	-19	-17	V		P_4.1.12

[1)] Not subject to production test, specified by design.

[2)] For more details on activation time please see the User Manual.

5 High-side gate drive channels

The device includes two high-side pre-driver channels for driving external normal level n-channel MOSFETs.

The device includes a charge pump for driving the gates of the two external MOSFETs. The state of the gate drive outputs are controlled by a pair of input pins for each channel.

The states of the input pins HSIN1, HSIN2, HSDIS1 and HSDIS2 can be verified by reading the appropriate register.

The status of the high-side driver output is monitored by the device and is accessible in a register.

An external shunt resistor is required in the high-side driver circuit for overcurrent detection. The voltage drop across this resistor is monitored by the device, and the driver is turned off if the overcurrent threshold voltage is exceeded. The overcurrent detection function includes a fixed delay timer.

The value of the overcurrent threshold can be configured by writing to the overcurrent threshold register.

If an overcurrent fault is detected, the channel is turned off and a high-side overcurrent fault flag is set.

The HSINx signals can be controlled by SPI instead of the HSINx pin if configured accordingly.

5.1 Electrical characteristics

Table 6 Electrical characteristics

V_S = 5.5 V to 40 V, V_{DD} = 4.75 V to 5.25 V, V_{IO} = 3.1 V to 5.25 V, T_j = -40°C to +150°C, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High-side driver							
High-side blanking time	T_{BL_HS}	4	8	12	µs		P_5.1.6
SHx output state threshold	V_{TH_SHX}		V_S / 2		V		P_5.1.7
SHx pull down current	I_{PD_SHX}		200	300	µA		P_5.1.8
Short to battery filter time	T_{FL_STB}		64		µs		P_5.1.9
High level output GHx vs. SHx	V_{OH_HS1}	6.75		15	V	V_S = 5.5 V, I_{GHX} < 25 µA	P_5.1.10
High level output GHx vs. SHx	V_{OH_HS2}	8		15	V	V_S > 12 V, I_{GHX} < 25 µA	P_5.1.11
Low level output GHx vs. SHx	V_{OL_HS}	-2		1	V		P_5.1.12
Turn on delay time	T_{ON_HS}			100	µs	From command to 80%, Q_{GHX} = 20 nC [1]	P_5.1.13
Turn off delay time	T_{OFF_HS}			100	µs	From command to 20%, Q_{GHX} = 20 nC [1]	P_5.1.14
Gate driver output current	I_{GHX}	2	4	6	mA	V_S = 5 V, V_{CP} - V_S = 10 V, V_{SHX} = 0 V, V_{GHX} = 5 V	P_5.1.15
GHx negative clamp voltage	V_{CL_GHX}	-1			V		P_5.1.16
SHx bias current	I_{OFF_SHX}			50	µA	Channel off	P_5.1.17
Overcurrent filter time	T_{FLT_OC}		4		µs		P_5.1.18
Overcurrent threshold 000_b	I_{OC0}	15	25	35	mV		P_5.1.19
Overcurrent threshold 001_b	I_{OC1}	40	50	60	mV		P_5.1.20
Overcurrent threshold 010_b	I_{OC2}	65	75	85	mV		P_5.1.21
Overcurrent threshold 011_b	I_{OC3}	90	100	110	mV		P_5.1.22
Overcurrent threshold 100_b	I_{OC4}	115	125	135	mV		P_5.1.23
Overcurrent threshold 101_b	I_{OC5}	140	150	160	mV		P_5.1.24
Overcurrent threshold 110_b	I_{OC6}	165	175	185	mV		P_5.1.25
Overcurrent threshold 111_b	I_{OC7}	190	200	210	mV		P_5.1.26

[1] Not subject to production test, specified by design.

6 Two wire Hall Effect sensor interfaces

The device includes eight interface channels for two-wire Hall Effect sensors. Four of the channels include a digital output.

The channels detect the supply current of the two-wire sensor. Each channel provides a path from the ground pin of the sensor to ground.

The analogue output of each channel at the pin SRx is a current sink proportional to the detected sensor current.

An internal register contains the detected state of each sensor channel.

The device includes four digital outputs, SD1-4. The state of the output pin is the same as the value of the respective bit in the sensor state register.

Each channel is short-circuit protected by a current limitation function. In a short circuit condition, the current flowing into the SINx input pin is actively limited. There is no overcurrent shutdown function for the sensor interface channels.

Each sensor interface channel includes overtemperature shutdown.

If the overtemperature fault is active and simultaneously overcurrent is detected, the affected channel is disabled. Also, the SRx pin is driven to a voltage near to ground potential, and the SDx pin is driven HIGH.

Each channel can be individually disabled.

6.1 Electrical characteristics

Table 7 Electrical characteristics

V_S = 5.5 V to 40 V, V_{DD} = 4.75 V to 5.25 V, V_{IO} = 3.1 V to 5.25 V, T_j = -40°C to +150°C, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Hall sensor interface							
Ratio of sensor input current vs. SRx pin current	k_{ilis}	19	20	21		For 4 mA < I_{SINX} < 20 mA	P_6.1.1
Voltage drop SINx vs. GND	V_{DO_SINX}			0.4	V	I_{SINX} = 20 mA	P_6.1.2
Voltage drop SINx vs. GND (open circuit)	$V_{DO\_OC\_SINX}$			0.2	V	I_{SINX} = 0 mA[1)]	P_6.1.19
Short to supply threshold current	I_{CL_SINX}	20	30	40	mA		P_6.1.3
SINx current with interface disabled	I_{DIS_SINX}			50	µA		P_6.1.4
SRx current with interface disabled	I_{DIS_SRX}			2.5	µA		P_6.1.5
SDx high threshold	I_{TH_H}	11.5			mA	R_{SRX} = 3.5 kΩ, V_{DD} = 5.0 V	P_6.1.6
SDx low threshold	I_{TH_L}			8.5	mA	R_{SRX} = 3.5 kΩ, V_{DD} = 5.0 V	P_6.1.7
SDx hysteresis	I_{TH_HYS}	0.7	0.8	0.9	mA	R_{SRX} = 3.5 kΩ, V_{DD} = 5.0 V	P_6.1.8
SDx filter time constant	T_{FLT_SDX}	1		8	µs		P_6.1.9
SRx pin saturation voltage	V_{SAT_SRX}	0.6	1	1.5	V		P_6.1.10
SRx pin overtemperature shutdown voltage	V_{OTSD_SRX}			0.5	V	I_{SRX} = 1.5 mA	P_6.1.11
SRx chopper ripple frequency	F_{OSC_CHOP}		1		MHz		P_6.1.12
SRx settling time after activation of sensor channel	T_{ACT_SRX}			75	µs	1)	P_6.1.13
SRx settling time from sensor high to sensor low current	T_{FALL_SRX}			25	µs	1)	P_6.1.14
Speed sensor operational frequency	F_{MAX_SINX}			15	kHz	1)	P_6.1.15
Speed sensor pulse-width distortion	F_{PWDIS}	-10		10	µs		P_6.1.16
SDx output low voltage	V_{OL_SDX}			0.4	V	I_{SDX} = 1 mA	P_6.1.17
SDx output high voltage	V_{OH_SDX}	V_{DD} - 1			V	I_{SDX} = -1 mA	P_6.1.18

1) Not subject to production test, specified by design.

7 SPI interface

7.1 SPI frame

MOSI SPI frame

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RN/W	PARITY	0	0	0	ADDR[2]	ADDR[1]	ADDR[0]	DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]

MISO SPI frame

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RN/W	PARITY	FAULT comm.	FAULT global	0	ADDR[2]	ADDR[1]	ADDR[0]	DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]

Note: The parity bit (odd) is calculated over the entire frame (bit 15 + bits 13 - 0)

7.2 Timing diagram

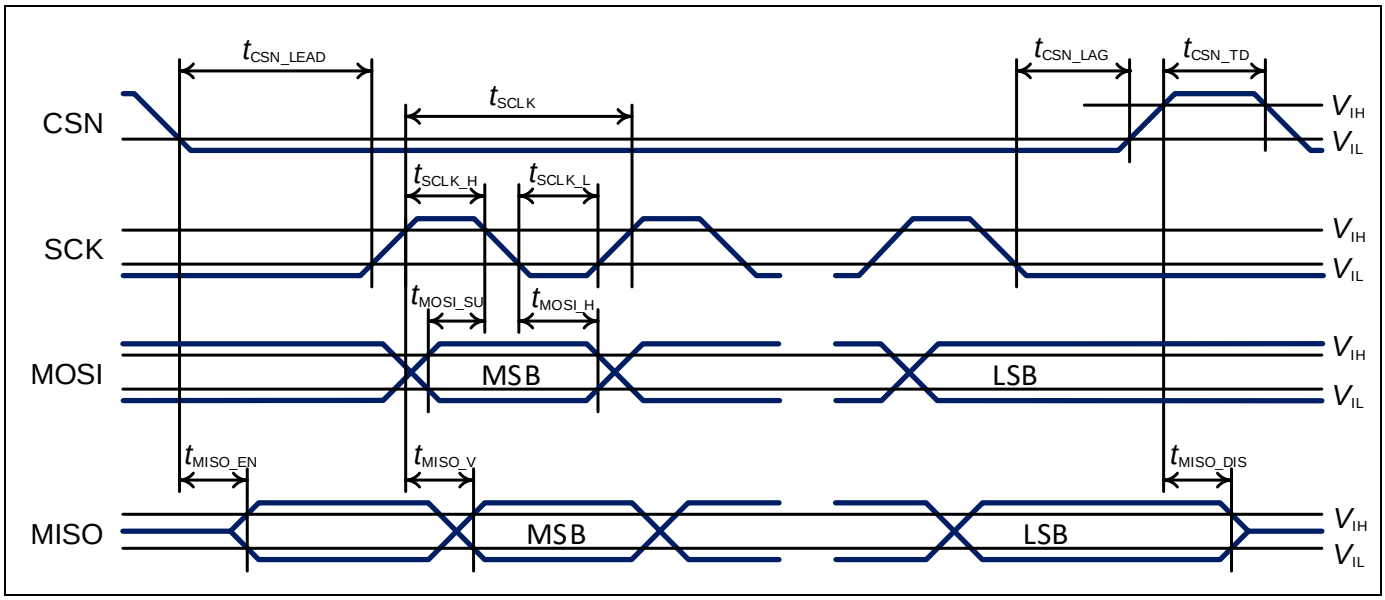

Figure 3 SPI signal timing diagram

7.2.1 Electrical characteristics SPI interface

Table 8 Electrical characteristics

V_S = 5.5 V to 40 V, V_{DD} = 4.75 V to 5.25 V, V_{IO} = 3.1 V to 5.25 V, T_j = -40 °C to +150 °C, all voltages with respect to ground (GNDD), positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Serial clock frequency	f_{SCK}			6	MHz	1) 2)	P_7.2.1
Serial clock high time	t_{SCK_H}	65			ns	1)	P_7.2.2
Serial clock low time	t_{SCK_L}	65			ns	1)	P_7.2.3
Enable lead time (falling CSN to rising SCK)	t_{CSN_LEAD}	150			ns	1)	P_7.2.4
Enable lag time (falling SCK to rising CSN)	t_{CSN_LAG}	150			ns	1)	P_7.2.5
Transfer delay time (rising CSN to falling CSN)	t_{CSN_TD}	1			µs	1)	P_7.2.6
Data setup time (required time SI to falling SCK)	t_{MISO_SU}	20			ns	1)	P_7.2.7
Data hold time (required time falling SCK to MOSI)	t_{MOSI_H}	20			ns	1)	P_7.2.8
Output enable time (falling CSN to MISO valid)	t_{MISO_EN}			200	ns	C_{MISO} = 200 pF 1)	P_7.2.9
Output disable time (rising CSN to MISO tri-state)	t_{MISO_DIS}			200	ns	C_{MISO} = 200 pF 1)	P_7.2.10
Output data valid time with capacitive load	t_{MISO_V}			100	ns	C_{MISO} = 200 pF 1)	P_7.2.11
MISO rise time	t_{MISO_R}			50	ns	C_{MISO} = 200 pF 1)	P_7.2.12
MISO fall time	t_{MISO_F}			50	ns	C_{MISO} = 200 pF 1)	P_7.2.13
Input pin capacitance: CSN, SCK, MOSI	C_{IN}			20	pF	1)	P_7.2.14
MISO pin capacitance	C_{MISO_HIZ}			25	pF	Tri-state 1)	P_7.2.15

1) Not subject to production test, specified by design.

2) Output load capacitance on MISO pin is ≤ 25 pF.

8 Package outlines

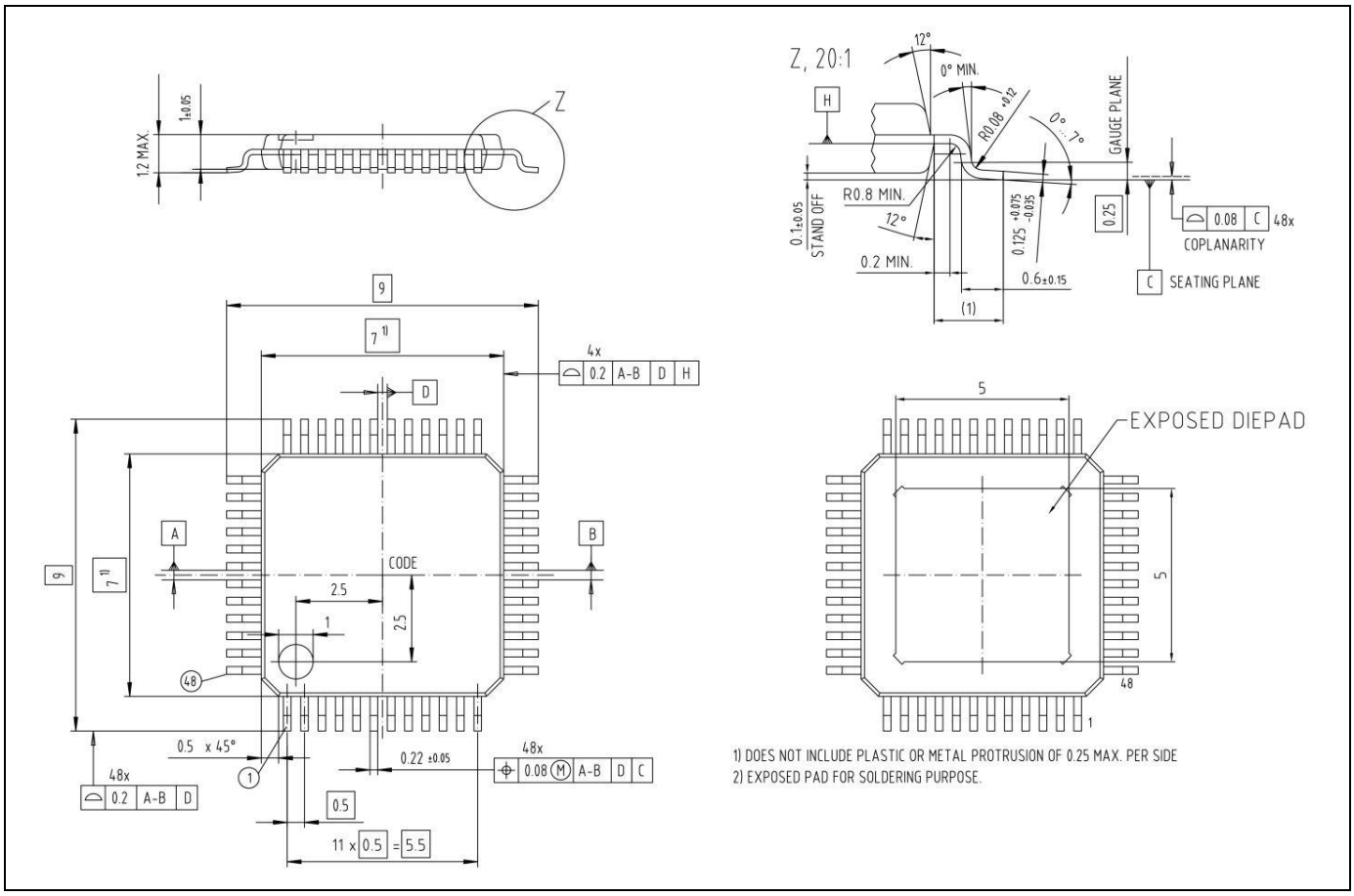

Figure 4 Package outline PG-TQFP-48-9

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages

Revision history

Document version	Date of release	Description of changes
1.0	2019-02-20	• Datasheet created

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