

# TLE9371VSJ

## CAN signal improvement transceiver



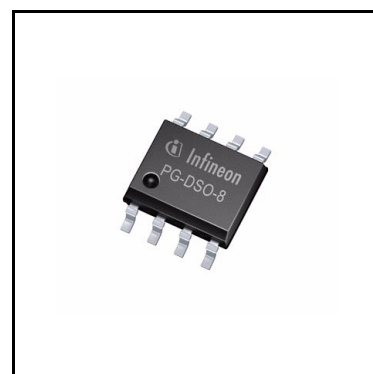
RoHS



CAN FD SIC

### Features

- Compliant to ISO 11898-2:2016, SAE J2284-4/-5
- Tx-based CAN FD SIC according to CiA 601-4
- Loop delay symmetry for CAN FD data frames up to 8 Mbit/s
- $V_{IO}$  input for voltage adaption to the microcontroller interface (3.3 V or 5 V)
- Standby mode with minimized quiescent current
- Transmitter supply  $V_{CC}$  can be turned off in standby mode for additional quiescent current savings
- Wake-up indication on the RxD output
- Wide common mode range for electromagnetic immunity (EMI)
- Excellent ESD robustness  $\pm 8$  kV HBM and IEC 61000-4-2
- CAN short circuit proof to ground, battery,  $V_{CC}$  and  $V_{IO}$
- TxD timeout function
- Very low CAN bus leakage current in power-down state
- Overtemperature protection
- Protected against automotive transients according to ISO 7637 and SAE J2962-2
- Green Product (RoHS compliant)



### Potential applications

- Gateway module
- Body control module (BCM)
- Engine control unit (ECU)
- ADAS
- Radar

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

### Description

The TLE9371VSJ is the first high-speed CAN transceiver generation with signal improvement, used in HS Controller Area Networks (CAN) for automotive applications and also for industrial applications. It is

designed to fulfill the requirements of ISO 11898-2 (2016) physical layer specification as well as SAE J1939 and SAE J2284.

The TLE9371VSJ is available in a halogen free and RoHS compliant PG-DSO-8 package.

As an interface between the physical bus layer and the HS CAN, the TLE9371VSJ protects the microcontroller against interference generated in the network. A very high ESD robustness and the optimized RF immunity allows the use in automotive applications without additional protection devices, such as suppressor diodes or common mode chokes.

While the TLE9371VSJ is not supplied the transmitter is switched off and behaves passive with the lowest possible load to all other nodes of the HS CAN.

Based on the high symmetry of the CANH and CANL output signals, the TLE9371VSJ provides very low electromagnetic emission (EME) within a wide frequency range. The TLE9371VSJ fulfills stringent EMC test limits without additional external circuitry, such as a common mode choke.

Due to the excellent symmetry combined with the optimized delay symmetry of the receiver the TLE9371VSJ supports CAN FD data frames. Depending on the size of the network and its parasitic effects the device supports a transmission rate up to 8 Mbit/s.

Dedicated low-power modes, like standby mode require very low quiescent current while the device is powered up. In standby mode the typical quiescent current on  $V_{IO}$  is below 10  $\mu$ A while the device can still wake up from a bus signal on the HS CAN bus.

Fail-safe features such as overtemperature protection, output current limitation and the TxD timeout feature protect the TLE9371VSJ and the external circuitry from damage.

Type	Package	Marking
TLE9371VSJ	PG-DSO-8	9371V

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## Block diagram

### 1 Block diagram

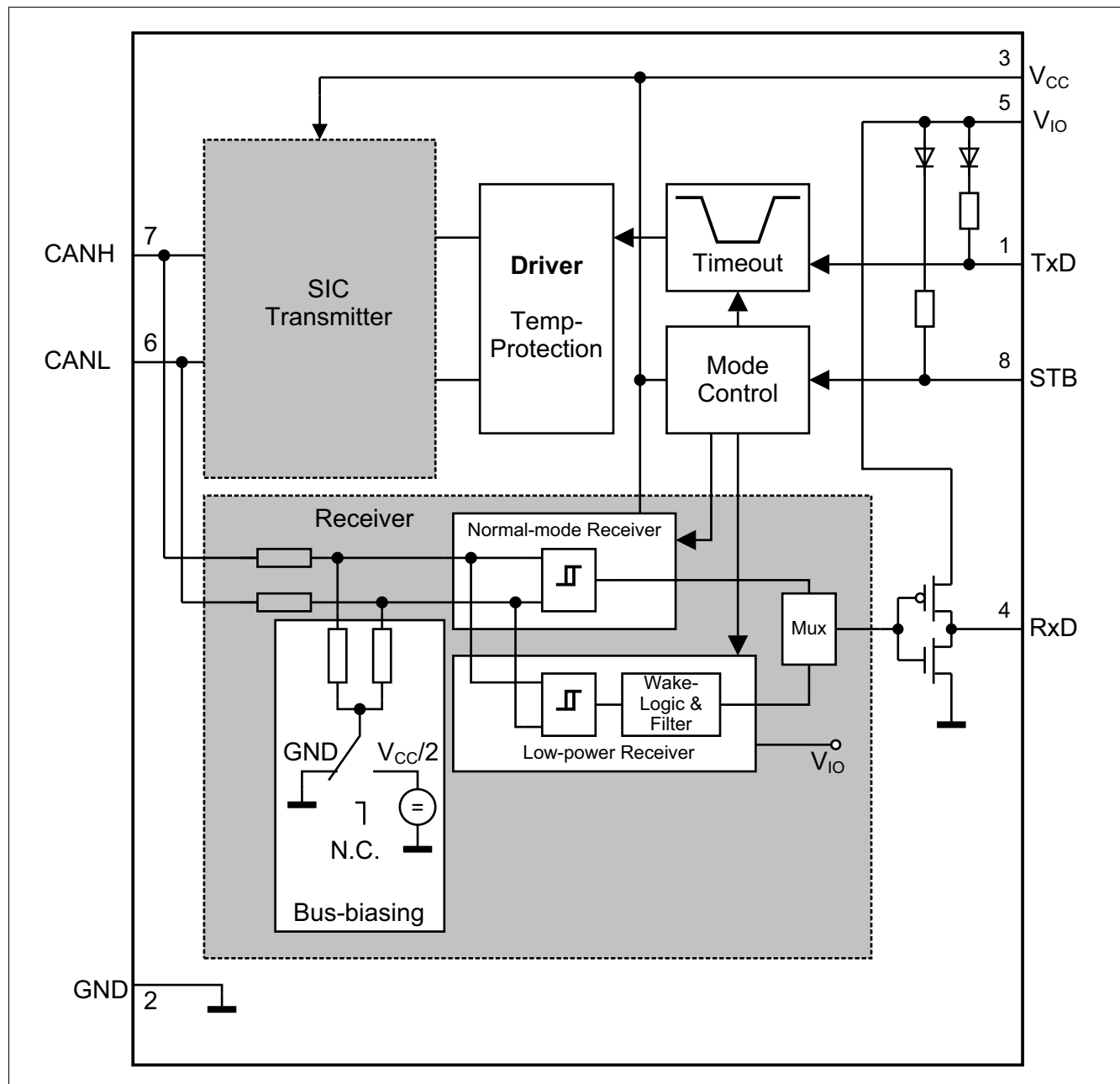


Figure 1 Block diagram

## Pin configuration

## 2 Pin configuration

### 2.1 Pin assignment

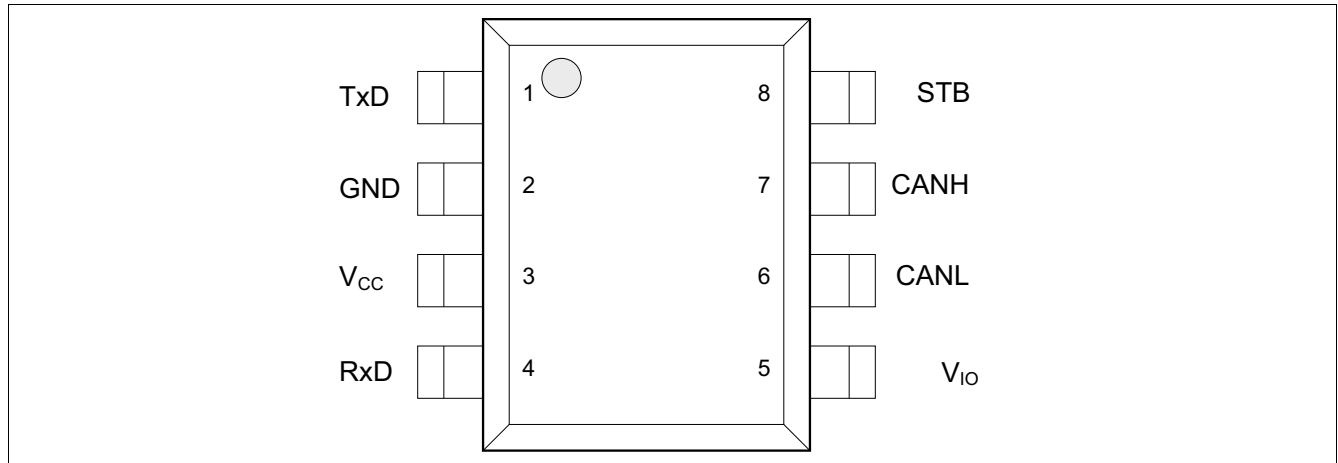


Figure 2 Pin configuration

### 2.2 Pin definitions and functions

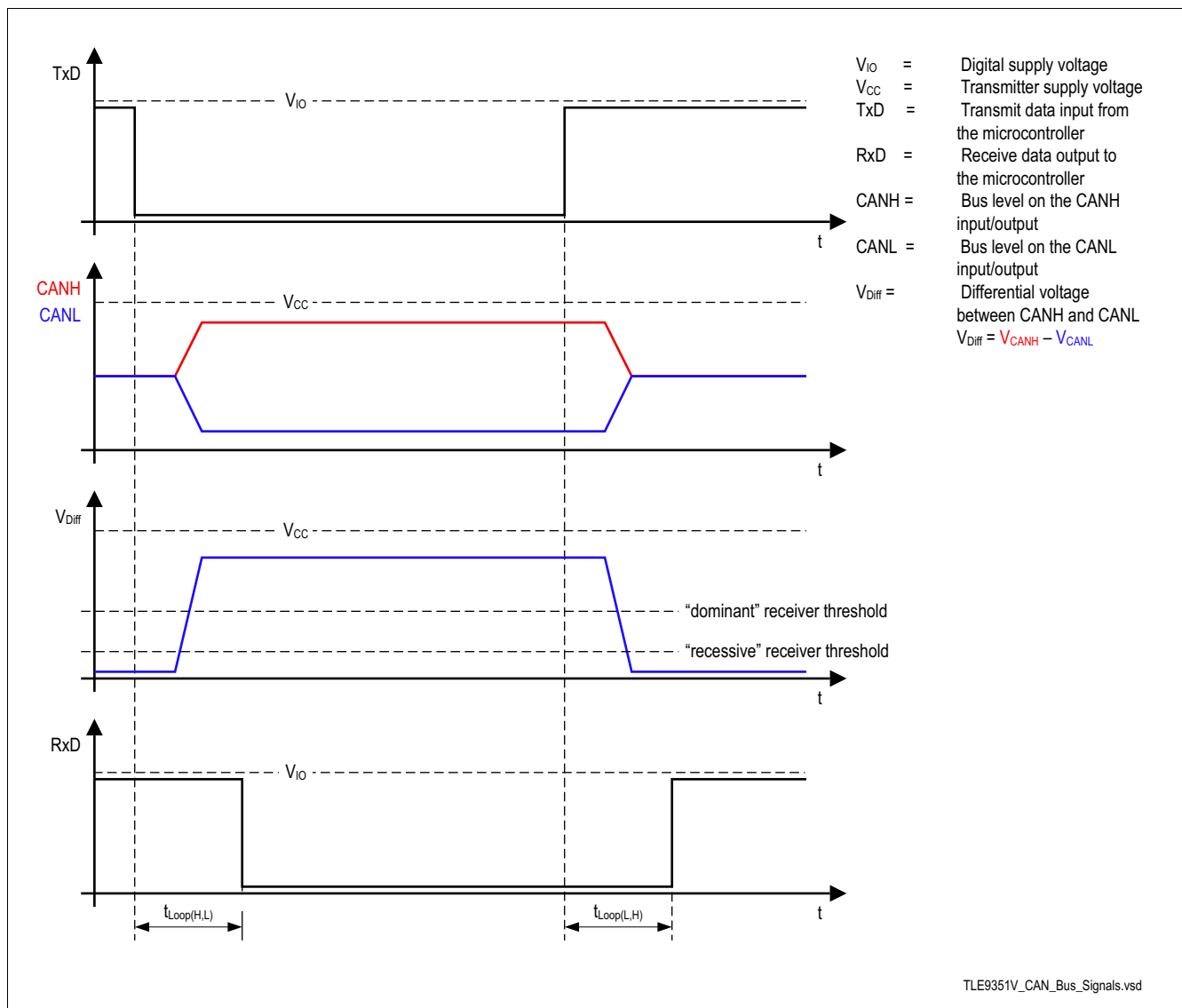
Table 1 Pin definitions and functions

Pin No.	Symbol	Function
1	TxD	<b>Transmit data input;</b> Internal pull-up to $V_{IO}$ , "low" for dominant state.
2	GND	<b>Ground</b>
3	$V_{CC}$	<b>Transmitter supply voltage;</b> 1 $\mu$ F decoupling capacitor to GND required, $V_{CC}$ can be turned off in standby mode.
4	RxD	<b>Receive data output;</b> "Low" in dominant state.
5	$V_{IO}$	<b>Digital supply voltage;</b> Supply voltage input to adapt the logical input and output voltage levels of the transceiver to the microcontroller supply. Supply for the low-power receiver. 100 nF decoupling capacitor to GND required.
6	CANL	<b>CAN bus low level I/O;</b> "Low" in dominant state.
7	CANH	<b>CAN bus high level I/O;</b> "High" in dominant state.
8	STB	<b>Standby input;</b> Internal pull-up to $V_{IO}$ , "low" for normal-operating mode.

### 3 High-speed CAN functional description

HS CAN is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. The use of the Controller Area Network (abbreviated CAN) within road vehicles is described by the international standard ISO 11898. According to the 7-layer OSI reference model the physical layer of a HS CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes within the network. The physical layer specification of a CAN bus system includes all electrical specifications of a CAN. The CAN transceiver is part of the physical layer. The TLE9371VSJ is a high-speed CAN transceiver with a dedicated bus wake-up function as defined in the latest ISO 11898-2 HS CAN standard.

#### 3.1 High-speed CAN physical layer



**Figure 3 High-speed CAN bus signals and logic signals**

## High-speed CAN functional description

The TLE9371VSJ is a high-speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. A HS CAN is a two wire, differential network, which allows data transmission rates up to 8 Mbit/s. The characteristic for a HS CAN is that the logical high level and logical low level (microcontroller interface) are converted into a differential signal (CAN bus interface) with the states dominant and recessive, see [Figure 3](#).

The CANH and CANL pins are the interface to the CAN bus and both pins operate as an input and output. The RxD and TxD pins are the interface to the microcontroller. The pin TxD is the serial data input from the CAN controller, the RxD pin is the serial data output to the CAN controller. The device includes a receiver and a transmitter unit, allowing the transceiver to send data to the bus medium and monitor the data from the bus medium at the same time, see [Figure 1](#). The device converts the serial data stream from the transmit data input TxD, into a differential output signal on the CAN bus, provided by the CANH and CANL pins. The receiver stage of the device monitors the data on the CAN bus and converts them to a serial, single-ended signal on the RxD output pin. A “low” signal on the TxD pin creates a dominant signal on the CAN bus. The receiver converts this dominant signal to a “low” signal on the RxD pin, see [Figure 3](#). The feature of broadcasting data to the CAN bus and listening to the data traffic on the CAN bus simultaneously is essential to support the bit-to-bit arbitration within the network.

The voltage levels for HS CAN transceivers are defined in ISO 11898-2. Whether a data bit is dominant or recessive depends on the voltage difference between the CANH and CANL pins:

$$V_{\text{Diff}} = V_{\text{CANH}} - V_{\text{CANL}}$$

For a dominant signal on the CAN bus the high-speed transceiver creates a differential signal of  $V_{\text{Diff}} \geq 1.5 \text{ V}$ . To receive a recessive signal from the CAN bus the amplitude of the differential  $V_{\text{Diff}} \leq 0.5 \text{ V}$ .

In a partially supplied high-speed CAN, the CAN bus nodes have different power supply conditions. Some nodes are connected to the common power supply while other nodes are disconnected from the power supply and in power-down state. Regardless of whether the CAN bus node is supplied or not, each node connected to the common bus media must not interfere with the communication. The device supports partially-supplied networks. In power-down state, the receiver input resistors are switched off and the transceiver input has a high resistance.

For permanently supplied ECUs, the HS CAN transceiver, the device provides a stand-by mode. In stand-by mode, the power consumption of the device is optimized to a minimum, while the device is still able to recognize wake-up patterns on the CAN bus and signal the wake-up event to the external microcontroller.

The voltage level on the digital input TxD and on the digital output RxD is determined by the power supply level at the  $V_{\text{IO}}$  pin. Depending on the voltage level at the  $V_{\text{IO}}$  pin, the signal levels on the logic pins (STB, TxD and RxD) are compatible with microcontrollers having a 5 V or 3.3 V I/O supply. Usually the digital power supply  $V_{\text{IO}}$  of the transceiver is connected to the I/O power supply of the microcontroller, see [Figure 15](#).

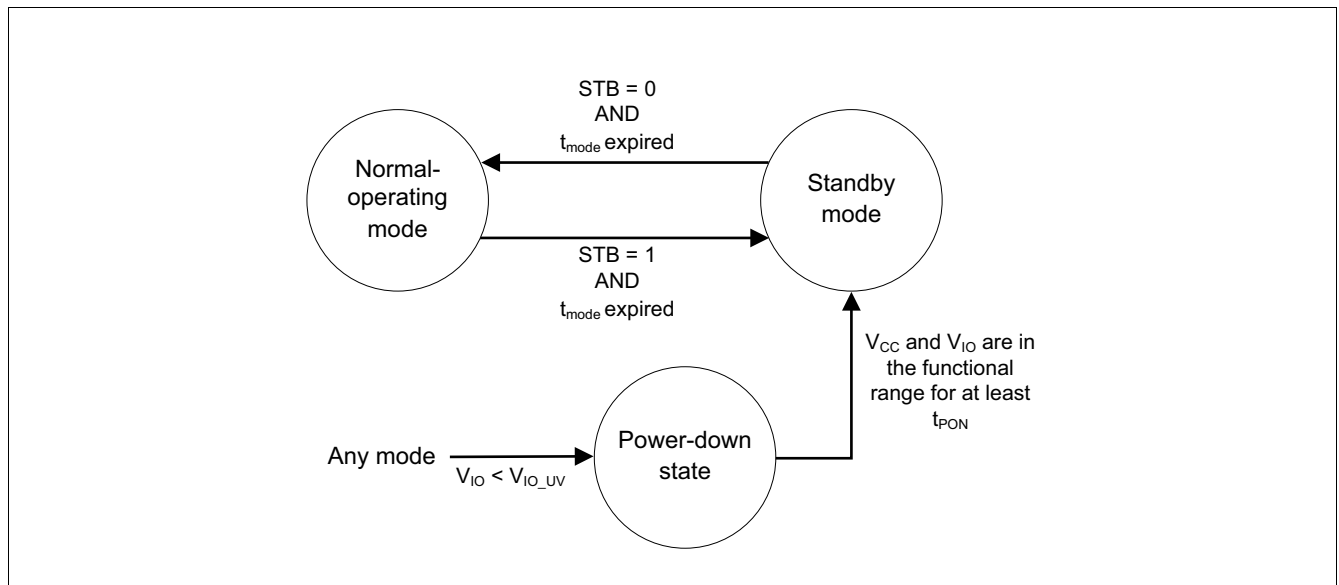
## Modes of operation

### 4 Modes of operation

The device supports the following modes of operation, see [Figure 4](#):

- Normal-operating mode
- Standby mode

The mode selection input pin STB triggers mode changes. If a wake-up event occurs on the HS CAN bus, then the device indicates that on the RxD output pin in stand-by mode, but it does not trigger a mode change. Undervoltage on VCC disables the transmitter output stage. An undervoltage event on the digital supply VIO powers down the device.



**Figure 4** Mode state diagram

## Modes of operation

### 4.1 Normal-operating mode

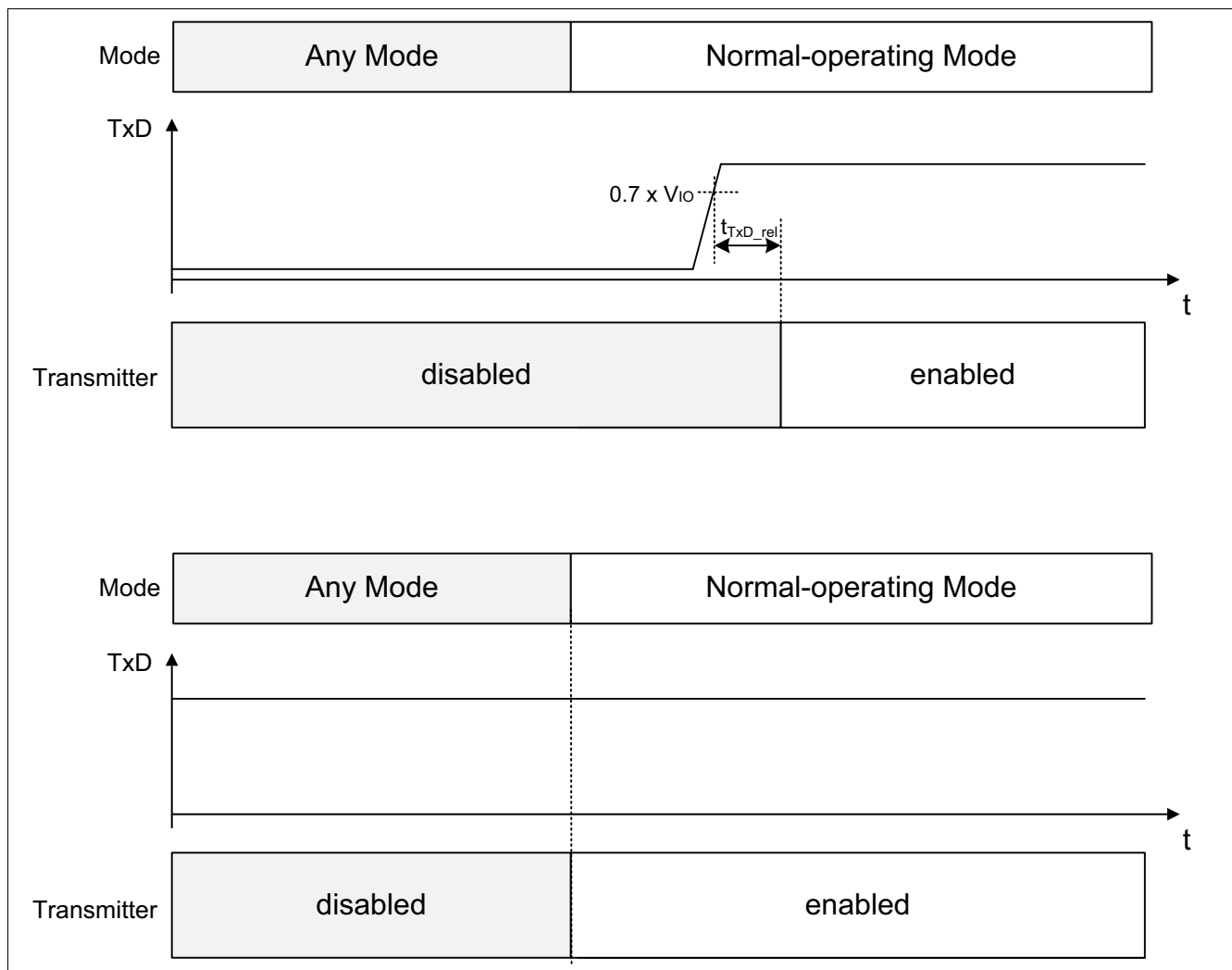
In normal-operating mode all functions of the device are available and the device is fully functional. Data can be received from the HS CAN bus as well as be transmitted to the HS CAN bus.

- The transmitter is enabled and drives data stream on the TxD input pin to the bus pins CANH and CANL
- The receiver is enabled and converts the signals from the bus to a serial data stream on the RxD output pin
- The bus biasing is connected to  $V_{CC}/2$  if  $V_{CC} > V_{CC\_UV}$
- The TxD timeout function is enabled, see [Chapter 5.4](#)
- The overtemperature protection is enabled, see [Chapter 5.6](#)
- The undervoltage detection on  $V_{CC}$  is enabled, see [Chapter 5.3](#)

Conditions for entering normal-operating mode of the device:

- If  $V_{IO} > V_{IO\_UV}$  and the STB pin is “low”, then the device enters normal-operating mode after  $t_{Mode}$  from standby mode, see [Figure 4](#)

If a “low” signal is applied on TxD input pin during a mode change to normal-operating mode, device disables the transmitter as long as “low” signal is applied on the TxD input pin. If a “high” signal is applied on the TxD input pin for at least  $t_{TxD\_rel}$ , then the device enables the transmitter, see [Figure 5](#).



**Figure 5** Mode change to normal-operating mode with dominant signal on TxD

## **Modes of operation**

### **4.2 Standby mode**

The standby mode is the low-power mode of the device. In standby mode the following functions are defined:

- The transmitter is disabled and does not drive the data stream on the TxD input pin to the bus pins CANH and CANL
- The normal-mode receiver is disabled and the data available on the bus is blocked.
- The device monitors the CAN bus for a valid wake-up pattern, see [Chapter 4.4](#).
- The RxD output pin indicates a CAN bus wake-up, see [Chapter 4.4.2](#)
- Bus biasing is connected to GND
- TxD dominant timeout function is disabled
- The overtemperature protection is disabled
- The undervoltage detection on  $V_{CC}$  is disabled, see [Chapter 5.3](#)

Conditions for entering standby mode of the device:

- If  $V_{IO} > V_{IO\_UV}$  and the STB pin is “high”, then the device enters standby mode after  $t_{Mode}$  from normal-operation mode
- If  $V_{CC}$  and  $V_{IO}$  are in the functional range for at least  $t_{PON}$ , then the device enters standby mode from power-down state

## Modes of operation

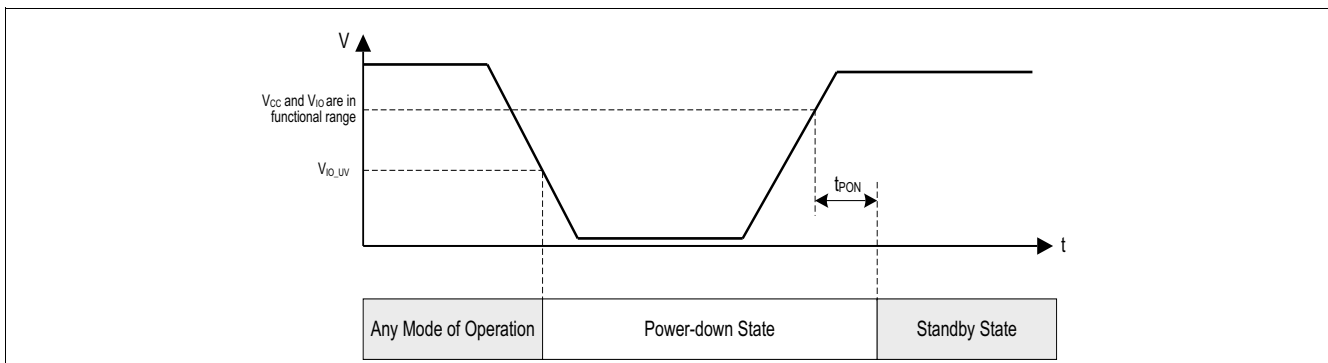
### 4.3 Power-down state

In power-down state the device is not functional and has the following behavior:

- The transmitter and receiver are disabled
- The bus biasing is set to high impedance
- The TxD timeout function is disabled
- The overtemperature protection is disabled
- The undervoltage detection on  $V_{CC}$  is disabled
- RxD follows the  $V_{IO}$  voltage

Conditions for entering power-down state of the device:

- $V_{IO}$  is below the  $V_{IO\_UV}$  threshold



**Figure 6** Power-down and power-up behavior

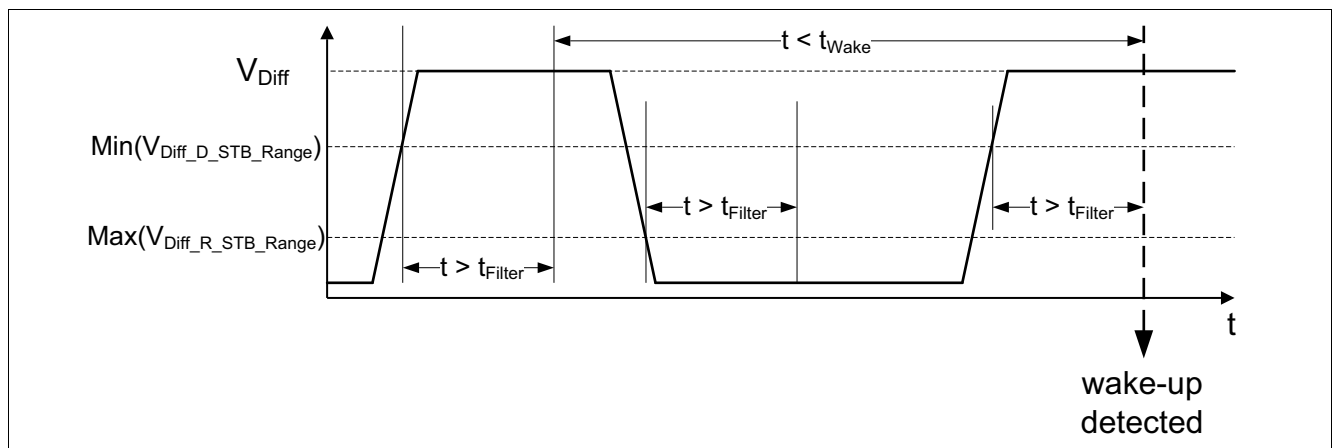
## Modes of operation

### 4.4 Bus wake-up pattern (WUP) detection

The device has implemented the bus wake-up mechanism according to ISO 11898-2:2016. In standby mode the low power receiver monitors the activity on the CAN bus and in case it detects a wake-up pattern, it indicates the wake-up signal on the RxD output pin. A wake-up event does not trigger a mode change. The device remains in standby mode until the microcontroller has requested a mode change to the normal operating mode.

#### 4.4.1 Bus wake-up pattern (WUP)

The wake-up pattern contains a dominant signal with the pulse width  $t_{\text{Filter}}$ , followed by a recessive signal with the pulse width  $t_{\text{Filter}}$  and another dominant signal with the pulse width  $t_{\text{Filter}}$ .  $t_{\text{Wake}}$  starts at the first valid dominant pulse (pulse width  $> t_{\text{Filter}}$ ). The subsequent recessive and dominant pulse must occur within  $t_{\text{Wake}}$  to fulfill a wake-up pattern, see [Figure 7](#). As long as the device does not detect a wake-up event, the RxD output remains “high”.

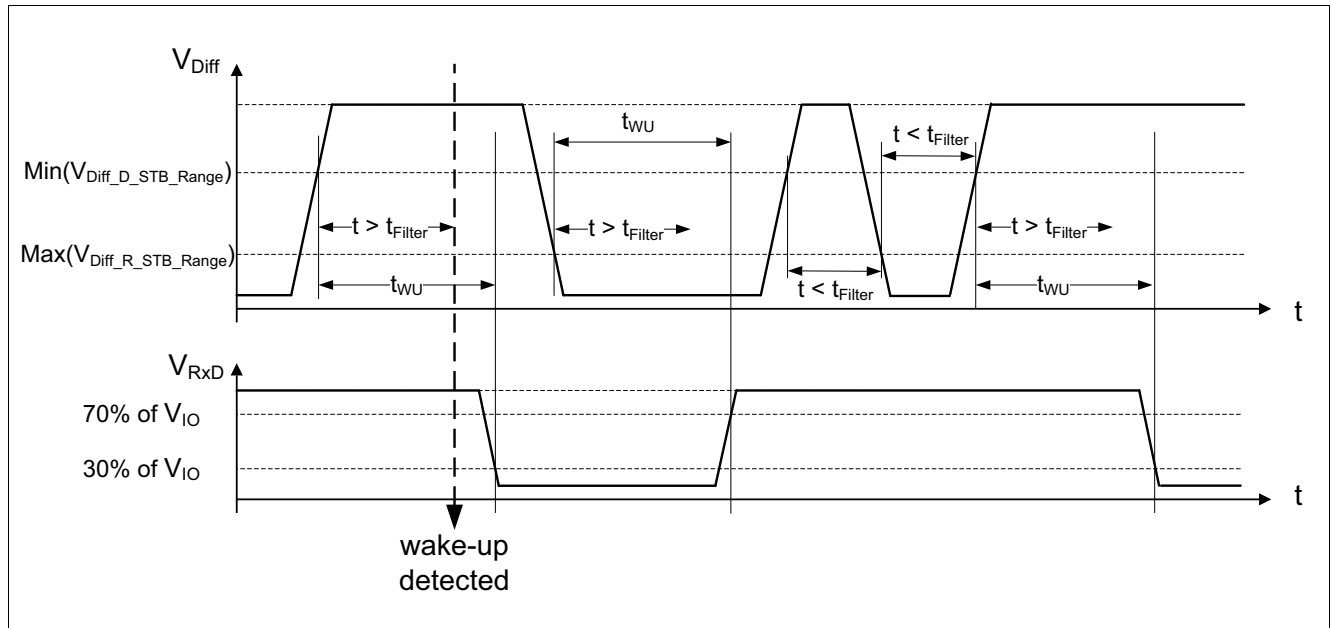


**Figure 7** Remote wake-up signal

#### 4.4.2 RxD pin wake-up behavior

If the device detects a wake-up event, then it sets the RxD output pin to “low” and then the RxD output follows the CAN bus signal with the delay of  $t_{\text{WU}}$  as long as the pulse width exceeds the filter time  $t_{\text{Filter}}$ , see [Figure 8](#).

## Modes of operation



**Figure 8 RxD signal follows the CAN bus signal**

If at least one of the following conditions is fulfilled, then the device disables the RxD pin wake up behavior:

- A mode change to normal-operating mode is performed during a wake-up pattern
- The voltage supply  $V_{IO} < V_{IO\_UV}$

## 5 Fail safe functions

### 5.1 Short circuit protection

The CANH and CANL bus pins are proven to cope with a short circuit fault against GND and against the supply voltages. A current limiting circuit protects the transceiver against damages. If the device heats up due to a continuous short on the CANH or CANL pin, the internal overtemperature protection switches off the bus transmitter.

### 5.2 Unconnected logic input pins

If the input pins are not connected and floating, then the integrated pull-up resistors at the digital input pins force the device into fail safe behavior, see [Table 2](#).

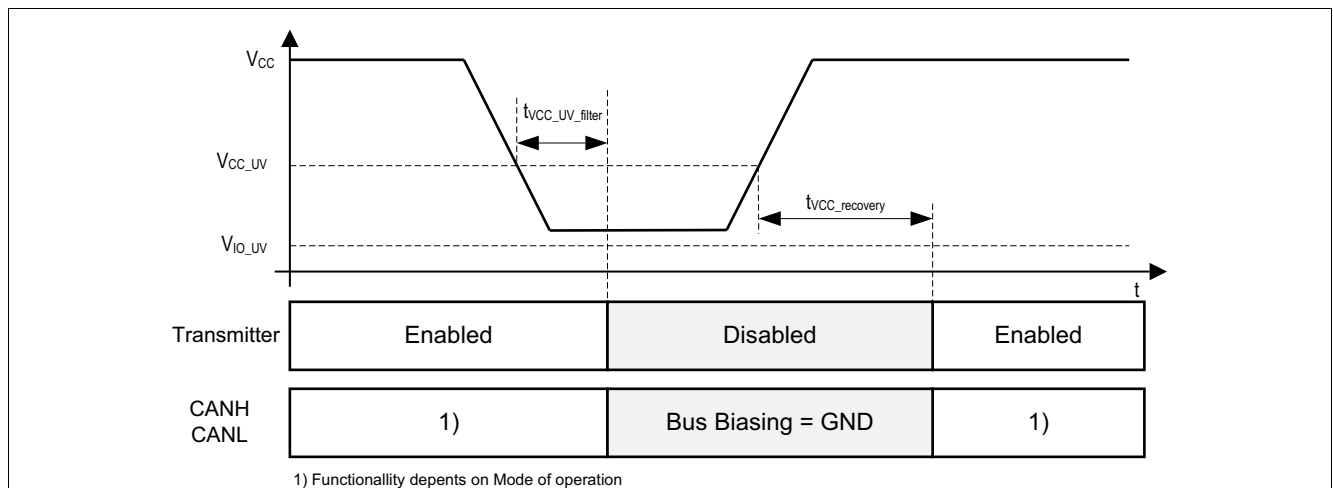
**Table 2** Unconnected logical input pins

Input signal	Default state	Comment
TxD	“High”	Pull-up resistor to $V_{IO}$
STB	“High”	Pull-up resistor to $V_{IO}$

### 5.3 $V_{CC}$ undervoltage

If  $V_{CC} < V_{CC\_UV}$ , then the  $V_{CC}$  supply of the transceiver is in undervoltage condition with the following functions independent of the transceiver mode, see [Figure 9](#):

- Transmitter is deactivated
- The bus biasing is set to GND



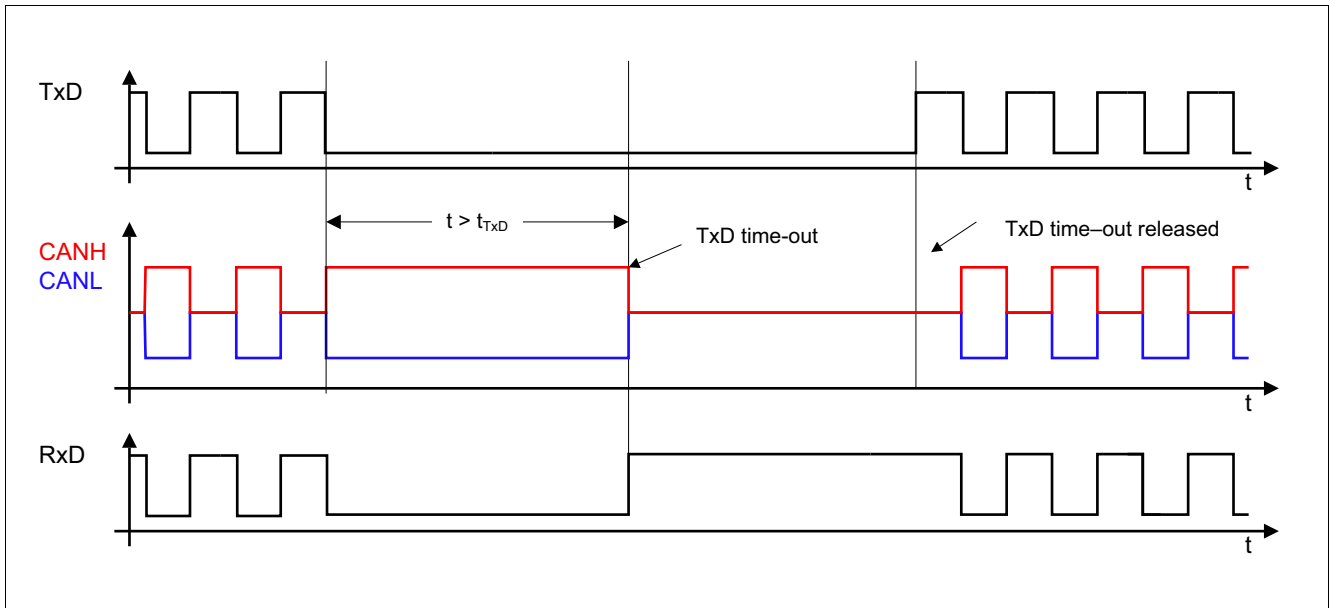
**Figure 9** Undervoltage on the transmitter supply  $V_{CC}$

### 5.4 TxD timeout function

If the logical signal on the TxD pin is permanently “low”, then the TxD timeout feature protects the CAN bus from blocked communication due to this errant logic signal. A permanent “low” signal on the TxD pin can occur due to a locked-up microcontroller or in a short circuit on the printed circuit board, for example. In normal-operating mode, a “low” signal on the TxD pin for the time  $t > t_{TxD\_TO}$  enables the TxD timeout feature

## Fail safe functions

and the device disables the transmitter, see [Figure 10](#). The receiver is still active and the RxD output pin continues monitoring data on the bus.



**Figure 10** TxD timeout function

### 5.5 Delay time for mode change

The HS CAN transceiver device changes the mode of operation within the time window  $t_{\text{Mode}}$ . During the mode change from standby mode to a non-low power mode the device sets the RxD output to “high” and RxD does not reflect the status on the CANH and CANL input pins.

### 5.6 Overtemperature protection

The device has an integrated overtemperature detection to protect the device against thermal overstress of the transmitter. The overtemperature protection is only active in normal-operating mode. If an overtemperature condition ( $T_{\text{Junction}} \geq T_{\text{JSD}}$ ) occurs, then the temperature sensor disables the transmitter while the transceiver remains in normal-operating mode. After the device cools down ( $T_{\text{Junction}} < T_{\text{JSD}}$ ) the device activates the transmitter again, see [Figure 11](#). A hysteresis is implemented within the temperature sensor.

Fail safe functions

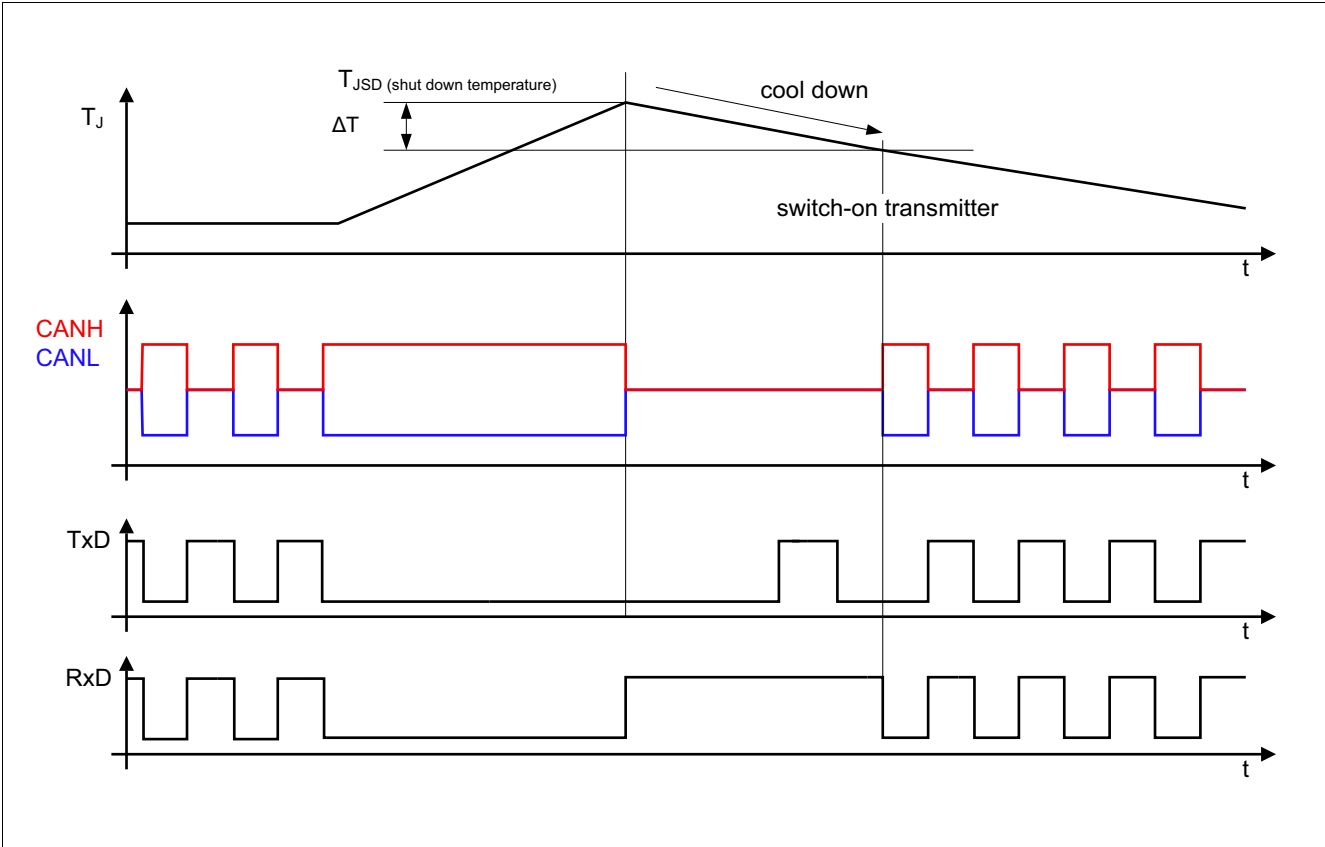


Figure 11 Overtemperature protection

## 6 General product characteristics

### 6.1 Absolute maximum ratings

**Table 3 Absolute maximum ratings voltages, currents and temperatures<sup>1)</sup>**

All voltages with respect to ground; positive current flowing into pin;  
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Transmitter supply voltage	V <sub>CC</sub>	-0.3	–	6.0	V	–	P_7.1.1
Digital supply voltage	V <sub>IO</sub>	-0.3	–	6.0	V	–	P_7.1.2
CANH and CANL DC voltage versus GND	V <sub>CANH</sub>	-40	–	40	V	–	P_7.1.3
Differential voltage between CANH and CANL	V <sub>CAN_Diff</sub>	-40	–	40	V	–	P_7.1.4
Voltages at the digital I/O pins: STB, TxD	V <sub>MAX_IO</sub>	-0.3	–	6.0	V	–	P_7.1.8
Voltages at the digital I/O pins: RxD	V <sub>MAX_RxD</sub>	-0.3	–	V <sub>IO</sub> +0.3	V	–	P_7.1.9
Currents							
RxD output current	I <sub>RxD</sub>	-5	–	5	mA	–	P_7.1.11
Temperatures							
Junction temperature	T <sub>j</sub>	-40	–	150	°C	–	P_7.1.12
Storage temperature	T <sub>S</sub>	-55	–	150	°C	–	P_7.1.13
ESD robustness							
ESD robustness at CANH, CANL versus GND	V <sub>ESD_HBM_CAN</sub>	-8	–	8	kV	2) HBM; 100 pF via 1.5 kΩ	P_7.1.14
ESD robustness at all other pins	V <sub>ESD_HBM_ALL</sub>	-2	–	2	kV	2) HBM; 100 pF via 1.5 kΩ	P_7.1.15
ESD robustness at corner pins	V <sub>ESD_CDM_CP</sub>	-750	–	750	V	3) CDM	P_7.1.16
ESD robustness at any other pins	V <sub>ESD_CDM</sub>	-500	–	500	V	3) CDM	P_7.1.17

1) Not subject to production test, specified by design.

2) Human body model (HBM) robustness according to AE - Q100-002

3) Charge device model (CDM) robustness according to AEC - Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard.

*Note: Latchup robustness: class II according to AEC - Q100-04.*

**General product characteristics**

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal-operating range. Protection functions are not designed for continuous repetitive operation.*

**General product characteristics**

## 6.2 Functional range

**Table 4 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltages							
Transmitter supply voltage	V <sub>CC</sub>	4.75	–	5.25	V	–	P_7.2.1
Digital supply voltage	V <sub>IO</sub>	3.0	–	5.5	V	–	P_7.2.2
Thermal parameters							
Junction temperature	T <sub>j</sub>	-40	–	150	°C	1)	P_7.2.3

1) Not subject to production test, specified by design.

*Note:* Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 6.3 Thermal resistance

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit [www.jedec.org](http://www.jedec.org).

**Table 5 Thermal resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistances							
Junction to ambient PG-DSO-8	$R_{thJA\_DSO8}$	–	120	–	K/W	2)	P_7.3.2
Thermal shutdown (junction temperature)							
Thermal shutdown temperature, rising	$T_{JSD}$	170	180	190	°C	Temperature falling: minimum 150°C	P_7.3.3
Thermal shutdown hysteresis	$\Delta T$	5	10	20	K	–	P_7.3.4

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board. The product (chip and package) was simulated on a 76.2 mm × 114.3 mm × 1.5 mm board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu).

## Electrical characteristics

## 7 Electrical characteristics

### 7.1 Power supply interface

#### 7.1.1 Current consumption

**Table 6** Current consumption

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption at $V_{CC}$ normal-operating mode, recessive state	$I_{CC\_R}$	–	2	4	mA	$V_{TxD} = V_{IO}$ ; $V_{STB} = 0 \text{ V}$ ; $V_{CANH} = V_{CANL} = V_{CC}/2$	P_8.1.5
Current consumption at $V_{CC}$ normal-operating mode, dominant state	$I_{CC\_D}$	–	38	48	mA	$V_{TxD} = V_{STB} = 0 \text{ V}$ ; $t < t_{TxD}$	P_8.1.9
Current consumption at $V_{IO}$ normal-operating mode	$I_{IO}$	–	–	2	mA	$V_{STB} = 0 \text{ V}$ ; $V_{Diff} = 0 \text{ V}$ ; recessive state	P_8.1.12
Current consumption at $V_{CC}$ standby mode	$I_{CC(STB)}$	–	–	5	$\mu\text{A}$	$V_{TxD} = V_{STB} = V_{IO}$	P_8.1.16
Current consumption at $V_{IO}$ standby mode	$I_{IO(STB)}$	–	7	18	$\mu\text{A}$	$V_{TxD} = V_{STB} = V_{IO}$ ; $0 \text{ V} < V_{CC} < 5.25 \text{ V}$	P_8.1.19
Current consumption at $V_{IO}$ standby mode	$I_{IO\_STB\_85}$	–	–	12	$\mu\text{A}$	<sup>1)</sup> $V_{TxD} = V_{STB} = V_{IO}$ ; $T_j < 85^\circ\text{C}$ ; $0 \text{ V} < V_{CC} < 5.25 \text{ V}$	P_8.1.21

## Electrical characteristics

### 7.1.2 Undervoltage detection

**Table 7 Undervoltage detection**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
$V_{CC}$ undervoltage threshold	$V_{CC\_UV}$	4.25	4.35	4.5	V	–	P_8.1.25
$V_{CC}$ undervoltage filter time	$t_{VCC\_UV\_filter}$	1	–	10	$\mu\text{s}$	<sup>1)</sup>	P_8.1.27
$V_{CC}$ undervoltage recovery time	$t_{VCC\_recovery}$	–	–	70	$\mu\text{s}$	<sup>1)</sup>	P_8.1.28
$V_{IO}$ undervoltage threshold	$V_{IO\_UV}$	2.0	2.5	3.0	V	–	P_8.1.29
Power-up delay time	$t_{PON}$	–	–	280	$\mu\text{s}$	<sup>1)</sup> Figure 6	P_8.1.33

1) Not subject to production test, specified by design.

## Electrical characteristics

### 7.2 CAN controller interface

**Table 8** CAN controller interface

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver output RxD							
“High” level output current	$I_{\text{RxD\_H}}$	–	-2	-1	mA	$V_{\text{RxD}} = V_{\text{IO}} - 0.4 \text{ V};$ $V_{\text{Diff}} < 0.5 \text{ V}$	P_8.2.1
“Low” level output current	$I_{\text{RxD\_L}}$	1	2	–	mA	$V_{\text{RxD}} = 0.4 \text{ V};$ $V_{\text{Diff}} > 0.9 \text{ V}$	P_8.2.3
Transmitter input TxD							
“High” level input voltage	$V_{\text{TxD\_H}}$	$0.7 \times V_{\text{IO}}$	–	6.0	V	Recessive state	P_8.2.4
“Low” level input voltage	$V_{\text{TxD\_L}}$	-0.3	–	$0.3 \times V_{\text{IO}}$	V	Dominant state	P_8.2.6
Internal pull-up resistor TxD	$R_{\text{TxD}}$	35	50	70	kΩ	–	P_8.2.9
Input capacitance	$C_{\text{TxD}}$	–	–	10	pF	<sup>1)</sup>	P_8.2.10
TxD dominant timeout	$t_{\text{TxD}}$	1	–	4	ms	Normal-operating mode	P_8.2.11
Standby input STB							
“High” level input voltage	$V_{\text{Mode\_H}}$	$0.7 \times V_{\text{IO}}$	–	6.0	V	–	P_8.2.14
“Low” level input voltage	$V_{\text{Mode\_L}}$	-0.3	–	$0.3 \times V_{\text{IO}}$	V	Normal-operating mode	P_8.2.16
Internal pull-up resistor	$R_{\text{Mode}}$	35	50	70	kΩ	–	P_8.2.19
Input capacitance	$C_{\text{Mode}}$	–	–	10	pF	<sup>1)</sup>	P_8.2.20

1) Not subject to production test, specified by design.

## Electrical characteristics

### 7.3 Receiver

**Table 9 Receiver characteristics**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Common mode range	$V_{CMR}$	-12	–	12	V	–	P_8.3.1
Differential range dominant state, normal-operating mode	$V_{Diff\_D\_Range}$	0.9	–	8.0	V	<sup>1)</sup> $V_{CMR}$	P_8.3.4
Differential range recessive state, normal-operating mode	$V_{Diff\_R\_Range}$	-3.0	–	0.5	V	<sup>1)</sup> $V_{CMR}$	P_8.3.6
Differential range dominant state, standby mode	$V_{Diff\_D\_STB\_Range}$	1.15	–	8.0	V	<sup>1)</sup> $V_{CMR}$	P_8.3.8
Differential range recessive state, standby mode	$V_{Diff\_R\_STB\_Range}$	-3.0	–	0.4	V	<sup>1)</sup> $V_{CMR}$	P_8.3.10
Single ended internal resistance	$R_{CAN\_H}$ , $R_{CAN\_L}$	30	–	50	k $\Omega$	<sup>1)</sup> recessive state; $-2 \text{ V} \leq V_{CANH} \leq 7 \text{ V}$ ; $-2 \text{ V} \leq V_{CANL} \leq 7 \text{ V}$	P_8.3.12
Differential internal resistance	$R_{Diff}$	60	–	100	k $\Omega$	<sup>1)</sup> recessive state; $-2 \text{ V} \leq V_{CANH} \leq 7 \text{ V}$ ; $-2 \text{ V} \leq V_{CANL} \leq 7 \text{ V}$	P_8.3.13
Input resistance deviation between CANH and CANL	$\Delta R_i$	-1	–	1	%	<sup>1)</sup> recessive state; $V_{CANH} = V_{CANL} = 5 \text{ V}$	P_8.3.14
Input capacitance CANH, CANL versus GND	$C_{In}$	–	20	40	pF	<sup>1)2)</sup>	P_8.3.15
Differential input capacitance	$C_{InDiff}$	–	10	20	pF	<sup>1)2)</sup>	P_8.3.16

1) Not subject to production test, specified by design.

2) S2P-method;  $f = 10 \text{ MHz}$ .

## Electrical characteristics

### 7.4 Transmitter

**Table 10 Transmitter characteristics**

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANL, CANH recessive state output voltage	$V_{CANL,H}$	2.0	2.5	3.0	V	Normal-operating mode; $V_{TxD} = V_{IO}$ ; no load	P_8.4.1
CANH, CANL recessive state differential output voltage $V_{Diff\_R\_NM} = V_{CANH} - V_{CANL}$	$V_{Diff\_R\_NM}$	-50	–	50	mV	Normal-operating mode; $V_{TxD} = V_{IO}$ ; no load	P_8.4.3
CANL dominant state output voltage, normal-operating mode	$V_{CANL}$	0.5	–	2.25	V	$V_{TxD} = 0 \text{ V}$ ; $45 \Omega < R_L < 65 \Omega$	P_8.4.5
CANH dominant state output voltage, normal-operating mode	$V_{CANH}$	2.75	–	4.5	V	$V_{TxD} = 0 \text{ V}$ ; $45 \Omega < R_L < 65 \Omega$	P_8.4.6
Differential voltage dominant state, normal-operating mode	$V_{Diff\_D\_NM}$	1.5	2.0	3.0	V	$V_{Diff} = V_{CANH} - V_{CANL}$ ; $V_{TxD} = 0 \text{ V}$ ; $50 \Omega < R_L < 65 \Omega$	P_8.4.7
Differential voltage extended bus load	$V_{Diff\_EXT\_BL}$	1.4	2.0	3.3	V	Dominant state; normal-operating mode; $V_{TxD} = 0 \text{ V}$ ; $45 \Omega < R_L < 70 \Omega$	P_8.4.8
Differential voltage dominant state high extended bus load normal-operating mode	$V_{Diff\_HEXT\_BL}$	1.5	–	5.0	V	<sup>1)</sup> $V_{TxD} = 0 \text{ V}$ ; $R_L = 2240 \Omega$	P_8.4.9
CANH, CANL recessive output voltage difference standby mode	$V_{Diff\_STB}$	-0.2	–	0.2	V	No load	P_8.4.10
CANL, CANH recessive output voltage standby mode	$V_{CANL,H\_STB}$	-0.1	–	0.1	V	No load	P_8.4.11
Driver symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	$V_{SYM}$	$0.95 \times V_{CC}$	$1.0 \times V_{CC}$	$1.05 \times V_{CC}$	V	<sup>1)2)</sup> $C_1 = 4.7 \text{ nF}$	P_8.4.12
CANL short circuit current	$I_{CANLsc}$	-115	–	115	mA	$-3 \text{ V} < V_{CANLshort} < 18 \text{ V}$ ; $t < t_{TxD}$ ; $V_{TxD} = 0 \text{ V}$	P_8.4.13
CANH short circuit current	$I_{CANHsc}$	-115	–	115	mA	$-3 \text{ V} < V_{CANHshort} < 18 \text{ V}$ ; $t < t_{TxD}$ ; $V_{TxD} = 0 \text{ V}$	P_8.4.14

## Electrical characteristics

**Table 10 Transmitter characteristics** (cont'd)

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH leakage current	$I_{CANH, Ik}$	-5	–	5	$\mu\text{A}$	$V_{CC} = V_{IO} = 0 \text{ V};$ $0 \text{ V} < V_{CANH} \leq 5 \text{ V};$ $V_{CANH} = V_{CANL}$	P_8.4.15
CANL leakage current	$I_{CANL, Ik}$	-5	–	5	$\mu\text{A}$	$V_{CC} = V_{IO} = 0 \text{ V};$ $0 \text{ V} < V_{CANL} \leq 5 \text{ V};$ $V_{CANH} = V_{CANL}$	P_8.4.17
Signal improvement resistance	$R_{SI}$	75	–	125	$\Omega$		P_8.4.19
Signal improvement time	$t_{SIC}$	450	–	530	ns		P_8.4.20

1) Not subject to production test, specified by design.

2)  $V_{SYM}$  observed during dominant and recessive state and also during the transition from dominant to recessive and vice versa, while TxD is stimulated by a square wave signal. This parameter must be valid for all the possible transmission rates.

## Electrical characteristics

### 7.5 Dynamic transceiver parameters

**Table 11** Electrical characteristics dynamic transceiver parameters

4.75 V <  $V_{CC}$  < 5.25 V; 3.0 V <  $V_{IO}$  < 5.5 V;  $R_L = 60 \Omega$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Loop delay from TxD to RxD	$t_{\text{Loop}}$	80	–	190	ns	$C_1 = 0 \text{ pF}$ ; $C_2 = 100 \text{ pF}$ ; $C_{\text{RxD}} = 25 \text{ pF}$ ; $C_{\text{VCC}} = 100 \text{ nF}$ ; $R_L = 60 \Omega$ ; $V_{\text{TxD}} = \text{rise (10\% to 90\%)}$ and fall (90% to 10%) time < 10 ns; 125 kbit/s < $1/t_{\text{Bit}}$ < 8 Mbit/s; see <a href="#">Figure 12</a> , <a href="#">Figure 13</a>	P_8.5.1
Transmitter propagation delay TxD to bus (“high” until recessive; “low” until dominant)	$t_{\text{prop\_T}}$	30	–	80	ns	$C_1 = 0 \text{ pF}$ ; $C_2 = 100 \text{ pF}$ ; $C_{\text{VCC}} = 100 \text{ nF}$ ; $R_L = 60 \Omega$ ; $V_{\text{TxD}} = \text{rise (10\% to 90\%)}$ and fall (90% to 10%) time < 10 ns; see <a href="#">Figure 12</a> , <a href="#">Figure 13</a>	P_8.5.3
Propagation delay bus to RxD (dominant until “low”; recessive until “high”)	$t_{\text{prop\_R}}$	30	–	110	ns	$C_1 = 0 \text{ pF}$ ; $C_2 = 100 \text{ pF}$ ; $C_{\text{RxD}} = 25 \text{ pF}$ ; $C_{\text{VCC}} = 100 \text{ nF}$ ; $R_L = 60 \Omega$ ; $V_{\text{TxD}} = \text{rise (10\% -> 90\%)}$ and fall (90% -> 10%) time < 10 ns; see <a href="#">Figure 12</a> , <a href="#">Figure 13</a>	P_8.5.4

#### Delay times

Delay time for mode change	$t_{\text{Mode}}$	–	–	20	$\mu\text{s}$	–	P_8.5.5
Transmitter release time after entering normal-operating mode in dominant state	$t_{\text{TxD\_rel}}$	–	–	5	$\mu\text{s}$	–	P_8.5.6
CAN activity filter time	$t_{\text{Filter}}$	0.5	–	1.8	$\mu\text{s}$	–	P_8.5.7
Bus wake-up timeout	$t_{\text{Wake}}$	0.8	–	10	ms	1)	P_8.5.8
Bus wake-up delay time	$t_{\text{WU}}$	–	–	5	$\mu\text{s}$	–	P_8.5.9

## Electrical characteristics

**Table 11** Electrical characteristics dynamic transceiver parameters (cont'd)

4.75 V < V<sub>CC</sub> < 5.25 V; 3.0 V < V<sub>IO</sub> < 5.5 V; R<sub>L</sub> = 60 Ω; -40°C < T<sub>j</sub> < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN FD characteristics							
Loop delay symmetry	$\Delta t_{\text{Bit(RxD)}}$	-30	–	20	ns	$\Delta t_{\text{Bit(RxD)}} = t_{\text{Bit(RxD)}} - t_{\text{Bit(TxD)}}$ ; $C_1 = 0 \text{ pF}$ ; $C_2 = 100 \text{ pF}$ ; $C_{\text{RxD}} = 25 \text{ pF}$ ; $C_{\text{VCC}} = 100 \text{ nF}$ ; $R_L = 60 \text{ }\Omega$ ; $V_{\text{TxD}}$ = rise (10% to 90%) and fall (90% to 10%) time < 10 ns; 125 kbit/s < 1/ $t_{\text{Bit}}$ < 8 Mbit/s; see <a href="#">Figure 12</a> , <a href="#">Figure 13</a>	P_8.5.10
Receiver propagation delay symmetry (received recessive bit width)	$\Delta t_{\text{Rec}}$	-20	–	15	ns	$\Delta t_{\text{Rec}} = t_{\text{Bit(RxD)}} - t_{\text{Bit(Bus)}}$ ; $C_1 = 0 \text{ pF}$ ; $C_2 = 100 \text{ pF}$ ; $C_{\text{RxD}} = 25 \text{ pF}$ ; $C_{\text{VCC}} = 100 \text{ nF}$ ; $R_L = 60 \text{ }\Omega$ ; $V_{\text{TxD}}$ = rise (10% to 90%) and fall (90% to 10%) time < 10 ns; 125 kbit/s < 1/ $t_{\text{Bit}}$ < 8 Mbit/s; see <a href="#">Figure 12</a> , and <a href="#">Figure 14</a>	P_8.5.11
Transmitter propagation delay symmetry (transmitted recessive bit width)	$\Delta t_{\text{Bit(Bus)}}$	-10	–	10	ns	$\Delta t_{\text{Bit(Bus)}} = t_{\text{Bit(Bus)}} - t_{\text{Bit(TxD)}}$ ; $C_1 = 0 \text{ pF}$ ; $C_2 = 100 \text{ pF}$ ; $C_{\text{RxD}} = 25 \text{ pF}$ ; $C_{\text{VCC}} = 100 \text{ nF}$ ; $R_L = 60 \text{ }\Omega$ ; $V_{\text{TxD}}$ = rise (10% to 90%) and fall (90% to 10%) time < 10 ns; 125 kbit/s < 1/ $t_{\text{Bit}}$ < 8 Mbit/s; see <a href="#">Figure 12</a> and <a href="#">Figure 14</a>	P_8.5.12

1) Not subject to production test, specified by design.

Electrical characteristics

7.6 Diagrams

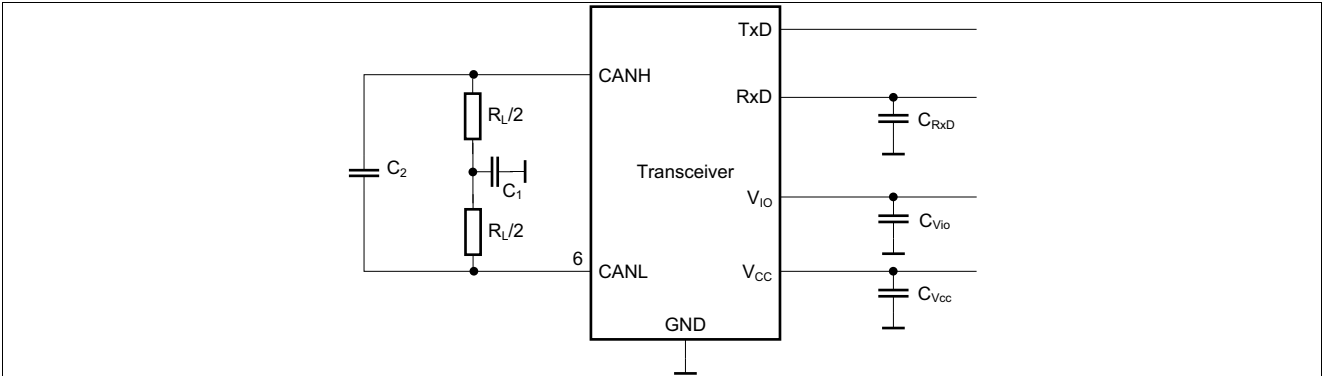


Figure 12 Test circuit

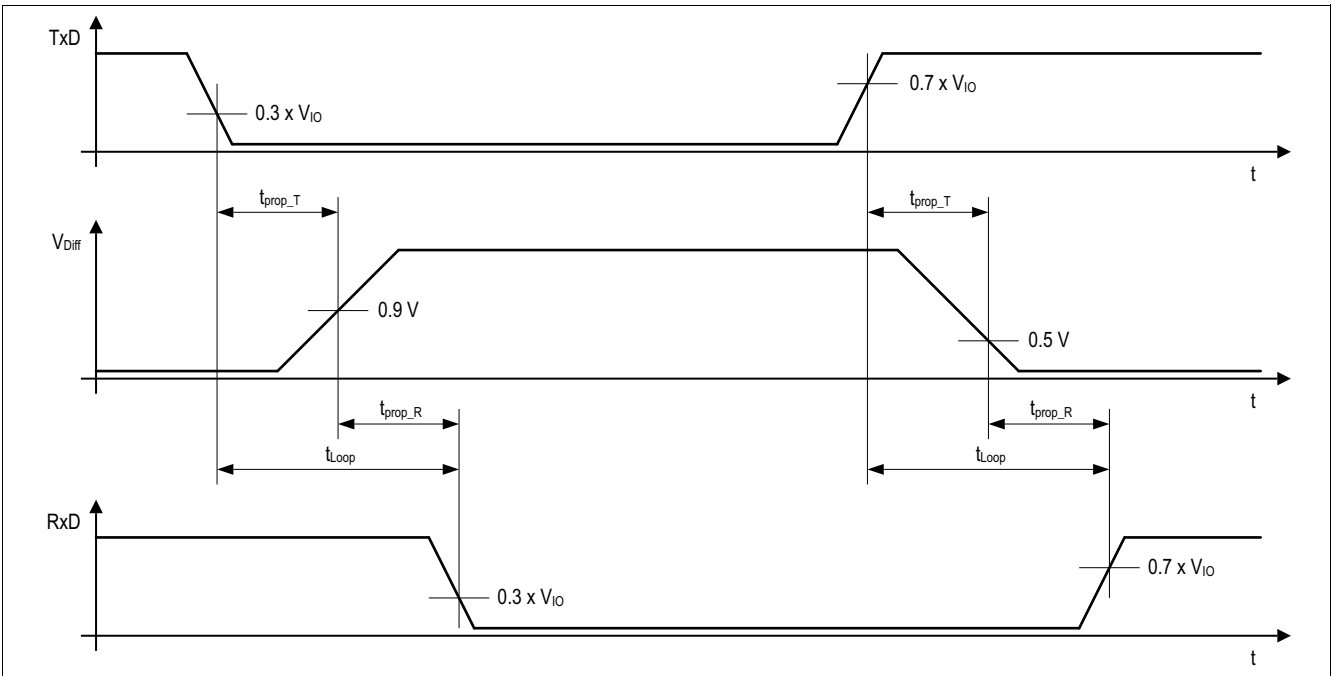


Figure 13 Timing diagram for dynamic characteristics

Electrical characteristics

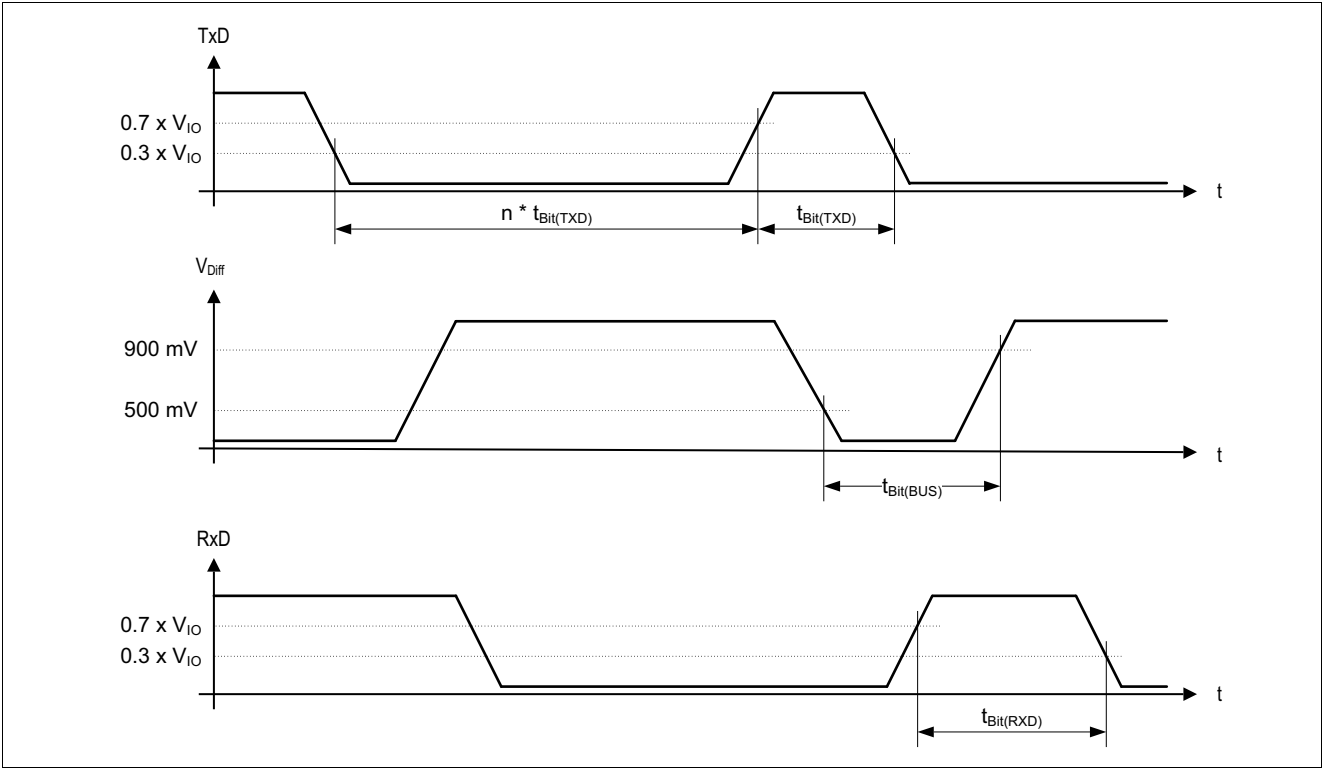


Figure 14 CAN FD electrical parameters

## 8 Application information

### 8.1 ESD robustness according to IEC 61000-4-2

Tests for ESD robustness according to IEC 61000-4-2 Gun test (150 pF, 330  $\Omega$ ) have been performed. The results and test conditions are available in a separate test report.

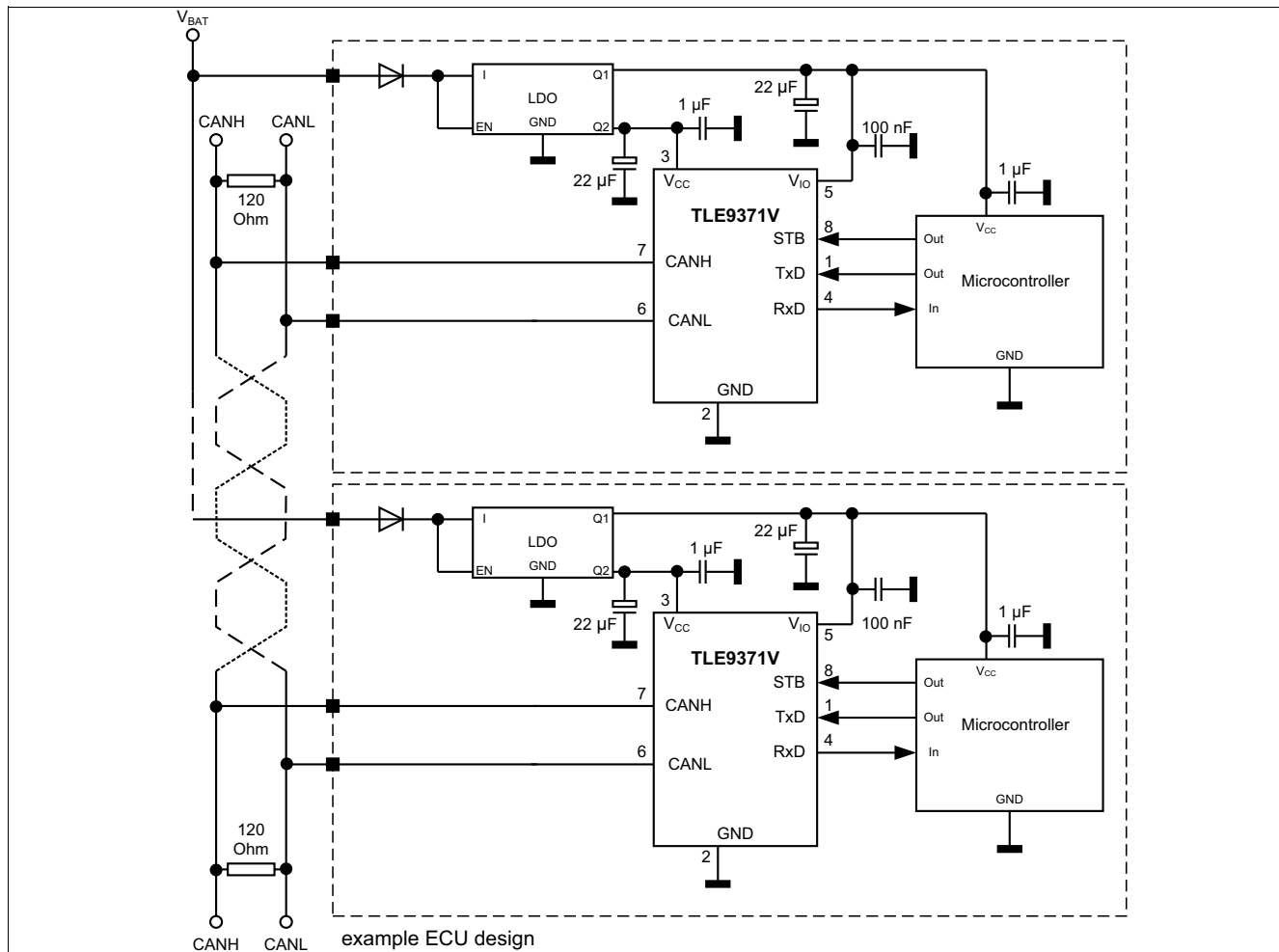
**Table 12 ESD robustness according to IEC 61000-4-2**

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin CANH and CANL versus GND	$\geq +8$	kV	<sup>1)</sup> Positive pulse
Electrostatic discharge voltage at pin CANH and CANL versus GND	$\leq -8$	kV	<sup>1)</sup> Negative pulse

1) Not subject to production test. ESD robustness ESD GUN according to GIFT / ICT paper: "EMC Evaluation of CAN Transceivers, version IEC TS62228", section 4.3. (DIN EN 61000-4-2).

Tested by external test facility IBEE Zwickau – EMC test report available on request.

### 8.2 Application example



**Figure 15 Application diagram**

## **Application information**

### **8.3 Voltage adaption to the microcontroller supply**

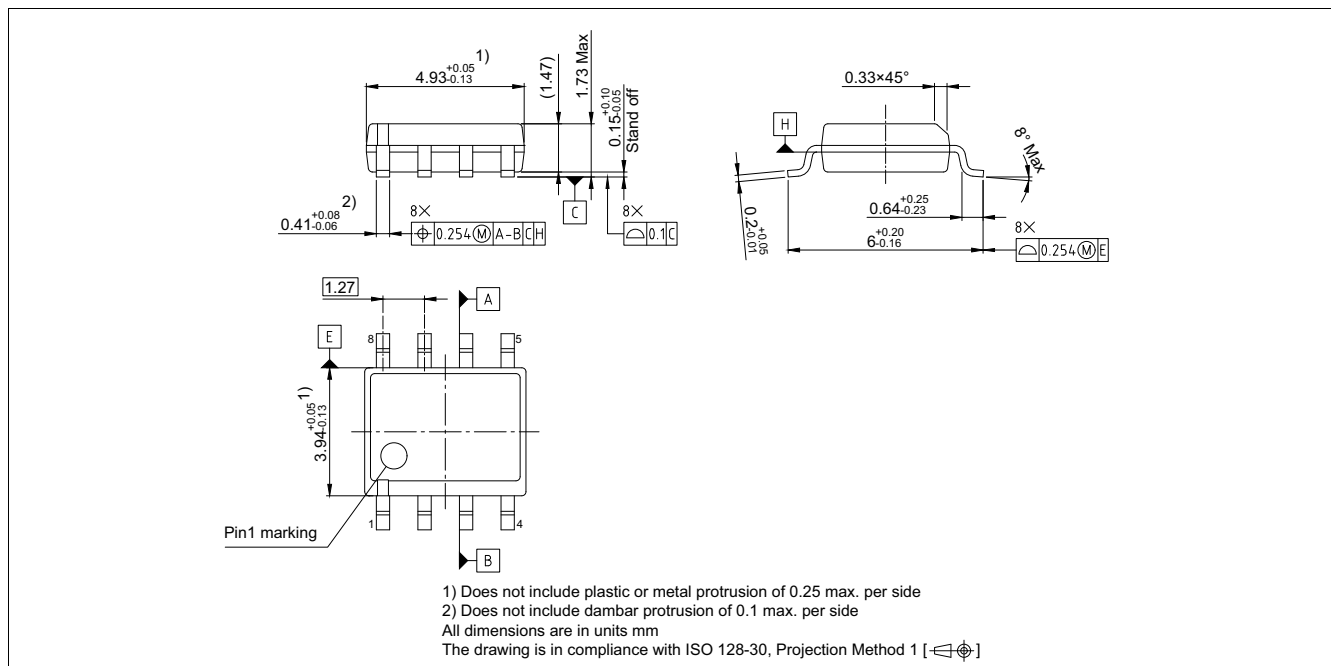
To adapt the levels of the digital input and output of the device to the I/O levels of the microcontroller, connect the power supply pin  $V_{IO}$  to the microcontroller voltage supply, see **Figure 15**.

*Note:* In case no dedicated digital supply voltage  $V_{IO}$  is required in the application, connect the digital supply voltage  $V_{IO}$  to the transmitter supply  $V_{CC}$ .

### **8.4 Further application information**

- For further information you may visit: <http://www.infineon.com/tle9371vsj>

## 9 Package information



**Figure 16 PG-DSO-8**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

<https://www.infineon.com/packages>

**Revision history**

## **10 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.0	2023-02-28	Datasheet created

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