Industrial Temp, Single Port 10/100 Mb/s Ethernet Physical Layer Transceiver

Check for Samples: TLK100

1 Introduction

1.1 Features

- **Temperature From –40°C to 85°C**
- **Low Power Consumption, < 200mW Typical**
- **Cable Diagnostics**
- **Error-Free Operation up to 200 Meters Under Typical Conditions**
- **3.3V MAC Interface**
- **Auto-MDIX for 10/100 Mb/s**
- **Energy Detection Mode**
- **25 MHz Clock Out**
- **MII Serial Management Interface (MDC and MDIO)**
- **IEEE 802.3u MII**
- **IEEE 802.3u Auto-Negotiation and Parallel Detection**
- **IEEE 802.3u ENDEC, 10BASE-T Transceivers and Filters**
- **Bus I/O Protection - ±16kV JEDEC HBM**
- **IEEE 802.3u PCS, 100BASE-TX Transceivers**
- **Enables IEEE1588 Time-Stamping**
- **IEEE 1149.1 JTAG**
- **Integrated ANSI X3.263 Compliant TP-PMD Physical Sublayer with Adaptive Equalization and Baseline Wander Compensation**
- **Programmable LED Support Link, 10/100 Mb/s Mode, Activity, and Collision Detect**
- **10/100 Mb/s Packet BIST (Built in Self Test)**
- **48-pin TQFP Package (7mm) × (7mm)**

1.2 Applications

- **Industrial Controls and Factory Automation**
- **General Embedded Applications**

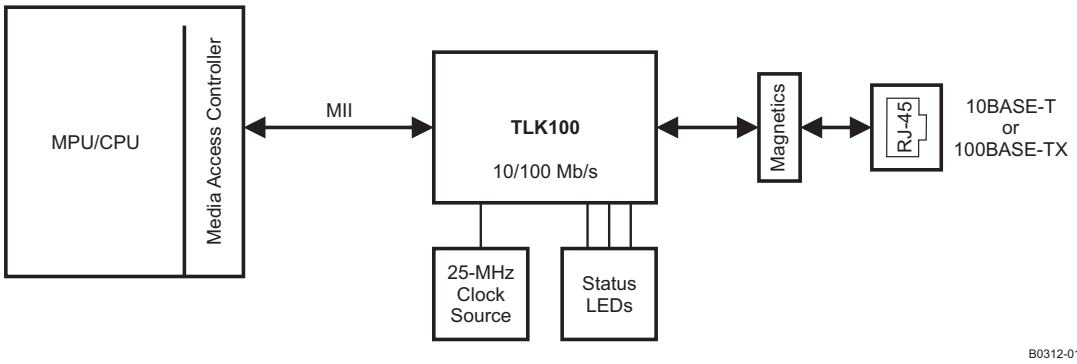
1.3 General Description

The TLK100 is a single-port Ethernet PHY for 10BaseT and 100Base TX signaling. It integrates all the physical-layer functions needed to transmit and receive data on standard twisted-pair cables. This device supports the standard Media Independent Interface (MII) for direct connection to a Media Access Controller (MAC).

The TLK100 is designed for power-supply flexibility, and can operate with a single 3.3V power supply or with combinations of 3.3V, 1.8V, and 1.1V power supplies for reduced power operation.

The TLK100 uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT 5 twisted-pair wiring. It not only meets the requirements of IEEE 802.3, but maintains high margins in terms of cross-talk and alien noise.

1.4 System Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

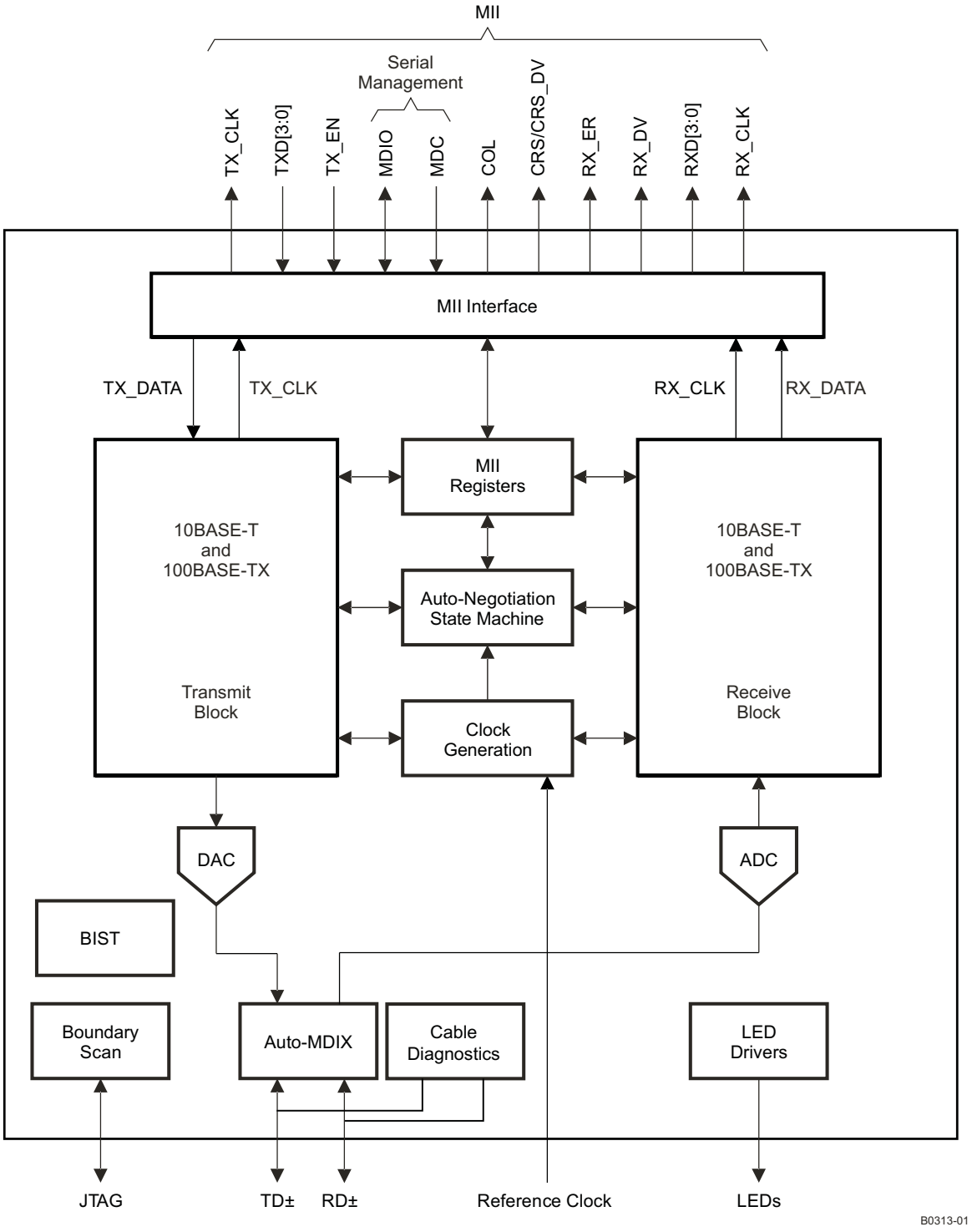
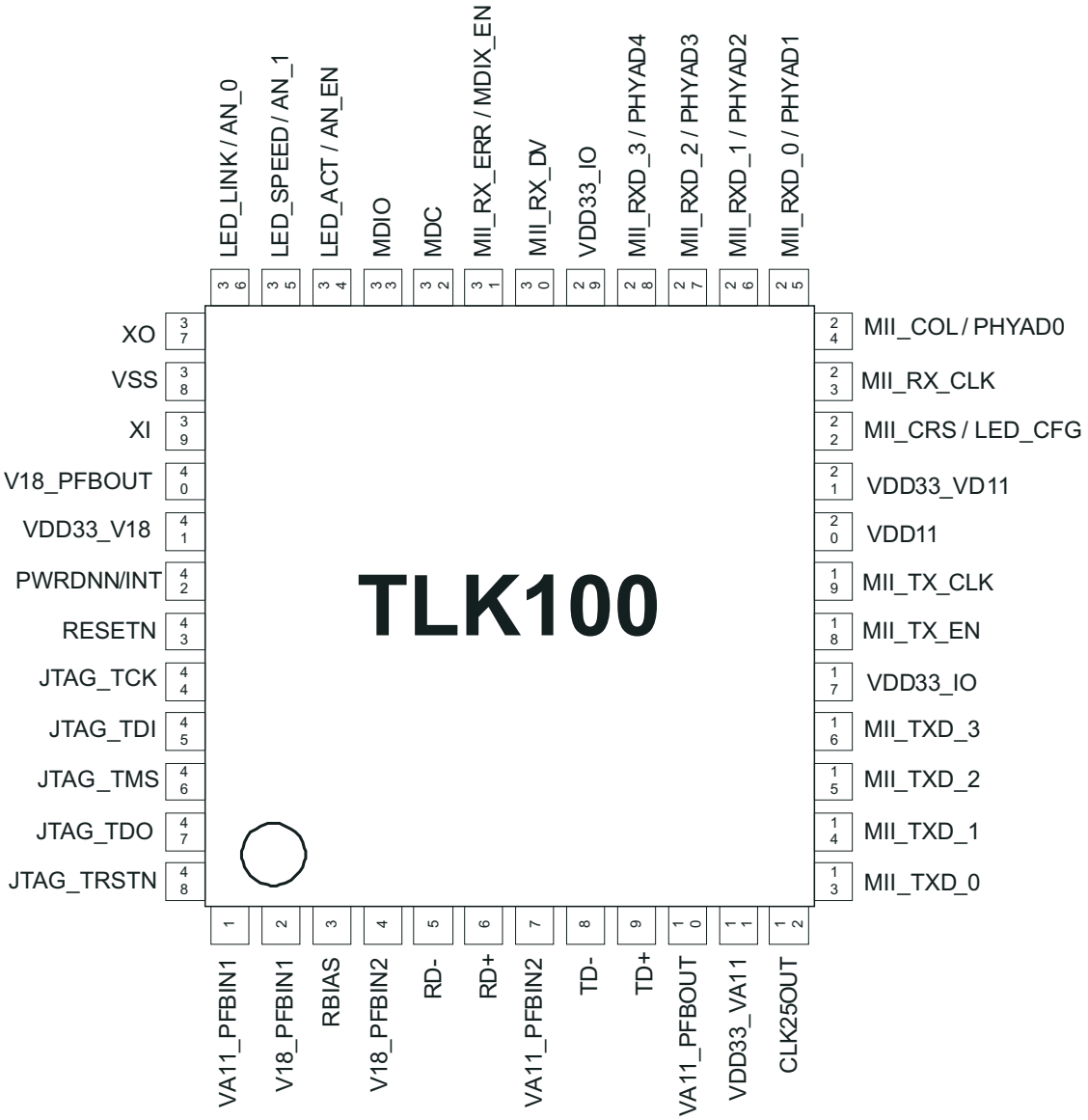


Figure 1-1. TLK100 Functional Block Diagram

1.5 Pin Layout

Figure 1-2. TLK100 PIN DIAGRAM, TOP VIEW



2 Pin Descriptions

The TLK100 pins are classified into the following interface categories (each interface is described in the sections that follow):

- Serial Management Interface
- MAC Data Interface
- Clock Interface
- LED Interface
- JTAG Interface
- Reset and Power Down
- Configuration (Jumper) Options
- 10/100 Mb/s PMD Interface
- Special Connect Pins
- Power and Ground pins

Note: Configuration pin option. See Section 2.7 for *Jumper Definitions*.

The definitions below define the functionality of each pin.

Type: I	Input
Type: O	Output
Type: I/O	Input/Output
Type: OD	Open Drain
Type: PD, PU	Internal Pulldown/Pullup
Type: S	Configuration Pin (All configuration pins have weak internal pullups or pulldowns. If a different default value is needed, then use an external 2.2kΩ resistor. See Section 2.7 for details.)

2.1 Serial Management Interface

PIN		TYPE	DESCRIPTION
NAME	NO.		
MDC	32	I	**MANAGEMENT DATA CLOCK:** Clock signal for the management data input/output (MDIO) interface. The maximum MDC rate is 25 MHz; there is no minimum MDC rate. MDC is **not** required to be synchronous to the MII_TX_CLK or the MII_RX_CLK.
MDIO	33	I/O	**MANAGEMENT DATA I/O:** Bidirectional command / data signal synchronized to MDC. Either the local controller or the TLK100 may drive the MDIO signal. This pin requires a pull-up resistor with value 1.5 kΩ.

2.2 MAC Data Interface

PIN		TYPE	DESCRIPTION
NAME	NO.		
MII_TX_CLK	19	O, PD	**MII TRANSMIT CLOCK:** : MII Transmit Clock provides 25MHz or 2.5MHz reference clock depending on the speed.
MII_TX_EN	18	I, PD	**MII TRANSMIT ENABLE:** MII_TX_EN is presented on the rising edge of the MII_TX_CLK . It indicates the presence of valid data inputs on MII_TXD[3:0]. It is an active high signal.
MII_TXD_0 MII_TXD_1 MII_TXD_2 MII_TXD_3	13 14 15 16	IS, I, PD	**MII TRANSMIT DATA:** The transmit data nibble received from the MAC that is synchronous to the rising edge of the MII_TX_CLK.
MII_RX_CLK	23	O	**MII RECEIVE CLOCK:** MII receive clock provides a 25MHz or 2.5MHz reference clock, depending on the speed, that is derived from the received data stream.
MII_RX_DV	30	S, O, PD	**MII RECEIVE DATA VALID:** This pin indicates valid data is present on the corresponding MII_RXD[3:0].
MII_RX_ERR/MDIX_EN	31	S, O, PU	**MII RECEIVE ERROR**: This pin indicates that an error symbol has been detected within a received packet.
MII_RXD_0/PHYAD1 MII_RXD_1/PHYAD2 MII_RXD_2/PHYAD3 MII_RXD_3/PHYAD4	25 26 27 28	S, O, PD	**MII RECEIVE DATA:** Symbols received on the cable are decoded and presented on these pins synchronous to MII_RX_CLK. They contain valid data when MII_RX_DV is asserted.
MII_CRS/LED_CFG	22	S, O, PU	**MII CARRIER SENSE:** This pin is asserted high when the receive medium is non-idle.
MII_COL/PHYAD0	24	S, O, PU	**MII COLLISION DETECT:** In Full Duplex Mode this pin is always low. In 10BASE-T/100BASE-TX half-duplex modes, this pin is asserted HIGH only when both the transmit and receive media are non-idle.

2.3 Clock Interface

PIN		TYPE	DESCRIPTION
NAME	NO.		
XI	39	I	**CRYSTAL/OSCILLATOR INPUT:** Reference clock. 25MHz ±50 ppm tolerance crystal reference or oscillator input. The TLK100 supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator source connected to pin XI only.
XO	37	O	**CRYSTAL OUTPUT:** Reference Clock output. XO pin is used for crystal only. This pin should be left floating when an oscillator input is connected to XI.
CLK25OUT	12	O	**25 MHz CLOCK OUTPUT:** In MII mode, this pin provides a 25 MHz clock output to the system. This allows other devices to use the reference clock from the TLK100 without requiring additional clock sources.

2.4 LED Interface

(See Table 3-3 for LED Mode Selection)

PIN		TYPE	DESCRIPTION
NAME	NO.		
LED_LINK/AN_0	36	S, O, PU	This pin indicates the status of the link in Mode 1. When the link is good the LED will be ON. In Mode 2 and Mode 3, this pin indicates transmit and receive activity in addition to the status of the Link. The LED is ON when Link is good. It will blink when the transmitter or receiver is active.
LED_SPEED/AN_1	35	S, O, PU	This pin indicates the speed of the link. It is ON when the link speed is 100 Mb/s and OFF when it is 10 Mb/s.
LED_ACT/AN_EN	34	S, O, PU	In mode 1 this pin indicates if there is any activity on the link. It is ON (pulse) when activity is present on either Transmit or Receive channel. In Mode 3, this LED output may be programmed to indicate Full-duplex status.

2.5 JTAG Interface

PIN		TYPE	DESCRIPTION
NAME	NO.		
JTAG_TCK	44	I, PU	This pin is the test clock.This pin has a weak internal pullup.
JTAG_TDI	45	I, PU	This pin is the test data input.This pin has a weak internal pullup.
JTAG_TDO	47	O	This pin is the test data output.
JTAG_TMS	46	I, PU	This pin selects the test mode. This pin has a weak internal pullup.
JTAG_TRSTN	48	I, PU	This pin is an active low asynchronous test reset. This pin has a weak internal pullup.

2.6 Reset and Power Down

PIN		TYPE	DESCRIPTION
NAME	NO.		
RESETN	43	I, PU	This pin is an active Low reset input that initializes or re-initializes all the internal registers of the TLK100. Asserting this pin low for at least 1 µs will force a reset process to occur. All jumper options are reinitialized as well.
PWRDNN/INT	42	I, OD, PU	Register access is required for this pin to be configured either as power down or as an interrupt. The default function of this pin is power down. When this pin is configured for a power down function, an active low signal on this pin will put the device is power down mode. When this pin is configured as an interrupt pin then this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pull-up. Some applications may require an external pull-up resistor.

2.7 Jumper Options

Jumper option is an elegant way to configure the TLK100 into specific modes of operation. Some of the functional pins are used as jumper options. The logic states of these pins are sampled during reset and are used to configure the device into specific modes of operation. Below table shows the pins used for the jumper option and its description. The functional pin name is indicated in parentheses.

A 2.2 kΩ resistor should be used for pull-down or pull-up to change the default jumper option. If the default option is required, then there is no need for external pull-up or pull down resistors. Since these pins may have alternate functions after reset is deasserted, they should not be connected directly to VCC or GND.

<table>
<tr><th colspan="2">PIN</th><th>TYPE</th><th></th></tr>
<tr><th>NAME</th><th>NO.</th><th></th><th>DESCRIPTION</th></tr>
<tr><td>PHYAD0 (MII_COL)
PHYAD1 (MII_RXD_0)
PHYAD2 (MII_RXD_1)
PHYAD3 (MII_RXD_2)
PHYAD4 (MII_RXD_3)</td><td>24
25
26
27
28</td><td>S, O, PD</td><td>The TLK100 provides five PHY address pins, the states of which are latched into an internal register at system hardware reset. The TLK100 supports PHY Address jumpering values 0 (<00000>) through 31 (<11111>). All PHYAD[4:0] pins have weak internal pull-down resistors.</td></tr>
<tr><td>AN_EN (LED_ACT)
AN_1 (LED_SPEED)
AN_0 (LED_LINK)</td><td>34
35
36</td><td>S, O, PU</td><td>AN_EN: When high, this puts the part into advertised Auto-Negotiation mode with the capability set by AN_0 and AN_1 pins. When low, this puts the part into Forced Mode with the capability set by AN_0 and AN_1 pins.

AN_0 / AN_1: These input pins control the forced or advertised operating mode of the TLK100 according to the following table. The value on these pins is set by connecting the input pins to GND (0) or VCC (1) through 2.2 kΩ resistors. These pins should NEVER be connected directly to GND or VCC.

The status of these pins are latched into the Basic Mode Control Register and the Auto_Negotiation Advertisement Register during Hardware-Reset.

The default is 111 since these pins have internal pull-ups.
<table>
<tr><th>AN_EN</th><th>AN_1</th><th>AN_0</th><th>Forced Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>10BASE-T, Half-Duplex</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>10BASE-T, Full-Duplex</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>100BASE-TX, Half-Duplex</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>100BASE-TX, Full-Duplex</td></tr>
<tr><th>AN_EN</th><th>AN_1</th><th>AN_0</th><th>Advertised Mode</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>10BASE-T, Half/Full-Duplex</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>10BASE-TX, Half/Full-Duplex</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>10BASE-T, Half-Duplex
100BASE-TX, Half-Duplex</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>10BASE-T, Half/Full-Duplex
100BASE-TX, Half/Full-Duplex</td></tr>
</table></td></tr>
<tr><td>LED_CFG (MII_CRS)</td><td>22</td><td>S, O, PU</td><td>This jumpering option along with LEDCR register bit determines the mode of operation of the LED pins. Default is Mode 1. All modes are also configurable via register access. See the table in the LED Interface Section.</td></tr>
<tr><td>MDIX_EN (MII_RX_ERR)</td><td>31</td><td>S, O, PU</td><td>This jumpering option sets the Auto-MDIX mode. By default it enables MDIX. An external pull-down will disable Auto-MDIX mode.</td></tr>
</table>

2.8 10 Mb/s and 100 Mb/s PMD Interface

PIN		TYPE	DESCRIPTION
NAME	NO.		
TD–, TD+	8, 9	I/O	Differential common driver transmit output (PMD Output Pair). These differential outputs are automatically configured to either 10BASE-T or 100BASE-TX signaling. In Auto-MDIX mode of operation, this pair can be used as the Receive Input pair. These pins require 1.8V or 3.3V bias for operation.
RD–, RD+	5, 6	I/O	Differential receive input (PMD Input Pair). These differential inputs are automatically configured to accept either 100BASE-TX or 10BASE-T signaling. In Auto-MDIX mode of operation, this pair can be used as the Transmit Output pair. These pins require 1.8V or 3.3V bias for operation.

2.9 Power and Bias Connections

PIN		TYPE	DESCRIPTION
NAME	NO.		
RBIAS	3	I	Bias Resistor Connection. Use a 4.99kΩ 1% resistor connected from RBIAS to GND.
V18_PFBOUT	40	O	1.8V Power Feedback Output. A 1µF capacitor (ceramic preferred), should be placed close to the V18_PFBOUT. In single supply operation, connect this pin should be connected to V18_PFBIN1 and V18_PFBIN2 (pin 2 and pin 4). See Figure 2-1 for proper placement pin. In multiple supply operation, when supplying 1.8V from external supply, this pin should be connected together with VDD33_V18 (pin 41), V18_PFBIN1 and V18_PFBIN2 (pin 2 and pin 4) to the 1.8V external supply source. See Figure 2-2 for proper placement pin.
VA11_PFBOUT	10	O	1.1V Analog Power Feedback Output. A 1 µF capacitor (Ceramic preferred), should be placed close to the VA11_PFBOUT. In single supply operation this pin should be connected to VA11_PFBIN1 and V11_PFBIN2 (pin 1 and pin 7). See Figure 2-1 for proper placement pin. In multiple supply operation, when supplying 1.1V from external supply, this pin should be connected together with VDD33_VA11 (pin 11), V11_PFBIN1 and V11_PFBIN2 (pin 1 and pin 7) to 1.1V external supply source. See Figure 2-3 for proper placement pin.
V18_PFBIN1 V18_PFBIN2	2 4	I	1.8V Power Feedback Input. These pins are fed with power from V18_PFBOUT (pin 40) in single supply operation. 1.8V from external source in multiple supply operation. A small 1µF capacitor should be connected close to each pin.
VA11_PFBIN1 VA11_PFBIN2	1 7	I	1.1V Analog Power Feedback Input. These pins are fed with power from: VA11_PFBOUT (pin 10) in single supply operation. 1.1V from external source in multiple supply operation. A small capacitor of 0.1 µF should be connected close to each pin.
VDD11	20	O	1.1V Core Power Output. A capacitor of 1µF (Ceramic preferred) , should be placed close to the VDD11
VDD33_IO	17 29	P	I/O 3.3V Supply
VDD33_VA11	11	P	External supply input to 1.1V analog regulator This pin should be connected to 3.3V or 2.5V external supply, in single supply operation. In multiple supply operation this pin should be connected to external 1.1V supply source.
VDD33_V18	41	P	External supply input to 1.8V regulator In single supply operation, this pin should be connected to a 3.3V or 2.5V external supply. In multiple supply operation this pin should be connected to an external 1.8V supply source.
VDD33_VD11	21	P	External supply input to 1.1V Core regulator This pin should be connected to 3.3V or 2.5V external supply, in single supply operation. In multiple supply operation this pin should be connected to external 1.1V supply source.
VSS	38	P	Ground pin for Oscillator
GNDPAD	49	P	Ground Pad

2.10 Power Supply Configuration

The TLK100 provides best-in-class flexibility of power supplies.

- Single supply operation – If a single 3.3V power supply is desired, the TLK100 will sense the presence of the supply and configure the internal voltage regulators to provide all necessary supply voltages. To operate in this mode, connect the TLK100 supply pins according to the following scheme:

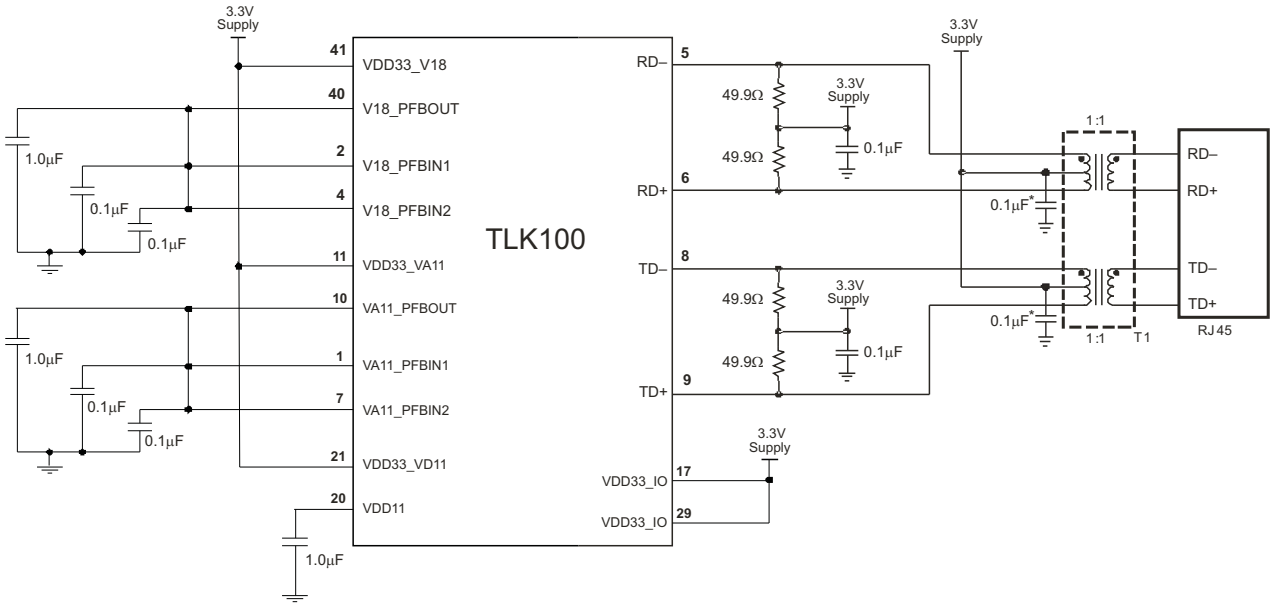


Figure 2-1. Power Scheme for Single Supply Operation

- Multiple Supply operation – When additional 1.8V and/or 1.1V external power rails are available, the TLK100 can be configured in various ways as given in Table 2-1. This gives the highest flexibility for the user and enables significant reduction in power consumption. When using multiple external supplies, the internal regulators must be disabled by appropriate device connections.
  - When an external 1.8V rail is available – Connect the external 1.8V to all following TLK100 pins to enable proper operation: V18_PFBOUT (pin 40), V18_PFBIN1 (pin 2), V18_PFBIN2 (pin 4) and VDD33_V18 (pin 41). In addition, connect the 1.8V rail to the transformer center tap to further reduce the transmission power, as shown in Figure 2-2:

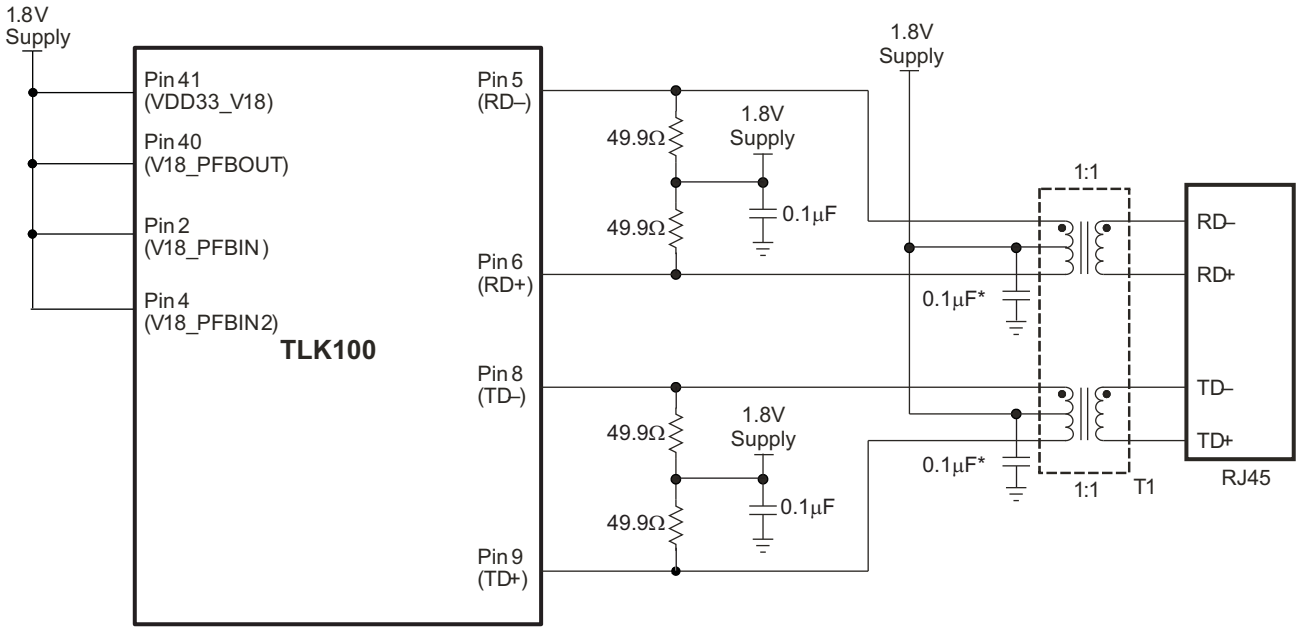


Figure 2-2. Power Scheme for Operation With External 1.8V Supply

– External 1.1V rail – When external 1.1V rail is available – Connect the external 1.1V to the following pins: VA11_PFBOUT (pin 10), VDD11 (pin 20), VA11_PFBIN1 (pin 1), VA11_PFBIN2 (pin 7), VDD33_VA11 (pin 11) and VDD33_VD11 (pin 21) as shown in Figure 2-3:

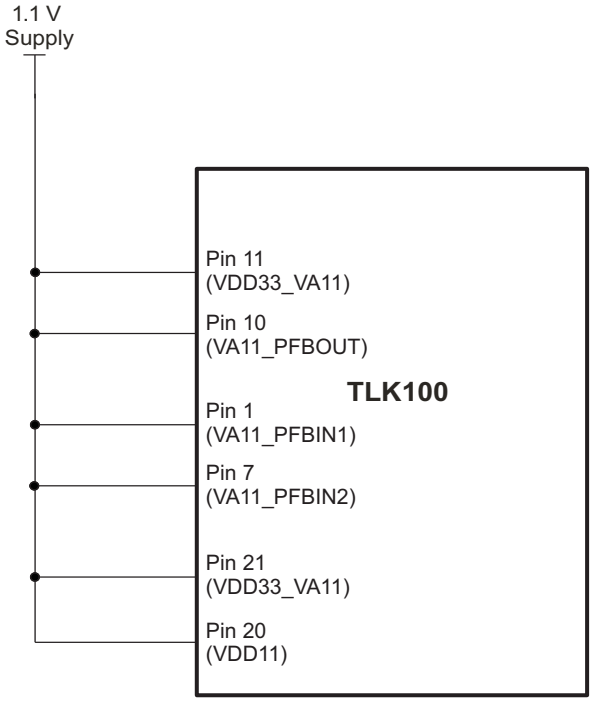


Figure 2-3. Power Scheme for Operation With External 1.1V Supply

- Lowest-power operation – When 1.1V and 1.8V supplies are already available in addition to 3.3V, designers can take advantage of the lowest-power configuration of the TLK100. By supplying external 1.8 and 1.1V as explained above, all the internal regulators are powered down and the device is fully driven by the external supplies giving the lowest power operation.

Other power supply options – Because the TLK100 incorporates independent voltage regulators, designers may take advantage of several optional configurations, depending on available power supplies. See Table 2-1 for these options.

Table 2-1. Power Supply Options

Mode	MAC I/F (3.3V)	Transformer CT (3.3V or 1.8V)	(1.8V)		(1.1V)	
	Voltage Source	Voltage Source	Regulator (ON/OFF)	Voltage Source	Regulators (ON/OFF)	Voltage Source
Single Supply Operation	3.3V from external supply	3.3V from external supply	ON	3.3V from external supply	ON	3.3V from external supply
	3.3V from external supply	3.3V from external supply	ON	3.3V from external supply	ON	2.5V from external supply
	3.3V from external supply	3.3V from external supply	ON	3.3V from external supply	OFF	1.1V from external supply
	3.3V from external supply	3.3V from external supply	ON	2.5V from external supply	ON	3.3V from external supply
	3.3V from external supply	3.3V from external supply	ON	2.5V from external supply	ON	2.5V from external supply
	3.3V from external supply	3.3V from external supply	ON	2.5V from external supply	OFF	1.1V from external supply
	3.3V from external supply	1.8V from external supply	OFF	1.8V from external supply	ON	3.3V from external supply
	3.3V from external supply	1.8V from external supply	OFF	1.8V from external supply	ON	2.5V from external supply
Lowest Power Consumption	3.3V from external supply	1.8V from external supply	OFF	1.8V from external supply	OFF	1.1V from external supply

When operating with multiple supplies, it is recommended that the 3.3V supply ramps up at least 200ms before the 1.8V and 1.1V supplies ramp up.

3 Configuration

This section includes information on the various configuration options available with the TLK100. The configuration options described below include:

- Auto-Negotiation
- Auto-MDIX
- PHY Address
- LED Interface
- Loopback Functionality
- BIST
- Cable Diagnostics

3.1 Auto-Negotiation

The TLK100 device can auto-negotiate to operate in 10BASE-T or 100BASE-TX. If Auto-Negotiation is enabled, then the TLK100 device negotiates with the link partner to determine the speed and duplex with which to operate. If the link partner is unable to Auto-Negotiate, the TLK100 device would go into the parallel detect mode to determine the speed of the link partner. Under parallel detect mode, the duplex mode is fixed at half-duplex.

The TLK100 supports four different Ethernet protocols (10 Mb/s Half Duplex, 10 Mb/s Full Duplex, 100 Mb/s Half Duplex, and 100 Mb/s Full Duplex), so the inclusion of Auto-Negotiation ensures that the highest performance protocol will be selected based on the advertised ability of the Link Partner. The Auto-Negotiation function within the TLK100 can be controlled either by internal register access or by the use of the AN_EN, AN_1 and AN_0 pins.

The state of AN_EN, AN_0 and AN_1 pins determines whether the TLK100 is forced into a specific mode or Auto-Negotiation will advertise a specific ability (or set of abilities) as given in Table 2-1. These pins allow configuration options to be selected without requiring internal register access. The state of AN_EN, AN_0 and AN_1, upon power-up/reset, determines the state of bits [8:5] of the ANAR register (0x04h).

Table 3-1. Auto-Negotiation Modes

AN_EN	AN_1	AN_0	Forced Mode
0	0	0	10BASE-T, Half-Duplex
0	0	1	10BASE-T, Full-Duplex
0	1	0	100BASE-TX, Half-Duplex
0	1	1	100BASE-TX, Full-Duplex
AN_EN	**AN_1**	**AN_0**	**Advertised Mode**
1	0	0	10BASE-T, Half/Full-Duplex
1	0	1	10BASE-TX, Half/Full-Duplex
1	1	0	10BASE-T, Half Duplex 100BASE-TX, Half Duplex
1	1	1	10BASE-T, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex

The Auto-Negotiation function can also be controlled by internal register access using registers as defined by the IEEE 802.3u specification. For further detail regarding Auto-Negotiation, see Clause 28 of the IEEE 802.3u specification.

3.2 Auto-MDIX

The TLK100 device automatically determines whether or not it needs to cross over between pairs so that an external crossover cable is not required. If the TLK100 device interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 determines which device performs the crossover.

Auto-MDIX is enabled by default and can be configured via jumper or via PHYCR (0x10h) register, bits [6:5].

The crossover can be manually forced through bit 5 of PHYCR (0x10h) register. Neither Auto-Negotiation nor Auto-MDIX is required to be enabled in forcing crossover of the MDI pairs.

Auto-MDIX can be used in the forced 100BT mode but not in the forced MDIX mode. As in modern networks all the nodes are 100BT, having the Auto-MDIX working in the forced 100BT mode will resolve the link faster without the need for the long Auto-Negotiation.

3.3 PHY Address

The 5 PHY address inputs pins are shared with the MII_RXD[3:0] pins and COL pin as shown in Table 3-2.

Table 3-2. PHY Address Mapping

PIN #	PHYAD FUNCTION	RXD FUNCTION
24	PHYAD0	MII_COL
25	PHYAD1	MII_RXD_0
26	PHYAD2	MII_RXD_1
27	PHYAD3	MII_RXD_2
28	PHYAD4	MII_RXD_3

Each TLK100 or port sharing an MDIO bus in a system must have a unique physical address. With 5 address input pins, the TLK100 can support PHY Address values 0 (<00000>) through 31 (<11111>). The address-pin states are latched into an internal register at device power-up and hardware reset. Because all the PHYAD[4:0] pins have weak internal pull-down resistors, the default setting for the PHY address is 00000 (0x00h).

See Figure 3-1 for an example of a PHYAD connection to external components. In this example, the PHYAD configuration results in address 00010 (0x02h).

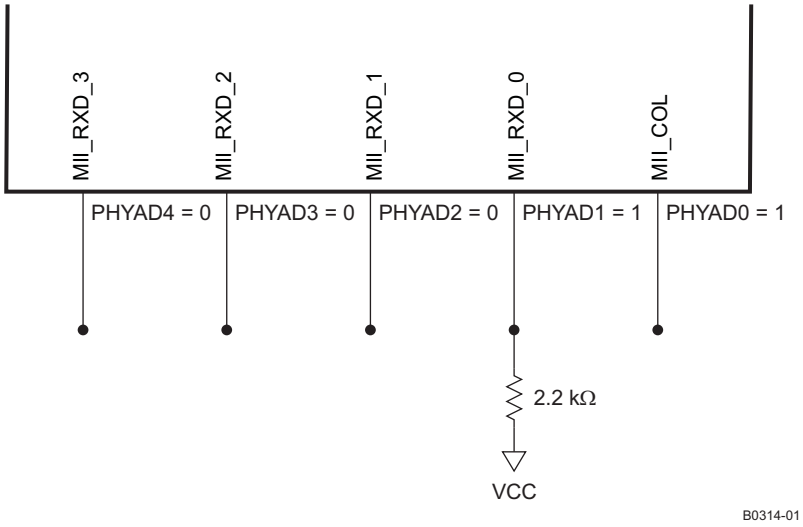


Figure 3-1. PHYAD Configuration Example

3.4 LED Interface

The TLK100 supports three configurable Light Emitting Diode (LED) pins. The device supports three LED configurations: Link, Speed, and Activity. Functions are multiplexed among the LEDs into three modes. The LEDs can be controlled by configuration pin and/or internal register bits. Bits 6:5 of the LED Direct Control register (LEDCR) selects the LED mode as described in Table 3-3.

Table 3-3. LED Mode Select

Mode	LED_CFG[1] (bit 6)	LED_CFG[0] (bit 5) or (pin 22)	LED_LINK	LED_SPEED	LED_ACT
1	don't care	1	ON for Good Link OFF for No Link	ON in 100 Mb/s OFF in 10 Mb/s	ON Pulse for Activity OFF for No Activity
2	0	0	ON for Good Link BLINK for Activity	ON in 100 Mb/s OFF in 10 Mb/s	None
3	1	0	ON for Good Link BLINK for Activity	ON in 100 Mb/s OFF in 10 Mb/s	ON for Full Duplex OFF for Half Duplex

The LED_LINK pin in Mode 1 indicates the link status of the port. It is OFF when no LINK is present. In Mode 2 and Mode 3 it is ON to indicate Link is good and BLINK to indicate activity is present on either transmit or receive channel. The blink rate is decided by the bits 9:8 of the LEDCR register (0x18). The default blink rate is 5Hz.

The LED_SPEED pin indicates 10 or 100 Mb/s data rate of the port. This LED is ON when the device is operating in 100 Mb/s operation. The functionality of this LED is independent of mode selected.

The LED_ACT pin in Mode 1 indicates the presence of either transmit or receive activity. The LED is ON (Pulse) for Activity and OFF for No Activity. The width of the pulse is determined by the bits 14:13 of the LEDCR register (0x18). The default pulse width is 200ms. In mode 3 this pin indicates the Duplex status of operation. The LED is ON for Full Duplex and OFF for Half Duplex.

Bits 2:0 of the LEDCR register defines the polarity of the signals on the LED pins.

Since the Auto-Negotiation (AN) configuration options share the LED output pins, the external components required for configuration-pin programming and those for LED usage must be considered in order to avoid contention.

See Figure 3-2 for an example of AN connections to external components. In this example, the AN programming results in Auto-Negotiation with 10/100 Half/Full-Duplex advertised.

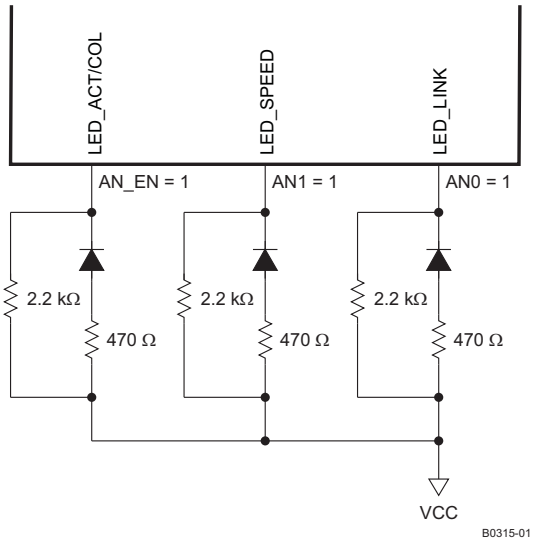


Figure 3-2. AN Pin Configuration and LED Loading Example

3.5 Loopback Functionality

The TLK100 provides several options for Loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the TLK100 digital and analog data path. Generally, the TLK100 may be configured to one of the Near-end loopback modes or to the Far-end (reverse) loopback.

3.5.1 Near-End Loopback

Near-end loopback provides the ability to loop the transmitted data back to the receiver via the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits with several options being provided. Figure 3-3 shows the PHY near-end loopback functionality.

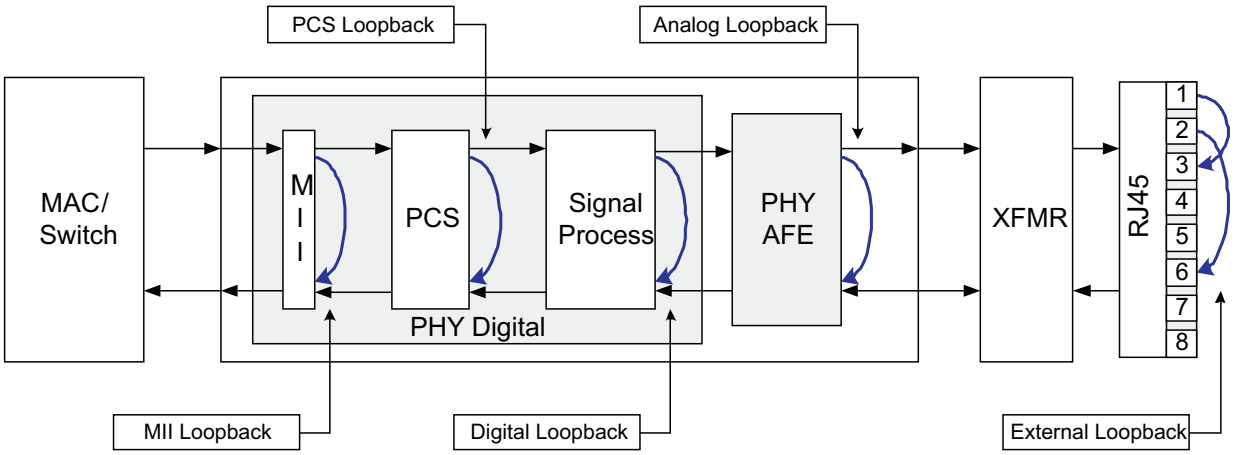


Figure 3-3. Block Diagram, Near-End Loopback Mode

The Near-end Loopback mode is selected by setting the respective bit in the BIST Control Register (BISCR), MII register address 0x16. Bits 3:0 of the BISCR register are used to set the loopback mode according to the following:

- Bit [0]: MII Loopback
- Bit [1]: PCS Loopback (in 100BaseTX only)
- Bit [2]: Digital Loopback
- Bit [3]: Analog Loopback

While in Loopback mode the data is looped back and also transmitted onto the media. To ensure proper operation in Analog Loopback mode 100Ω terminations should be attached to the RJ45 connector.

External Loopback can be performed while working in normal mode (Bits 3:0 of the BISCR register are assert to 0 and on RJ45 connector pin 1 is shorted to pin 3 and pin 2 is shorted to pin 6).

To maintain the desired operating mode, Auto-Negotiation should be disabled before selecting Loopback mode. This is not relevant for external-loopback mode.

3.5.2 Far-End Loopback

Far-end (Reverse) loopback is a special test mode to allow testing the PHY from link partner side. In this mode data that is received from the link partner pass through the PHY's receiver, looped back on the MII and transmitted back to the link partner. Figure 3-4 shows Far-end loopback functionality.

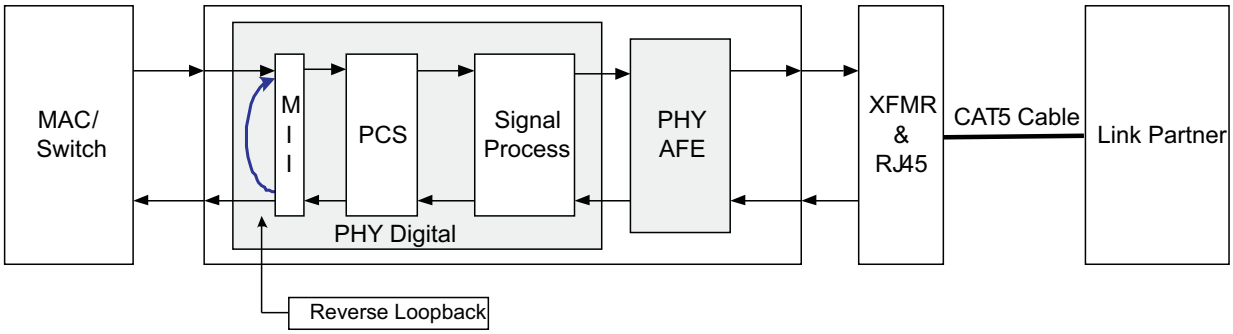


Figure 3-4. Block Diagram, Far-End Loopback Mode

The Reverse Loopback mode is selected by setting bit 4 in the BIST Control Register (BISCR), MII register address 0x16.

While in Reverse Loopback mode the data is looped back and also transmitted onto the MAC Interface and all data signals that come from the MAC are ignored.

3.6 BIST

The TLK100 incorporates an internal PRBS Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be utilized to test the integrity of the transmit and receive data paths. The BIST testing can be performed using both internal loopback (digital or analog) or external loop back using a cable fixture. The BIST simulates a real data transfer scenarios using real packets on the lines. The BIST allows full control of the packets lengths and of the Inter Packet Gap (IPG)

The BIST is implemented with independent transmit and receive paths, with the transmit block generating a continuous stream of a pseudo random sequence. The TLK100 generates a 23-bit pseudo random sequence for doing the BIST test. The received data is compared to the generated pseudo-random data by the BIST Linear Feedback Shift Register (LFSR) to determine the BIST pass/fail status. The number of error bytes that the PRBS checker received is stored in the BISECR register (0x72h).The number of transmitted bytes that the PRBS checker received is stored in the BISBCR register (0x71h). The status of whether the PRBS checker is locked to the incoming receive bit stream, whether the PRBS is in sync or not and whether the packet generator is busy or not can be found by reading the BISSR register (0x17h).

The PRBS test can be put in a continuous mode or single mode by using the bit 15 of the BISCR register (0x16h). In the continuous mode, when one of the PRBS counter reaches the maximum value the counter starts counting from zero again. In the single mode when the PRBS counter reaches its maximum value the PRBS checker stops counting.

TLK100 allows the user to control the length of the PRBS packet. By programming the BISPLR register (0x7Bh) register one can set the length of the PRBS packet. There is also an option to generate a single packet transmission of two types 64 and 1518 bytes through register bit – bit13 of the BISCR register (0x16h). The single generated packet is composed of a constant data.

3.7 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for reliable, comprehensive and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies, and connectors deployed results with the need to non-intrusively identify and report cable faults. TI cable diagnostic unit provides extensive information about cable integrity.

The TLK100 offers the following capabilities in its Cable Diagnostic tools kit:

1. Time Domain Reflectometry (TDR).
2. Active Link Cable Diagnostic (ALCD).
3. Digital Spectrum Analyzer (DSA)

3.7.1 TDR

The TLK100 uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations in addition to estimation of the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, and any other discontinuities on the cable.

The TLK100 device transmits a test pulse of known amplitude (1V) down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, bad connector and the end of the cable itself. After the pulse transmission the TLK100 measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors), and improperly-terminated cables with an accuracy of ±1m.

To do this, the TLK100 uses a RAM with up to 256 samples to record all the input sampled data (Equals to max possible measured cable length of over 200m). The TLK100 also uses soft data averaging to reduce noise and improve accuracy. The TLK100 is capable of recording up to five reflections within the tester pair. In case more than 5 reflections were recorded the TLK100 will save the last 5 of them.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication/addition and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (e.g. CAT5/CAT5e/CAT6).

3.7.2 ALCD

The TLK100 also supports Active Link Cable Diagnostic (ALCD). The ALCD offers a passive method to estimate the cable length during active link. It uses passive digital signal processing based on adapted data thus enabling measurement of cable length with an active link partner.

The ALCD also uses pre-defined parameters according to the cable properties (e.g. CAT5/CAT5e/CAT6) in order to achieve higher accuracy in the estimated cable length. The ALCD Cable length measurement accuracy is +/-5m for the pair used in the Rx path (due to the passive nature of the test we measure only the pair on the Rx path).

3.7.3 DSA

The TLK100 also offers a unique capability of Digital Spectrum Analyzer (DSA). The DSA enables a detailed analysis of the channel frequency response (Magnitude only). The DSA has the following capabilities:

- Produce channel frequency response in resolution of 119.2Hz.
- Save up to 512 bins per DSA run.
- Full control in the analyzed frequency bins location and resolution.
- Programmable options for input data for the DSA:
  - Use raw data taken directly from the channel
  - Use adapted data that passed digital signal processing
- Use additional filtering for smoothing the total channel frequency response.
- Build in averaging for more accurate results

NOTE: For an example of the DSA output please see appendix A

To reset the cable diagnostic registers, set bit 14 of RAMCR2 register (0x0D01) to '1'. Writing software global reset 0x001F bit 15 does not reset the cable diagnostic registers.

4 Interfaces

4.1 Media Independent Interface (MII)

The Media Independent Interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC in 100B-TX and 10B-T modes. The MII is fully compliant with IEEE802.3-2002 clause 22.

The MII consists of the data signals MII_TXD[3:0] and MII_RXD[3:0], transmit and receive valid signals MII_TX_EN and MII_RX_DV, error signal MII_RX_ERR and transmit/receive clocks MII_TX_CLK and MII_RX_CLK. In addition, the interface consists of asynchronous line status signals MII_CRS and MII_COL, indicating carrier sense and collision. Data on MII_TXD[3:0] and MII_RXD[3:0] are latched with reference to the edges of MII_RX_CLK and MII_TX_CLK clocks respectively as defined in the MII timing diagrams 22-14 and 22-15 of IEEE802.3-2002 clause 22. Both clocks are sourced by the PHY. In 100B-TX mode, the MII_RX_CLK and MII_TX_CLK source 25MHz clocks and in 10B-T, they source 2.5MHz clocks.

Figure 4-1 describes the MII signals connectivity.

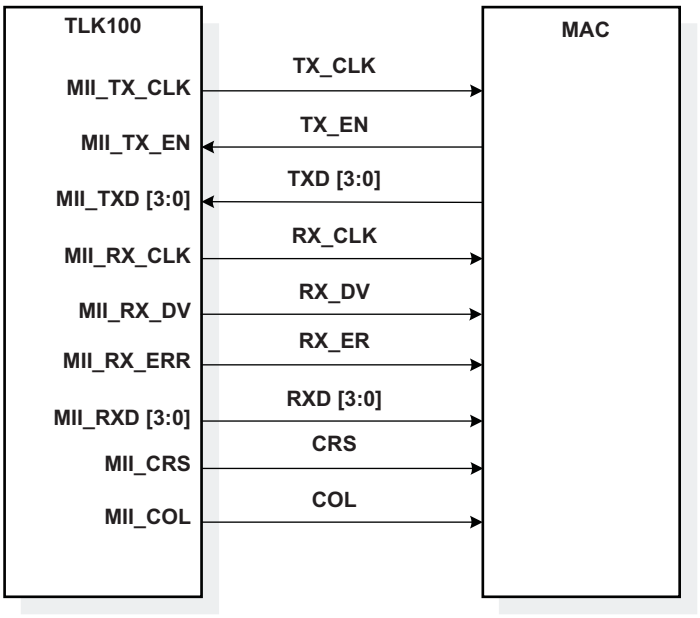


Figure 4-1. MII Signaling

The isolate register 0.10 defined in IEEE802.3-2002 used to electrically isolate the PHY from the MII (if set, all transactions on the MII interface are ignored by the PHY).

Additionally, the MII interface includes the carrier sense signal MII_CRS, as well as a collision detect signal MII_COL. The MII_CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in Half Duplex mode. The MII_COL signal asserts as an indication of a collision which can occur during half-duplex operation when both transmit and receive operation occur simultaneously.

4.2 Serial Management Interface

The Serial Management Interface (SMI), provides access to the TLK100's internal registers space for status information and configuration. The SMI is compatible with IEEE802.3-2002 clause 22. The implemented register set consists of all the registers required by the IEEE802.3-2002 in addition to several others, providing additional visibility and controllability of the TLK100 device.

The SMI includes the MDC management clock input and the management MDIO data pin. The MDC clock is sourced by the external management entity (also referred to as STA), and can run at maximum clock rate of 25MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

The MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC clock. The MDIO pin requires a pull-up resistor (1.5kΩ) which, during IDLE and turnaround, pulls MDIO high.

Up to 32 PHYs can share a common SMI bus. To distinguish between the PHYs, a 5-bit address is used. During power-up reset, the TLK100 latches the PHYAD[4:0] configuration pins (Pin 25 to Pin 28) to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up reset.

To maintain legal operation, SMI bus should remain inactive at least one MDC cycle after hard reset is de-asserted.

In normal MDIO transactions, the register address is taken directly from the management frame's **reg_addr** field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE802.3 and vendor specific). The data field is used for both reading and writing.

The Start code is indicated by a <01> pattern. This makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of Turnaround. The addressed TLK100 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. Figure 4-2 shows the timing relationship between MDC and the MDIO as driven/received by the Station (STA) and the TLK100 (PHY) for a typical register read access.

For write transactions, the station-management entity writes data to the addressed TLK100, thus eliminating the requirement for MDIO Turnaround. The Turnaround time is filled by the management entity by inserting <10>. Figure 4-3 shows the timing relationship for a typical MII register write access. The frame structure and general read/write transactions are shown in Table 4-1, Figure 4-2, and Figure 4-3.

Table 4-1. Typical MDIO Frame Format

MII Management Serial Protocol	<idle><start><op code><device addr><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx><idle>

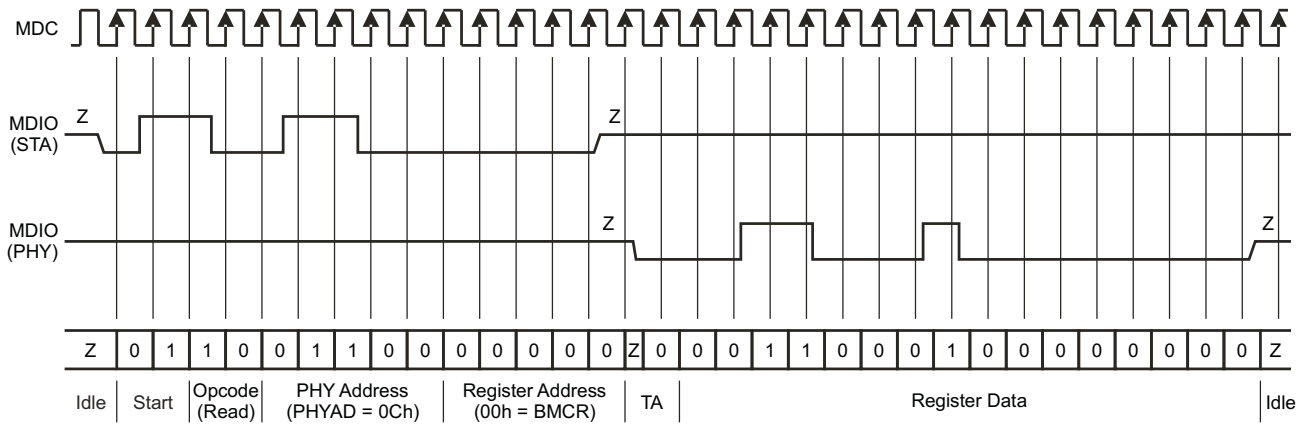


Figure 4-2. Typical MDC/MDIO Read Operation

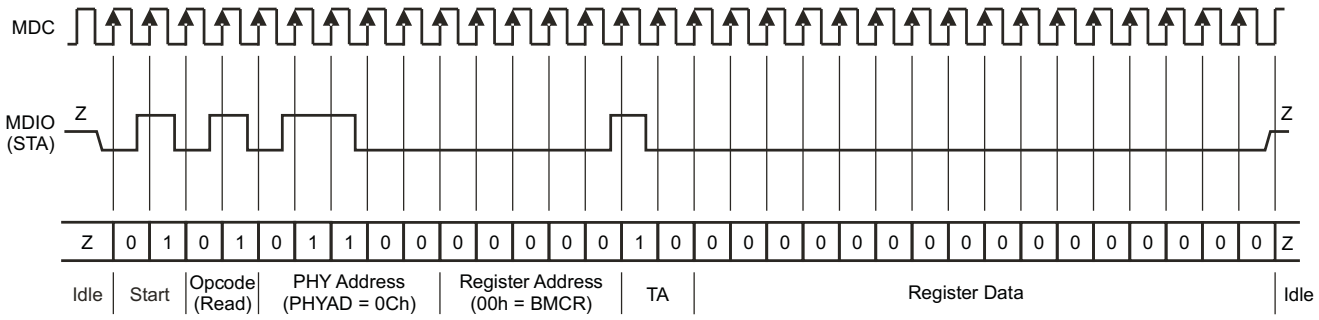


Figure 4-3. Typical MDC/MDIO Write Operation

4.2.1 Extended Address Space Access

The TLK100 SMI function supports read/write access to the extended register set using registers REGCR(0x000Dh) and ADDAR(0x000Eh) and the MDIO Manageable Device (MMD) indirect method defined in IEEE802.3ah Draft for clause 22 for accessing the clause 45 extended register set.

Accessing the standard register set, i.e. MDIO registers 0 to 31, can be performed using the normal direct MDIO access or the indirect method, except for register REGCR(0x000Dh) and ADDAR(0x000Eh) which can be accessed only using the normal MDIO transaction. The SMI function will ignore indirect accesses to these registers.

REGCR(0x000Dh) is the MDIO Manageable MMD access control. In general, register REGCR(4:0) is the device address DEVAD that directs any accesses of ADDAR(0x000Eh) register to the appropriate MMD. Specifically, the TLK100 uses the vendor specific **DEVAD[4:0] = "11111"** for accesses. All accesses through registers REGCR and ADDAR should use this DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address/data MMD register. It is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is 00, then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to 00, accesses to register ADDAR modify the extended register set address register. This address register should always be initialized in order to access any of the register within the extended register set.
- When REGCR[15:14] is set to 01, accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to 10, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to 11, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write accesses only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR.

4.2.1.1 Write Address Operation

To set the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

4.2.1.2 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

4.2.1.3 Write (no post increment) Operation

To write an extended register set register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note: steps (1) and (2) can be skipped if the address register was previously configured.

4.2.1.4 Read (no post increment) Operation

To read an extended register set register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads from register ADDAR (step 4) continue reading the register selected by the value in the address register.

Note: steps (1) and (2) can be skipped if the address register was previously configured.

4.2.1.5 Write (post increment) Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address from register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11. DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register, i.e address register is incremented after each access.

4.2.1.6 Read (post increment) Operation

To read an extended register set register and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register, i.e address register is incremented after each access.

5 Architecture

The TLK100 Fast Ethernet transceiver is physical layer core for Ethernet 100Base-TX and 10Base-T applications. It contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 3 and 5 unshielded twisted pair. The core supports the IEEE 802.3 Standard Fast Media Independent Interface (MII) for direct connection to a MAC/Switch port.

The TLK100 uses mixed signal processing to perform equalization, data recovery and error correction to achieve robust and low power operation over the existing CAT 5 twisted pair wiring. The TLK100 architecture not only meets the requirements of IEEE802.3, but maintains a high level of margin over the IEEE requirements for NEXT and Alien noise.

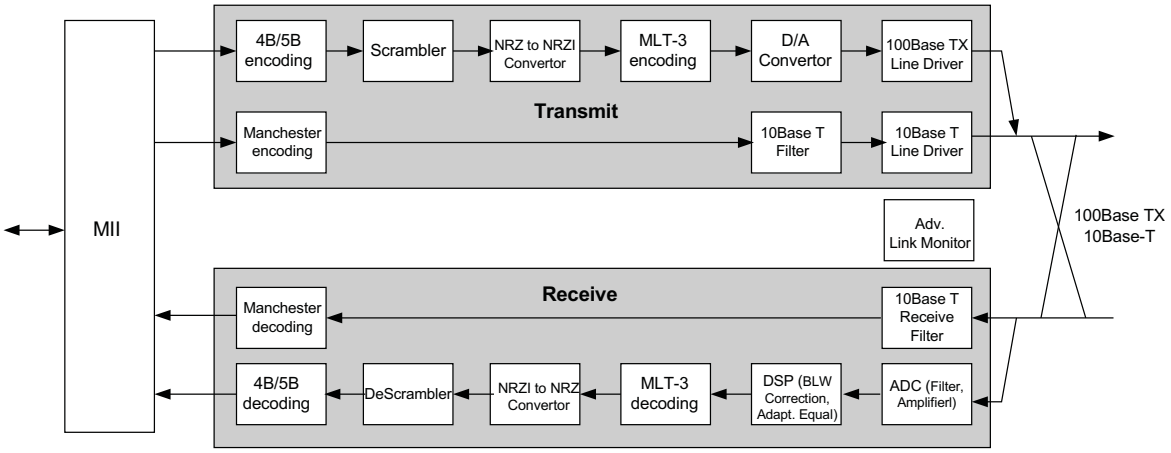


Figure 5-1. PHY Architecture

5.1 Transmit Path Encoder

In 10Base-T, the MAC feeds the 10Mbps transmit data through the MII in 4-bit wide nibbles. The data is serialized using an NRZI converter; Manchester encoded and sent to DAC to be transmitted through one of the twisted pairs of the cable. When no data is available from the MAC, the 10B-T encoder transmits NLP pulses to keep the link alive.

In 100Base-TX, the MAC feeds the 100Mbps transmit data in 4-bit wide nibbles through the MII interface. The data is encoded into 5-bit code groups, encapsulated with control code symbols and serialized. The control-code symbols indicate the start and end of the frame and code other information such as transmit errors. When no data is available from the MAC, IDLE symbols are constantly transmitted. The serialized bit stream is fed into a scrambler. The scrambled data stream passes through an NRZI encoder and then through an MLT3 encoder. Finally, it is fed to the DAC and transmitted through one of the twisted pairs of the cable.

5.1.1 4B/5B Encoding

The transmit data that is received from the MAC first passes through the 4B/5B encoder. This block encodes 4-bit nibble into 5-bit code-groups according to the Table 5-1. Each 4-bit data nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or they are considered as not valid.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4-bit preamble and data nibbles with corresponding 5-bit code-groups. At the end of the transmit packet, upon the de-assertion of Transmit Enable signal from the MAC, the code-group encoder adds the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously adds IDLEs into the transmit data stream until the next transmit packet is detected.

Table 5-1. 4B/5B Code Table

4-Bit Code	Symbol	5-Bit Code
0000	0	11110
0001	1	01001
0010	2	10100
0011	3	10101
0100	4	01010
0101	5	01011
0110	6	01110
0111	7	01111
1000	8	10010
1001	9	10011
1010	A	10110
1011	B	10111
1100	C	11010
1101	D	11011
1110	E	11100
1111	F	11101
IDLE AND CONTROL CODES		
DESCRIPTION	**Symbol(1)**	**5-Bit Code**
Inter-Packet IDLE	I	11111
First nibble of SSD	J	11000
Second nibble of SSD	K	10001
First nibble of ESD	T	01101
Second nibble of ESD	R	00111
Transmit Error Symbol	H	00100
INVALID CODES		
	V	00000
	V	00001
	V	00010
	V	00011
	V	00101
	V	00110
	V	01000
	V	01100

(1) Control code-groups I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.

5.1.2 Scrambler

The purpose of the scrambler is to flatten the power spectrum of the transmitted signal, thus reduce EMI. The scrambler seed is generated with reference to the PHY address so that multiple PHYs that reside within the system will not use the same scrambler sequence.

5.1.3 NRZI and MLT-3 Encoding

To comply with the TP-PMD standard for 100BASE-TX transmission over CAT-5 unshielded twisted pair cable, the scrambled data must be NRZI encoded. The serial binary data stream output from the NRZI encoder is further encoded to MLT-3. MLT-3 is a tri-level code where a change in the logic level represents a code bit '1' and the logic output remaining at the same level represents a code bit '0'.

5.1.4 Digital to Analog Converter

The multipurpose programmable transmit Digital to Analog Converter (DAC) receives digital coded symbols and generates filtered analog symbols to be transmitted on the line. In 100B-TX the DAC applies a low-pass shaping filter to minimize EMI. The DAC is designed to improve the return loss requirements and enable the use of low-cost transformers.

Digital pulse-shape filtering is also applied in order to conform to the pulse masks defined by standard and to reduce EMI and high frequency signal harmonics.

In 10Base-T, the Manchester coded symbols are fed through a pre-equalization filter.

5.2 Receive Path Decoder

In 10B-T, after the far end clock is recovered, the received Manchester symbols pass to the Manchester decoder. The serial decoded bit stream is aligned to the start of the frame, de-serialized to 4-bit wide nibbles and sent to the MAC through the MII.

In 100B-TX, the adaptive equalizer drives the received symbols to the MLT3 decoder. The decoded NRZ symbols are transferred to the descrambler block for de-scrambling and de-serialization.

5.2.1 Analog Front End

The Receiver Analog Front End (AFE) resides in front of the 100B-TX receiver. It consists of an Analog to Digital Converter (ADC), receive filters and a Programmable Gain Amplifier (PGA).

The ADC samples the input signal at the 125MHz clock recovered by the timing loop and feeds the data into the adaptive equalizer. The ADC is designed to optimize the SNR performance at the receiver input while utilizing high power-supply rejection ratio and maintaining low power. There is only one ADC in TLK100, which receives the analog input data from the relevant cable pair, according to MDI-MDIX resolution.

The PGA, digitally controlled by the adaptive equalizer, fully utilizes the dynamic range of the ADC by adjusting the incoming-signal amplitude. Generally, the PGA attenuates short-cable strong signals and amplifies long-cable weak signals.

5.2.2 Adaptive Equalizer

The adaptive equalizer removes Inter-Symbol Interference (ISI) from the received signal introduced by the channel and analog Tx/Rx filters. The TLK100 includes both Feed Forward Equalization (FFE) and Decision Feedback Equalization (DFE). The combination of the both adaptive modules with the adaptive gain control results in a powerful equalizer that can eliminate ISI and compensate over the cable attenuation for cables of up to 200m and even more. In addition, the Equalizer includes a Shift Gear Step mechanism to provide fast convergence on the one hand and small residual-adaptive noise in Steady state on the other hand.

5.2.3 Baseline Wander Correction

The DC offset of the transmitted signal is shifted down or up based on the polarity of the transmitted data because the MLT-3 data is coupled onto the CAT 5 cable through a transformer that is high-pass in nature. This phenomenon is called Baseline wander. To prevent corruption of the received data because of this phenomenon, the receiver corrects the baseline wander and can receive the ANSI TP-PMD defined "killer packet" with no bit errors.

5.2.4 NRZI and MMLT-3 Decoding

The TLK100 decodes the MLT-3 information from the Digital Adaptive Equalizer block to binary NRZI data. The NRZI-to-NRZ decoder is used to present NRZ-formatted data to the descrambler.

5.2.5 Descrambler

The descrambler is used to descramble the received NRZ data. It is further deserialized and the parallelized data is aligned to 5-bit code-groups and mapped into 4-bit nibbles. At initialization, the 100B-TX descrambler uses the IDLE-symbols sequence to lock on the far-end scrambler state. During that time, neither data transmission nor reception is enabled. After the far-end scrambler state is recovered, the descrambler constantly monitors the data and checks whether it still synchronized. If, for any reason, synchronization is lost, the descrambler tries to re-acquire synchronization using the IDLE symbols.

5.2.6 45/5B Decoder

The code-group decoder functions as a look up table that translates incoming 5-bit code-groups into 4-bit nibbles. The code-group decoder first detects the J/K code-group pair preceded by IDLE code-groups and replaces the J/K with a MAC preamble. Specifically, the J/K 10-bit code-group pair is replaced by the nibble pair (0101 0101). All subsequent 5-bit code-groups are converted to the corresponding 4-bit nibbles for the duration of the entire packet. This conversion ceases upon the detection of the T/R code-group pair denoting the End-of-Stream Delimiter (ESD), or on the reception of a minimum of two IDLE code-groups.

5.2.7 Timing Loop and Clock Recovery

The receiver must lock on the far-end transmitter clock in order to sample the data at the optimum timing. The timing loop recovers the far-end clock frequency and offset from the received data samples and tracks instantaneous phase drifts caused by timing jitter.

The TLK100 has a robust adaptive-timing loop (Tloop) mechanism that is responsible for tracking the Far-End TX clock and adjusting the AFE sampling point to the incoming signal. The Tloop implements an advanced tracking mechanism that when combined with different available phases, always keeps track of the optimized sampling point for the data, and thus offers a robust RX path to both PPM and Jitter. The TLK100 is capable of dealing with PPM and jitter at levels far higher than those defined by the standard.

5.2.8 Phase-Locked Loops (PLL)

In 10B-T the digital phase lock loop (DPLL) function recovers the far-end link-partner clock from the received Manchester signal The DPLL is able to combat clock jittering of up to ±18ns and frequency drifts of ±500ppm between the local PHY clock and the far-end clock. The DPLL feeds the decoder with a decoded serial bit stream.

The integrated analog Phase-Locked Loop (PLL) provides the clocks to the analog and digital sections of the PHY. The PLL is driven by an external reference clock (sourced at the XI,XO pins).

5.2.9 Link Monitor

The TLK100 implements the link monitor SM as defined by the IEEE 802.3 100BASE-TX Standard. In addition, the TLK100 enables several add-ons to the link monitor State Machine(SM) activated by configuration bits. These add-ons are supplementary to the IEEE standard and are enabled by default. The new add-ons include the recovery state which enables the PHY to attempt recovery in the event of a temporary energy loss situation or link failure before entering LINK_FAIL state, and thus, restarting the whole link establishment procedure. This allows significant reduction of the recovery time if the temporary link is lost.

To move to the LINK_DOWN state, the link monitor state machine relies on various criteria such as descrambler synchronization failure, SNR, and energy indications. These criteria allow the TLK100 to reach the fast link down time mode when required.

5.2.10 Signal Detect

The signal detect function of the TLK100 is incorporated to meet the specifications mandated by the ANSIFDDI TP-PMD Standard as well as the IEEE 802.3 100BASE-TX Standard for both voltage thresholds and timing parameters.

The energy-detector module provides signal-strength indication in various scenarios. Because it is based on an IIR filter, this robust energy detector has excellent reaction time and reliability. The filter output is compared to predefined thresholds in order to decide the presence or absence of an incoming signal.

The energy detector also implements hysteresis to avoid jittering in the signal-detect indication. In addition it has fully-programmable thresholds and listening-time periods, enabling shortening of the reaction time if required.

5.2.11 Bad SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is any transition from consecutive idle code-groups to non-idle code-groups which is not prefixed by the code-group pair /J/K. If this condition is detected, the TLK100 asserts MII_RX_ERR presents MII_RXD[3:0] = 1110 to the MII for the cycles that correspond to received 5B code-groups until at least two IDLE code groups are detected. In addition, the FCSCR register (0x42h) is incremented by one for every error in the nibble.

When at least two IDLE code groups are detected, RX_ER and MII_CRS become de-asserted.

5.3 10M Squelch

The squelch feature determines when valid data is present on the differential receive inputs. The TLK100 implements a squelch to prevent impulse noise on the receive inputs from being mistaken for a valid signal. Squelch operation is independent of the 10BASE-T operating mode. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BASE-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of a packet is checked by the squelch, and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) are rejected. When this first squelch level is exceeded correctly, the opposite squelch level must then be exceeded no earlier than 50ns. Finally, the signal must again exceed the original squelch level no earlier than 50ns to qualify as a valid input waveform, and not be rejected. This checking procedure results in the typical loss of three preamble bits at the beginning of each packet. When the transmitter is operating, five consecutive transitions are checked before indicating that valid data is present. At this time, the squelch circuitry is reset.

5.3.1 Collision Detection

When in Half-Duplex mode, a 10BASE-T collision is detected when receive and transmit channels are active simultaneously. Collisions are reported by the MII_COL signal on the MII.

The MII_COL signal remains set for the duration of the collision. If the PHY is receiving when a collision is detected, it is reported immediately (through the MII_COL pin).

5.3.2 Carrier Sense

Carrier Sense (MII_CRS) may be asserted due to receive activity after valid data is detected via the squelch function. For 10Mb/s Half Duplex operation, MII_CRS is asserted during either packet transmission or reception. For 10Mb/s Full Duplex operation, MII_CRS is asserted only during receive activity.

MII_CRS is de-asserted following an end-of-packet.

5.3.3 Jabber Function

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition. The jabber function monitors the TLK100 output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 100ms.

When disabled by the Jabber function, the transmitter stays disabled for the entire time that the ENDEC module's internal transmit enable is asserted. This signal must be de-asserted for approximately 500ms (the *unjab* time) before the Jabber function re-enables the transmit outputs.

The Jabber function is only available and active in 10BASE-T mode.

5.3.4 Automatic Link Polarity Detection and Correction

Swapping the wires within the twisted pair causes polarity errors. Wrong polarity affects the 10B-T PHYs. The 100B-TX is invulnerable to polarity problems because it uses MLT3 encoding. The 10B-T automatically detects reversed polarity according to the received link pulses or data.

5.3.5 10Base-T Transmit and Receive Filtering

External 10BASE-T filters are not required when using the TLK100, as the required signal conditioning is integrated into the device. Only isolation transformers and impedance matching resistors are required for the 10BASE-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated by at least 30dB.

5.3.6 10Base-T Operational Modes

The TLK100 has two basic 10BASE-T operational modes:

- Half Duplex mode – In Half Duplex mode the TLK100 functions as a standard IEEE 802.3 10BASE-T transceiver supporting the CSMA/CD protocol.
- Full Duplex mode – In Full Duplex mode the TLK100 is capable of simultaneously transmitting and receiving without asserting the collision signal. The TLK100 10 Mb/s ENDEC is designed to encode and decode simultaneously.

5.4 Auto MDI/MDI-X Crossover

The auto MDI/MDI-X crossover function detects wire crossover (also referred to as MDI/MDI-X). It automatically performs the pair swaps such that each transmitter is connected to its link partner receiver and vice versa, without using an external crossed cable. The auto MDI/MDI-X crossover function is capable of establishing a link with PHYs that do not implement a cross over mechanism.

Table 5-2. MDI/MDI-X Pair Swaps Combinations

PIN	MDI		MDI-X	
	10B-T	100B-TX	10B-T	100B-TX
TD± (pin 8,9)	TD	TD	RD	RD
RD± (pin 5,6)	RD	RD	TD	TD

Detecting link pulses or energy on one or more of the MDI pins determines the crossover state and whether there is a need to perform a swap. If both link partners implement the MDI/MDI-X crossover, then a random algorithm, compliant with one described in IEEE 802.3 section 40.4.4 is used. If the other link partner is a legacy 10B-T PHY then the same algorithm is used. If the other link partner is a legacy 100B-TX PHY, then the crossover state is determined according to the signal detection function.

As described, the link partners' configuration and abilities, whether they use the auto negotiation and/or activate a crossover mechanism, greatly influence the method picked by the crossover function to

determine if and how to cross. In some of the configurations, there may be situations in which the link is not established. Particularly, it may occur if the TLK100 is forced to operate in 10B-T or 100B-TX modes (auto-negotiation is disabled) and the other link partner activates auto-negotiation. For that reason, it is recommended to disable the auto MDI/MDI-X function prior to disabling the auto-negotiation. However, the user has the full ability to control the auto negotiation and the auto MDI/MDIX independently.

The cross-over mechanism can be turned off and forced to the MDI or MDI-X state by setting configuration pin MDIX_EN (Pin 31), whose state is latched during power-up reset. When MDIX_EN is set to '0', then the crossover mechanism is disabled and the PHY operates in MDI or MDI/X mode respectively. If the pin is set to '1', then the cross-over mechanism is enabled and MDI/MDI-X state is selected during operation.

The auto MDI/MDI-X crossover function is controlled by register PHYCR(0x10) bits [6:5]. MDI/MDI-X status can be read through register PHYSR(0x11) bit 8.

5.5 Auto Negotiation

5.5.1 Operation

The auto negotiation function, described in detail in IEEE802.3 chapter 28, provides the means to exchange information between two devices and automatically configure both of them to take maximum advantage of their abilities. The auto negotiation uses the 10B-T link pulses. It encapsulates the transmitted data in sequence of pulses, also referred to as a Fast Link Pulses (FLP) burst. The FLP Burst consists of a series of closely spaced 10B-T link integrity test pulses that form an alternating clock/data sequence. Extraction of the data bits from the FLP Burst yields a Link Code Word that identifies the operational modes supported by the remote device, as well as some information used for the auto negotiation function's handshake mechanism.

The information exchanged between the devices during the auto-negotiation process consists of the devices' abilities such as duplex support and speed. It allows higher levels of the network (MAC) to send to the other link partner vendor-specific data (via the Next Page mechanism, see below), and provides the mechanism for both parties to agree on the highest performance mode of operation.

When auto negotiation has started, the TLK100 transmits FLP on one twisted pair and listens on the other, thus trying to find out whether the other link partner supports the auto negotiation function as well. The decision on what pair to transmit/listen depends on the MDI/MDI-X state. If the other link partner activates auto negotiation, then the two parties begin to exchange their information. If the other link partner is a legacy PHY or does not activate the auto negotiation, then the TLK100 uses the parallel detection function, as described in IEEE802.3 chapters 40 and 28, to determine 10B-T or 100B-TX operation modes. BMCR Register bit 6 reports whether the link was established using the auto negotiation or parallel detection functions.

5.5.2 Initialization and Restart

The TLK100 initiates the auto negotiation function if it is enabled through the configuration jumper options AN_EN, AN_1 and AN_0 (pins 34,35,36) and one of the following events has happened:

1. Hardware reset de-assertion.
2. Software reset (via register).
3. Auto negotiation restart (via register BMCR (0x0000h) bit 9).
4. Power-up sequence (via register BMCR (0x0000h) bit 11).

The auto-negotiation function is also initiated when the auto-negotiation enable bit is set in register BMCR (0x0000h) bit 12 and one of the following events has happened:

1. Software restart.
2. Transitioning to *link_fail* state, as described in IEEE802.3.

To disable the auto-negotiation function during operation, clear register BMCR (0x0000h) bit 12. During operation, setting/resetting this register does not affect the TLK100 operation. For the changes to take place, issue a restart command through register BMCR (0x0000h) bit 9.

5.5.3 Configuration Bits

The auto-negotiation options can be configured through the configuration bits AN_EN, AN_1 and AN_0 as described in Table 5-3. The configuration bits allow the user to disable/enable the auto negotiation, and select the desirable advertisement features.

During hardware/software reset, the values of these configuration bits are latched into the auto-negotiation registers and available for user read and modification.

Table 5-3. Auto-Negotiation Modes

AN_EN	AN_1	AN_0	Forced Mode
0	0	0	10BASE-T, Half-Duplex
0	0	1	10BASE-T, Full-Duplex
0	1	0	100BASE-TX, Half-Duplex
0	1	1	100BASE-TX, Full-Duplex
AN_EN	**AN1**	**AN0**	**Advertised Mode**
1	0	0	10BASE-T, Half/Full-Duplex
1	0	1	10BASE-TX, Half/Full-Duplex
1	1	0	10BASE-T,Half-Duplex 100BASE-TX, Half-Duplex
1	1	1	10BASE-T,Half/Full-Duplex 100BASE-TX, Half/Full-Duplex

5.5.4 Next Page Support

The TLK100 supports the optional feature of the transmission and reception of auto-negotiation additional (vendor specific) next pages.

If next pages are needed, then the user must set register ANAR(0x0004h) bit 15 to '1'. The next pages are then sent and received through registers ANNPTR(0x0007h) and ANLNPTR(0x0008h), respectively. The user must poll register ANER(0x0006h) bit 1 to check whether a new page has been received, and then read register ANLNPTR for the received next page's content. Only after register ANLNPTR is read may the user write to register ANNPTR the next page to be transmitted. After register ANNPTR is written, new next pages overwrite the contents of register ANLNPTR.

If register ANAR(0x0004h) bit 15 is set, then the next page sequence is controlled by the user, meaning that the auto-negotiation function always waits for register ANNPTR to be written before transmitting the next page.

If additional user-defined next pages are transmitted and the link partner has more next pages to send, it is the user's responsibility to keep writing null pages (of value 0x2001) to register ANNPTR until the link partner notifies that it has sent its last page (by setting bit 15 of its transmitted next page to zero).

6 Reset and Power Down Operation

At power up it is recommended to have the external reset pin (RESETN) active (low). The RESETN pin should be de-asserted 200µs after the power is ramped up to allow the internal circuits to settle and for the internal regulators to be stabilized. If required during normal operation, the device can be reset by a hardware or software reset.

6.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1µs, to the RESETN. This will reset the device such that all registers will be reinitialized to default values and the hardware configuration values will be re-latched into the device (similar to the power-up/reset operation).

6.2 Software Reset

A software reset is accomplished by setting the reset bit (bit 15) of the BMCR register (0x00h). This bit only resets the IEEE defined standard registers in the address space 0x00h to 0x07h. The software global reset is accomplished by setting bit 15 of register PDN (0x001F) to '1'. This bit resets IEEE defined registers (0x00h to 0x07h) and all the extended registers except for the cable-diagnostic registers and RAM registers. For resetting the cable diagnostics and RAM registers, bit 14 of register RAMCR2 (0x0D01) should be set to '1'. The time from the point when the reset bit is set to the point the when software reset has concluded is approximately 1.3 µs.

The software global reset resets the device such that all registers are reset to default values and the hardware configuration values are maintained. Software driver code must wait 3 µs following a software reset before allowing further serial MII operations with the TLK100.

6.3 Power Down/Interrupt

The Power Down and Interrupt functions are multiplexed on pin 42 of the device. By default, this pin functions as a power down input and the interrupt function is disabled. This pin can be configured as an interrupt output pin by setting bit 15 (INTN_OE) to '1' and bit 12 (INTN_OEN) to '0' of the MINTCR (0x14h) register. Bit 13 of the same MINTCR register is used to set the polarity of the interrupt.

6.3.1 Power Down Control Mode

The PWRDNN/INT pin can be asserted low to put the device in a Power Down mode. An external control signal can be used to drive the pin low, overcoming the weak internal pull-up resistor. Alternatively, the device can be configured to initialize into a Power Down state by use of an external pulldown resistor on the PWRDNN/INT pin.

6.3.2 Interrupt Mechanisms

The interrupt function is controlled via register access. All interrupt sources are disabled by default. The MINTMR register provides independent interrupt enable bits for the different interrupts supported by TLK100. The PWRDNN/INT pin is asynchronously asserted low when an interrupt condition occurs. The source of the interrupt can be determined by reading the interrupt status register MINTSR (0x13h). One or more bits in the MINTSR will be set, denoting all currently pending interrupts. Reading of the MINTSR clears ALL pending interrupts.

6.4 Power Down Modes

TLK100 supports four types of power saving modes. The lowest power consumption is in the "Extreme Low Power" mode (ELP). To enter into the ELP mode the PWRDNN/INT pin is pulled LOW.

To enable the power-down modes described below, set bit 11 of register BMCR (0x00h) to '1'. In all power-down modes, the entire PHY is powered down except for the SMI interface; the PHY stays in that condition as long as the value of bit 11 of register BMCR (0x00h) remains '1'. When this bit is cleared, the PHY powers up and returns to the last state it was in before it was powered down.

In General Power Down mode, bits 9 and 8 of the PHYCR register (0x10h) should be set to "01". Additionally, bit 4 of the PHYCR register (0x10h) should be set to '1' so as to power down the internal PLL. The SMI would operate on the reference clock.

In Active sleep mode, or Energy-Detect mode, every 1.4 seconds a Normal Link Pulse (NLP) is sent to wake up the link-partner. To enter into the active sleep mode, bits 9 and 8 of register PHYCR (0x10h) is set to "10". Automatic powerup is done when the link partner is detected.

In passive sleep mode, all core blocks are powered down. Automatic power-up is done when the link partner is detected. To enter into the passive sleep mode, bits 9 and 8 of register PHYCR (0x10h) is set to "11".

7 Design Guidelines

7.1 TPI Network Circuit

Figure 7-1 shows the recommended circuit for a 10/100 Mb/s twisted pair interface. Below is a partial list of recommended transformers. It is important that the user realize that variations with PCB and component characteristics require that the application be tested to verify that the circuit meets the requirements of the intended application.

- Pulse H1102
- Pulse HX1188

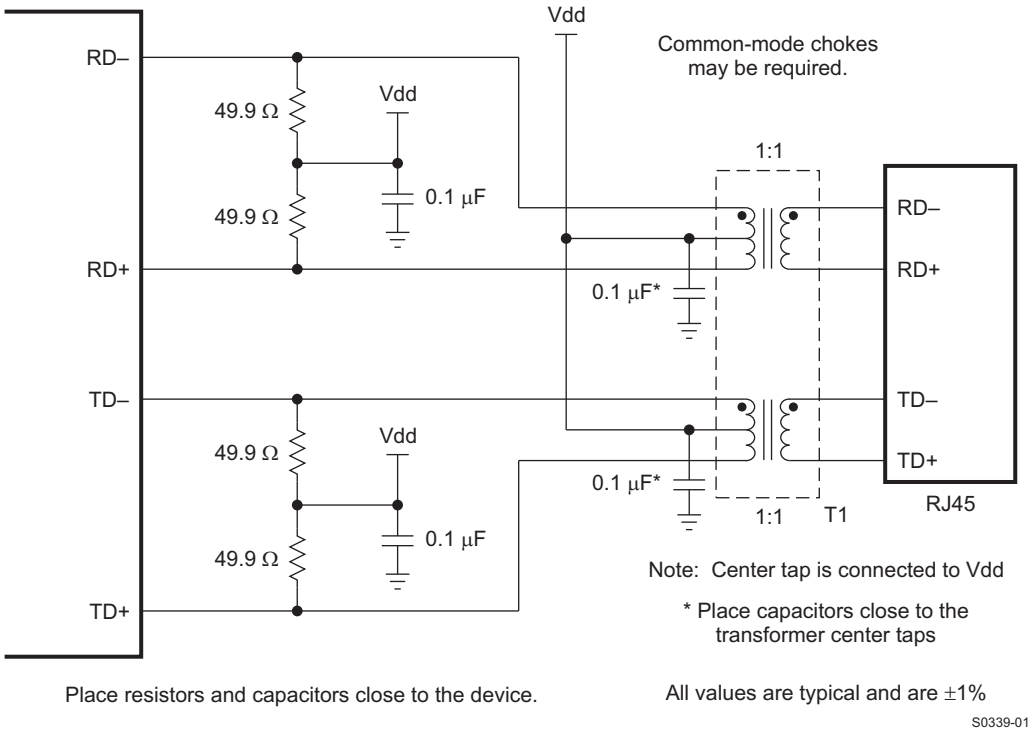


Figure 7-1. 10/100 Mb/s Twisted Pair Interface

7.2 Clock In (XI) Requirements

The TLK100 supports an external CMOS-level oscillator source or an internal oscillator with an external crystal.

7.2.1 Oscillator

If an external clock source is used, XI should be tied to the clock source and XO should be left floating. The amplitude of the oscillator should be a nominal voltage of 1.8V.

7.2.2 Crystal

The use of a 25MHz, parallel, 20pF-load crystal resonator is recommended if a crystal source is desired. Figure 7-2 shows a typical connection for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads.

The oscillator circuit is designed to drive a parallel resonance AT-cut crystal with a minimum drive level of 100µW and a maximum of 500µW. If a crystal is specified for a lower drive level, a current limiting resistor should be placed in series between XO and the crystal.

As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, set the values for C_{L1} and C_{L2} at 33pF, and R_1 should be set at 0Ω.

Specification for 25MHz crystal are listed in Table 7-2.

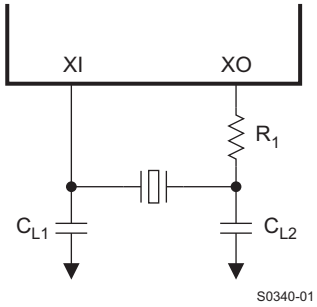


Figure 7-2. Crystal Oscillator Circuit

Table 7-1. 25 MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm
Rise / Fall Time	10%–90%			8	nsec
Jitter (Short term)	Cycle-to-cycle		50		psec
Jitter (Long term)	Accumulative over 10 ms			1	nsec
Symmetry	Duty Cycle	40%		60%	
Load Capacitance			15	30	pF

Table 7-2. 25 MHz Crystal Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
	At 25°C			±50	ppm
Frequency Stability	1 year aging			±5	ppm
Load Capacitance		10		40	pF

7.3 Thermal Vias Recommendation

The following thermal via guidelines apply to GNDPAD, pin 49:

1. Thermal via size = 0.2 mm
2. Recommend 4 vias
3. Vias have a center to center separation of 2 mm.

Adherence to this guideline is required to achieve the intended operating temperature range of the device. Figure 7-3 illustrates an example layout.

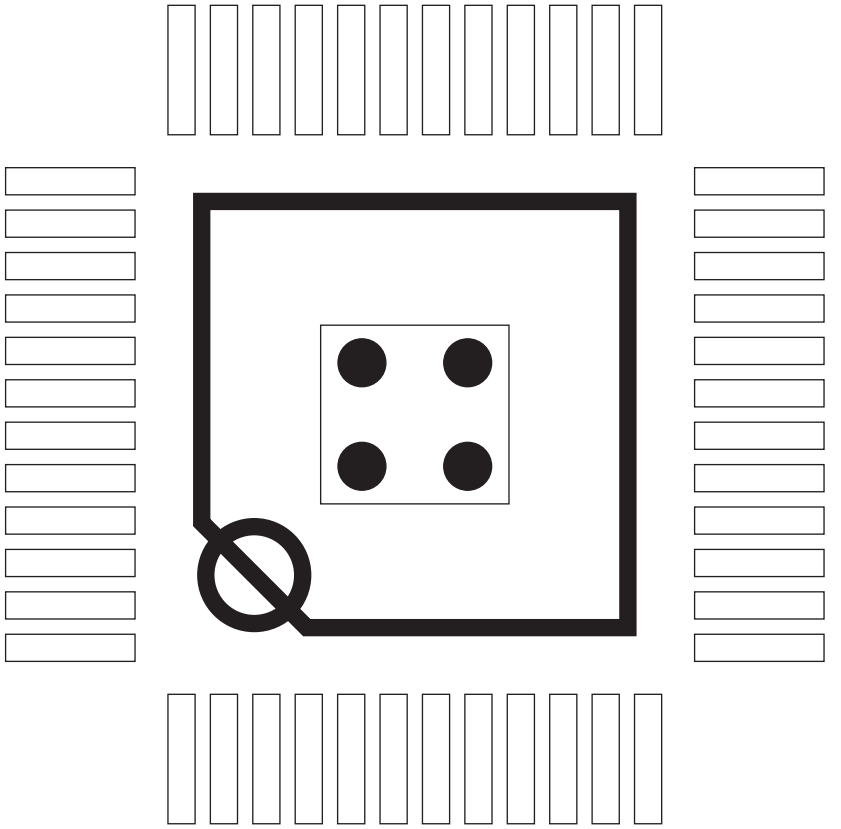


Figure 7-3. Example Layout

8 Register Block

Table 8-1. Register Map

OFFSET HEX	ACCESS	TAG	DESCRIPTION
00h	RW	BMCR	Basic Mode Control Register
01h	RO	BMSR	Basic Mode Status Register
02h	RO	PHYIDR1	PHY Identifier Register #1
03h	RO	PHYIDR2	PHY Identifier Register #2
04h	RW	ANAR	Auto-Negotiation Advertisement Register
05h	RO	ANLPAR	Auto-Negotiation Link Partner Ability Register
06h	RO	ANER	Auto-Negotiation Expansion Register
07h	RW	ANNPTR	Auto-Negotiation Next Page TX
08h	RO	ANLNPTR	Auto-Negotiation Link Partner Ability Next Page Register
09h–0Ch	RW	RESERVED	RESERVED
0Dh	RW	REGCR	Register control register
0Eh	RW	ADDAR	Address or Data register
0Fh	RW	RESERVED	RESERVED
EXTENDED REGISTERS			
10h	RW	PHYCR	PHY Control Register
11h	RO	PHYSR	PHY Status Register
12h	RW	MINTMR	MII Interrupt Mask Register
13h	RO	MINTSR	MII Interrupt Status Register
14h	RW	MINTCR	MII Interrupt Control Register
15h	RO	RECR	Receive Error Counter Register
16h	RW	BISCR	BIST Control Register
17h	RO	BISSR	BIST Status Register
18h	RW	LEDCR	LED Direct Control Register
19h	RW	RESERVED	RESERVED
1Ah	RW	CDCR	Cable Diagnostic Control Register
1Bh	RW	CDSR	Cable Diagnostic Status Register
1Ch	RO	CDRR	Cable Diagnostic Results Register
1Dh-1Eh	RW	RESERVED	RESERVED
1Fh	RW	PDR	Power Down Register
42h	RO	FCSCR	False Carrier Sense Counter Register
70h	RW	RXCCR	RX Channel Control Register
71h	RO	BISBCR	BIST Byte Count Register
72h	RO	BISECR	BIST Error Count Register
7Bh	RW	BISPLR	BIST Packet Length Register
7Ch	RW	BISIPGR	BIST Inter Packet Gap Register
80h	RW	TDRSMR	TDR State Machine Enable Register
90h	RW	TDRPAR	TDR Pattern Amplitude Register
94h	RW	TDRMPR	TDR Manual Pulse Register
0C00h–0C0Ch	RW		TDR Algorithm Registers
0C26h–0C2Ah	RW		ALCD/DSA Registers
0D00h, 0D01h, 0D04h	RW		RAM registers
0107h	RW		CD Pre Test Configuration 1 Register
010Fh	RW		CD Pre Test Configuration 2 Register
00AC	RW		LPF Bypass Register

Table 8-2. Register Table

Register Name	Addr	Tag	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Basic Mode Control Register	00h	BMCR	Reset	Loopback	Speed Selection	Auto-Neg Enable	Power Down	Isolate	Restart Auto-Neg	Duplex Mode	Collision Test	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Basic Mode Status Register	01h	BMSR	100Base -T4	100Base -TX FDX	100Base -TX HDX	10Base-T FDX	10Base-T HDX	Reserved	Reserved	Reserved	Reserved	MF Preamble Suppress	Auto-Neg Complete	Remote Fault	Auto-Neg Ability	Link Status	Jabber Detect	Extended Capability
PHY Identifier Register 1	02h	PHYIDR 1	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB	OUI MSB
PHY Identifier Register 2	03h	PHYIDR 2	OUI LSB	OUI LSB	OUI LSB	OUI LSB	OUI LSB	OUI LSB	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	VNDR_ MDL	MDL_ REV	MDL_ REV	MDL_ REV	MDL_ REV
Auto-Negotiation Advertisement Register	04h	ANAR	Next Page Ind	Reserved	Remote Fault	Reserved	ASM_DI R	PAUSE	T4	TX_FD	TX	10_FD	10	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection
Auto-Negotiation Link Partner Ability Register (Base Page)	05h	ANLPAR	Next Page Ind	ACK	Remote Fault	Reserved	ASM_DI R	PAUSE	T4	TX_FD	TX	10_FD	10	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection	Protocol Selection
Auto-Negotiation Expansion Register	06h	ANER	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PDF	LP_NP_ ABLE	NP_ ABLE	PAGE_ RX	LP_AN_AB LE
Auto-Negotiation Next Page TX Register	07h	ANNPTR	Next Page Ind	Reserved	Message Page	ACK2	TOG_TX	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE
Auto-Negotiate Link Partner Ability Page Register	08h	ANLNPTR	Next Page Ind	Reserved	Message Page	ACK2	TOG_TX	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE	CODE
RESERVED	09-0Ch	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register Control Register	0Dh	REGCR	Function	Function	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DEVICE ADDRESS	DEVICE ADDRESS	DEVICE ADDRESS	DEVICE ADDRESS	DEVICE ADDRESS
Address or Data Register	0Eh	ADDAR	Addr/ Data	Addr/ Data	Addr /Data	Addr /Data	Addr/ Data	Addr/ Data	Addr /Data	Addr /Data	Addr/ Data	Addr/ Data	Addr /Data	Addr /Data	Addr/ Data	Addr/ Data	Addr /Data	Addr /Data
RESERVED	0Fh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
EXTENDED REGISTERS																		
PHY Control Register	10h	PHYCR	TX FIFO Depth	TX FIFO Depth	Reserved	Reserved	Reserved	Force Link Good	Power Down Mode	Power Down Mode	Reserved	Auto MDI-X Enable	Manual MDI-X Enable	Disable PLL	Reserved	Reserved	Reserved	Disable Jabber
PHY Status Register	11h	PHYSR	Reserved	Speed	Duplex	Page Received	Auto Nego Complete	Link Status	Reserved	MDI Cross over	Reserved	Sleep Mode	Reserved	Reserved	Reserved	Reserved	Polarity	Jabber
MII Interrupt Mask Register	12h	MINTMR	Auto Nego error Enable	Speed Change Enable	Duplex Mode Change Enable	Page Received Enable	Auto Nego Complete Enable	Link Status Change Enable	Reserved	Reserved	FIFO Over Under flow Enable	MDI cross over change Enable	Reserved	Sleep Mode Change Enable	Reserved	Reserved	Polarity Change Enable	Jabber Interrupt Enable
MII Interrupt Status Register	13h	MINTSR	Auto Nego Error	Speed Changed	Duplex Mode Changed	Page Received	Auto Nego Complete	Link Status Changed	Reserved	Reserved	FIFO Over Underflow	MDI Crossover Changed	Reserved	Sleep Mode Changed	Reserved	Reserved	Polarity Changed	Jabber
MII Interrupt Control Register	14h	MINTCR	Interrupt Pin Enable	Reserved	Interrupt Polarity	Interrupt Pin Enable	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Receive Error Counter Register	15h	RECR	RXCERNT	RXCERNT	RXCERNT	RXCERNT	RXCERNT	RXCERNT	RXCERNT	RXCERNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT	RXERCNT
BIST Control Register	16h	BISCR	PRBS Count Mode	Generate PRBS Packets	64 bit mode	Packet Generation Enable	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Loopback Mode	Loop back Mode	Loop back Mode	Loop back Mode	Loop back Mode

Table 8-2. Register Table (continued)

Register Name	Addr	Tag	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BIST Status Register	17h	BISSR	Reserved	Reserved	Reserved	Reserved	PRBS Locked	PRBS Sync Loss	PRBS Generator busy	Core Power Mode Status	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BIST Byte Count Register	71h	BISBCR	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count	PRBS Count
BIST Error Count Register	72h	BISECR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PRBS Error Count	PRBS Error Count	PRBS Error Count	PRBS Error Count	PRBS Error Count	PRBS Error Count	PRBS Error Count	PRBS Error Count
BIST Packet Length register	7Bh	BISPLR	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length	PRBS Packet Length
BIST Inter Packet Gap Register	7Ch	BISIPGR	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length	PRBS IPG Length
LED Control Register	18h	LEDCR	LED Enable	Pulse Width	Pulse Width	Force Interrupt	Reserved	Reserved	Blink Rate	Blink Rate	Reserved	LED Mode	LED Mode	Reserved	Reserved	LED ACT Polarity	LED SPEED Polarity	LED LINK Polarity
Power Down Register	1Fh	PDR	Software Global Reset	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
False Carrier Sense Counter Register	42h	FCSCR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Idle_error_count	Idle_error_count	Idle_error_count	Idle_error_count	Idle_error_count	Idle_error_count	Idle_error_count	Idle_error_count
RX Channel Control Register	70h	RXCCR	Rese-rved	Rese-rved	Rese-rved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Polarity Inversion	Mdix	Reserved	Reserved
Cable Diagnostic Register	1Ah	CDCR	Reserved	Reserved	ALCD/ DSA test start	TDR test Start	Reserved	Cable Diag result Select	Cable Diag result Select	Cable Diag result Select	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Channel Select
Cable Diagnostic Status Register	1Bh	CDSR	ALCD/ DSA Done	TDR Fail	TDR Done	Reserved	Reserved	Reserved	DSA Input Signal	DSA Input Signal	DSA Input Signal	DSA Input Signal	DSA Enalbe	ALCD/ DSA mode	Reserved	Reserved	Reserved	Reserved
Cable Diagnostic Results Register	1Ch	CDRR	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results	Cable Diag Results
TDR State Machine Enable	80h	TDRSMR	Cmn_tdr_sm_mode	Cmn_tdr_tx_sm_mode	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TDR Pattern Amplitude Register	90h	TDRPAR	Rese- rved	Rese- rved	Rese- rved	Rese- rved	Rese- rved	Rese- rved	Rese- rved	Rese- rved	Rese- rved	Rese- rved	Rese- rved	TDR pattern	TDR pattern	TDR pattern	TDR pattern	TDR pattern
TDR Manual Pulse Register	94h	TDRMPR	Rese-rved	Rese-rved	Rese-rved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TDR_TX_START	Reserved
TDR Algorithm Registers	0C00h – 0C0Ch		Cable Diagnostic algorithm related registers															
ALCD/DSA Registers	0C26h – 0C2Ah																	
CD Pre test Configuration	0107h, 010Fh																	
LPF Bypass Register	00ACh																	

8.1 Register Definition

In the register definitions under the ‘Default’ heading, the following definitions hold true:

- RW = Read Write access
- SC = Register sets on event occurrence and Self-Clears when event ends
- RW/SC = Read Write Access/Self Clearing bit
- RO = Read Only access
- COR = Clear on Read
- RO/COR = Read Only, Clear on Read
- RO/P = Read Only, Permanently set to a default value
- LL = Latched Low and held until read, based upon the occurrence of the corresponding event
- LH = Latched High and held until read, based upon the occurrence of the corresponding event

8.1.1 Basic Mode Control Register (BMCR)

Table 8-3. Basic Mode Control Register (BMCR), address 0x0000

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	Reset	0, RW/SC	**PHY Software Reset:** 1 = Initiate software Reset / Reset in Process. 0 = Normal operation. Writing a 1 to this bit causes the PHY to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The configuration is relatched.
14	Loopback	0, RW	**Loopback:** 1 = Loopback enabled. 0 = Normal operation. When loopback mode is activated, the transmitter data presented on TXD is looped back to RXD internally
13	Speed Selection	Jumper, RW	**Speed Select:** When auto-negotiation is disabled writing to this bit allows the port speed to be selected. 1 = 100 Mb/s 0 = 10 Mb/s
12	Auto-Negotiation Enable	Jumper, RW	**Auto-Negotiation Enable:** Configuration pin (jumper) controls initial value at reset. 1 = Auto-Negotiation Enabled – bits 8 and 13 of this register are ignored when this bit is set. 0 = Auto-Negotiation Disabled – bits 8 and 13 determine the port speed and duplex mode.
11	Power Down	0, RW	**Power Down:** 1 = Enables Power Down Modes - General Power Down Mode, Active Sleep Mode and Passive Sleep Mode (see register 0x10) 0 = Normal operation.
10	Isolate	0, RW	**Isolate:** 1 = Isolates the Port from the MII with the exception of the serial management. 0 = Normal operation.
9	Restart Auto-Negotiation	0, RW/SC	**Restart Auto-Negotiation:** 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0 = Normal operation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it self-clears. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit.
8	Duplex Mode	Jumper, RW	**Duplex Mode:** When auto-negotiation is disabled writing to this bit allows the port Duplex capability to be selected. 1 = Full Duplex operation. 0 = Half Duplex operation.
7	Collision Test	0, RW	**Collision Test:** 1 = Collision test enabled. 0 = Normal operation
6:0	RESERVED	0, RO	**RESERVED:** Write ignored, read as 0.

8.1.2 Basic Mode Status Register (BMSR)

Table 8-4. Basic Mode Status Register (BMSR), address 0x0001

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	100BASE-T4	0, RO/P	**100BASE-T4 Capable:** This protocol is not available. Always 0 = Device does not perform 100BASE-T4 mode.
14	100BASE-TX Full Duplex	1, RO/P	**100BASE-TX Full Duplex Capable:** 1 = Device able to perform 100BASE-TX in full duplex mode. 0 = Device not able to perform 100BASE-TX in full duplex mode.
13	100BASE-TX Half Duplex	1, RO/P	**100BASE-TX Half Duplex Capable:** 1 = Device able to perform 100BASE-TX in half duplex mode. 0 = Device not able to perform 100BASE-TX in half duplex mode.
12	10BASE-T Full Duplex	1, RO/P	**10BASE-T Full Duplex Capable:** 1 = Device able to perform 10BASE-T in full duplex mode. 0 = Device not able to perform 10BASE-T in full duplex mode.
11	10BASE-T Half Duplex	1, RO/P	**10BASE-T Half Duplex Capable:** 1 = Device able to perform 10BASE-T in half duplex mode. 0 = Device not able to perform 10BASE-T in half duplex mode.
10:7	RESERVED	0, RO	**RESERVED:** Write as 0, read as 0.
6	MF Preamble Suppression	1, RO/P	**Preamble suppression Capable:** 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. 0 = Device will not perform management transaction with preambles suppressed.
5	Auto-Negotiation Complete	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation process complete. 0 = Auto-Negotiation process not complete (either still in process, disabled, or reset)
4	Remote Fault	0, RO/LH	**Remote Fault:** 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected.
3	Auto-Negotiation Ability	1, RO/P	**Auto Negotiation Ability:** 1 = Device is able to perform Auto-Negotiation. 0 = Device is not able to perform Auto-Negotiation.
2	Link Status	0, RO/LL	**Link Status:** 1 = Valid link established (for either 10 or 100 Mb/s operation). 0 = Link not established.
1	Jabber Detect	0, RO/LH	**Jabber Detect:** This bit only has meaning in 10 Mb/s mode. 1 = Jabber condition detected. 0 = No Jabber. condition detected.
0	Extended Capability	1, RO/P	**Extended Capability**: 1 = Extended register capabilities. 0 = Basic register set capabilities only.

The PHY Identifier Registers #1 and #2 together form a unique identifier for the TLK100. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management. The IEEE-assigned OUI for Texas Instruments is 080028h.

8.1.3 PHY Identifier Register #1 (PHYIDR1)

Table 8-5. PHY Identifier Register #1 (PHYIDR1), address 0x0002

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	OUI_MSB	<0010 0000 0000 0000>, RO/P	**OUI Most Significant Bits:** Bits 3 to 18 of the OUI (080028h) are stored in bits 15 to 0 of this register. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

8.1.4 PHY Identifier Register #2 (PHYIDR2)

Table 8-6. PHY Identifier Register #2 (PHYIDR2), address 0x0003

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	OUI_LSB	<101000>, RO/P	**OUI Least Significant Bits:** Bits 19 to 24 of the OUI (080028h) are mapped from bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	<100000>, RO/P	**Vendor Model Number:** The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	<0001>, RO/P	**Model Revision Number:** Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field is incremented for all major device changes.

8.1.5 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they are transmitted to its link partner during Auto- Negotiation.

Table 8-7. Auto Negotiation Advertisement Register (ANAR), address 0x0004

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	**Next Page Indication:** 0 = Next Page Transfer not desired. 1 = Next Page Transfer desired.
14	RESERVED	0, RO/P	**RESERVED by IEEE:** Writes ignored, Read as 0.
13	RF	0, RW	**Remote Fault:** 1 = Advertises that this device has detected a Remote Fault. 0 = No Remote Fault detected.
12	RESERVED	0, RW	**RESERVED for Future IEEE use:** Write as 0, Read as 0
11	ASM_DIR	0, RW	**Asymmetric PAUSE Support for Full Duplex Links:** 1 = Asymmetric PAUSE implemented. 0 = Asymmetric PAUSE not implemented.
10	PAUSE	0, RW	**PAUSE Support for Full Duplex Links:** 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	T4	0, RO/P	**100BASE-T4 Support:** 1 = 100BASE-T4 is supported by the local device. 0 = 100BASE-T4 not supported.
8	TX_FD	Jumper, RW	**100BASE-TX Full Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the local device. 0 = 100BASE-TX Full Duplex not supported.
7	TX	Jumper, RW	**100BASE-TX Support:** 1 = 100BASE-TX is supported by the local device. 0 = 100BASE-TX not supported.
6	10_FD	Jumper, RW	**10BASE-T Full Duplex Support:** 1 = 10BASE-T Full Duplex is supported by the local device. 0 = 10BASE-T Full Duplex not supported.
5	10	Jumper, RW	**10BASE-T Support:** 1 = 10BASE-T is supported by the local device. 0 = 10BASE-T not supported.
4:0	Selector	<00001>, RW	**Protocol Selection Bits:** These bits contain the binary encoded protocol selector supported by this port. <00001> indicates that this device supports IEEE 802.3u.

8.1.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page)

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation. The content changes after the successful auto-negotiation if Next-pages are supported.

Table 8-8. Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page), address 0x0005

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	**Next Page Indication:** 0 = Link Partner does not desire Next Page Transfer. 1 = Link Partner desires Next Page Transfer.
14	ACK	0, RO	**Acknowledge:** 1 = Link Partner acknowledges reception of the ability data word. 0 = Not acknowledged. The Auto-Negotiation state machine will automatically control the this bit based on the incoming FLP bursts.
13	RF	0, RO	**Remote Fault:** 1 = Remote Fault indicated by Link Partner. 0 = No Remote Fault indicated by Link Partner.
12	RESERVED	0, RO	**RESERVED for Future IEEE use:** Write as 0, read as 0.
11	ASM_DIR	0, RO	**ASYMMETRIC PAUSE:** 1 = Asymmetric pause is supported by the Link Partner. 0 = Asymmetric pause is not supported by the Link Partner.
10	PAUSE	0, RO	**PAUSE:** 1 = Pause function is supported by the Link Partner. 0 = Pause function is not supported by the Link Partner.
9	T4	0, RO	**100BASE-T4 Support:** 1 = 100BASE-T4 is supported by the Link Partner. 0 = 100BASE-T4 is not supported by the Link Partner.
8	TX_FD	0, RO	**100BASE-TX Full Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the Link Partner. 0 = 100BASE-TX Full Duplex is not supported by the Link Partner.
7	TX	0, RO	**100BASE-TX Support:** 1 = 100BASE-TX is supported by the Link Partner. 0 = 100BASE-TX is not supported by the Link Partner.
6	10_FD	0, RO	**10BASE-T Full Duplex Support:** 1 = 10BASE-T Full Duplex is supported by the Link Partner. 0 = 10BASE-T Full Duplex is not supported by the Link Partner.
5	10	0, RO	**10BASE-T Support:** 1 = 10BASE-T is supported by the Link Partner 0 = 10BASE-T is not supported by the Link Partner.
4:0	Selector	<0 0000>, RO	**Protocol Selection Bits:** Link Partner's binary encoded protocol selector.

8.1.7 Auto-Negotiate Expansion Register (ANER)

This register contains additional Local Device and Link Partner status information.

Table 8-9. Auto-Negotiate Expansion Register (ANER), address 0x0006

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:5	RESERVED	0, RO	**RESERVED:** Writes ignored, Read as 0.
4	PDF	0, RO	**Parallel Detection Fault:** 1 = A fault has been detected via the Parallel Detection function. 0 = A fault has not been detected.
3	LP_NP_ABLE	0, RO	**Link Partner Next Page Able:** 1 = Link Partner does support Next Page. 0 = Link Partner does not support Next Page.
2	NP_ABLE	1, RO/P	**Next Page Able:** 1 = Indicates local device is able to send additional *Next Pages*. 0 = Indicates local device is not able to send additional *Next Pages*.
1	PAGE_RX	0, RO/COR	**Link Code Word Page Received:** 1 = Link Code Word has been received, cleared on a read. 0 = Link Code Word has not been received.
0	LP_AN_ABLE	0, RO	**Link Partner Auto-Negotiation Able:** 1 = indicates that the Link Partner supports Auto-Negotiation. 0 = indicates that the Link Partner does not support Auto-Negotiation.

8.1.8 Auto-Negotiate Next Page Transmit Register (ANNPTR)

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 8-10. Auto-Negotiation Next Page Transmit Register (ANNPTR), address 0x0007

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	**Next Page Indication:** 0 = No other Next Page Transfer desired. 1 = Another Next Page desired.
14	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
13	MP	1, RW	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK2	0, RW	**Acknowledge2:** 1 = Will comply with message. 0 = Cannot comply with message. Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	TOG_TX	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was 0. 0 = Value of toggle bit in previously transmitted Link Code Word was 1. Toggle is used by the Arbitration function within Auto-Negotiation to synchronize with the Link Partner during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	<000 0000 0001>, RW	This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code is interpreted as a *Message Page*, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interpreted as an *Unformatted Page*, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

8.1.9 Auto-Negotiation Link Partner Ability Next Page Register (ANLNPTR)

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 8-11. Auto-Negotiation Link Partner Ability Register Next Page (ANLNPTR), address 0x0008

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	**Next Page Indication:** 1 = No other Next Page Transfer desired. 0 = Another Next Page desired
14	ACK	0, RO	**Acknowledge:** 1 = Link Partner acknowledges reception of the ability data word. 0 = Not acknowledged. The Auto-Negotiation state machine will automatically control this bit based on the incoming FLP bursts. Software should not attempt to write to this bit.
13	MP	1, RO	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK2	0, RO	**Acknowledge2:** 1 = Will comply with message. 0 = Cannot comply with message Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	Toggle	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was 0. 0 = Value of toggle bit in previously transmitted Link Code Word was 1. Toggle is used by the Arbitration function within Auto-Negotiation to synchronize with the Link Partner during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	<000 0000 0001>, RO	**Code:** This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interpreted as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

8.2 Register Control Register (REGCR)

This register contains the device address to be written to access the extended registers. Write 0x1F into bits 4:0 of this register. It also contains selection bits for auto increment of the data register.

Table 8-12. Register Control Register (REGCR), address 0x000D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	Function	0, RW	00 = Address 01 = Data, no post increment 10 = Data, post increment on read and write 11 = Data, post increment on write only
13:5	RESERVED	0, RO	**RESERVED: Writes ignored, read as 0**.
4:0	DEVAD	0, RW	Device Address

8.3 Address or Data Register (ADDAR)

This is the address/data register.

Table 8-13. Data Register (ADDAR), address 0x000E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	Addr/data	0, RW	If REGCR register 15:14 = 00, holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data register

8.4 Extended Registers

8.4.1 PHY Control Register (PHYCR)

This register provides quick access to commonly accessed PHY control information.

Table 8-14. PHY Control Register (PHYCR), address 0x0010

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	TX FIFO Depth	0x1,RW	00 = 4 nibbles 01 = 5 nibbles 10 = 6 nibbles 11 = 8 nibbles
13:12	Reserved	0,RO	Ignore on read
11	Reserved	0,RO	Ignore on read
10	Force Link Good	0,RW	1 = Force link_ctrl_en10/100 according to selected speed in register 0x0 0 = Do Normal operation
9:8	Power Down Mode	00,RW	00 = Normal mode 01 = General Power Down mode: Besides SMI module everything is powered down, if bit [4] set to '1', PLL is also powered down. When PLL is powered down, Reference clock is used. 10 = Active Sleep mode – same as passive sleep, but also send NLP every ~1.4 Sec to wake up link-partner. Automatic power-up is done when link partner is detected. 11 = Passive Sleep Mode - Besides SMI and energy detect modules, everything is powered down. Automatic power-up is done when link partner is detected. Bit 11 of the BMCR register(0x00) to '1' for all of these power down modes.
7	Reserved	0,RW	Reserved
6	Auto MDI-X Enable	SOR,RW	1 = Enable automatic crossover 0 = Disable automatic crossover
5	Manual MDI-X Mode	0,RW	0 = Manual MDI configuration 1 = Manual MDI-X configuration
4	Disable PLL	0,RW	1 = Disable PLL 0 = Enable PLL
3:1	Reserved	0,RO	Ignore on read
0	Disable Jabber	0,RW	1 = Disable Jabber function 0 = Enable Jabber function

8.4.2 PHY Status Register (PHYSR)

This register implements the PHY Specific Status register.

Table 8-15. PHY Status Register (PHYSR), address 0x0011

BIT	NAME	DEFAULT	DESCRIPTION
15	Reserved	0,RO	Ignore on read
14	Speed	0,RO	0 = 10Mbps 1 = 100Mbps
13	Duplex	0,RO	1 = Full duplex 0 = Half duplex
12	Page Received	0,RO, LH	1 = Page received 0 = Page not received
11	Auto-Negotiation Complete	0,RO	1 = Auto-Negotiation completed or disabled 0 = Auto-Negotiation enabled and not completed
10	Link Status	0,RO	1 = Link is up 0 = Link is down
9	Reserved	0,RO	Ignore on read
8	MDI Crossover Status	0,RO	1 = MDI-X 0 = MDI
7	Reserved	0,RO	Ignore on read
6	Sleep Mode Status	0,RO	1 = Sleep 0 = Active
5:2	Reserved	0,RO	Ignore on read
1	Polarity	0,RO	10BT data/nlp polarity. "1" - positive polarity. "0" - negative polarity.
0	Jabber	0,RO	1 = Jabber 0 = No Jabber

8.4.3 MII Interrupt Mask Register (MINTMR)

This register contains enables for various interrupt functions supported by TLK100.

Table 8-16. MII Interrupt Mask Register (MINTMR), address 0x0012

BIT	NAME	DEFAULT	DESCRIPTION
15	Auto-Negotiation Interrupt Enable	0, RW	1 = Enable interrupt 0 = Disable interrupt
14	Speed Changed Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt
13	Duplex Mode Changed Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt
12	Page Received Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt
11	Auto-Negotiation Completed Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt
10	Link Status Changed Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt
9:8	Reserved	0,RO	Ignore on read
7	FIFO Overflow/Underflow Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt
6	MDI Crossover Changed Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt
5	Reserved	0,RO	Ignore on read
4	Sleep Mode Changed Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt
3:2	Reserved	0,RO	Ignore on read
1	Polarity Changed Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt
0	Jabber Interrupt Enable	0,RW	1 = Enable interrupt 0 = Disable interrupt

8.4.4 MII Interrupt Status Register (MINTSR)

This register gives the status of the different interrupt function supported by TLK100.

Table 8-17. MII Interrupt Status Register (MINTSR), address 0x0013

BIT	NAME	DEFAULT	DESCRIPTION
15	Auto-Negotiation Error	0, RO, LH	1 = Auto-Negotiation error has occurred 0 = Auto-Negotiation error has not occurred
14	Speed Changed	0,RO, LH	1 = Link speed has changed 0 = Link speed has not changed
13	Duplex Mode Changed	0,RO, LH	1 = Duplex mode has changed 0 = Duplex mode has not changed
12	Page Received	0,RO, LH	1 = Page has been received 0 = Page has not been received
11	Auto-Negotiation Completed	0,RO, LH	1 = Auto-Negotiation has completed 0 = Auto-Negotiation has not completed
10	Link Status Changed	0,RO, LH	1 = Link status has changed 0 = Link status has not changed
9:8	Reserved	0,RO	Ignore on read
7	FIFO Overflow/Underflow	0,RO, LH	1 = FIFO Overflow/Underflow occurred 0 = FIFO Overflow/Underflow did not occur
6	MDI Crossover Changed	0,RO, LH	1 = MDI crossover has changed 0 = MDI crossover has not changed
5	Reserved	0,RO	Ignore on read
4	Sleep Mode Changed	0,RO, LH	1 = Sleep mode has changed 0 = Sleep mode has not changed
3:2	Reserved	0,RO	Ignore on read
1	Polarity Changed	0,RO, LH	1 = Data polarity has changed 0 = Data polarity has not changed
0	Jabber	0,RO, LH	1 = Jabber detected 0 = Jabber not detected

8.4.5 MII Interrupt Control Register (MINTCR)

This register enables to control the polarity and enabling the interrupts.

Table 8-18. MII Interrupt Control Register (MINTCR), address 0x0014

BIT	NAME	DEFAULT	DESCRIPTION		
15	INTN_OE	0,RW	Bit 15	Bit 12	Pin 42 Function
			0	0	Power Down
			0	1	Power Down
			1	0	Interrupt
			1	1	Power Down
14	Reserved	0,RO			Ignore on read
13	Interrupt Polarity	1,RW			1 = Interrupt pin is active low 0 = Interrupt pin is active high
12	INTN_OEN	1,RW			Refer to the table given in the bit 15 description.
11:0	Reserved	0,RO			Ignore on read

8.4.6 Receiver Error Counter Register (RECR)

This counter keeps count of the number of receive errors.

Table 8-19. Receiver Error Counter Register (RECR), address 0x0015

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	RX Error Count	0, RO, SC	Receive errors counter (saturates in max value, clears on dummy write)

8.4.7 BIST Control Register (BISCR)

This register is used for configuring the PRBS BIST and to select the loopback point in the signal chain.

Table 8-20. BIST Control Register (BISCR), address 0x0016

BIT	NAME	DEFAULT	DESCRIPTION
15	PRBS Count Mode	0, RW	1 = Continuous mode, when on of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again 0 = Single mode, When one of the PRBS counters reaches it's max value, PRBS checker stops counting.
14	Generate PRBS Packets	0, RW	1 = When packet generator is enabled, generate continuous packets with PRBS data. When packet generator is disabled, PRBS checker is still enabled. 0 = When packet generator is enabled, generate single packet with constant data. PRBS gen/check is disabled.
13	Packet Generation 64 bit mode	0, RW	1 = Transmit 64 byte packets in packet generation mode 0 = Transmit 1518 byte packets in packet generation mode
12	Packet Generation Enable	0, RW	1 = Enable packet/PRBS generator 0 = Disable packet/PRBS generator
11:5	Reserved	0, RO	Ignore on read
4:0	Loopback Mode	0, RW	Selects loop back mode: Near-end Loopbacks [00001] – MII Loopback [00010] – PCS Loopback (In 100BaseTX only) [00100] – Digital Loopback [01000] – Analog Loopback (requires 100Ω termination) Far-end Loopback: [10000] – Reverse Loopback

8.4.8 BIST STATUS Register (BISSR)

This register gives the status of the PRBS test and the sleep mode of the core.

Table 8-21. BIST STATUS Register (BISSR), address 0x0017

BIT	NAME	DEFAULT	DESCRIPTION
15:12	Reserved	0,RO	Ignore on read
11	PRBS Locked	0,RO	1 = PRBS checker is locked on received byte stream 0 = PRBS checker is not locked
10	PRBS Sync Loss	0,RO,LH	1 = PRBS checker has lost sync 0 = PRBS checker has not lost sync
9	Packet Generator Busy	0,RO	1 = Packet generator is in process 0 = Packet generator is not in process
8	Core Power Mode Status	0,RO	1 = Core is in normal power mode 0 = Core is powered down or in sleep mode
7:0	Reserved	0,RO	Ignore on read

8.4.9 BIST Byte Count Register (BISBCR)

This register gives the total number of bytes received by the PRBS checker.

Table 8-22. BIST Count Register (BISBCR), address 0x0071

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	prbs_byte_cnt	0, RO	Holds number of total bytes that received by the PRBS checker. Value in this register is locked when write is done to register 0x0072 bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFF (see register 0x0016)

8.4.10 BIST Error Count Register (BISECR)

This register gives the total number of error bytes that was received by the PRBS checker.

Table 8-23. BIST Error Count Register (BISECR), address 0x0072

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	Reserved	0, RO	Ignore on read
7:0	prbs_err_cnt	0, RO	Holds number of erroneous bytes received by the PRBS checker. Value in this register is locked when write is done to bit[0] or bit[1] (see below). When PRBS Count Mode set to zero, count stops on 0xFF (see register 0x0016) **Notes:** Writing bit 0 generates a **lock** signal for the PRBS counters Writing bit 1 generates a **lock and clear** signal for the PRBS counters

8.4.11 BIST Packet Length Register (BISPLR)

This register allows programming the length of the PRBS packet in bytes.

Table 8-24. BIST Packet Length Register (BISPLR), address 0x007B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	Cfg_pkt_len_prbs	0X5DC,RW	Length of PRBS packets in bytes

8.4.12 BIST Inter Packet Gap Register (BISIPGR)

This register allows programming the inter packet gap, in bytes, between the PRBS packets.

Table 8-25. BIST Inter Packet Gap Register (BISIPGR), address 0x007C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	Cfg_ipg_len	0X7D,RW	Inter-packet gap (in bytes) between PRBS packets

8.4.13 LED Direct Control Register (LEDCR)

This register provides the ability to directly control any or all LED outputs. The polarity, pulse width and blink rates can be programmed using this register.

Table 8-26. LED Direct Control Register (LEDCR), address 0x0018

BIT	NAME	DEFAULT	DESCRIPTION
15	LEDs Enable	1,RW	1 = Enable LEDs 0 = Disable LEDs
14:13	Pulse Width	0x2,RW	00 = 50mSec 01 = 100mSec 10 = 200mSec 11 = 500mSec
12	Force Interrupt	0,RW	1 = Assert interrupt pin 0 = Normal interrupt mode
11:10	Reserved	0,RO	Ignore on read
9:8	Blink Rate	0x2,RW	00 = 20Hz (50mSec) 01 = 10Hz (100mSec) 10 = 5Hz (200mSec) 11 = 2Hz (500mSec)
7	Reserved	0,RO	Ignore on read
6:5	LED Mode	0,SOR,RW	01 = Mode1 00 = Mode2 10 = Mode3
4:3	Reserved	0,RO	Ignore on read
2	LED ACT Polarity	SOR,RW	0 = Active low 1 = Active high
1	LED SPEED Polarity	SOR,RW	0 = Active low 1 = Active high
0	LED LINK Polarity	SOR,RW	0 = Active low 1 = Active high

8.4.14 Power Down Register (PDR)

This register provides control for doing a software reset of the PHY.

Table 8-27. Power Down Register (PDR), address 0x001F

BIT	NAME	DEFAULT	DESCRIPTION
15	Software Global Reset	0,RW,SC	1 = Reset PHY (Same effect as in hardware reset, including registers reset) 0 = Normal mode
14:0	Reserved	0,RO	Always write zero

8.4.15 False Carrier Sense Counter Register (FCSCR)

This register counts the error nibbles between the IDLE nibbles (BAD_SSD), in nibble time. This count register is reset when this register is read.

Table 8-28. False Carrier Sense Counter Register (FCSCR), address 0x0042

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0, RO	Ignore on read
7:0	idle_err_count_100	0, RO	**IDLE error counter value.** Counts received error nibbles between IDLE nibbles (BAD_SSD), in nibble time. **Note:** Reading this register clears the **idle_err_count_100** counter

8.4.16 RX Channel Control Register (RXCCR)

This register allows configuration of RX channel. By programming bits 3,2 of this register to '1' the channels can be mirrored.

Table 8-29. RX Channel Control Register (RXCCR), address 0x0070

BIT	NAME	DEFAULT	FUNCTION
15:4	Reserved	0,RO	Ignore on read
3	Polarity_inv	0,RW	When 1 Change the polarity of: 1 = Polarity of RD and TD is inverted 0 = Polarity of RD and TD is not inverted
2	Mdix	0,RW	1 = MDIX 0 = MDI
1:0	Reserved	0,RW	Always write 0

8.5 Cable Diagnostic Registers

8.5.1 Cable Diagnostic Registers (CDCR)

This register is used to select the channel for which cable diagnostics test needs to be done. It has the enable bits for the diagnostic tests and also allows one to choose which TDR peak and location will be written to the CDRR register (0x001C).

Table 8-30. Cable Diagnostic Registers (CDCR), address 0x001A

BIT	NAME	DEFAULT	DESCRIPTION
15:14	Reserved	0,RW, SC	Always 0
13	ALCD/DSA Test Start	0,RW, SC	1 = Start ALCD/DSA test. 0 = Do not start ALCD/DSA test
12	TDR Test Start	0,RW, SC	1 = Start TDR test 0 = Do not start TDR test
11	Reserved	0,RO	Reserved
10:8	Cable Diagnostics Result Select	0,RW	Selects the output of register 0x1C as follows: 0: {TDR peak 0 amplitude, TDR peak 0 location} 1: {TDR peak 1 amplitude, TDR peak 1 location} 2: {TDR peak 2 amplitude, TDR peak 2 location} 3: {TDR peak 3 amplitude, TDR peak 3 location} 4: {TDR peak 4 amplitude, TDR peak 4 location} 6: ALCD Length
8:1	Reserved	0,RO	Ignore on read
0	Channel Select	0,RW	Selects channel for Cable Diagnostics Test 0 = TD± 1 = RD±

8.5.2 Cable Diagnostic Status Register (CDSR)

This register gives the status of the cable diagnostic tests. It also allows configuring different modes of the ALCD and DSA tests.

Table 8-31. Cable Diagnostic Status Register (CDSR), address 0x001B

BIT	NAME	DEFAULT	DESCRIPTION
15	ALCD/DSA Done	0,RO	1 = ALCD/DSA is done 0 = ALCD/DSA is not done
14	TDR Fail	1,RO	1 = TDR has failed 0 = TDR has not failed
13	TDR Done	0,RO	1 = TDR is done 0 = TDR is not done
12:10	Reserved	0x4,RO	Ignore on read
9:6	DSA Input Signal	7,RW	7 = ALCD 5 = DSA Adaptive data mode 3 = DSA Raw data mode Others are reserved
5	DSA Enable	0,RW	1 = DSA Engine is enabled 0 = DSA Engine is disabled
4	ALCD/DSA mode	1,RW	1 = DSA Raw data mode 0 = ALCD/DSA Adaptive data mode
3:0	Reserved	0,RO	Ignore on read

8.5.3 Cable Diagnostic Results Register (CDRR)

This register gives the result of the cable diagnostic tests. The software will post process this result.

Table 8-32. Cable Diagnostic Results Register (CDRR), address 0x001C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	Cable Diagnostics Result Register	0, RO	As specified in register 0x1A bits [11:8]

8.5.4 TDR State Machine Enable (TDRSMR)

This register allows configuration of the TDR state machines. Only when the bits 15, 14 of this register are set to ‘1’ the registers 0x0090 and 0x0094 can be used.

Table 8-33. TDR State Machine Enable Register (TDRSMR), address 0x0080

BIT	NAME	TYPE	RESET	FUNCTION
15	cmn_tdr_sm_mode	RW	0	1 = Configure TDR state machine mode. This bit is cleared when TDR is complete
14	cmn_tdr_tx_sm_mode	RW	0	1 = Configure TDR transmit state machine mode. This bit is cleared when the TDR is complete.
13:0	Reserved	RW	0	Reserved

8.5.5 TDR Pattern Amplitude Register (TDRPAR)

This register allows to program the pattern used to generate the TDR pulses. Bits 4:0 of this register give the amplitude of the TDR pulse. A value of 0x8 maps to an amplitude of 1V. For values from 0x8 to 0xF the amplitude is saturated to 1V. The TDR pattern is 16 symbols long. So, sixteen consecutive writes to this register are required. The value of these bits for each write determines the amplitude for that symbol. Each symbol is 8ns wide. For this register to function, the bits 15,14 of TDRSMR register (0x0080) should be set to '1'

Table 8-34. TDR Pattern Amplitude Register (TDRPAR), address 0x0090

BIT	NAME	DEFAULT	FUNCTION
15:5	Reserved	0,RO	Ignore on read
4:0	tdr_pattern_din_config	0,RW	Configure TDR Transmit Pattern.

8.5.6 TDR Manual Pulse Register (TDRMPR)

This register allows to program a manual TDR pulse. When bit 1 of this register is set then the pattern programmed in the TDRPAR register is put on the TD line. If the TDRPAR register is not programmed then a default TDR pulse is put on the TD line. It is NOT used for TDR measurements.

Table 8-35. TDR Manual Pulse Register (TDRMPR), address 0x0094

BIT	NAME	DEFAULT	FUNCTION
15:2	Reserved	0,RO	Ignore on read
1	tdr_tx_start	0,RW	1 = Start TDR pattern transmission 0 = Do not start TDR pattern transmission
0	Reserved	0x0,RW	Reserved

8.5.7 TDR Channel Silence Register (TDRCSR)

This register allows programming of the TDR channel silence timers.

Table 8-36. TDR Channel Silence Register (TDRCSR), address 0x0C00

BIT	NAME	DEFAULT	FUNCTION
15:14	Reserved	0,RO	Ignore on read
13:12	cfg_link_down_timer	0x2,RW	Hold time, to make sure the link failed: 0x0 – no hold time. 0x1 – 500ms hold time. 0x2 – 1s hold time. 0x3 – 2s hold time.
11:10	cfg_post_silence_time	0x1,RW	The needed silence time after the TDR test: 0x0 – no silence needed. 0x1 – 10ms of silence. 0x2 – 100ms of silence. 0x3 – 1s of silence.
9:8	cfg_pre_silence_time	0x1,RW	The needed silence time before the TDR test: 0x0 – no silence needed. 0x1 – 10ms of silence. 0x2 – 100ms of silence. 0x3 – 1s of silence.
7:0	cfg_silence_th	0xC8,RW	Energy calculator threshold value, to break silence.

8.5.8 TDR Control Register (TDRCR)

This register allows configuring the TDR modes.

Table 8-37. TDR Control Register (TDRCR), address 0x0C01

BIT	NAME	DEFAULT	FUNCTION
15:11	Reserved	0x02,RO	Ignore on read
10	cfg_tdr_tx_mode	0x1,RW	1 – Enable TDR TX transmission mode
9	Reserved	0,RW	Reserved
8:6	cfg_soft_avr_cycles	0x7,RW	Number of averaging cycles: 0x0 – TDR disabled. 0x1 – 1 TDR cycle (no averaging). 0x2 – 2 TDR cycles. 0x3 – 4 TDR cycles. 0x4 – 8 TDR cycles. 0x5 – 16 TDR cycles. 0x6 – 32 TDR cycles. 0x7 – 64 TDR cycles.
5:3	cfg_post_cmp_size	0x4,RW	Number of forward samples for peak detection comparison.
2:0	cfg_pre_cmp_size	0x3,RW	Number of backward samples for peak detection comparison.

8.5.9 TDR Clock Cycles Register (TDRLCR)

This register allows configuring the number of clock cycles in a pattern TDR test.

Table 8-38. TDR Clock Cycles Register (TDRLCR), address 0x0C02

BIT	NAME	DEFAULT	FUNCTION
15:8	Reserved	0,RO	Ignore on read
7:0	cfg_ptrn_cycle_time	0xFF,RW	Number of clock cycles in a TDR pattern test.

8.5.10 TDR Low Threshold Register (TDRLT1)

This register allows configuring the threshold for finding the peaks of the reflected signal in the TDR test.

Table 8-39. TDR Low Threshold Register (TDRLT1), address 0x0C03

BIT	NAME	DEFAULT	FUNCTION
15	Reserved	0,RO	Ignore on read
14:8	cfg_ptrn_low_th_1	0xC,RW	Peak (absolute) low threshold value 1, for TX pattern.
7	Reserved	0,RO	Ignore on read
6:0	cfg_ptrn_low_th_0	0x10,RW	Peak (absolute) low threshold value 0, for TX pattern.

8.5.11 TDR Low Threshold Register (TDRLT2)

This register allows configuring the threshold for finding the peaks of the reflected signal in the TDR test.

Table 8-40. TDR Low Threshold Register (TDRLT2), address 0x0C04

BIT	NAME	DEFAULT	FUNCTION
15	Reserved	0,RO	Ignore on read
14:8	cfg_ptrn_low_th_3	0x7,RW	Peak (absolute) low threshold value 3, for TX pattern.
7	Reserved	0,RO	Ignore on read
6:0	cfg_ptrn_low_th_2	0x9,RW	Peak (absolute) low threshold value 2, for TX pattern.

8.5.12 TDR Low Threshold Register (TDRLT3)

This register allows configuring the threshold for finding the peaks of the reflected signal in the TDR test.

Table 8-41. TDR Low Threshold Register (TDRLT3), address 0x0C05

BIT	NAME	DEFAULT	FUNCTION
15	Reserved	0,RO	Ignore on read
14:8	cfg_ptrn_low_th_5	0x4,RW	Peak (absolute) low threshold value 5, for TX pattern.
7	Reserved	0,RO	Ignore on read
6:0	cfg_ptrn_low_th_4	0x5,RW	Peak (absolute) low threshold value 4, for TX pattern.

8.5.13 TDR Low Threshold Register (TDRLT4)

This register allows configuring the threshold for finding the peaks of the reflected signal in the TDR test.

Table 8-42. TDR Low Threshold Register (TDRLT4), address 0x0C06

BIT	NAME	DEFAULT	FUNCTION
15	Reserved	0,RO	Ignore on read
14:8	cfg_ptrn_low_th_7	0x3,RW	Peak (absolute) low threshold value 7, for TX pattern.
7	Reserved	0,RO	Ignore on read
6:0	cfg_ptrn_low_th_6	0x3,RW	Peak (absolute) low threshold value 6, for TX pattern.

8.5.14 TDR High Threshold Register (TDRHT1)

This register allows configuring the threshold for finding the peaks of the reflected signal in the TDR test.

Table 8-43. TDR High Threshold Register (TDRHT1), address 0x0C07

BIT	NAME	DEFAULT	FUNCTION
15	Reserved	0,RO	Ignore on read
14:8	cfg_ptrn_High_th_1	0x53,RW	Peak (absolute) High threshold value 1, for TX pattern.
7	Reserved	0,RO	Ignore on read
6:0	cfg_ptrn_High_th_0	0x53,RW	Peak (absolute) High threshold value 0, for TX pattern.

8.5.15 TDR High Threshold Register (TDRHT2)

This register allows configuring the threshold for finding the peaks of the reflected signal in the TDR test.

Table 8-44. TDR High Threshold Register (TDRHT2), address 0x0C08

BIT	NAME	DEFAULT	FUNCTION
15	Reserved	0,RO	Ignore on read
14:8	cfg_ptrn_High_th_3	0x4A,RW	Peak (absolute) High threshold value 3, for TX pattern.
7	Reserved	0,RO	Ignore on read
6:0	cfg_ptrn_High_th_2	0x53,RW	Peak (absolute) High threshold value 2, for TX pattern.

8.5.16 TDR High Threshold Register (TDRHT3)

This register allows configuring the threshold for finding the peaks of the reflected signal in the TDR test.

Table 8-45. TDR High Threshold Register (TDRHT3), address 0x0C09

BIT	NAME	DEFAULT	FUNCTION
15	Reserved	0,RO	Ignore on read
14:8	cfg_ptrn_High_th_5	0x2F,RW	Peak (absolute) High threshold value 5, for TX pattern.
7	Reserved	0,RO	Ignore on read
6:0	cfg_ptrn_High_th_4	0x3A,RW	Peak (absolute) High threshold value 4, for TX pattern.

8.5.17 TDR High Threshold Register (TDRHT4)

This register allows configuring the threshold for finding the peaks of the reflected signal in the TDR test.

Table 8-46. TDR High Threshold Register (TDRHT4), address 0x0C0A

BIT	NAME	DEFAULT	FUNCTION
15	Reserved	0,RO	Ignore on read
14:8	cfg_ptrn_High_th_7	0x1F,RW	Peak (absolute) High threshold value 7, for TX pattern.
7	Reserved	0,RO	Ignore on read
6:0	cfg_ptrn_High_th_6	0x26,RW	Peak (absolute) High threshold value 6, for TX pattern.

8.5.18 TDR Pattern Control Register 1 (TDRLCR1)

This register allows configuring the forward shadow values for the TDR test.

Table 8-47. TDR Pattern Control Register 1 (TDRLCR1), address 0x0C0B

BIT	NAME	DEFAULT	FUNCTION
15:12	Reserved	0,RO	Ignore on read
11:9	cfg_ptrn_fr_shdw_inc	0x1,RW	Forward shadow area from peak detection increment factor (X/128).
8:5	cfg_ptrn_init_fr_shdw	0x6,RW	Forward shadow area from peak detection initial samples size.
4:0	cfg_ptrn_init_skip	0x10, RW	Initial skip (ignore) samples number from Tx start.

8.5.19 TDR Pattern Control Register 2 (TDRLCR2)

This register allows configuring the gear threshold values for the TDR test.

Table 8-48. TDR Pattern Control Register 2 (TDRLCR2), address 0x0C0C

BIT	NAME	DEFAULT	FUNCTION
15:9	Reserved	0,RO	Ignore on read
8:4	cfg_ptrn_gear_tout	0x14,RW	Thresholds gear shifts distance in samples
3:0	Reserved	0x8,RO	Ignore on read

8.5.20 DSA Configuration Register 1 (DSACR1)

This register allows use of the smoothing filter during the DSA tests.

Table 8-49. DSA Configuration Register 1 (DSACR1), address 0x0C26

BIT	NAME	DEFAULT	FUNCTION
15:7	Reserved	0x180,RO	Ignore on read
6	cfg_dsa_smooth_filt_byps	0x1,RW	0 = Disable DSA engine smooth filter bypass 1 = Enable DSA engine smooth filter bypass
5:0	Reserved	0x04,RO	Ignore on read

8.5.21 DSA Configuration Register 2 (DSACR2)

This register allows configuration of the DSA taps are used for the DSA tests. We specify the first and last taps in use and the DSA uses all the taps between them.

Table 8-50. DSA Configuration Register 2 (DSACR2), address 0x0C27

BIT	NAME	DEFAULT	FUNCTION
15:8	cfg_dsa_en_last_coeff_num	0x1E,RW	Last coefficient number used by the DSA engine
7:0	cfg_dsa_en_first_coeff_num	0x0,RW	First coefficient number used by the DSA engine

8.5.22 DSA Start Frequency (DSASFR)

This register allows configuration of the starting frequency for the spectrum analysis of the DSA engine. It represents 1.9 kHz resolution in the frequency domain.

Table 8-51. DSA Start Frequency (DSASFR), address 0x0C28

BIT	NAME	DEFAULT	FUNCTION
15:0	cfg_start_freq	0x0,RW	Starting frequency for the DSA

8.5.23 DSA Frequency Control (DSAFCR)

This register defines the average factor we will use in the DSA. In addition it defines the frequency step for the DSA. The field represents resolution of 119.2 Hz.

Table 8-52. DSA Frequency Control (DSAFCR), address 0x0C29

BIT	NAME	DEFAULT	FUNCTION
15:12	cfg_dsa_average	0xA,RW	Averaging factor for DSA engine – 2X cycles
11	Reserved	0x0,RO	Reserved
10:0	cfg_dsa_inc_factor	0x400,RW	DSA Frequency increment factor (frequency step)

8.5.24 DSA Output Control (DSAOCR)

This register configures which DSA outputs are selected to the 16 bit RAM available bits. The files configure the MSB location of the DSA engine.

Table 8-53. DSA Output Control (DSAOCR), address 0x0C2A

BIT	NAME	DEFAULT	FUNCTION
15:12	cfg_dsa_output_msb	0x0,RW	DSA output MSB select. Select which bits of the DSA output are saved in the RAM
11:0	Reserved	0x003,RO	Reserved

8.5.25 RAM Control 1 (RAMCR1)

This register enables the RAM in order to read the DSA results.

Table 8-54. RAM Control 1 (RAMCR1), address 0x0D00

BIT	NAME	DEFAULT	FUNCTION
15	cpu_ram_en	0x0,RW	1 = Enable CPU access to RAM 0 = Disable CPU access to RAM
14:0	Reserved	0x0,RO	Reserved

8.5.26 RAM Control 2 (RAMCR2)

This register enables resetting the RAM memory and address prior to starting the DSA test

Table 8-55. RAM Control 2 (RAMCR2), address 0x0D01

BIT	NAME	DEFAULT	FUNCTION
15	man_cable_diag_restart	0x0,RW	1= Restart cable diagnostics block manual 0 = Do not restart cable diagnostics block manual
14	man_cable_diag_reset	0x0,RW	1= Soft reset of cable diagnostics block manual 0 = Do not reset cable diagnostics block manual
13	reset_ram_addr_indx	0x0,RW	1= Reset RAM address index 0 = Do not reset RAM address index
12:0	Reserved	0x0,RO	Reserved

8.5.27 RAM Data Out (RAMDR)

This register is the DSA output result register.

Table 8-56. RAM Data Out (RAMDR), address 0x0D04

BIT	NAME	DEFAULT	FUNCTION
15:0	RAM Data Out	0x0,RW	RAM data out

8.5.28 CD Pre Test Configuration Control 1 (CDPTC1R)

This register enables cable diagnostic pre test configuration.

Table 8-57. CD Pre Test Configuration Control 1 (CDPTC1R), address 0x0107

BIT	NAME	DEFAULT	FUNCTION
15:9	Reserved	0x0,RO	Reserved
8	cd_pre_test_cfg_en	0,RW	1 = Enable Cable diagnostic pre test configuration 0 = Disable Cable diagnostic pre test configuration
7:0	Reserved	0,RO	Reserved

8.5.29 CD Pre Test Configuration Control 2 (CDPTC2R)

This register latches the outcome of enabling the cable diagnostic pre test configuration.

Table 8-58. CD Pre Test Configuration Control 2 (CDPTC2R), address 0x010F

BIT	NAME	DEFAULT	FUNCTION
15:4	Reserved	0x034,RO	Reserved
3	cd_pre_test_cfg_latched	0,RW	1 = Cable Diagnostic pre test configuration is latched 0 = Cable Diagnostic pre test configuration is not latched
2:0	Reserved	0,RO	Reserved

8.5.30 LPF Bypass (LPFBR)

This register enables to bypass the LPF for the DSA tests.

Table 8-59. LPF Bypass (LPFBR), address 0x00AC

BIT	NAME	DEFAULT	FUNCTION
15:11	Reserved	0x0,RO	Reserved
10	dsa_lpf_bypass	0,RW	1 = Bypass DSA LPF 0 = Do not bypass DSA LPF
9:0	Reserved	0,RO	Reserved

9 Electrical Specifications

All parameters are derived by test, statistical analysis, or design.

9.1 ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
VDD33_IO, VDD33_VA11, VDD33_V18, VDD33_VD11	Supply voltage	–0.3 to 3.8	V
V18_PFBIN1, V18_PFBIN2		–0.3 to 2.2	V
VA11_PFBIN1, VA11_PFBIN2		–0.3 to 1.8	V
XI	DC Input voltage	–0.3 to 2.2	V
TD-, TD+, RD-, RD+		–0.3 to 6	V
Other Inputs		–0.3 to 3.8	V
XO	DC Output voltage	–0.3 to 2.2	V
Other outputs		–0.3 to 3.8	V
Maximum die temperature θ_J		105	°C
ESD	IEC 60749-26 ESD (human-body model)(2)	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model)(2)	±16	
	JEDEC Standard 22, Test Method A114 (human-body model), all pins	1.5	
	JEDEC Standard 22, Test Method C101 (charged-device model), all pins	1.5	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) On pins TD+, TD-, RD+, RD-, with VDD33_IO, VDD33_VA11 VDD33_V18, VDD33_VD11, V18_PFBIN1, V18_PFBIN2, VA11_PFBIN1, VA11_PFBIN2, VA11_PFBOUT, V18_PFBOUT, VDD11, VSS connected to ground potential.

9.2 THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance (no airflow)		26.8		°C/W
θ_{JB}	Junction-to-board thermal resistance		16.2		
θ_{JC}	Junction-to-case thermal resistance		40		

9.3 RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
VDD33_VA11,VDD33_V18, VDD33_VD11	Core Supply voltage	2.38	3.3	3.6	V
VDD33_IO	I/O 3.3V Supply	3.0	3.3	3.6	V
V18_PFBIN1, V18_PFBIN2	External Supply(1)	1.7	1.8	1.9	V
VA11_PFBIN1, VA11_PFBIN2		1.04	1.1	1.15	V
T_A	Ambient temperature(2)	–40		85	°C
P_D	Power dissipation(3)			189	mW

(1) When the internal voltage regulator is not used and the external supply is used
(2) Provided that GNDPAD, pin 49, is soldered down. See Thermal Vias Recommendation for more detail.
(3) For 100Base-TX, When external 1.8V, 1.1 and 3.3V supplies are used.

9.4 DC CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage (1)		2.0			V
V_{IL}	Input low voltage (1)				0.8	V
I_{IH}	Input high current	$V_{IN} = V_{CC}$			10	µA
I_{IL}	Input low current	V_{IN} = GND			10	µA
V_{OL}	Output low voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = –4 mA	V_{CC} – 0.5			V
I_{OZ}	3-State leakage	$V_{OUT} = V_{CC}$, V_{OUT} = GND			±10	µA
V_{TPTD_100}	100M transmit voltage		0.95	1	1.05	V
$V_{TPTDsym}$	100M transmit voltage symmetry				±2%	
V_{TPTD_10}	10M transmit voltage		2.2	2.5	2.8	V
C_{IN1}	CMOS input capacitance			5		pF
COUT1	CMOS output capacitance			5		pF
SD_{THon}	100BASE-TX Signal detect turnon threshold				1000	mV diff pk-pk
SD_{THoff}	100BASE-TX Signal detect turnoff threshold		200			mV diff pk-pk
V_{TH1}	10BASE-T Receive threshold				585	mV

(1) Nominal V_{CC} of VDD33_IO = 3.3V

9.5 POWER SUPPLY CHARACTERISTICS

The data was measured from a TLK100 evaluation board. The current from each of the power supply is measured and the power dissipation is computed. For the single 3.3V external supply case the power dissipation across the internal linear regulator is also included. All the power dissipation numbers are measured at the nominal power supply and typical temperature of 25°C.

9.5.1 Active Power

PARAMETER	TEST CONDITIONS	FROM THE POWER SUPPLIES	FROM THE CENTER TAP	UNIT
100BASE-T /W Traffic (full packet 1518B rate)	Multiple External Supplies	146	43	mW
	Single 3.3V external supply	316	80	
10BASE-T /W Traffic (full packet 1518B rate)	Multiple External Supplies	84	205	
	Single 3.3V external supply	189	205	

9.5.2 Power Down Power

PARAMETER	TEST CONDITIONS	FROM THE POWER SUPPLIES	UNIT
Extreme Low Power Mode	Multiple External Supplies	14.2	mW
	Single 3.3V external supply	23.1	
General Power Down Mode (1)	Multiple External Supplies	18.2	
	Single 3.3V external supply	33	
Passive Sleep Mode	Multiple External Supplies	51.4	
	Single 3.3V external supply	102.3	
Active Sleep Mode	Multiple External Supplies	51.4	
	Single 3.3V external supply	102.3	

(1) The internal PLL is disabled. System works of the Refclk

9.6 AC Specifications

Table 9-1. Power Up Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Reset deassertion time from power up			200		µs
t_2	Time from reset deassertion to the hardware configuration pins transition to output drivers	Hardware Configuration Pins are described in the Pin Description section.		46		ns

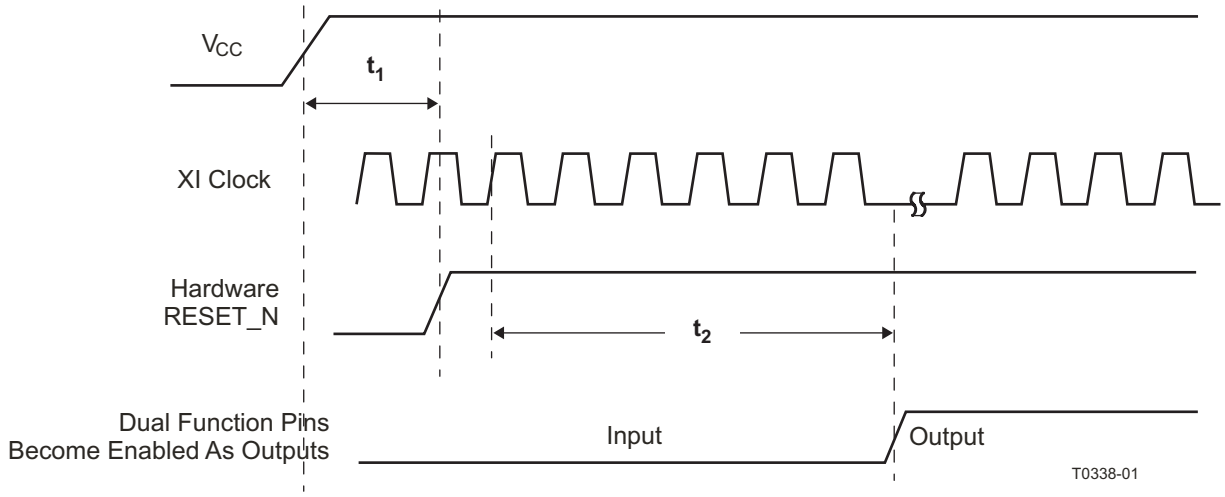


Figure 9-1. Power Up Timing

NOTE

It is important to choose pull-up and/or pull-down resistors for each of the hardware configuration pins that provide fast RC time constants in order to latch-in the proper value prior to the pin transitioning to an output driver.

Table 9-2. Reset Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	RESET pulse width	XI Clock must be stable for at min. of 1ms during RESET pulse low time.	1			µs

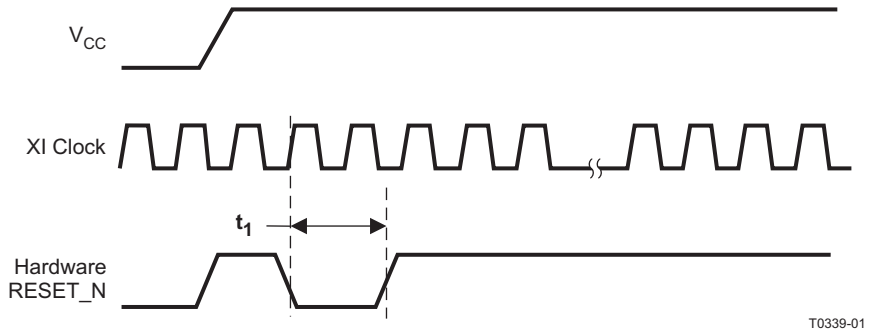


Figure 9-2. Reset Timing

Table 9-3. MII Serial Management Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	MDC Frequency			2.5	25	MHz
t_2	MDC to MDIO (Output) Delay Time		0			ns
t_3	MDIO (Input) to MDC Hold Time		10			ns
t_4	MDIO (Input) to MDC Setup Time		10			ns

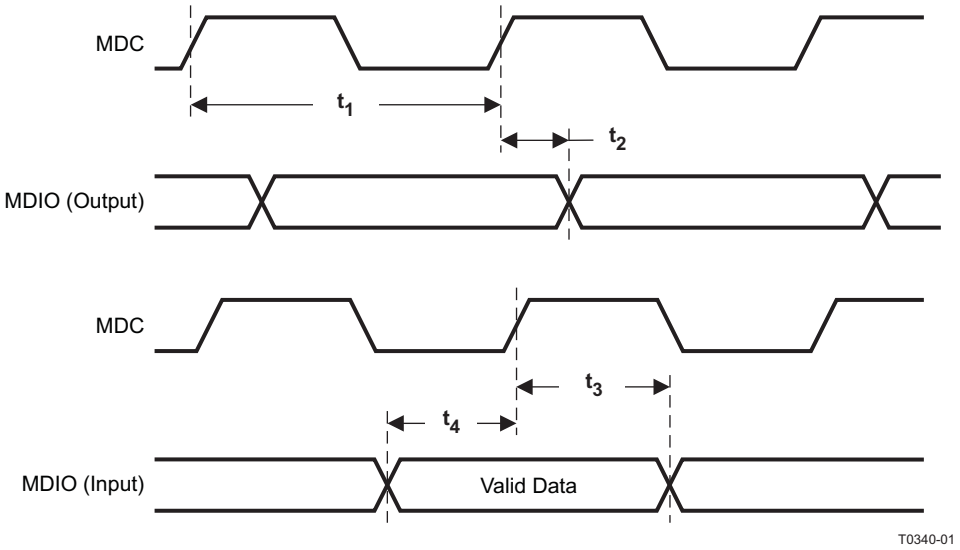


Figure 9-3. MII Serial Management Timing

Table 9-4. 100Mb/s MII Transmit Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_CLK High Time	100 Mb/s Normal mode	16	20	24	ns
t_2	TX_CLK Low Time					
t_3	TXD[3:0], TX_EN Data Setup to TX_CLK	100 Mb/s Normal mode	10			ns
t_4	TXD[3:0], TX_EN Data Hold from TX_CLK	100 Mb/s Normal mode	0			ns

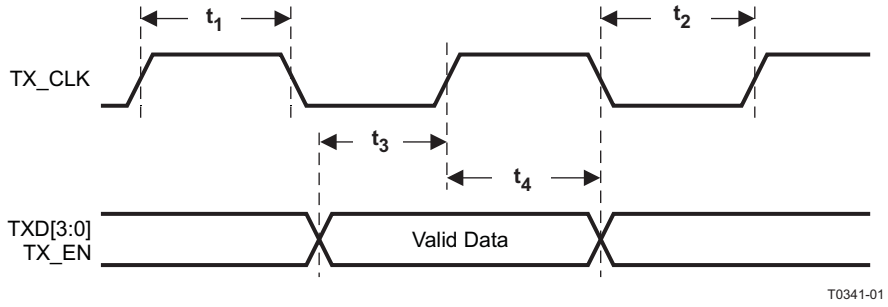


Figure 9-4. 100Mb/s MII Transmit Timing

Table 9-5. 100Mb/s MII Receive Timing

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	RX_CLK High Time	100 Mb/s Normal mode	16	20	24	ns
t_2	RX_CLK Low Time					
t_3	RX_CLK to RXD[3:0], RX_DV, RX_ER Delay	100 Mb/s Normal mode	10		30	ns

(1) RX_CLK may be held low or high for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.

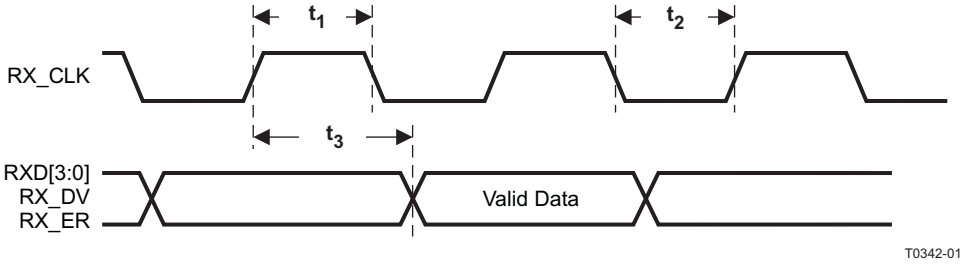


Figure 9-5. 100Mb/s MII Receive Timing

Table 9-6. 100BASE-TX Transmit Packet Latency Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_CLK to PMD Output Pair Latency	100 Mb/s Normal mode[1]		8.6		bits

(1) For Normal mode, latency is determined by measuring the time from the first rising edge of TX_CLK occurring after the assertion of TX_EN to the first bit of the 'J' code group as output from the PMD Output Pair. 1 bit time = 10ns in 100 Mb/s mode.

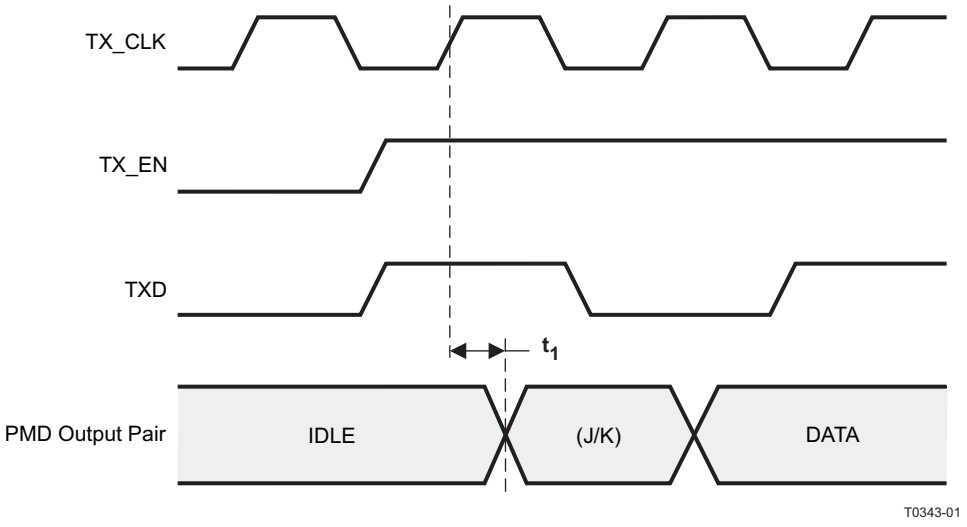


Figure 9-6. 100BASE-TX Transmit Packet Latency Timing

Table 9-7. 100BASE-TX Transmit Packet Deassertion Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_CLK to PMD Output Pair deassertion	100 Mb/s Normal mode		8.6		bits

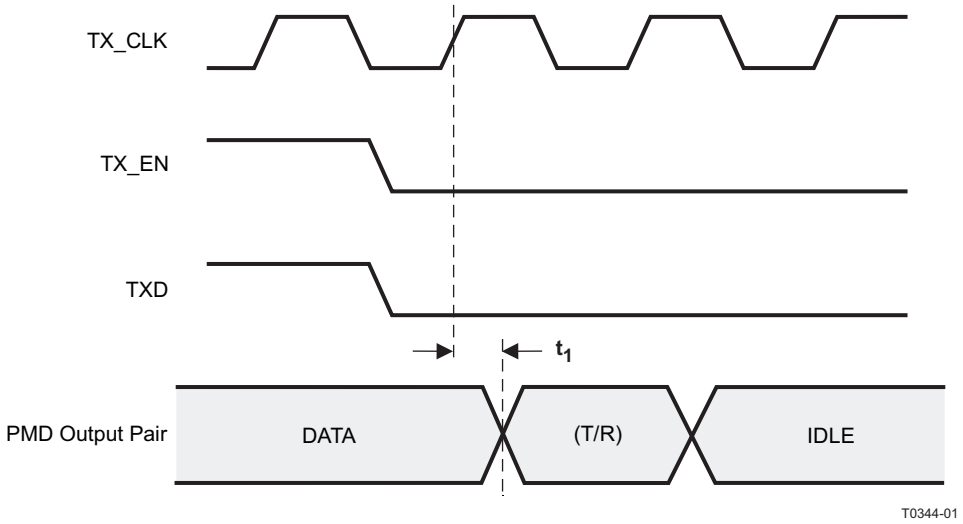


Figure 9-7. 100BASE-TX Transmit Packet Latency Timing

Table 9-8. 100BASE-TX Transmit Timing ($t_{R/F}$ and Jitter)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	100 Mb/s PMD Output Pair t_R and t_F (1)		3	4	5	ns
	100 Mb/s t_R and t_F Mismatch (2)				500	ps
t_2	100 Mb/s PMD Output Pair Transmit Jitter				1.4	ns

(1) Rise and fall times taken at 10% and 90% of the +1 or -1 amplitude.
(2) Normal Mismatch is the difference between the maximum and minimum of all rise and fall times.

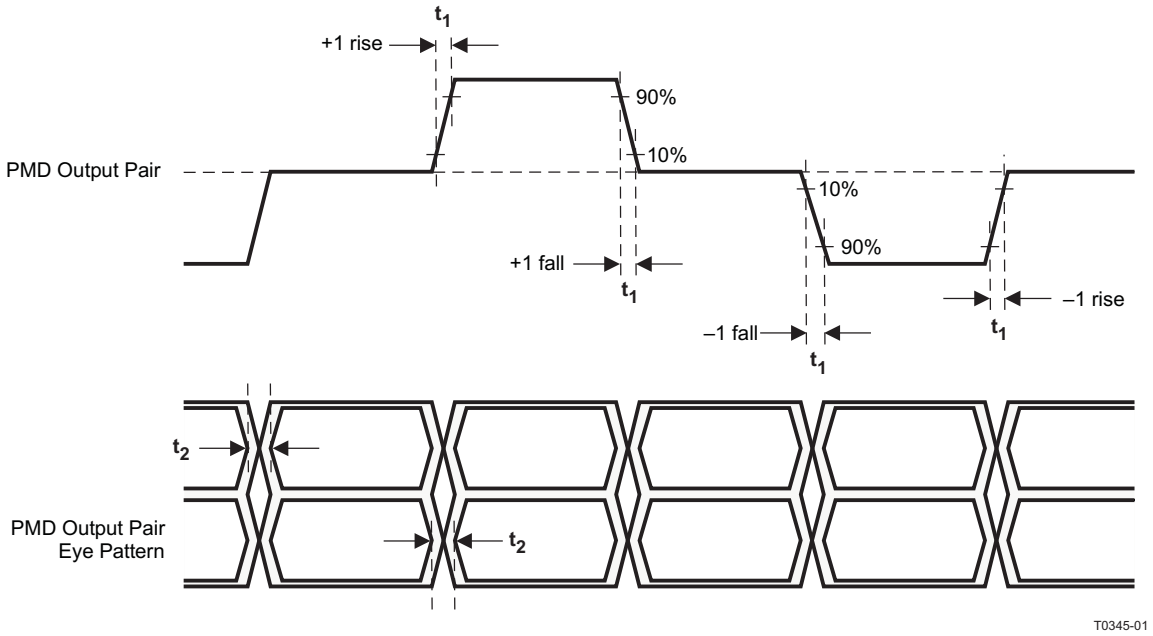


Figure 9-8. 100BASE-TX Transmit Timing ($t_{R/F}$ and Jitter)

Table 9-9. 100BASE-TX Receive Packet Latency Timing

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
t_1	Carrier Sense ON Delay(2)	100 Mb/s Normal mode		13.6		bits(3)
t_2	Receive Data Latency	100 Mb/s Normal mode		18.4		bits

(1) PMD Input Pair voltage amplitude is greater than the Signal Detect Turn-On Threshold Value.
(2) Carrier Sense On Delay is determined by measuring the time from the first bit of the “J” code group to the assertion of Carrier Sense.
(3) 1 bit time = 10 ns in 100 Mb/s mode

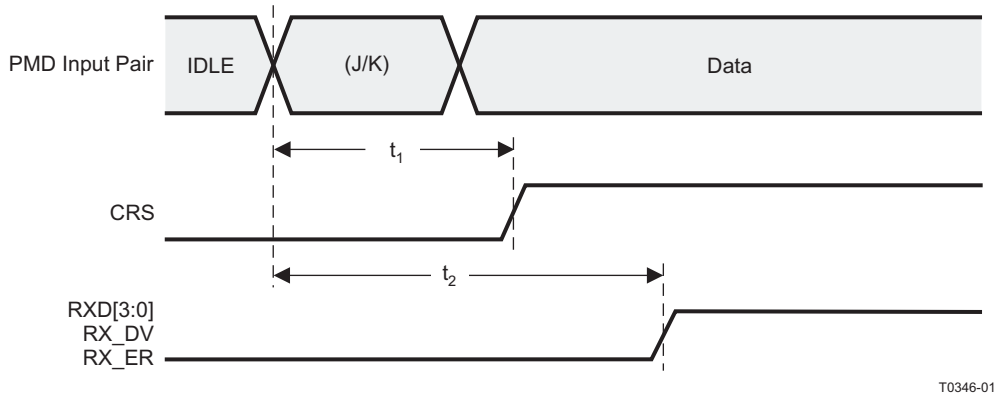


Figure 9-9. 100BASE-TX Receive Packet Latency Timing

Table 9-10. 100BASE-TX Receive Packet Deassertion Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Carrier Sense OFF Delay(1)	100 Mb/s Normal mode		13.6		bits(2)

(1) Carrier Sense Off Delay is determined by measuring the time from the first bit of the “T” code group to the deassertion of Carrier Sense.
(2) 1 bit time = 10 ns in 100 Mb/s mode

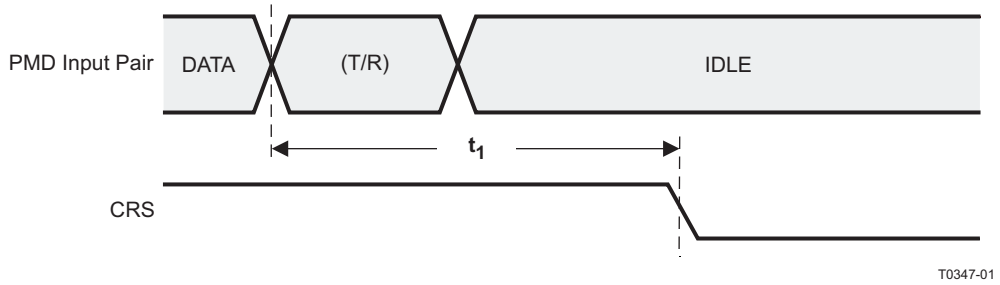


Figure 9-10. 100BASE-TX Receive Packet Deassertion Timing

Table 9-11. 10 Mb/s MII Transmit Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_CLK Low Time	10 Mb/s MII mode	190	200	210	ns
t_2	TX_CLK High Time					
t_3	TXD[3:0], TX_EN Data Setup to TX_CLK ↓	10 Mb/s MII mode	25			ns
t_4	TXD[3:0], TX_EN Data Hold from TX_CLK ↑	10 Mb/s MII mode	0			ns

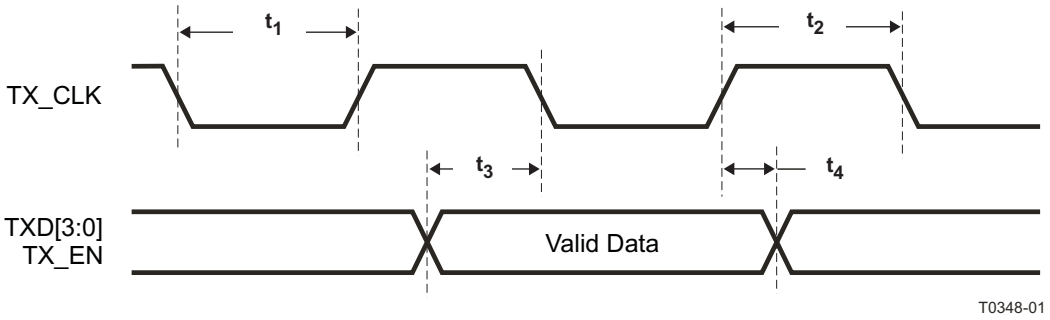


Figure 9-11. 10 Mb/s MII Transmit Timing

Table 9-12. 10Mb/s MII Receive Timing

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	RX_CLK High Time		160	200	240	ns
t_2	RX_CLK Low Time					
t_3	RX_CLK rising edge delay from RXD[3:0], RX_DV Valid	10 Mb/s MII mode	100			ns
t_4	RX_CLK to RXD[3:0], RX_DV Delay	10 Mb/s MII mode	100			ns

(1) RX_CLK may be held low for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.

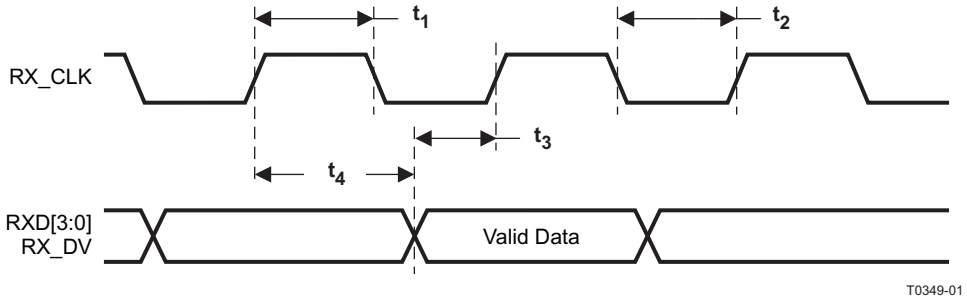


Figure 9-12. 10Mb/s MII Receive Timing

Table 9-13. 10BASE-T Transmit Timing (Start of Packet)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
t_1	Transmit Output Delay from the Falling Edge of TX_CLK	10 Mb/s MII mode		5.8		bits

(1) (1) 1 bit time = 100ns in 10Mb/s.

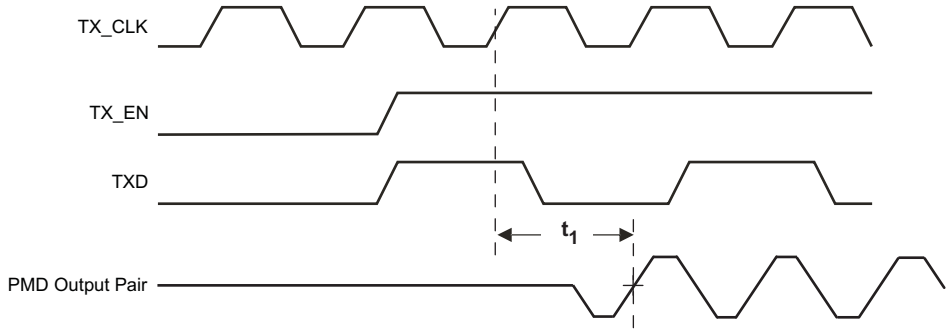


Figure 9-13. 10BASE-T Transmit Timing (Start of Packet)

Table 9-14. 10BASE-T Transmit Timing (End of Packet)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	End of Packet High Time (with '0' ending bit)		250	310		ns
t_2	End of Packet High Time (with '1' ending bit)		250	310		ns

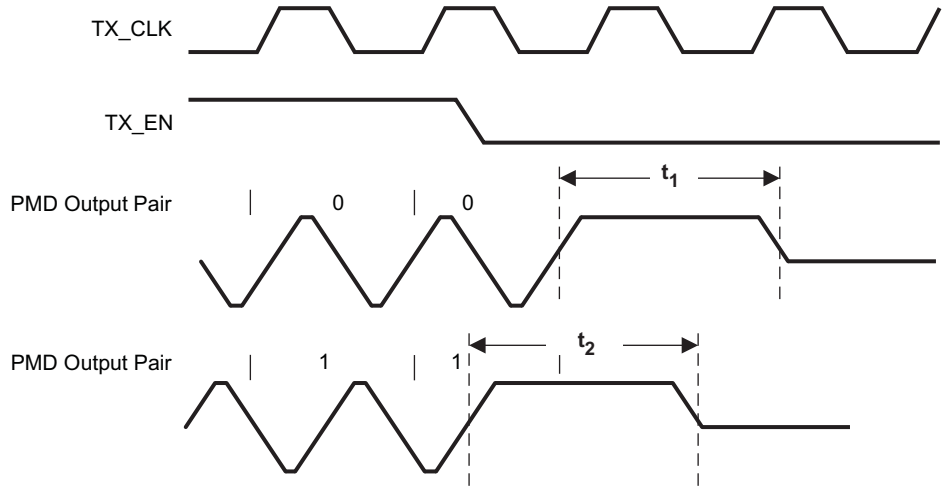


Figure 9-14. 10BASE-T Transmit Timing (End of Packet)

Table 9-15. 10BASE-T Receive Timing (Start of Packet)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Carrier Sense Turn On Delay (PMD Input Pair to MII_CRS)			550	1000	ns
t_2	RX_DV Latency(1)			9.3		bits
t_3	Receive Data Latency	Measurement shown from SFD		14		bits

(1) 10BASE-T RX_DV Latency is measured from first bit of decoded SFD on the wire to the assertion of RX_DV

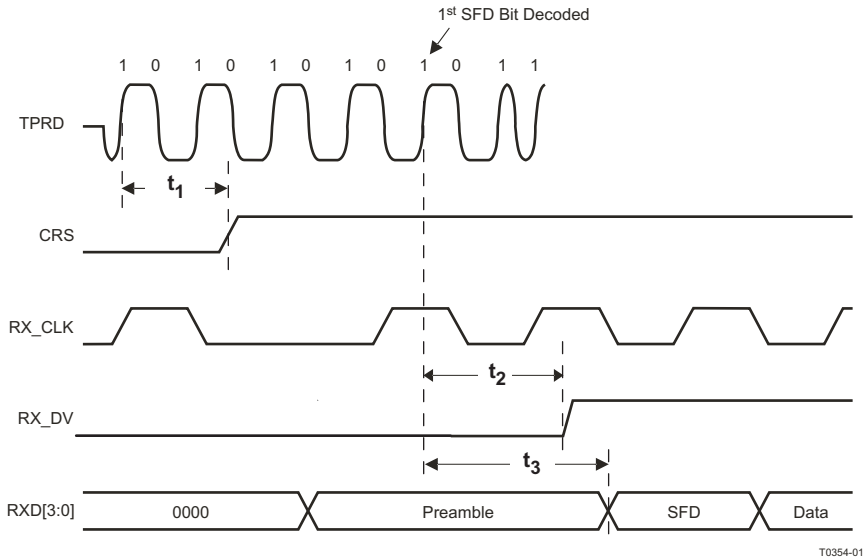


Figure 9-15. 10BASE-T Receive Timing (Start of Packet)

Table 9-16. 10BASE-T Receive Timing (End of Packet)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Carrier Sense Turn Off Delay			1.3		µs

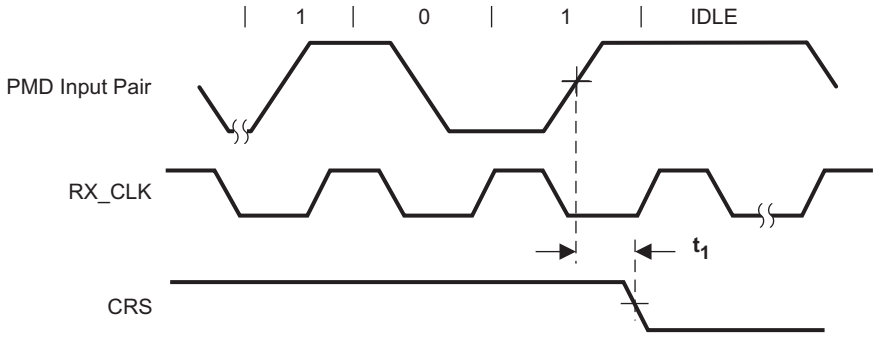


Figure 9-16. 10BASE-T Receive Timing (End of Packet)

Table 9-17. 10Mb/s Jabber Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Jabber Activation Time			100		ms

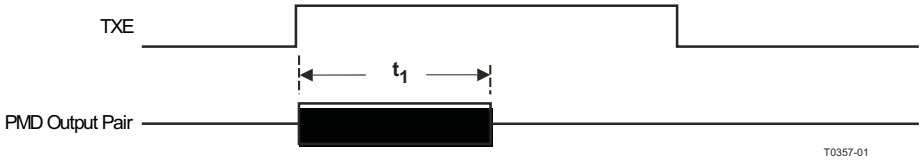


Figure 9-17. 10Mb/s Jabber Timing

Table 9-18. 10BASE-T Normal Link Pulse Timing

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Pulse Period			16		ms
t_2	Pulse Width			100		ns

(1) Transmit timing

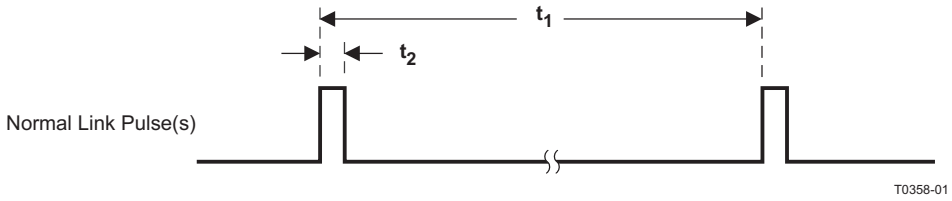


Figure 9-18. 10BASE-T Normal Link Pulse Timing

Table 9-19. Auto-Negotiation Fast Link Pulse (FLP) Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Clock Pulse to Clock Pulse Period			125		µs
t_2	Clock Pulse to Data Pulse Period	Data = 1		62		µs
t_3	Clock, Data Pulse Width			114		ns
t_4	FLP Burst to FLP Burst Period			16		ms
t_5	Burst Width			2		ms

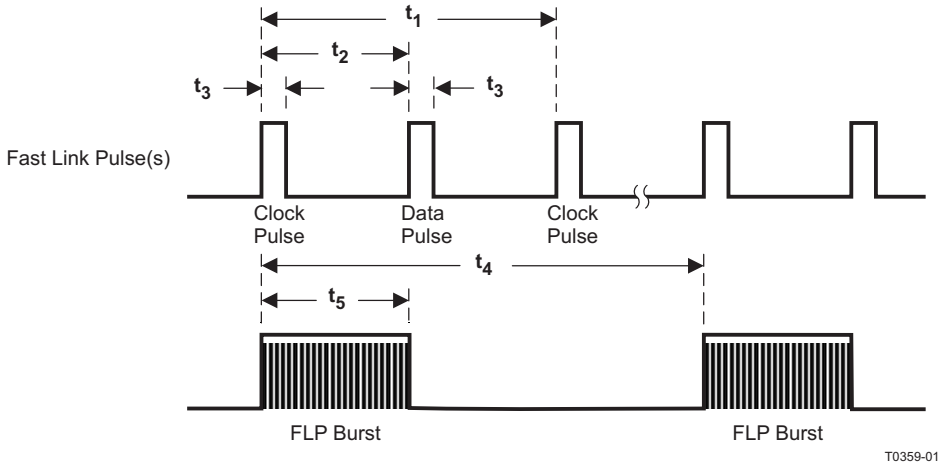
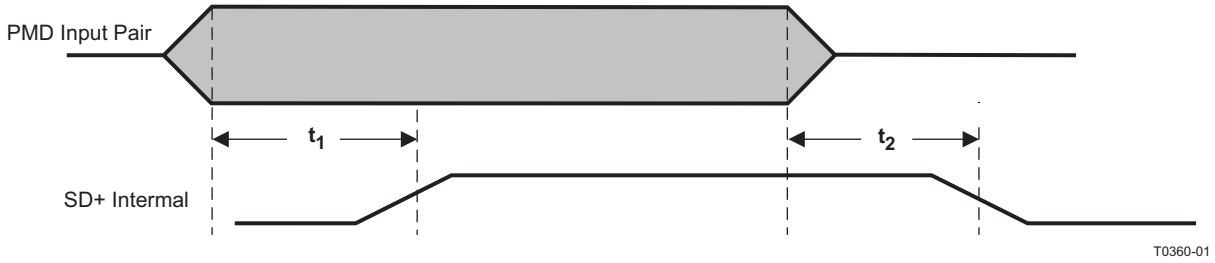


Figure 9-19. Auto-Negotiation Fast Link Pulse (FLP) Timing

Table 9-20. 100BASE-TX Signal Detect Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	SD Internal Turn-on Time				100	µs
t_2	SD Internal Turn-off Time				500	µs

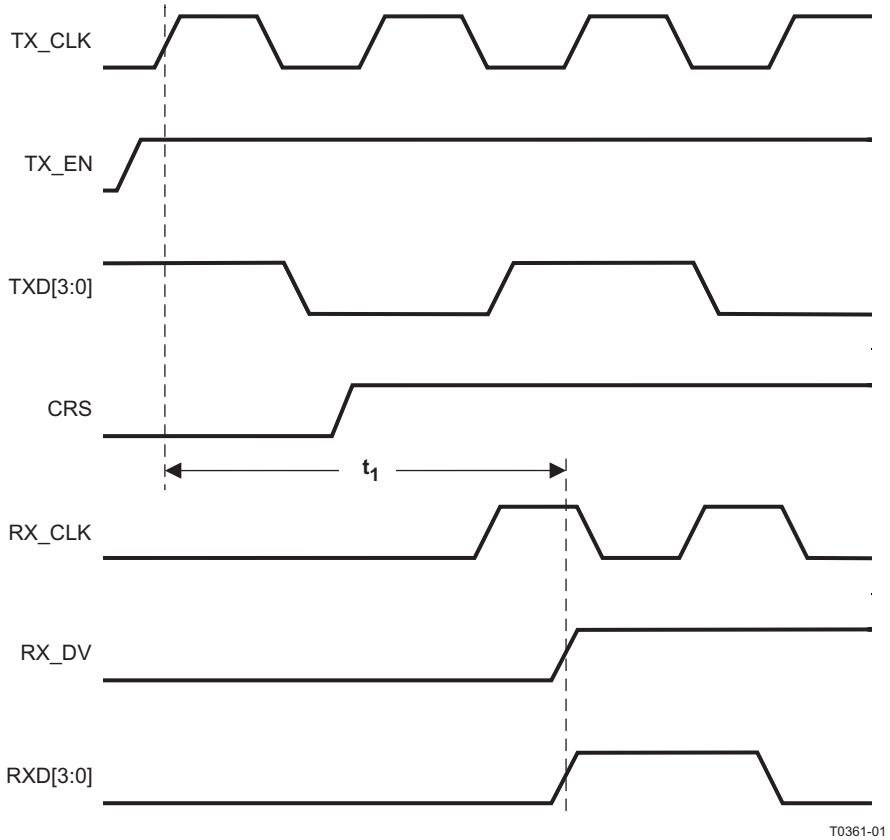


NOTE: The signal amplitude on PMD Input Pair must be TP-PMD compliant.

Figure 9-20. 100BASE-TX Signal Detect Timing

Table 9-21. 100 Mb/s Internal Loopback Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_EN to RX_DV Loopback	100 Mb/s internal loopback mode		272		ns



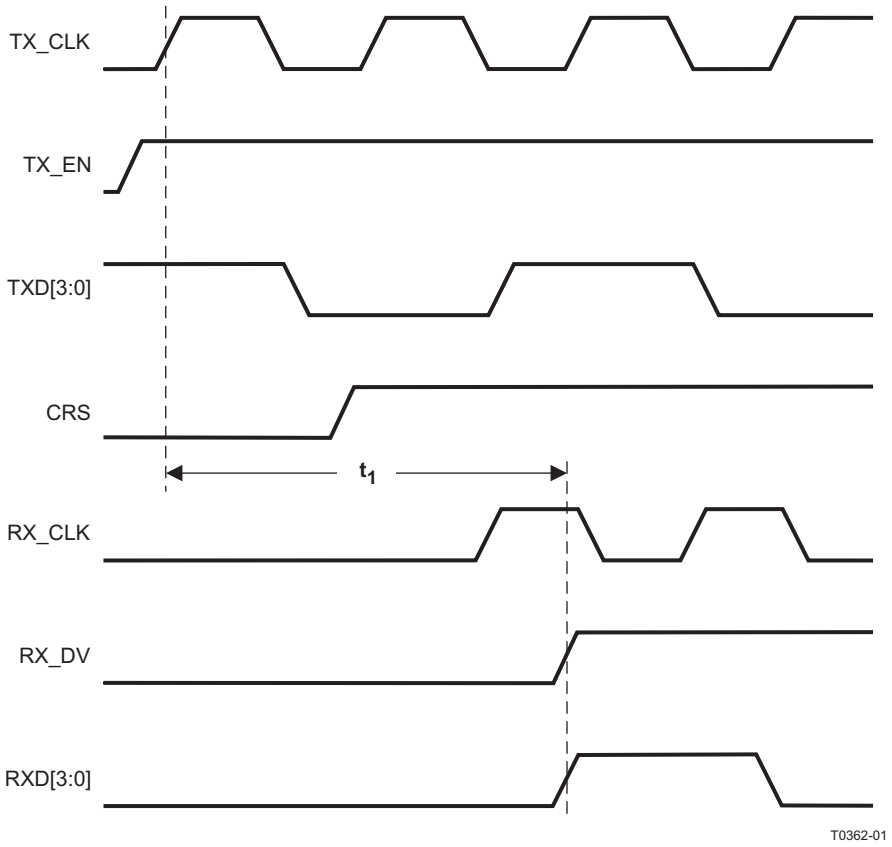
(1) Due to the nature of the descrambler function, all 100BASE-TX Loopback modes will cause an initial *dead-time* of up to 550 µs during which time no data is present at the receive MII outputs. The 100BASE-TX timing specified is based on device delays after the initial 550µs *dead-time*.

(2) Measurement is made from the first rising edge of TX_CLK after assertion of TX_EN.

Figure 9-21. 100 Mb/s Internal Loopback Timing

Table 9-22. 10 Mb/s Internal Loopback Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_EN to RX_DV Loopback	10 Mb/s internal loopback mode			2.4	µs



NOTE: Measurement is made from the first rising edge of TX_CLK after assertion of TX_EN.

Figure 9-22. 10 Mb/s Internal Loopback Timing

Table 9-23. Isolation Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	From Deassertion of S/W or H/W Reset to transition from Isolate to Normal mode			65		ns

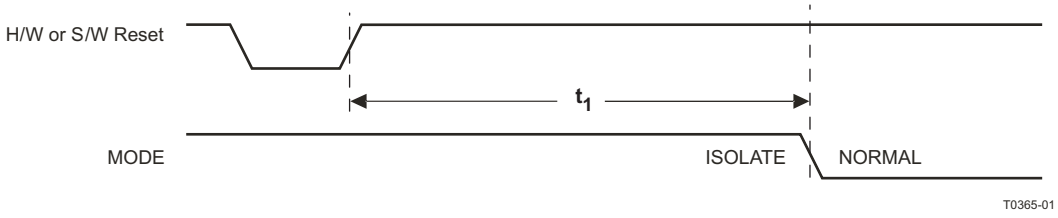


Figure 9-23. Isolation Timing

Table 9-24. 25 MHz_OUT Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	25 MHz_OUT(1) propagation delay	Relative to XI			8.8	ns
t_2	25 MHz_OUT(1) High Time	MII mode		20		ns
t_3	25 MHz_OUT(1) Low Time			20		

(1) 25 MHz_OUT characteristics are dependent upon the XI input characteristics.

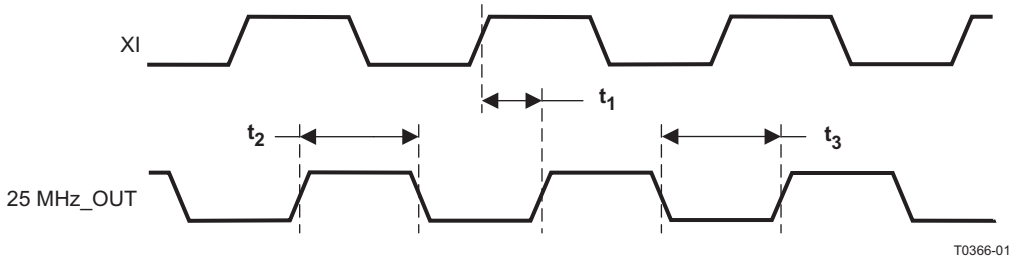


Figure 9-24. 25 MHz_OUT Timing

Table 9-25. 100 Mb/s MII Loopback Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	RX_CLK to RXD[3:0], RX_DV, RX_ER Delay	100 Mb/s MII Loopback mode			1	ns

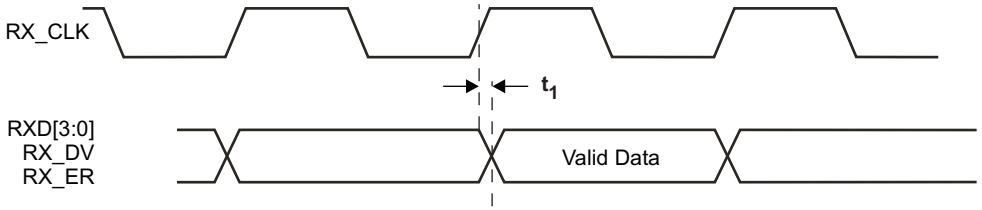
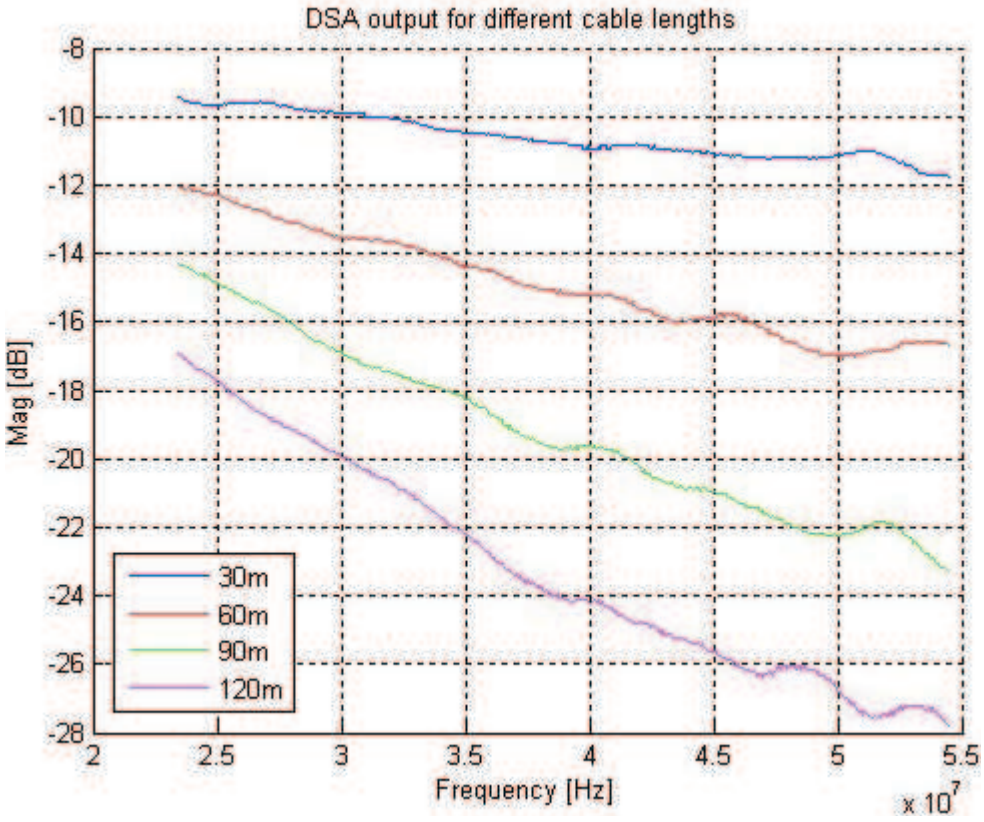


Figure 9-25. 100 Mb/s MII Loopback Timing

10 Appendix A: Digital Spectrum Analyzer (DSA) Output

The following figure is an example of the DSA output. In the figure, 512 samples of the spectral analysis of 4 different cable lengths are provided. The first bin is 23.4 MHz. Each following bin represents 61kHz increment. A view of the LPF nature of the channel and how it increases as longer cables are used is seen.



Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (August 2009) to B Revision ..... **Page**

- Added bullet item " Enables IEEE1588 Time-Stamping" 1
- Added recommendation on operating with multiple supplies 12
- Changed figure (AN Pin Configuration and LED Loading Example) - 110Ω resistors to 470Ω resistors. 16
- Added Interfaces section 21
- Added Architecture section 26
- Changed note from "On pins TD+, TD-, RD+, RD-, VDD33_IO, VDD33_VA11 VDD33_V18, VDD33_VD11, V18_PFBIN1, V18_PFBIN2, VA11_PFBIN1, VA11_PFBIN2, VA11_PFBOUT, V18_PFBOUT, VDD11, VSS." to "On pins TD+,TD-,RD+,RD- with VDD33_IO .... VDD11_VSS connected to ground potential." 69

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK100PHP	NRND	HTQFP	PHP	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLK100	
TLK100PHPR	NRND	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLK100	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

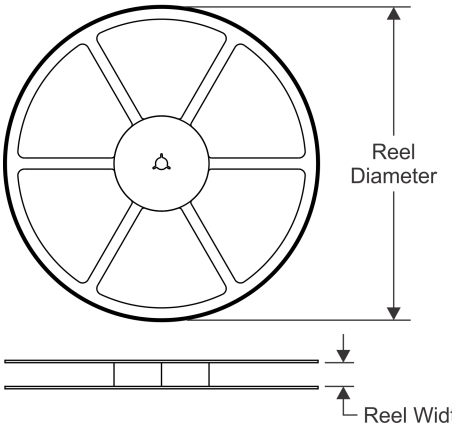
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

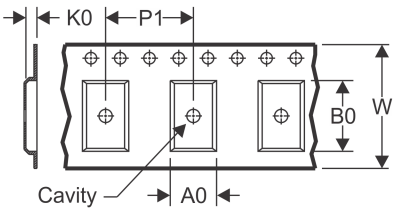
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

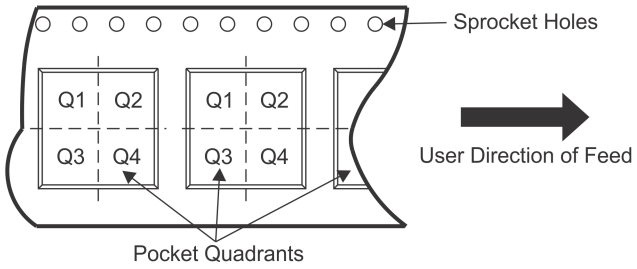


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

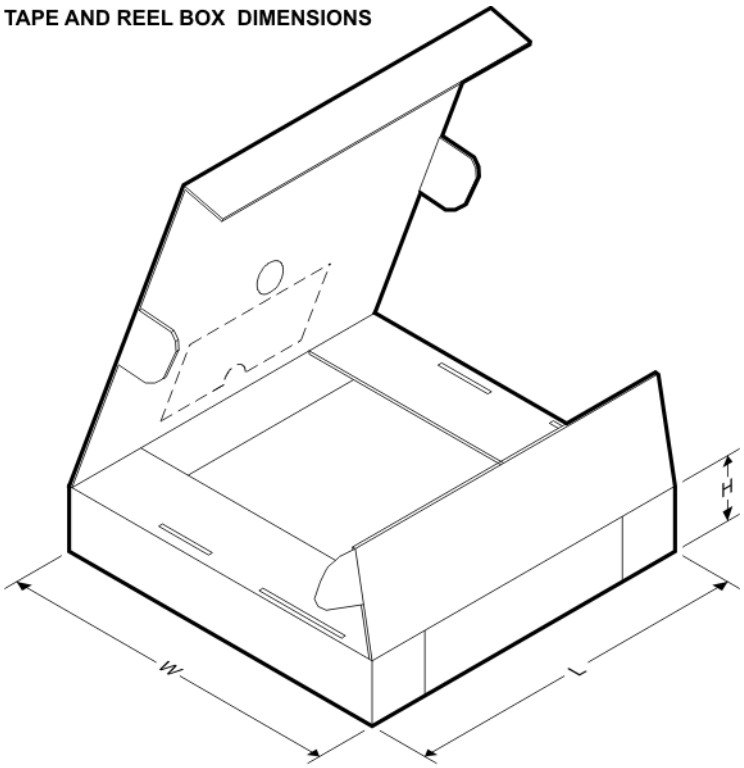
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLK100PHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

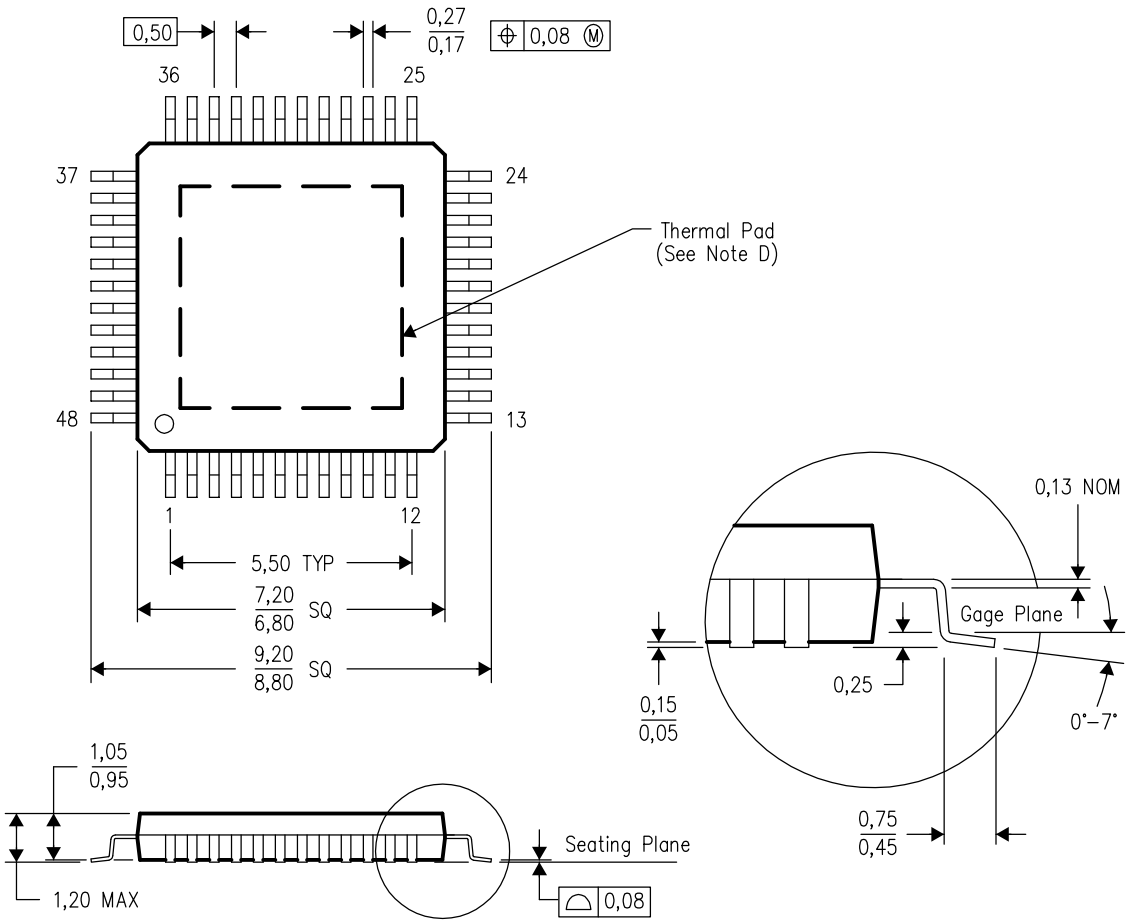
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLK100PHPR	HTQFP	PHP	48	1000	350.0	350.0	43.0

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

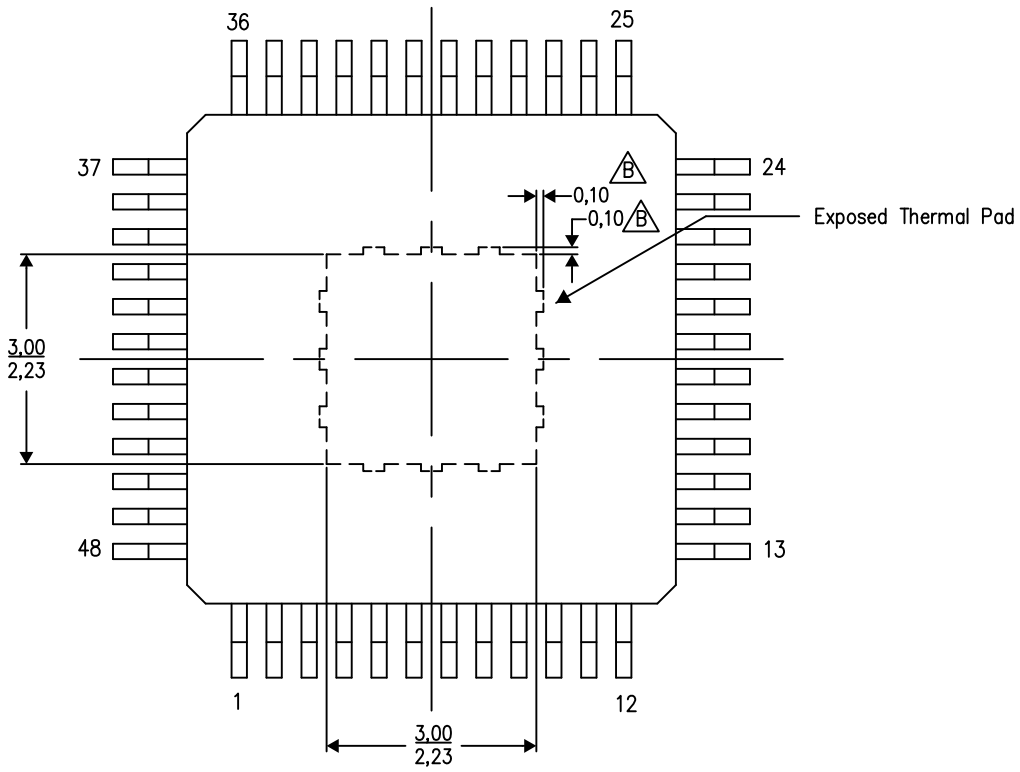
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206329–10/P 03/15

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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