

TLP513

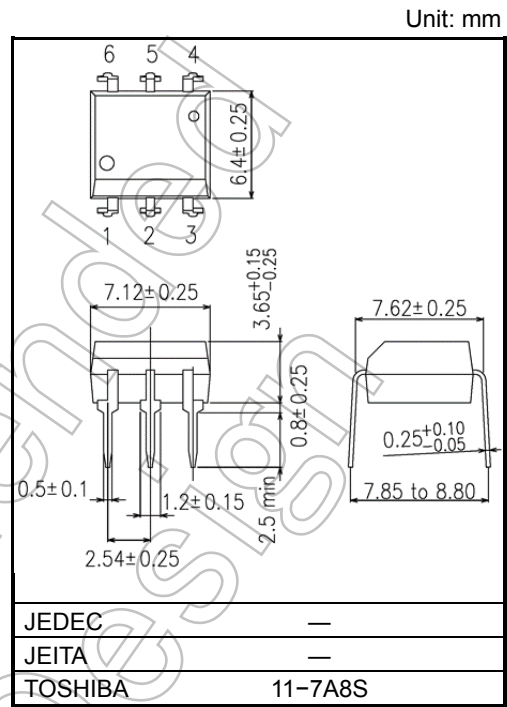
Line Receiver
 Microprocessor System Interface
 Data transfers between circuits of different potentials
 Computer Terminal Interface
 Ground Loop Elimination

TLP513 is a 6-PIN DIP photocoupler, which consists of an infrared emitting diode and a high-gain, high-speed IC detector chip. It has a Schottky clamped transistor and has an open collector output type.

- Threshold input current : $I_F = 5 \text{ mA (max)}$
- Switching Speed : 10 MBd
- Guaranteed performance over temperature: 0 to 70°C
- Isolation voltage : 2500 V_{rms} (min)
- UL-recognized : UL 1577, File No.E67349

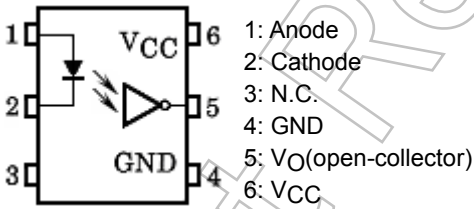
Truth Table (positive Logic)

Input	Output
H	L
L	H

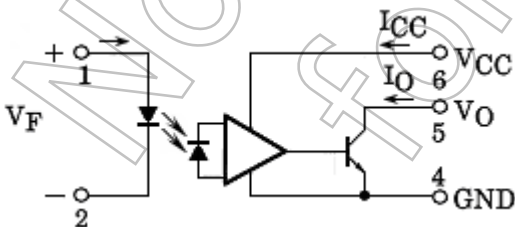


Weight: 0.4 g (typ.)

Pin Configuration (top View)



Schematic



Note: A 0.1 μF bypass capacitor must be connected between pins 6 and 4.

Start of commercial production
 1987-09

Absolute Maximum Rating (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I_F	20	mA
	Forward current derating (Ta ≥ 85°C)	$\Delta I_F / \Delta T_a$	-1.6	mA/°C
	Pulse forward current (Note 1)	I_{FP}	40	mA
	Peak transient forward current (Note 2)	I_{FPT}	1	A
	Reverse voltage	V_R	5	V
	Input power dissipation	P_D	100	mW
	Input power dissipation derating (Ta ≥ 85°C)	$\Delta P_D / ^\circ C$	-2.5	mW/°C
Detector	Output current	I_O	25	mA
	Output voltage	V_O	7	V
	Supply voltage (Note 3)	V_{CC}	7	V
	Output power dissipation	P_O	40	mW
	Output power dissipation derating (Ta ≥ 85°C)	$\Delta P_O / \Delta T_a$	-1.0	mW/°C
Storage temperature range		T_{stg}	-55 to 125	°C
Operating temperature range		T_{opr}	-40 to 85	°C
Lead solder temperature (10 s) (Note 4)	T_{sol}	260	°C	
Isolation voltage (Note 5)		BV_S	2500	V_{rms}

Note: Using continuously under heavy loads (e.g. application of high temperature/current/voltage and a significant change in temperature, etc.) may cause this product to decrease in reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 50 % duty cycle, 1 ms pulse width.

Note 2: Pulse width ≤ 1 μs, 300 pps.

Note 3: 1 minute maximum.

Note 4: Soldering is performed 2mm from the bottom of the package.

Note 5: AC, 60 s, R.H. ≤ 60 %

Device considered a two-terminal device: 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
'L' level input voltage	V_{FL}	-3	0	1.0	V
'H' level input current	I_{FH}	6.3*	8	20	mA
Supply voltage**	V_{CC}	4.5	5	5.5	V
Fan-out (TTL load)	N	—	—	8	—
Operating temperature	T_{opr}	0	—	70	°C

Note: The recommended operating conditions are given as a design guideline to obtain the expected performance of the device. In addition, each item is an independent guideline. In developing designs using this product, please confirm the specified characteristics shown in this document.

* 6.3 mA is a guard banded value which allows for at least 20 % CTR degradation.
Initial input current threshold is 5 mA or less.

** This item denotes the operating range and not the recommended operating conditions.

Electrical Characteristics

(Unless otherwise specified Ta = 0 to 70°C, VCC = 4.5 to 5.5 V, VFL ≤ 1.0 V)

Characteristics	Symbol	Test Conditions	Min	Typ.*	Max	Unit
Forward voltage	V _F	I _F = 10 mA, Ta = 25 °C	—	1.65	1.8	V
Temperature coefficient of forward voltage	ΔV _F / ΔTa	I _F = 10 mA	—	-2.0	—	mV / °C
Input reverse current	I _R	V _R = 5 V, Ta = 25 °C	—	—	10	μA
Input capacitance	C _T	V _F = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
“H” level output current	I _{OH}	V _F = 1.0 V, V _O = 5.5 V	—	—	250	μA
		V _F = 1.0 V, V _O = 5.5 V, Ta = 25 °C	—	0.5	10	
“L” level output voltage	V _{OL}	I _F = 5 mA, I _{OL} = 13 mA (sinking)	—	0.4	0.6	V
“H→L” threshold input current	I _{FH}	I _{OL} = 13 mA (sinking), V _{OL} = 0.6 V	—	—	5	mA
“H” level supply current	I _{CCH}	V _{CC} = 5.5 V, I _F = 0 mA	—	7	15	mA
“L” level supply current	I _{CCL}	V _{CC} = 5.5 V, I _F = 10 mA	—	12	18	mA
Isolation resistance	R _S	V _S = 500 V, R.H. ≤ 60 %, Ta = 25 °C (Note 7)	5 × 10 ¹⁰	10 ¹⁴	—	Ω
Input to output capacitance	C _S	V _S = 0 V, f = 1 MHz, Ta = 25 °C (Note 7)	—	0.6	—	pF

* : All typical values are at Ta = 25°C.

Switching Characteristics (Ta = 25°C, VCC = 5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	t _{pHL}	1	I _F = 0 → 7.5 mA, R _L = 350 Ω, C _L = 15 pF	—	60	120	ns
Propagation delay time (L→H)	t _{pLH}		I _F = 7.5 → 0 mA, R _L = 350 Ω, C _L = 15 pF	—	60	120	ns
Rise time, fall time (10 to 90%)	t _r , t _f		I _F = 0 → 7.5 mA, R _L = 350 Ω, C _L = 15 pF	—	30	—	ns
Common mode transient immunity at high level output	CM _H	2	I _F = 0 mA, R _L = 350 Ω, V _{CM} = 200 V, V _O (min) = 2 V (Note 8)	—	200	—	V / μs
Common mode transient immunity at low level output	CM _L		I _F = 7.5 mA, R _L = 350 Ω, V _{CM} = 200 V, V _O (max) = 0.8 V (Note 9)	—	-500	—	V / μs

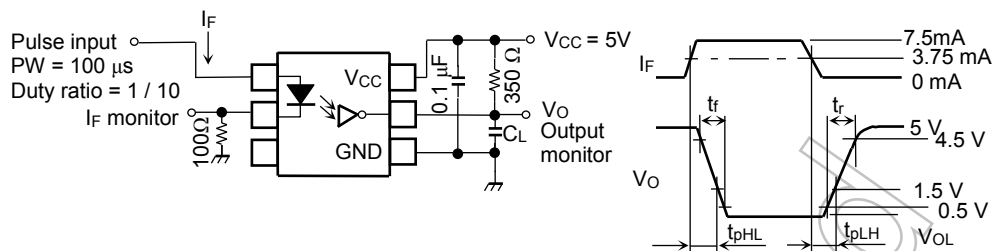
Note 6: The V_{CC} supply voltage to each TLP513 isolator must be bypassed by a 0.1 μF capacitor. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the V_{CC} and GND pins of each device.

Note 7: Device considered a 2-terminal device: Pins 1, 2 and 3 shorted together, and pins 4, 5 and 6 shorted together.

Note 8: CM_H: The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high output state (i.e., V_O > 2.0 V). Measured in volts per microsecond (V / μs).

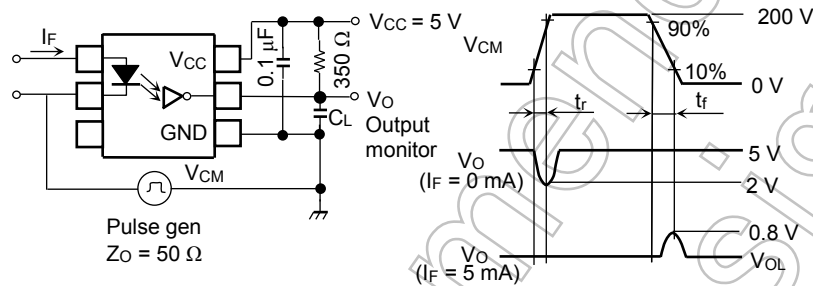
Note 9: CM_L: The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., V_O < 0.8 V). Measured in volts per microsecond (V / μs).

Test Circuit 1: Switching Time Test Circuit



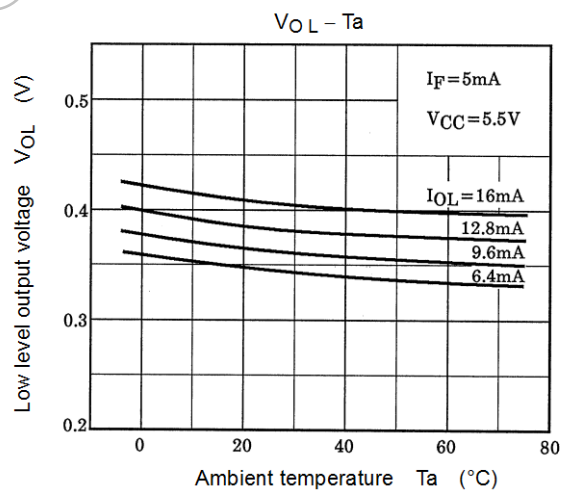
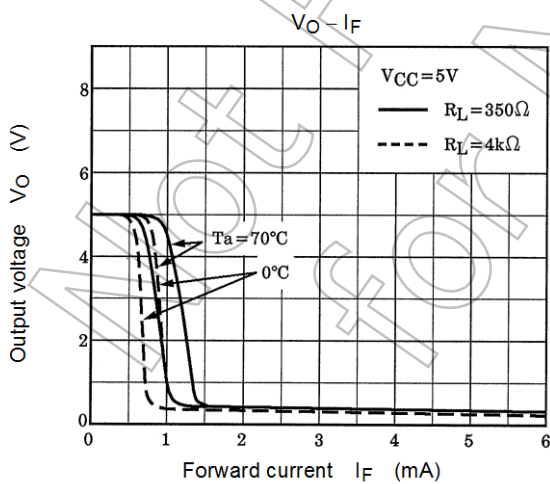
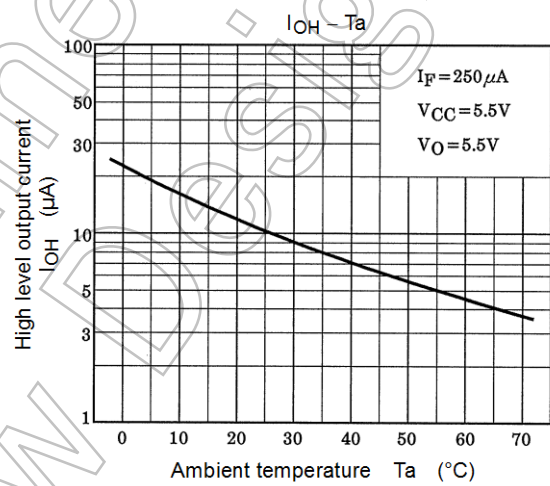
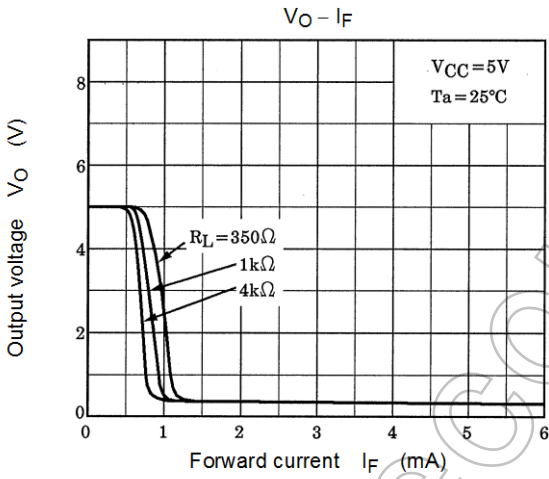
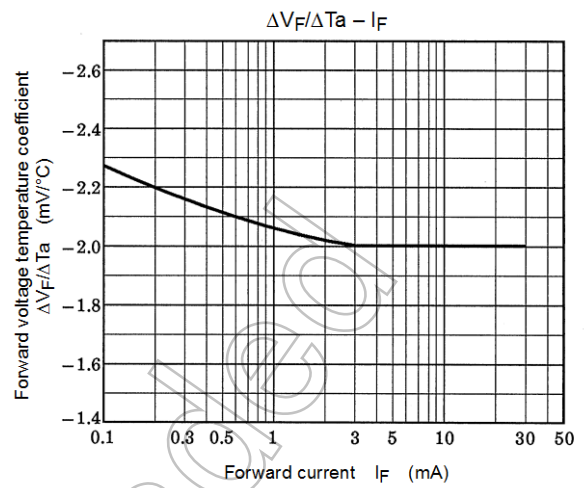
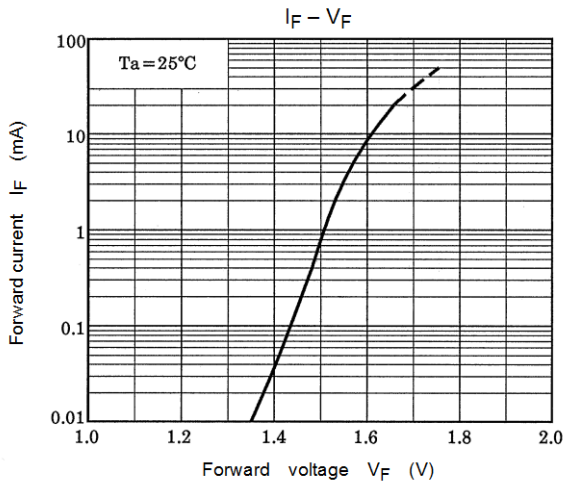
C_L is approximately 15 pF which includes probe and stray wiring

Test Circuit 2: Common Mode Noise Immunity Test Circuit

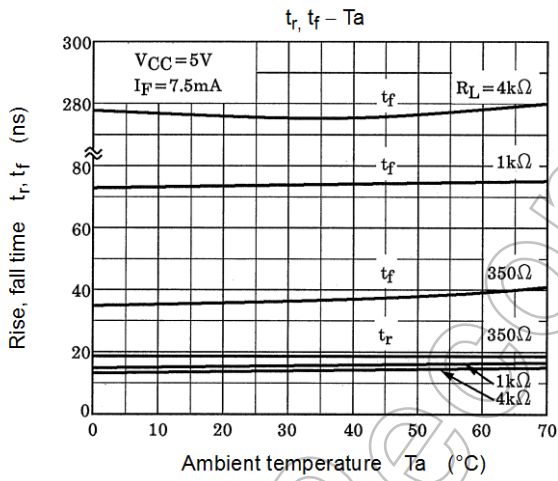
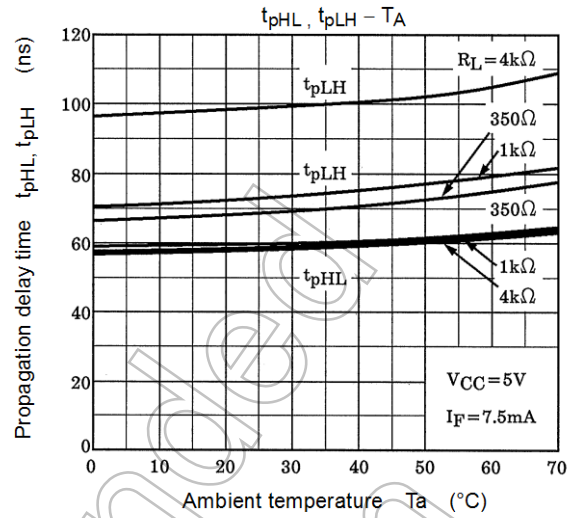
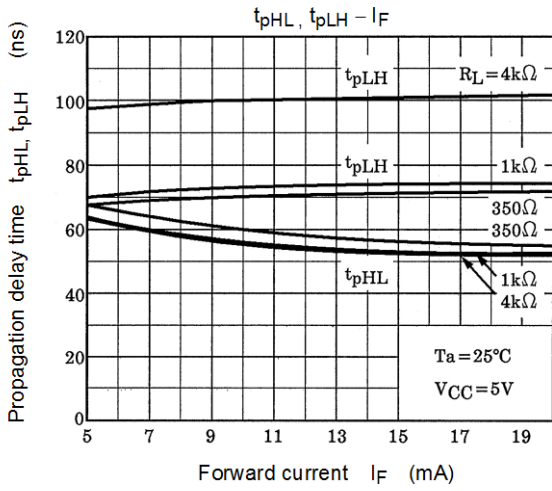


$$CM_H = \frac{160 \text{ (V)}}{t_r \text{ (}\mu\text{s)}}, \quad CM_L = \frac{160 \text{ (V)}}{t_f \text{ (}\mu\text{s)}}$$

C_L is approximately 15 pF which includes probe and stray wiring



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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