

TLP553

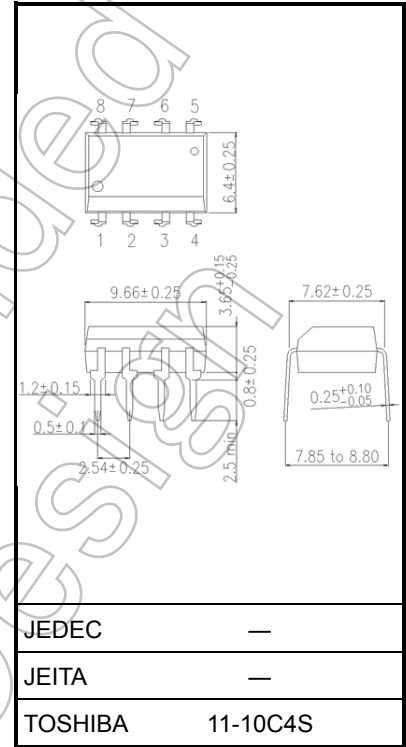
- Low input current line receiver
- Telephone ring detector
- Current loop receiver
- Interfaces for computer, measurement equipment and control equipment
- Data transfer between circuits of different potentials

TLP553 is a Darlington 8-pin DIP photocoupler, which consists of an infrared emitting diode a photodiode and a high-gain transistor integrated into a detector chip.

As it uses a high-speed, high-gain detector element, TLP553 is ideal for applications which require low-input current and high-speed data transmission.

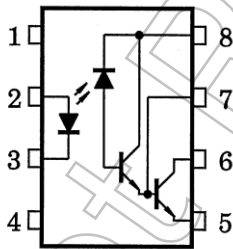
- Current transfer ratio: 400% (min)
@ $I_F = 0.5 \text{ mA}$
- Operating temperature: 0 to 70°C (guaranteed)
- Switching speed: $t_{pHL} = 2 \mu\text{s}$, $t_{pLH} = 4 \mu\text{s}$ (typ.)
@ $R_L = 4.7 \text{ k}\Omega$, $I_F = 0.5 \text{ mA}$
- Isolation voltage: 2500 V_{rms} (min)
- UL-recognized: UL 1577, File No.E67349

Unit: mm



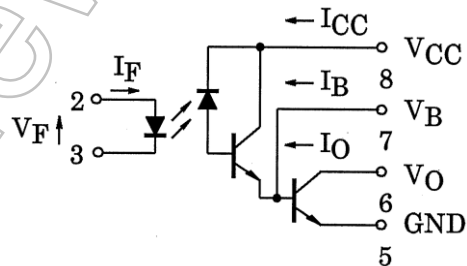
Weight: 0.54 g (typ)

Pin Configurations



- 1: N.C.
- 2: Anode
- 3: Cathode
- 4: N.C.
- 5: GND(emitter)
- 6: V_O (collector)
- 7: Base
- 8: V_{CC}

Schematic



Start of commercial production
1983-11

Absolute Maximum Rating (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current (Note 1)	IF	20	mA
	Pulse forward current (Note 2)	IFP	40	mA
	Peak transient forward current (Note 3)	IFPT	1	A
	Reverse voltage	VR	5	V
	Diode power dissipation (Note 4)	PD	35	mW
Detector	Output current (Note 5)	IO	60	mA
	Output voltage	VO	-0.5 to 18	V
	Supply voltage	VCC	-0.5 to 18	V
	Emitter-base voltage	VEB	0.5	V
	Output power dissipation (Note 6)	PO	100	mW
Storage temperature range		Tstg	-55 to 125	°C
Operating temperature range		Topr	-40 to 85	°C
Lead solder temperature (10 s) (Note 7)		Tsol	260	°C
Isolation voltage (Note 8)		BVs	2500	Vrms

Note: Using continuously under heavy loads (e.g. application of high temperature/current/voltage and a significant change in temperature, etc.) may cause this product to decrease in reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Derate 0.27 mA/°C above 50 °C.

Note 2: 50 % duty cycle, 1 ms pulse width.

Note 3: Pulse width ≤ 1 μs, 300 pps.

Note 4: Derate 0.47 mW/°C above 50 °C.

Note 5: Derate 0.6 mA/°C above 25 °C.

Note 6: Derate 1 mW/°C above 25 °C.

Note 7: Soldering is performed 2mm from the bottom of the package.

Note 8: AC, 60 s, R.H. ≤ 60 %

Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Supply voltage	VCC	—	—	16	V
Input current	IF	0.5	—	15	mA
Output current	IO	—	—	30	mA
Operating temperature	Topr	0	—	70	°C

Note: The recommended operating conditions are given as a design guideline to obtain expected performance of the device. In addition, each item is an independent guideline. In developing designs using this product, please confirm the specified characteristics shown in this document.

Electrical Characteristics (Unless otherwise specified Ta = 0 to 70°C)

Characteristics	Symbol	Test Conditions	Min	Typ*	Max	Unit
Forward voltage	V _F	I _F = 1.6 mA, Ta = 25 °C	—	1.55	1.7	V
Temperature coefficient of forward voltage	ΔV _F /ΔTa	I _F = 1.6 mA	—	-2.1	—	mV/°C
Input reverse current	I _R	V _R = 5 V, Ta = 25 °C	—	—	10	μA
Input capacitance	C _T	V _F = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
"H" level output current	I _{OH}	V _F = 0.8 V, V _O = V _{CC} = 18 V	—	0.1	100	μA
"H" level supply current	I _{CC} H	V _{CC} = 5 V, I _F = 0 mA V _O = Open	—	10	—	nA
"L" level supply current	I _{CC} L	V _{CC} = 5 V, I _F = 1.6 mA V _O = Open	—	0.3	—	mA
Current transfer ratio	I _O / I _F	I _F = 0.5 mA, V _O = 0.4 V V _{CC} = 4.5 V	400	1000	—	%
		I _F = 1.6 mA, V _O = 0.4 V V _{CC} = 4.5 V	500	900	—	
"L" level output voltage	V _{OL}	I _F = 1.6 mA, I _O = 6.4 mA V _{CC} = 4.5 V	—	0.1	0.4	V
		I _F = 5 mA, I _O = 15 mA V _{CC} = 4.5 V	—	0.1	0.4	
		I _F = 12 mA, I _O = 24 mA V _{CC} = 4.5 V	—	0.2	0.4	
Isolation resistance	R _S	V _S = 500 V, R.H. ≤ 60 % Ta = 25 °C (Note 9)	5×10 ¹⁰	10 ¹⁴	—	Ω
Input to output capacitance	C _S	V = 0 V, f = 1 MHz, Ta = 25 °C (Note 9)	—	0.6	—	pF

* : All typical values are at Ta = 25 °C.

Note 9: Device considered a 2-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Switching Characteristics (Ta = 25°C, Vcc = 5 V)

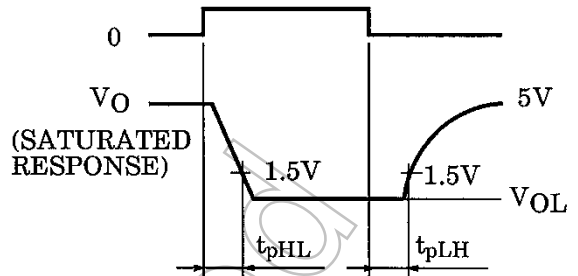
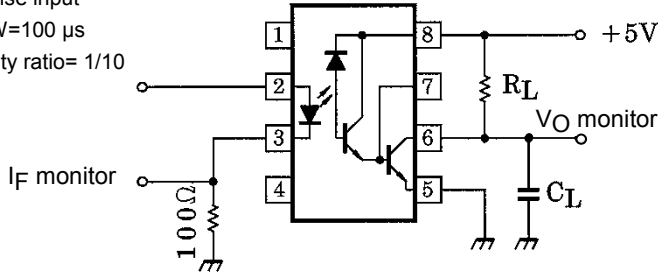
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ	Max	Unit
Propagation delay time (H→L)	t _{pHL}	1	I _F = 0.5 mA, R _L = 4.7 kΩ	—	2	25	μs
			I _F = 12 mA, R _L = 270 Ω	—	0.3	1	
Propagation delay time (L→H)	t _{pLH}		I _F = 1.6 mA, R _L = 2.2 kΩ	—	—	—	μs
			I _F = 0.5 mA, R _L = 4.7 kΩ	—	4	60	
			I _F = 12 mA, R _L = 270 Ω	—	1	7	
			I _F = 1.6 mA, R _L = 2.2 kΩ	—	—	—	
Common mode transient immunity at HIGH level output	CM _H	2	I _F = 0 mA, R _L = 2.2 kΩ (Note 10) V _{CM} = 400 V V _O (min) = 2 V	—	500	—	V/μs
Common mode transient immunity at LOW level output	CM _L		I _F = 1.6 mA, R _L = 2.2 kΩ (Note 11) V _{CM} = 400 V V _O (max) = 0.8 V	—	-500	—	V/μs

Note 10: CM_H: The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high output state (i.e., V_O > 2.0 V). Measured in volts per microsecond (V / μs).

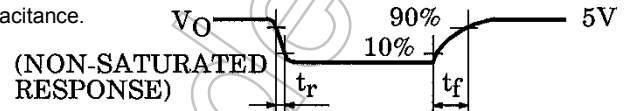
Note 11: CM_L: The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., V_O < 0.8 V). Measured in volts per microsecond (V / μs).

Test Circuit 1: t_{pHL} , t_{pLH} Test Circuit

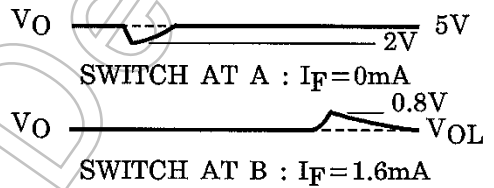
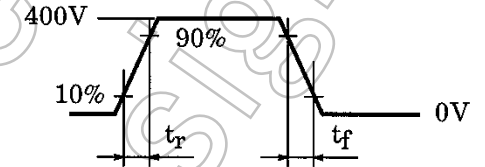
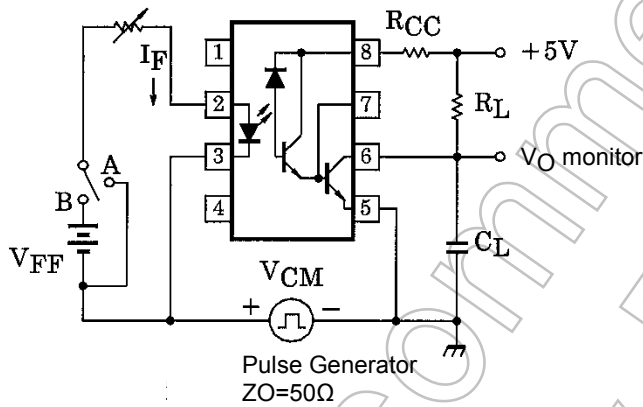
Pulse input
 PW=100 μ s
 Duty ratio= 1/10



C_L is approximately 15 pF which includes probe and stray wiring capacitance.

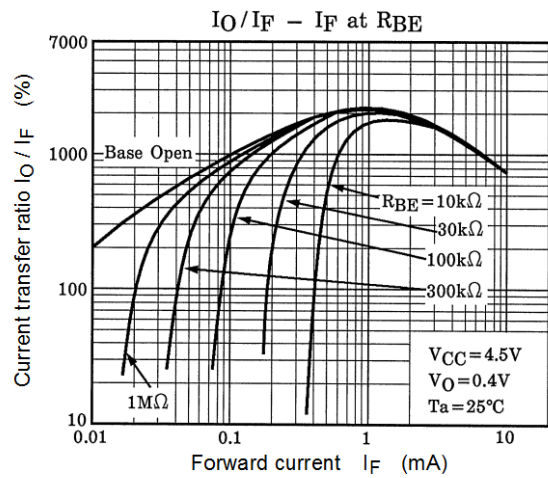
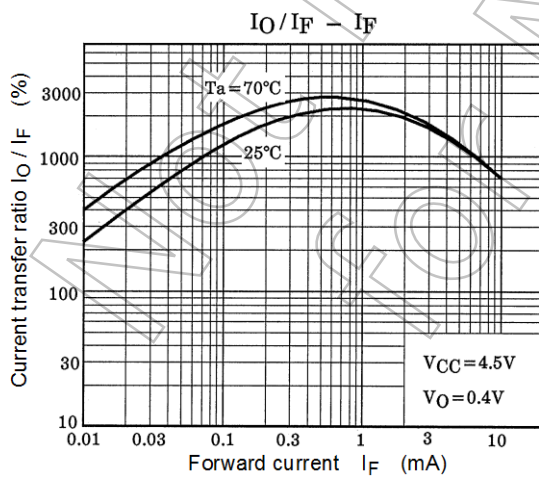
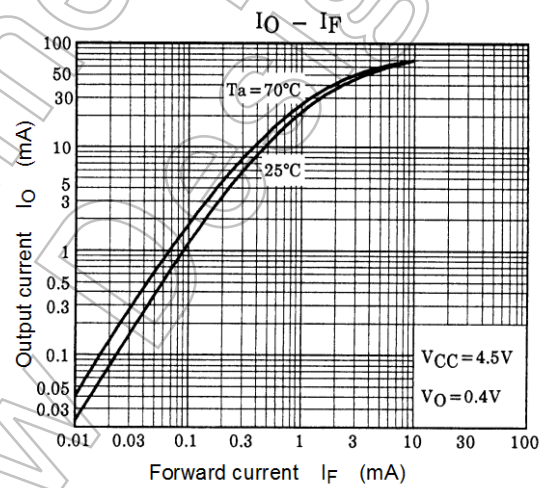
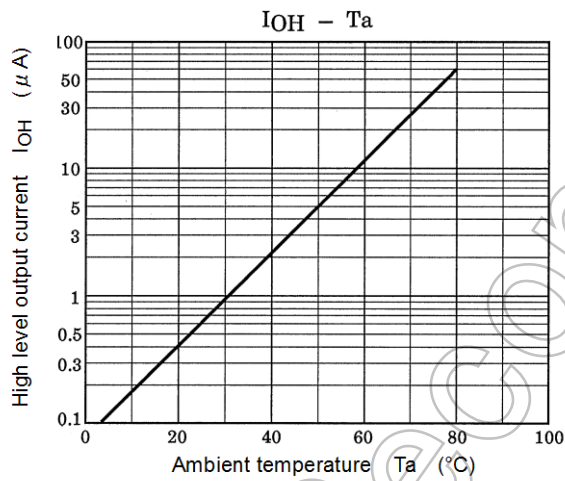
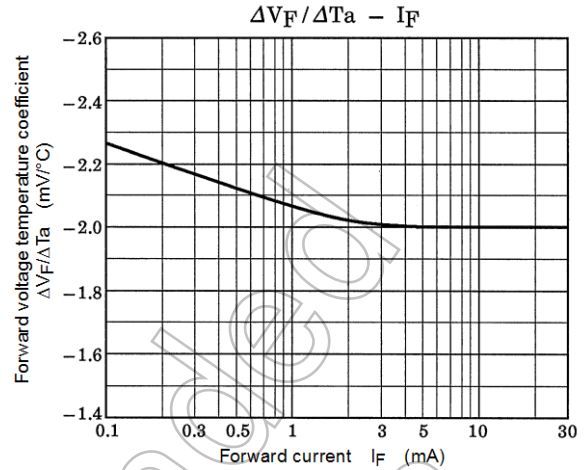
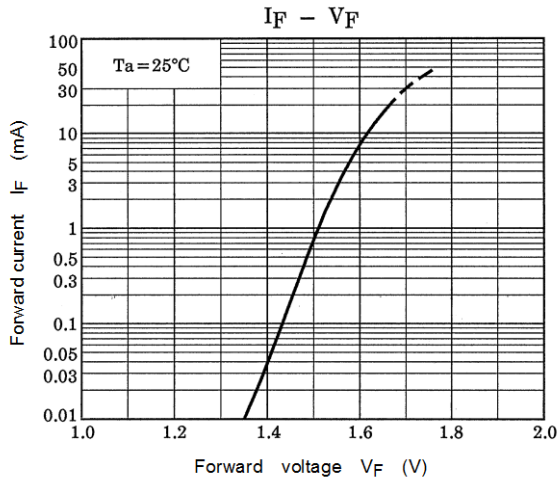


Test Circuit 2: Common Mode Noise Immunity Test Circuit

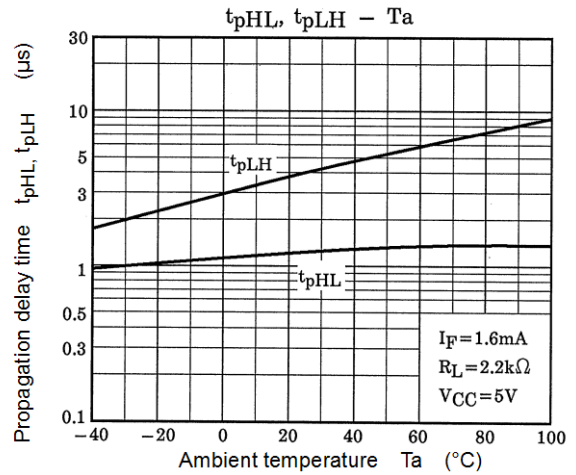
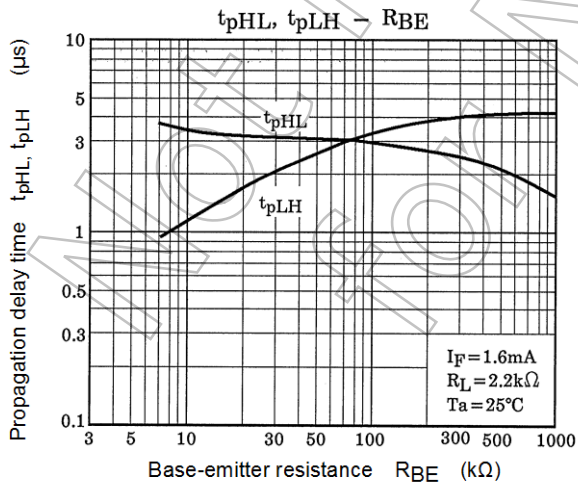
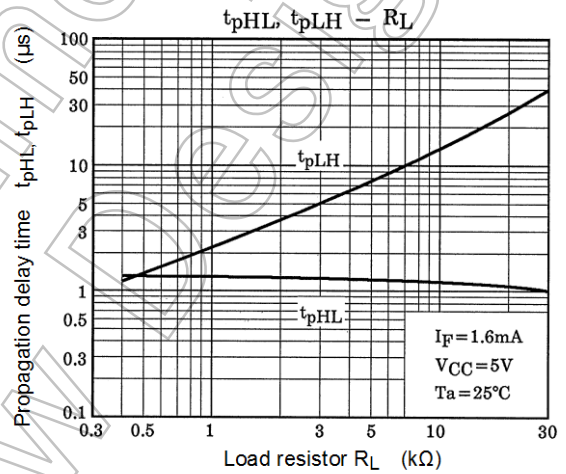
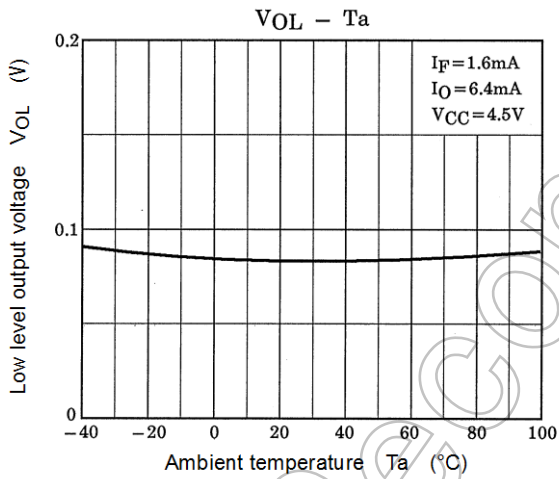
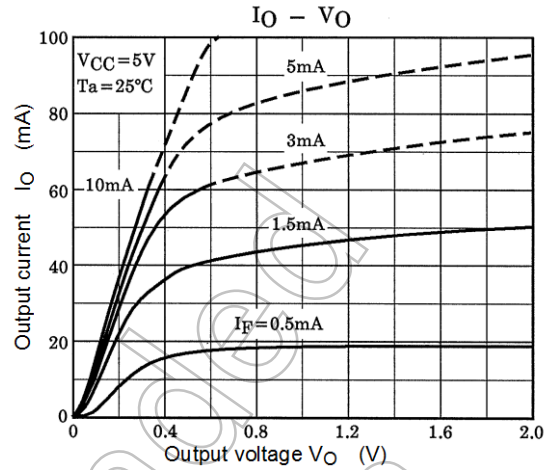
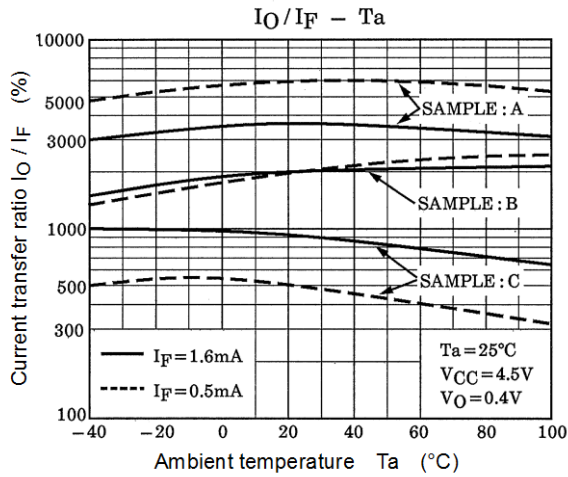


$$CM_H = \frac{320(V)}{t_r(\mu s)}, \quad CM_L = \frac{320(V)}{t_f(\mu s)}$$

C_L is approximately 15 pF which includes probe and stray wiring capacitance.



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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