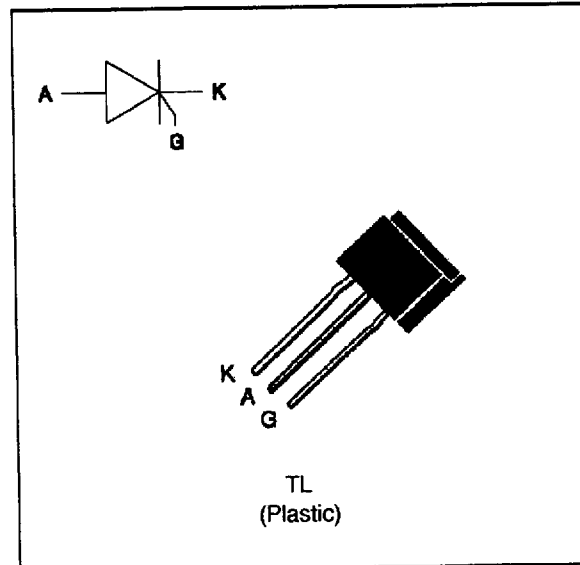


SENSITIVE GATE SCR
FEATURES

- LOW $I_{GT} \leq 200 \mu A$
- LOW $I_H \leq 5 mA$
- $I_T(RMS) = 4 A$

DESCRIPTION

The TLS 106 Silicon Controlled Rectifiers are high performance MESA diffused PNP devices glass passivated sensitive gate technology. These parts are intended to general purpose switching and phase control application.


ABSOLUTE RATINGS (limiting values)

Symbol	Parameter	Value	Unit	
$I_T(RMS)$	RMS on-state current (180° conduction angle)	$T_I = 25^\circ C$ 4	A	
$I_T(AV)$	Average on-state current (180° conduction angle, single phase circuit)	$T_I = 25^\circ C$ 2.5	A	
I_{TSM}	Non repetitive surge peak on-state current (T_J initial = 25°C)	$t_p = 8.3 ms$	37	A
		$t_p = 10 ms$	35	
i^2t	i^2t value	$t_p = 10 ms$ 6	A ² s	
di/dt	Critical rate of rise of on-state current Gate supply : $I_G = 10 mA$ $di_G/dt = 0.1 A/\mu s$	100	A/ μs	
T_{stg} T_J	Storage and operating junction temperature range	- 40 to + 150 - 40 to + 110	°C °C	
T_I	Maximum lead temperature for soldering during 4 s at 4.5 mm from case	230	°C	

Symbol	Parameter	TLS 106-					Unit
		05	1	2	4	6	
V_{DRM} V_{RRM}	Repetitive peak off-state voltage $T_J = 110^\circ C$ $R_{GK} = 1 K\Omega$	50	100	200	400	600	V

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
Rth (j-a)	Junction to ambient on printed circuit with Cu surface 1cm ²	50	°C/W
Rth (j-l) DC	Junction to leads for DC	15	°C/W

GATE CHARACTERISTICS (maximum values)

$P_G (AV) = 0.2W$ $P_{GM} = 3W$ ($t_p = 20 \mu s$) $I_{FGM} = 1.2A$ ($t_p = 20 \mu s$) $V_{RGM} = 5V$.

ELECTRICAL CHARACTERISTICS

Symbol	Test Conditions	Value	Unit
I _{GT}	V _D =12V (DC) R _L =140Ω T _J =25°C MAX	0.2	mA
V _{GT}	V _D =12V (DC) R _L =140Ω T _J =25°C MAX	1	V
V _{GD}	V _D =V _{DRM} R _L =3.3kΩ R _{GK} =1kΩ T _J =110°C MIN	0.1	V
t _{gt}	V _D =V _{DRM} I _G =10mA dI _G /dt=0.1A/μs T _J =25°C TYP	1.5	μs
I _L	I _G =1mA R _{GK} =1kΩ T _J =25°C MAX	7	mA
I _H	I _T =50mA R _{GK} =1kΩ T _J =25°C MAX	5	mA
V _{TM}	I _{TM} =4A t _p =380μs T _J =25°C MAX	1.9	V
I _{DRM} I _{RRM}	V _{DRM} Rated R _{GK} =1kΩ V _{RRM} Rated R _{GK} =1kΩ T _J =25°C MAX	0.01	mA
	T _J =110°C	0.3	
dV/dt	Linear slope up to V _D =67%V _{DRM} R _{GK} =1kΩ C _{GK} =0.1μF T _J =110°C MIN	10	V/μs
t _q	V _D =67%V _{DRM} I _{TM} =4A V _R =10V dI _{TM} /dt=10 A/μs dV _D /dt=2V/μs R _{GK} =1kΩ T _J =110°C TYP	100	μs

Fig.1 : Maximum average power dissipation versus average on-state current.

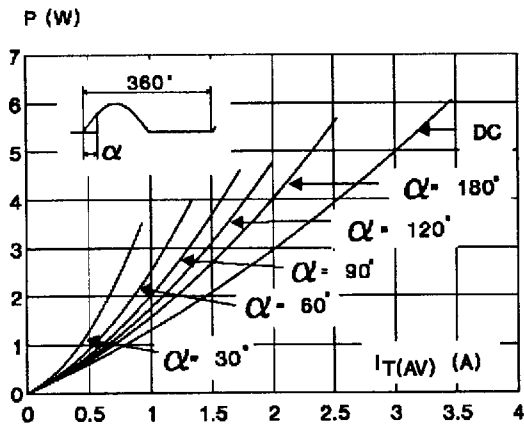


Fig.2 : Correlation between maximum average power dissipation and maximum allowable temperatures (Tamb and Tlead).

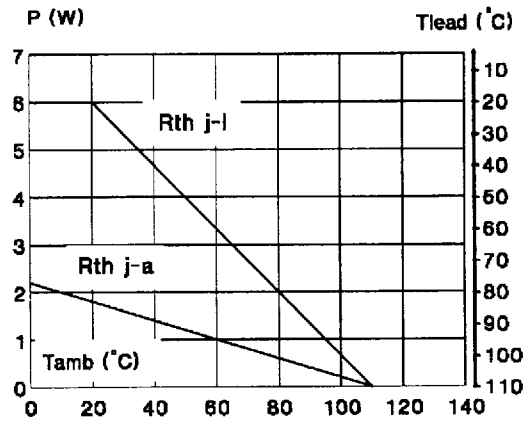


Fig.3 : Average on-state current versus leads temperature.

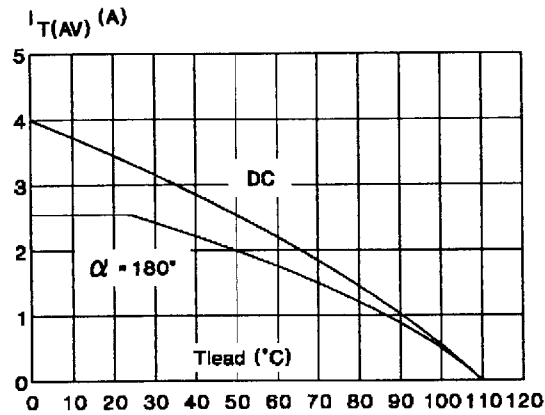


Fig.4 : Thermal transient impedance junction to ambient versus pulse duration.

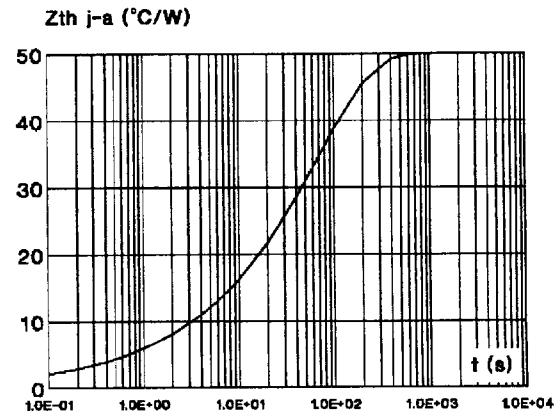


Fig.5 : Relative variation of gate trigger current versus junction temperature.

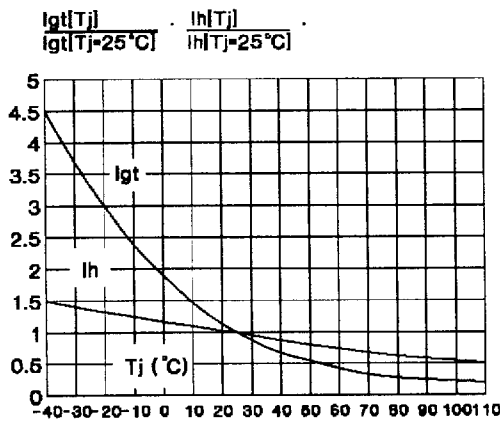
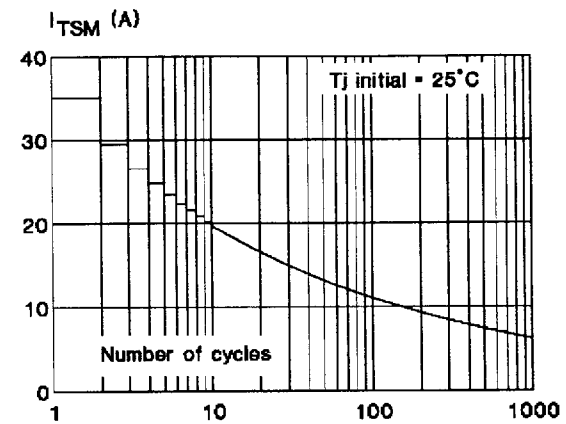


Fig.6 : Non repetitive surge peak on-state current versus number of cycles.



TLS 106

Fig.7 : Non repetitive surge peak on-state current for a sinusoidal pulse with width : $t \leq 10$ ms, and corresponding value of I^2t .

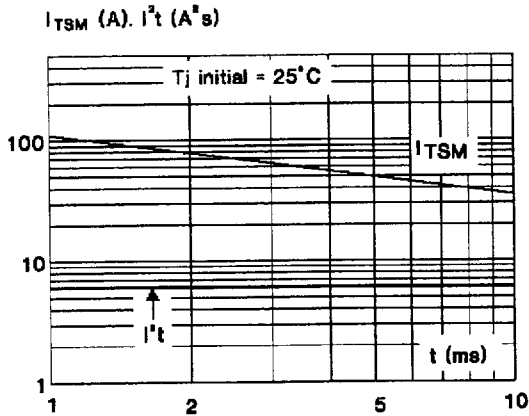
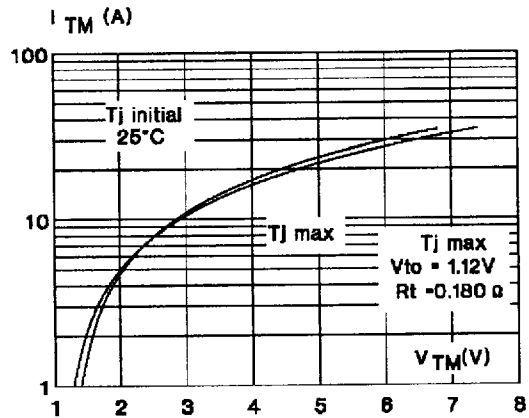
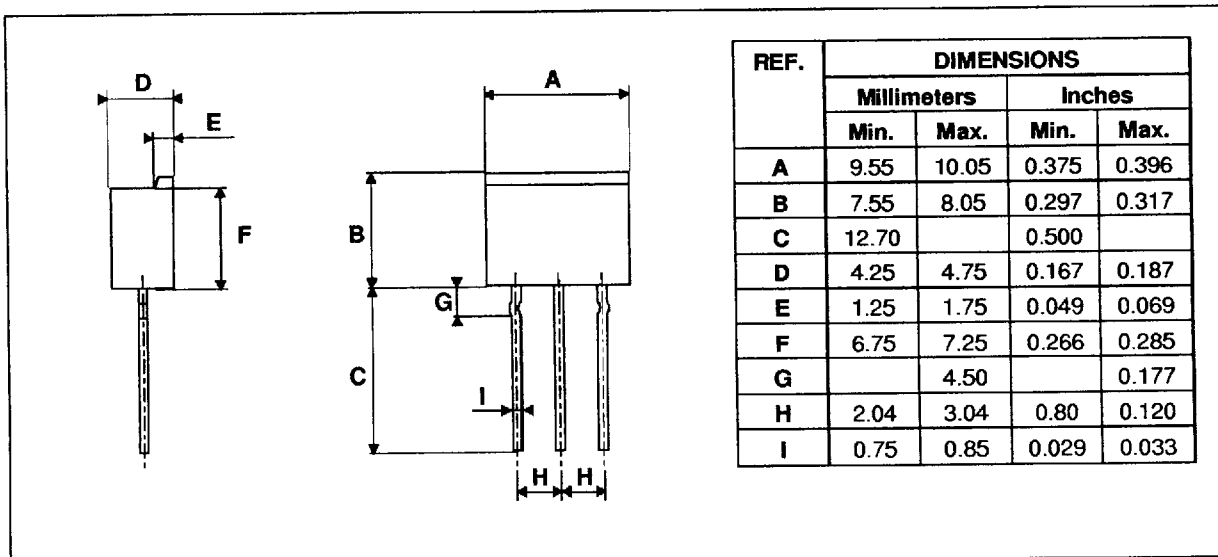


Fig.8 : On-state characteristics (maximum values).



PACKAGE MECHANICAL DATA

TL Plastic



Marking : type number
Weight : 0.8 g

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