Teralane Semiconductor
Product Data Sheet

TLS8103

132 RGB Segment x 132 Common Driver & Controller

For 65536 Colors STN LCD

Version 2.3
Jul., 2007

Precautions for light: Light has the effect of causing the electrons of semiconductor to move and may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB, COG, TCP and COF, etc) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip. Follow the precautions below when using this product:
1) During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
2) Test and inspect the product under an environment free of light source penetration.
3) Confirm that all surfaces around the IC will not be exposed to light source.

Contents

INTRODUCTION

TLS8103 is a low power single-chip CMOS Color STN LCD driver with integrated controller. It consists of 396 Segment and 132 Common driver circuits, which can drivers 132RGB x 132, 128RGB x 128 CSTN LCD panels.

TLS8103 integrates 132 x 132 x 16 bits Graphic Display Data RAM, On-Chip Oscillator, DC-DC Converter, and LCD driving voltage generation circuit to provide a low-cost solution. For being connected with microprocessors, TLS8103 supports four kinds of MCU interfaces: 8-bit 6800-series or 8080-series Parallel interface, 3-wires /4-wires Serial Peripheral Interface. TLS8103 adopts APT (Hi-Fas) and built-in capacitors architecture to achieve high-performance display by minimum power consumption and external components.

FEATURES

- **Display Resolution**: 132RGB x 132
- **On-chip Display Data SRAM**: 132 x 132 x 16 = 278,784 bits
- **Interface Color Modes**:
  - 256 colors RGB = (332) mode
  - 4096 colors RGB = (444) mode
  - Full colors 65K RGB = (565) mode
  - Truncated 262K colors (RGB) = (666) mode
  - Truncated 16M colors (RGB) = (888) mode
- **8 Colors Mode** for Display IDLE Power Saving
- **Microprocessor Interface**:
  - 8-bit 6800 Parallel interface
  - 8-bit 8080 Parallel interface
  - 3-wires Serial Interface
  - 4-wires Serial Interface
- **Special Display Modes**:
  - Area Scrolling
  - Partial windows moving
- **3 set (RGB) of CLUT** for 256 colors and 4096 colors map to 65K colors
- **3 set (RGB) of 128-steps Palettes** for panel gamma correction
- **On-chip Low Power Analog Circuit**:
  - Oscillator with internal resistors and capacitors
  - DC-DC Converter (x4, x5, x6, x7, x8) with internal booster capacitors
  - Extremely few external components: 4 capacitors
  - +/-64 steps electronic contrast control circuits
  - LCD driving voltage generation circuits
  - Programmable temperature compensation of VLCD and frame frequency
- **+/-128 Steps MTP** for LCD driving voltage calibration

- **Block Polarity Inversion** for low cross talk
- **Power Supply Voltage**:

VCC	= 2.5 ~ 3.3V (power supply for internal VDD regulator, whatever internal regulator close or open)
VDD	= 1.65 ~ 1.95V (external power supply for logic, when internal regulator close; internal regulator generate the power supply for logic, when internal regulator open)
VDDIO	= 1.65 ~ 3.3V (power for digital IO)
VCI	= 2.5 ~ 3.3V (power for analog)
VLCD	= max 18V (LCD driving voltage)

- **Package Type**: Application for COG

PAD ARRANGEMENT

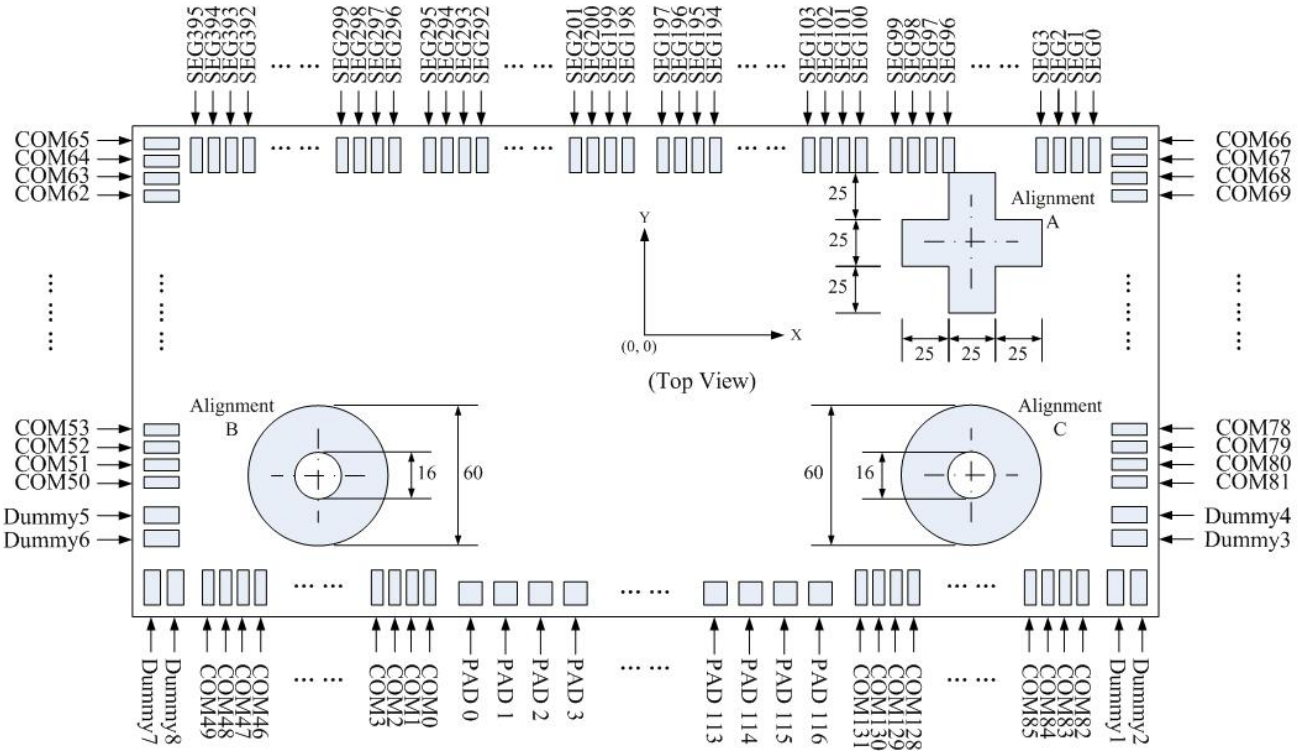

Figure 1 TLS8103 Pad arrangement diagram

Table 1 TLS8103 Pad bump size and alignment key coordinates

Item	Pad No.	Size(um)	
		X(um)	Y(um)
Die Size		11400	760
Die Thickness		400 (+/-25um)	
Pad Pitch	COM0~131, SEG0~395	26	
	PAD0-116	70	
	Dummy1~Dummy8	52	
Bumped Pad Size	COM49~COM0	13.5	115
	PAD0~PAD116	50	52
	COM131~COM82	13.5	115
	Dummy1, Dummy2	39	115
	Dummy3, Dummy4	115	39
	COM81~COM66	115	13.5
	SEG99~SEG0	13.5	115
	SEG197~SEG100	13.5	115
	SEG295~SEG198	13.5	115
	SEG395~SEG296	13.5	115
	COM65~COM50	115	13.5
	Dummy5, Dummy6	115	39
	Dummy7, Dummy8	39	115
Bump Height		15 (+/- 3um)	
Alignment Key		Coordinate	
		X	Y
	Alignment A	5007.43	173.80
	Alignment B	-5355.00	-115.70
	Alignment C	5355.00	-115.70

PAD CENTER COORDINATES

Table 2 TLS8103 Pad center coordinates

NUM	PADNAME	X	Y	LOCATION
1	dummy_pad7	-5621.000	-297.000	BOTTOM
2	dummy_pad8	-5569.000	-297.000	BOTTOM
3	COM_PAD<49>	-5530.000	-297.000	BOTTOM
4	COM_PAD<48>	-5504.000	-297.000	BOTTOM
5	COM_PAD<47>	-5478.000	-297.000	BOTTOM
6	COM_PAD<46>	-5452.000	-297.000	BOTTOM
7	COM_PAD<45>	-5426.000	-297.000	BOTTOM
8	COM_PAD<44>	-5400.000	-297.000	BOTTOM
9	COM_PAD<43>	-5374.000	-297.000	BOTTOM
10	COM_PAD<42>	-5348.000	-297.000	BOTTOM
11	COM_PAD<41>	-5322.000	-297.000	BOTTOM
12	COM_PAD<40>	-5296.000	-297.000	BOTTOM
13	COM_PAD<39>	-5270.000	-297.000	BOTTOM
14	COM_PAD<38>	-5244.000	-297.000	BOTTOM
15	COM_PAD<37>	-5218.000	-297.000	BOTTOM
16	COM_PAD<36>	-5192.000	-297.000	BOTTOM
17	COM_PAD<35>	-5166.000	-297.000	BOTTOM
18	COM_PAD<34>	-5140.000	-297.000	BOTTOM
19	COM_PAD<33>	-5114.000	-297.000	BOTTOM
20	COM_PAD<32>	-5088.000	-297.000	BOTTOM
21	COM_PAD<31>	-5062.000	-297.000	BOTTOM
22	COM_PAD<30>	-5036.000	-297.000	BOTTOM
23	COM_PAD<29>	-5010.000	-297.000	BOTTOM
24	COM_PAD<28>	-4984.000	-297.000	BOTTOM
25	COM_PAD<27>	-4958.000	-297.000	BOTTOM
26	COM_PAD<26>	-4932.000	-297.000	BOTTOM
27	COM_PAD<25>	-4906.000	-297.000	BOTTOM
28	COM_PAD<24>	-4880.000	-297.000	BOTTOM
29	COM_PAD<23>	-4854.000	-297.000	BOTTOM
30	COM_PAD<22>	-4828.000	-297.000	BOTTOM
31	COM_PAD<21>	-4802.000	-297.000	BOTTOM
32	COM_PAD<20>	-4776.000	-297.000	BOTTOM
33	COM_PAD<19>	-4750.000	-297.000	BOTTOM
34	COM_PAD<18>	-4724.000	-297.000	BOTTOM
35	COM_PAD<17>	-4698.000	-297.000	BOTTOM
36	COM_PAD<16>	-4672.000	-297.000	BOTTOM
37	COM_PAD<15>	-4646.000	-297.000	BOTTOM
38	COM_PAD<14>	-4620.000	-297.000	BOTTOM

39	COM_PAD<13>	-4594.000	-297.000	BOTTOM
40	COM_PAD<12>	-4568.000	-297.000	BOTTOM
41	COM_PAD<11>	-4542.000	-297.000	BOTTOM
42	COM_PAD<10>	-4516.000	-297.000	BOTTOM
43	COM_PAD<9>	-4490.000	-297.000	BOTTOM
44	COM_PAD<8>	-4464.000	-297.000	BOTTOM
45	COM_PAD<7>	-4438.000	-297.000	BOTTOM
46	COM_PAD<6>	-4412.000	-297.000	BOTTOM
47	COM_PAD<5>	-4386.000	-297.000	BOTTOM
48	COM_PAD<4>	-4360.000	-297.000	BOTTOM
49	COM_PAD<3>	-4334.000	-297.000	BOTTOM
50	COM_PAD<2>	-4308.000	-297.000	BOTTOM
51	COM_PAD<1>	-4282.000	-297.000	BOTTOM
52	COM_PAD<0>	-4256.000	-297.000	BOTTOM
53	GITOL	-4045.835	-327.800	BOTTOM
54	V0	-3975.835	-327.800	BOTTOM
55	V0	-3905.835	-327.800	BOTTOM
56	V0	-3835.835	-327.800	BOTTOM
57	V0	-3765.835	-327.800	BOTTOM
58	V0	-3695.835	-327.800	BOTTOM
59	V0	-3625.835	-327.800	BOTTOM
60	XV0	-3555.835	-327.800	BOTTOM
61	XV0	-3485.835	-327.800	BOTTOM
62	XV0	-3415.835	-327.800	BOTTOM
63	XV0	-3345.835	-327.800	BOTTOM
64	XV0	-3275.835	-327.800	BOTTOM
65	XV0	-3205.835	-327.800	BOTTOM
66	LCDVSS	-3135.835	-327.800	BOTTOM
67	LCDVSS	-3065.835	-327.800	BOTTOM
68	LCDVSS	-2995.835	-327.800	BOTTOM
69	LCDVSS	-2925.835	-327.800	BOTTOM
70	LCDVSS	-2855.835	-327.800	BOTTOM
71	LCDVSS	-2785.835	-327.800	BOTTOM
72	LCDVSS	-2715.835	-327.800	BOTTOM
73	LCDVSS	-2645.835	-327.800	BOTTOM
74	VSS	-2575.835	-327.800	BOTTOM
75	VSS	-2505.835	-327.800	BOTTOM
76	VSS	-2435.835	-327.800	BOTTOM
77	VSS	-2365.835	-327.800	BOTTOM
78	VSS	-2295.835	-327.800	BOTTOM
79	VSS	-2225.835	-327.800	BOTTOM
80	VSS	-2155.835	-327.800	BOTTOM
81	VSS	-2085.835	-327.800	BOTTOM
82	GND	-2015.835	-327.800	BOTTOM

83	GND	-1945.835	-327.800	BOTTOM
84	GND	-1875.835	-327.800	BOTTOM
85	GND	-1805.835	-327.800	BOTTOM
86	GND	-1735.835	-327.800	BOTTOM
87	GND	-1665.835	-327.800	BOTTOM
88	GND	-1595.835	-327.800	BOTTOM
89	GND	-1525.835	-327.800	BOTTOM
90	VDDIO	-1455.835	-327.800	BOTTOM
91	VDDIO	-1385.835	-327.800	BOTTOM
92	VDDIO	-1315.835	-327.800	BOTTOM
93	VDDIO	-1245.835	-327.800	BOTTOM
94	VDDIO	-1175.835	-327.800	BOTTOM
95	VDDIO	-1105.835	-327.800	BOTTOM
96	VDDIO	-1035.835	-327.800	BOTTOM
97	VDDIO	-965.835	-327.800	BOTTOM
98	VPP	-895.835	-327.800	BOTTOM
99	VPP	-825.835	-327.800	BOTTOM
100	VPP	-755.835	-327.800	BOTTOM
101	CL	-685.835	-327.800	BOTTOM
102	CLS	-615.835	-327.800	BOTTOM
103	VDDIO	-545.835	-327.800	BOTTOM
104	D_C	-475.835	-327.800	BOTTOM
105	RW_WR	-405.835	-327.800	BOTTOM
106	D<0>	-335.835	-327.800	BOTTOM
107	D<1>	-265.835	-327.800	BOTTOM
108	D<2>	-195.835	-327.800	BOTTOM
109	D<3>	-125.835	-327.800	BOTTOM
110	D<4>	-55.835	-327.800	BOTTOM
111	D<5>	14.165	-327.800	BOTTOM
112	D<6>	84.165	-327.800	BOTTOM
113	D<7>	154.165	-327.800	BOTTOM
114	GND	224.165	-327.800	BOTTOM
115	VDDIO	294.165	-327.800	BOTTOM
116	E_RD	364.165	-327.800	BOTTOM
117	RST	434.165	-327.800	BOTTOM
118	CSEL	504.165	-327.800	BOTTOM
119	PS<0>	574.165	-327.800	BOTTOM
120	PS<1>	644.165	-327.800	BOTTOM
121	PS<2>	714.165	-327.800	BOTTOM
122	GND	784.165	-327.800	BOTTOM
123	VDDIO	854.165	-327.800	BOTTOM
124	CS	924.165	-327.800	BOTTOM
125	TE	994.165	-327.800	BOTTOM
126	T1	1064.165	-327.800	BOTTOM

127	T2	1134.165	-327.800	BOTTOM
128	T3	1204.165	-327.800	BOTTOM
129	T4	1274.165	-327.800	BOTTOM
130	T5	1344.165	-327.800	BOTTOM
131	T6	1414.165	-327.800	BOTTOM
132	T7	1484.165	-327.800	BOTTOM
133	VDD	1554.165	-327.800	BOTTOM
134	VDD	1624.165	-327.800	BOTTOM
135	VDD	1694.165	-327.800	BOTTOM
136	VDD	1764.165	-327.800	BOTTOM
137	VDD	1834.165	-327.800	BOTTOM
138	VDD	1904.165	-327.800	BOTTOM
139	VDD	1974.165	-327.800	BOTTOM
140	VDD	2044.165	-327.800	BOTTOM
141	REG_OUT	2114.165	-327.800	BOTTOM
142	REG_OUT	2184.165	-327.800	BOTTOM
143	VCI	2254.165	-327.800	BOTTOM
144	VCI	2324.165	-327.800	BOTTOM
145	VCI	2394.165	-327.800	BOTTOM
146	VCI	2464.165	-327.800	BOTTOM
147	VCI	2534.165	-327.800	BOTTOM
148	VCI	2604.165	-327.800	BOTTOM
149	VCI	2674.165	-327.800	BOTTOM
150	VCI	2744.165	-327.800	BOTTOM
151	T8	2814.165	-327.800	BOTTOM
152	VCC	2884.165	-327.800	BOTTOM
153	VCC	2954.165	-327.800	BOTTOM
154	VCC	3024.165	-327.800	BOTTOM
155	VCC	3094.165	-327.800	BOTTOM
156	VCC	3164.165	-327.800	BOTTOM
157	VCC	3234.165	-327.800	BOTTOM
158	VDD_EN	3304.165	-327.800	BOTTOM
159	VM	3374.165	-327.800	BOTTOM
160	VM	3444.165	-327.800	BOTTOM
161	VM	3514.165	-327.800	BOTTOM
162	VM	3584.165	-327.800	BOTTOM
163	VG	3654.165	-327.800	BOTTOM
164	VG	3724.165	-327.800	BOTTOM
165	VG	3794.165	-327.800	BOTTOM
166	VG	3864.165	-327.800	BOTTOM
167	VG	3934.165	-327.800	BOTTOM
168	VG	4004.165	-327.800	BOTTOM
169	GITOR	4074.165	-327.800	BOTTOM
170	COM_PAD<131>	4256.000	-297.000	BOTTOM

171	COM_PAD<130>	4282.000	-297.000	BOTTOM
172	COM_PAD<129>	4308.000	-297.000	BOTTOM
173	COM_PAD<128>	4334.000	-297.000	BOTTOM
174	COM_PAD<127>	4360.000	-297.000	BOTTOM
175	COM_PAD<126>	4386.000	-297.000	BOTTOM
176	COM_PAD<125>	4412.000	-297.000	BOTTOM
177	COM_PAD<124>	4438.000	-297.000	BOTTOM
178	COM_PAD<123>	4464.000	-297.000	BOTTOM
179	COM_PAD<122>	4490.000	-297.000	BOTTOM
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182	COM_PAD<119>	4568.000	-297.000	BOTTOM
183	COM_PAD<118>	4594.000	-297.000	BOTTOM
184	COM_PAD<117>	4620.000	-297.000	BOTTOM
185	COM_PAD<116>	4646.000	-297.000	BOTTOM
186	COM_PAD<115>	4672.000	-297.000	BOTTOM
187	COM_PAD<114>	4698.000	-297.000	BOTTOM
188	COM_PAD<113>	4724.000	-297.000	BOTTOM
189	COM_PAD<112>	4750.000	-297.000	BOTTOM
190	COM_PAD<111>	4776.000	-297.000	BOTTOM
191	COM_PAD<110>	4802.000	-297.000	BOTTOM
192	COM_PAD<109>	4828.000	-297.000	BOTTOM
193	COM_PAD<108>	4854.000	-297.000	BOTTOM
194	COM_PAD<107>	4880.000	-297.000	BOTTOM
195	COM_PAD<106>	4906.000	-297.000	BOTTOM
196	COM_PAD<105>	4932.000	-297.000	BOTTOM
197	COM_PAD<104>	4958.000	-297.000	BOTTOM
198	COM_PAD<103>	4984.000	-297.000	BOTTOM
199	COM_PAD<102>	5010.000	-297.000	BOTTOM
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201	COM_PAD<100>	5062.000	-297.000	BOTTOM
202	COM_PAD<99>	5088.000	-297.000	BOTTOM
203	COM_PAD<98>	5114.000	-297.000	BOTTOM
204	COM_PAD<97>	5140.000	-297.000	BOTTOM
205	COM_PAD<96>	5166.000	-297.000	BOTTOM
206	COM_PAD<95>	5192.000	-297.000	BOTTOM
207	COM_PAD<94>	5218.000	-297.000	BOTTOM
208	COM_PAD<93>	5244.000	-297.000	BOTTOM
209	COM_PAD<92>	5270.000	-297.000	BOTTOM
210	COM_PAD<91>	5296.000	-297.000	BOTTOM
211	COM_PAD<90>	5322.000	-297.000	BOTTOM
212	COM_PAD<89>	5348.000	-297.000	BOTTOM
213	COM_PAD<88>	5374.000	-297.000	BOTTOM
214	COM_PAD<87>	5400.000	-297.000	BOTTOM

215	COM_PAD<86>	5426.000	-297.000	BOTTOM
216	COM_PAD<85>	5452.000	-297.000	BOTTOM
217	COM_PAD<84>	5478.000	-297.000	BOTTOM
218	COM_PAD<83>	5504.000	-297.000	BOTTOM
219	COM_PAD<82>	5530.000	-297.000	BOTTOM
220	dummy_pad1	5569.000	-297.000	BOTTOM
221	dummy_pad2	5621.000	-297.000	BOTTOM
222	dummy_pad3	5616.000	-147.600	RIGHT
223	dummy_pad4	5616.000	-95.600	RIGHT
224	COM_PAD<81>	5616.000	-56.600	RIGHT
225	COM_PAD<80>	5616.000	-30.600	RIGHT
226	COM_PAD<79>	5616.000	-4.600	RIGHT
227	COM_PAD<78>	5616.000	21.400	RIGHT
228	COM_PAD<77>	5616.000	47.400	RIGHT
229	COM_PAD<76>	5616.000	73.400	RIGHT
230	COM_PAD<75>	5616.000	99.400	RIGHT
231	COM_PAD<74>	5616.000	125.400	RIGHT
232	COM_PAD<73>	5616.000	151.400	RIGHT
233	COM_PAD<72>	5616.000	177.400	RIGHT
234	COM_PAD<71>	5616.000	203.400	RIGHT
235	COM_PAD<70>	5616.000	229.400	RIGHT
236	COM_PAD<69>	5616.000	255.400	RIGHT
237	COM_PAD<68>	5616.000	281.400	RIGHT
238	COM_PAD<67>	5616.000	307.400	RIGHT
239	COM_PAD<66>	5616.000	333.400	RIGHT
240	SEG_PAD<0>	5291.000	296.800	TOP
241	SEG_PAD<1>	5265.000	296.800	TOP
242	SEG_PAD<2>	5239.000	296.800	TOP
243	SEG_PAD<3>	5213.000	296.800	TOP
244	SEG_PAD<4>	5187.000	296.800	TOP
245	SEG_PAD<5>	5161.000	296.800	TOP
246	SEG_PAD<6>	5135.000	296.800	TOP
247	SEG_PAD<7>	5109.000	296.800	TOP
248	SEG_PAD<8>	5083.000	296.800	TOP
249	SEG_PAD<9>	5057.000	296.800	TOP
250	SEG_PAD<10>	5031.000	296.800	TOP
251	SEG_PAD<11>	5005.000	296.800	TOP
252	SEG_PAD<12>	4979.000	296.800	TOP
253	SEG_PAD<13>	4953.000	296.800	TOP
254	SEG_PAD<14>	4927.000	296.800	TOP
255	SEG_PAD<15>	4901.000	296.800	TOP
256	SEG_PAD<16>	4875.000	296.800	TOP
257	SEG_PAD<17>	4849.000	296.800	TOP
258	SEG_PAD<18>	4823.000	296.800	TOP

259	SEG_PAD<19>	4797.000	296.800	TOP
260	SEG_PAD<20>	4771.000	296.800	TOP
261	SEG_PAD<21>	4745.000	296.800	TOP
262	SEG_PAD<22>	4719.000	296.800	TOP
263	SEG_PAD<23>	4693.000	296.800	TOP
264	SEG_PAD<24>	4667.000	296.800	TOP
265	SEG_PAD<25>	4641.000	296.800	TOP
266	SEG_PAD<26>	4615.000	296.800	TOP
267	SEG_PAD<27>	4589.000	296.800	TOP
268	SEG_PAD<28>	4563.000	296.800	TOP
269	SEG_PAD<29>	4537.000	296.800	TOP
270	SEG_PAD<30>	4511.000	296.800	TOP
271	SEG_PAD<31>	4485.000	296.800	TOP
272	SEG_PAD<32>	4459.000	296.800	TOP
273	SEG_PAD<33>	4433.000	296.800	TOP
274	SEG_PAD<34>	4407.000	296.800	TOP
275	SEG_PAD<35>	4381.000	296.800	TOP
276	SEG_PAD<36>	4355.000	296.800	TOP
277	SEG_PAD<37>	4329.000	296.800	TOP
278	SEG_PAD<38>	4303.000	296.800	TOP
279	SEG_PAD<39>	4277.000	296.800	TOP
280	SEG_PAD<40>	4251.000	296.800	TOP
281	SEG_PAD<41>	4225.000	296.800	TOP
282	SEG_PAD<42>	4199.000	296.800	TOP
283	SEG_PAD<43>	4173.000	296.800	TOP
284	SEG_PAD<44>	4147.000	296.800	TOP
285	SEG_PAD<45>	4121.000	296.800	TOP
286	SEG_PAD<46>	4095.000	296.800	TOP
287	SEG_PAD<47>	4069.000	296.800	TOP
288	SEG_PAD<48>	4043.000	296.800	TOP
289	SEG_PAD<49>	4017.000	296.800	TOP
290	SEG_PAD<50>	3991.000	296.800	TOP
291	SEG_PAD<51>	3965.000	296.800	TOP
292	SEG_PAD<52>	3939.000	296.800	TOP
293	SEG_PAD<53>	3913.000	296.800	TOP
294	SEG_PAD<54>	3887.000	296.800	TOP
295	SEG_PAD<55>	3861.000	296.800	TOP
296	SEG_PAD<56>	3835.000	296.800	TOP
297	SEG_PAD<57>	3809.000	296.800	TOP
298	SEG_PAD<58>	3783.000	296.800	TOP
299	SEG_PAD<59>	3757.000	296.800	TOP
300	SEG_PAD<60>	3731.000	296.800	TOP
301	SEG_PAD<61>	3705.000	296.800	TOP
302	SEG_PAD<62>	3679.000	296.800	TOP

303	SEG_PAD<63>	3653.000	296.800	TOP
304	SEG_PAD<64>	3627.000	296.800	TOP
305	SEG_PAD<65>	3601.000	296.800	TOP
306	SEG_PAD<66>	3575.000	296.800	TOP
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316	SEG_PAD<76>	3315.000	296.800	TOP
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333	SEG_PAD<93>	2873.000	296.800	TOP
334	SEG_PAD<94>	2847.000	296.800	TOP
335	SEG_PAD<95>	2821.000	296.800	TOP
336	SEG_PAD<96>	2795.000	296.800	TOP
337	SEG_PAD<97>	2769.000	296.800	TOP
338	SEG_PAD<98>	2743.000	296.800	TOP
339	SEG_PAD<99>	2717.000	296.800	TOP
340	SEG_PAD<100>	2587.000	296.800	TOP
341	SEG_PAD<101>	2561.000	296.800	TOP
342	SEG_PAD<102>	2535.000	296.800	TOP
343	SEG_PAD<103>	2509.000	296.800	TOP
344	SEG_PAD<104>	2483.000	296.800	TOP
345	SEG_PAD<105>	2457.000	296.800	TOP
346	SEG_PAD<106>	2431.000	296.800	TOP

347	SEG_PAD<107>	2405.000	296.800	TOP
348	SEG_PAD<108>	2379.000	296.800	TOP
349	SEG_PAD<109>	2353.000	296.800	TOP
350	SEG_PAD<110>	2327.000	296.800	TOP
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352	SEG_PAD<112>	2275.000	296.800	TOP
353	SEG_PAD<113>	2249.000	296.800	TOP
354	SEG_PAD<114>	2223.000	296.800	TOP
355	SEG_PAD<115>	2197.000	296.800	TOP
356	SEG_PAD<116>	2171.000	296.800	TOP
357	SEG_PAD<117>	2145.000	296.800	TOP
358	SEG_PAD<118>	2119.000	296.800	TOP
359	SEG_PAD<119>	2093.000	296.800	TOP
360	SEG_PAD<120>	2067.000	296.800	TOP
361	SEG_PAD<121>	2041.000	296.800	TOP
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369	SEG_PAD<129>	1833.000	296.800	TOP
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372	SEG_PAD<132>	1755.000	296.800	TOP
373	SEG_PAD<133>	1729.000	296.800	TOP
374	SEG_PAD<134>	1703.000	296.800	TOP
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385	SEG_PAD<145>	1417.000	296.800	TOP
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387	SEG_PAD<147>	1365.000	296.800	TOP
388	SEG_PAD<148>	1339.000	296.800	TOP
389	SEG_PAD<149>	1313.000	296.800	TOP
390	SEG_PAD<150>	1287.000	296.800	TOP

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393	SEG_PAD<153>	1209.000	296.800	TOP
394	SEG_PAD<154>	1183.000	296.800	TOP
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406	SEG_PAD<166>	871.000	296.800	TOP
407	SEG_PAD<167>	845.000	296.800	TOP
408	SEG_PAD<168>	819.000	296.800	TOP
409	SEG_PAD<169>	793.000	296.800	TOP
410	SEG_PAD<170>	767.000	296.800	TOP
411	SEG_PAD<171>	741.000	296.800	TOP
412	SEG_PAD<172>	715.000	296.800	TOP
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422	SEG_PAD<182>	455.000	296.800	TOP
423	SEG_PAD<183>	429.000	296.800	TOP
424	SEG_PAD<184>	403.000	296.800	TOP
425	SEG_PAD<185>	377.000	296.800	TOP
426	SEG_PAD<186>	351.000	296.800	TOP
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428	SEG_PAD<188>	299.000	296.800	TOP
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431	SEG_PAD<191>	221.000	296.800	TOP
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446	SEG_PAD<206>	-273.000	296.800	TOP
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455	SEG_PAD<215>	-507.000	296.800	TOP
456	SEG_PAD<216>	-533.000	296.800	TOP
457	SEG_PAD<217>	-559.000	296.800	TOP
458	SEG_PAD<218>	-585.000	296.800	TOP
459	SEG_PAD<219>	-611.000	296.800	TOP
460	SEG_PAD<220>	-637.000	296.800	TOP
461	SEG_PAD<221>	-663.000	296.800	TOP
462	SEG_PAD<222>	-689.000	296.800	TOP
463	SEG_PAD<223>	-715.000	296.800	TOP
464	SEG_PAD<224>	-741.000	296.800	TOP
465	SEG_PAD<225>	-767.000	296.800	TOP
466	SEG_PAD<226>	-793.000	296.800	TOP
467	SEG_PAD<227>	-819.000	296.800	TOP
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473	SEG_PAD<233>	-975.000	296.800	TOP
474	SEG_PAD<234>	-1001.000	296.800	TOP
475	SEG_PAD<235>	-1027.000	296.800	TOP
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477	SEG_PAD<237>	-1079.000	296.800	TOP
478	SEG_PAD<238>	-1105.000	296.800	TOP

479	SEG_PAD<239>	-1131.000	296.800	TOP
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481	SEG_PAD<241>	-1183.000	296.800	TOP
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495	SEG_PAD<255>	-1547.000	296.800	TOP
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507	SEG_PAD<267>	-1859.000	296.800	TOP
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511	SEG_PAD<271>	-1963.000	296.800	TOP
512	SEG_PAD<272>	-1989.000	296.800	TOP
513	SEG_PAD<273>	-2015.000	296.800	TOP
514	SEG_PAD<274>	-2041.000	296.800	TOP
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516	SEG_PAD<276>	-2093.000	296.800	TOP
517	SEG_PAD<277>	-2119.000	296.800	TOP
518	SEG_PAD<278>	-2145.000	296.800	TOP
519	SEG_PAD<279>	-2171.000	296.800	TOP
520	SEG_PAD<280>	-2197.000	296.800	TOP
521	SEG_PAD<281>	-2223.000	296.800	TOP
522	SEG_PAD<282>	-2249.000	296.800	TOP

523	SEG_PAD<283>	-2275.000	296.800	TOP
524	SEG_PAD<284>	-2301.000	296.800	TOP
525	SEG_PAD<285>	-2327.000	296.800	TOP
526	SEG_PAD<286>	-2353.000	296.800	TOP
527	SEG_PAD<287>	-2379.000	296.800	TOP
528	SEG_PAD<288>	-2405.000	296.800	TOP
529	SEG_PAD<289>	-2431.000	296.800	TOP
530	SEG_PAD<290>	-2457.000	296.800	TOP
531	SEG_PAD<291>	-2483.000	296.800	TOP
532	SEG_PAD<292>	-2509.000	296.800	TOP
533	SEG_PAD<293>	-2535.000	296.800	TOP
534	SEG_PAD<294>	-2561.000	296.800	TOP
535	SEG_PAD<295>	-2587.000	296.800	TOP
536	SEG_PAD<296>	-2717.000	296.800	TOP
537	SEG_PAD<297>	-2743.000	296.800	TOP
538	SEG_PAD<298>	-2769.000	296.800	TOP
539	SEG_PAD<299>	-2795.000	296.800	TOP
540	SEG_PAD<300>	-2821.000	296.800	TOP
541	SEG_PAD<301>	-2847.000	296.800	TOP
542	SEG_PAD<302>	-2873.000	296.800	TOP
543	SEG_PAD<303>	-2899.000	296.800	TOP
544	SEG_PAD<304>	-2925.000	296.800	TOP
545	SEG_PAD<305>	-2951.000	296.800	TOP
546	SEG_PAD<306>	-2977.000	296.800	TOP
547	SEG_PAD<307>	-3003.000	296.800	TOP
548	SEG_PAD<308>	-3029.000	296.800	TOP
549	SEG_PAD<309>	-3055.000	296.800	TOP
550	SEG_PAD<310>	-3081.000	296.800	TOP
551	SEG_PAD<311>	-3107.000	296.800	TOP
552	SEG_PAD<312>	-3133.000	296.800	TOP
553	SEG_PAD<313>	-3159.000	296.800	TOP
554	SEG_PAD<314>	-3185.000	296.800	TOP
555	SEG_PAD<315>	-3211.000	296.800	TOP
556	SEG_PAD<316>	-3237.000	296.800	TOP
557	SEG_PAD<317>	-3263.000	296.800	TOP
558	SEG_PAD<318>	-3289.000	296.800	TOP
559	SEG_PAD<319>	-3315.000	296.800	TOP
560	SEG_PAD<320>	-3341.000	296.800	TOP
561	SEG_PAD<321>	-3367.000	296.800	TOP
562	SEG_PAD<322>	-3393.000	296.800	TOP
563	SEG_PAD<323>	-3419.000	296.800	TOP
564	SEG_PAD<324>	-3445.000	296.800	TOP
565	SEG_PAD<325>	-3471.000	296.800	TOP
566	SEG_PAD<326>	-3497.000	296.800	TOP

567	SEG_PAD<327>	-3523.000	296.800	TOP
568	SEG_PAD<328>	-3549.000	296.800	TOP
569	SEG_PAD<329>	-3575.000	296.800	TOP
570	SEG_PAD<330>	-3601.000	296.800	TOP
571	SEG_PAD<331>	-3627.000	296.800	TOP
572	SEG_PAD<332>	-3653.000	296.800	TOP
573	SEG_PAD<333>	-3679.000	296.800	TOP
574	SEG_PAD<334>	-3705.000	296.800	TOP
575	SEG_PAD<335>	-3731.000	296.800	TOP
576	SEG_PAD<336>	-3757.000	296.800	TOP
577	SEG_PAD<337>	-3783.000	296.800	TOP
578	SEG_PAD<338>	-3809.000	296.800	TOP
579	SEG_PAD<339>	-3835.000	296.800	TOP
580	SEG_PAD<340>	-3861.000	296.800	TOP
581	SEG_PAD<341>	-3887.000	296.800	TOP
582	SEG_PAD<342>	-3913.000	296.800	TOP
583	SEG_PAD<343>	-3939.000	296.800	TOP
584	SEG_PAD<344>	-3965.000	296.800	TOP
585	SEG_PAD<345>	-3991.000	296.800	TOP
586	SEG_PAD<346>	-4017.000	296.800	TOP
587	SEG_PAD<347>	-4043.000	296.800	TOP
588	SEG_PAD<348>	-4069.000	296.800	TOP
589	SEG_PAD<349>	-4095.000	296.800	TOP
590	SEG_PAD<350>	-4121.000	296.800	TOP
591	SEG_PAD<351>	-4147.000	296.800	TOP
592	SEG_PAD<352>	-4173.000	296.800	TOP
593	SEG_PAD<353>	-4199.000	296.800	TOP
594	SEG_PAD<354>	-4225.000	296.800	TOP
595	SEG_PAD<355>	-4251.000	296.800	TOP
596	SEG_PAD<356>	-4277.000	296.800	TOP
597	SEG_PAD<357>	-4303.000	296.800	TOP
598	SEG_PAD<358>	-4329.000	296.800	TOP
599	SEG_PAD<359>	-4355.000	296.800	TOP
600	SEG_PAD<360>	-4381.000	296.800	TOP
601	SEG_PAD<361>	-4407.000	296.800	TOP
602	SEG_PAD<362>	-4433.000	296.800	TOP
603	SEG_PAD<363>	-4459.000	296.800	TOP
604	SEG_PAD<364>	-4485.000	296.800	TOP
605	SEG_PAD<365>	-4511.000	296.800	TOP
606	SEG_PAD<366>	-4537.000	296.800	TOP
607	SEG_PAD<367>	-4563.000	296.800	TOP
608	SEG_PAD<368>	-4589.000	296.800	TOP
609	SEG_PAD<369>	-4615.000	296.800	TOP
610	SEG_PAD<370>	-4641.000	296.800	TOP

611	SEG_PAD<371>	-4667.000	296.800	TOP
612	SEG_PAD<372>	-4693.000	296.800	TOP
613	SEG_PAD<373>	-4719.000	296.800	TOP
614	SEG_PAD<374>	-4745.000	296.800	TOP
615	SEG_PAD<375>	-4771.000	296.800	TOP
616	SEG_PAD<376>	-4797.000	296.800	TOP
617	SEG_PAD<377>	-4823.000	296.800	TOP
618	SEG_PAD<378>	-4849.000	296.800	TOP
619	SEG_PAD<379>	-4875.000	296.800	TOP
620	SEG_PAD<380>	-4901.000	296.800	TOP
621	SEG_PAD<381>	-4927.000	296.800	TOP
622	SEG_PAD<382>	-4953.000	296.800	TOP
623	SEG_PAD<383>	-4979.000	296.800	TOP
624	SEG_PAD<384>	-5005.000	296.800	TOP
625	SEG_PAD<385>	-5031.000	296.800	TOP
626	SEG_PAD<386>	-5057.000	296.800	TOP
627	SEG_PAD<387>	-5083.000	296.800	TOP
628	SEG_PAD<388>	-5109.000	296.800	TOP
629	SEG_PAD<389>	-5135.000	296.800	TOP
630	SEG_PAD<390>	-5161.000	296.800	TOP
631	SEG_PAD<391>	-5187.000	296.800	TOP
632	SEG_PAD<392>	-5213.000	296.800	TOP
633	SEG_PAD<393>	-5239.000	296.800	TOP
634	SEG_PAD<394>	-5265.000	296.800	TOP
635	SEG_PAD<395>	-5291.000	296.800	TOP
636	COM_PAD<65>	-5616.000	333.400	LEFT
637	COM_PAD<64>	-5616.000	307.400	LEFT
638	COM_PAD<63>	-5616.000	281.400	LEFT
639	COM_PAD<62>	-5616.000	255.400	LEFT
640	COM_PAD<61>	-5616.000	229.400	LEFT
641	COM_PAD<60>	-5616.000	203.400	LEFT
642	COM_PAD<59>	-5616.000	177.400	LEFT
643	COM_PAD<58>	-5616.000	151.400	LEFT
644	COM_PAD<57>	-5616.000	125.400	LEFT
645	COM_PAD<56>	-5616.000	99.400	LEFT
646	COM_PAD<55>	-5616.000	73.400	LEFT
647	COM_PAD<54>	-5616.000	47.400	LEFT
648	COM_PAD<53>	-5616.000	21.400	LEFT
649	COM_PAD<52>	-5616.000	-4.600	LEFT
650	COM_PAD<51>	-5616.000	-30.600	LEFT
651	COM_PAD<50>	-5616.000	-56.600	LEFT
652	dummy_pad5	-5616.000	-95.600	LEFT
653	dummy_pad6	-5616.000	-147.600	LEFT

PIN DESCRIPTION

Table3 TLS8103 PIN function description table

Name	I/O	Description	No. of Pins
Power Supply Pins			
VCC	Power Supply	Power supply for internal logic power regulator. When use internal logic power regulator, VCC can be connected to 2.5V~3.3V; When use external logic power supply, VCC must be connected with a voltage supply > VDD. For a typical connection, when use internal logic power regulator, VCC can be connected together with VCI, and REG_OUT, VDD, are connected together; when use external logic power supply, VCC can be connected together with VCI.	
VDDIO	Power Supply	Power supply for digital I/O circuits. VDD<=VDDIO<=3.3V	
VDD	Power Supply	Power supply for digital logic and SRAM. It must be connected with a voltage supply 1.65V<VDD<1.95V	
VCI	Power Supply	Power supply for analog circuit.	
REG_OUT	Power Supply	Internal power Regulator output, when pin VDD_EN=H, REG_OUT output a 1.65V~1.95V voltage for VDD supply, please connect REG_OUT with an external capacitor for VDD supply stability; when pin VDD_EN=L, REG_OUT is high impedance, please leave REG_OUT floating.	
VDD_EN	I	When VDD_EN=H, internal power regulator is enabled and its status is controlled by internal register; when VDD_EN=L, internal power regulator is disabled, please provide external power supply for VDD.	
GND	Power Supply	Ground for digital logic, SRAM and internal power regulator circuit	
VSS	Power Supply	Ground for internal analog circuits.	
LCDVSS	Power Supply	Ground for internal LCD COM/SEG driving circuits.	
V0, XV0, Vm	Power Supply	Power supply pins for LCD COM driving circuits. V0 is the most positive voltage in TLS8103, and XV0 is the most negative voltage in TLS8103.	

		When the internal power circuit is active, the three voltage are generated as V0-Vm = Vm-XV0, and Vm = (1/N) x V0. N is the LCD bias. Please connect a capacitor between V0 and XV0 for their driving stability, and connect a capacitor between Vm and system ground for Vm driving stability.	
Vg	Power Supply	Power supply for LCD SEG driving circuit. When the internal power circuit is active, the Vg voltage are generated as Vg = 2 * Vm. Please connect a capacitor between Vg and system ground for Vg driving stability.	
VPP	Power Supply	MTP programming voltage supply. Left this pin open when normal function.	
MPU Interface I/O Pins			
D/C (SCK)	I	This pin is used to indicate that whether the data bus is data or command when parallel interface. D/C = "H": D7 – D0 are data. D/C = "L": D7 – D0 are command. It is also used as Serial Clock (SCK) when serial interface.	1
/RES	I	This is the reset pin. When this pin is set to "L", the system registers are set to the initialized status. Refer to the descriptions of Reset Circuits.	1
/CS	I	These are the chip select pins. The chip is set to active when /CS= "L".	1
E (/RD)	I	This pin is the enable indicator (6800 interface mode) or the read operation indicator (8080 interface mode). **For 6800 series interface applications:** This is the E pin. Setting E = "H" indicates a write/read operation. **For 8080 series interface applications:** This is the /RD pin. Setting /RD = "L" indicates the read operation and the data bus can be read by MPU. When using serial interface, this pin should be fixed to "H" or "L".	1

<table>
<tr><td>R/W
(/WR)</td><td>I</td><td>This pin is the read/write indicator (6800 interface mode) or write operation indicator (8080 interface mode).
For 6800 series interface applications:
This is the R/W pin. Setting R/W = “H” indicates a read operation (MPU can read data from the data bus) while setting R/W = “L” indicates the write.
For 8080 series interface applications:
This is the /WR pin. Setting /WR = “L” indicates the write operation.
When use serial interface, this pin should be fixed to “H” or “L”.</td><td>1</td></tr>
<tr><td>D7,
D6,
D5,
D4,
D3,
D2,
D1,
D0</td><td>I/O</td><td>When parallel interface, D7-D0 are the data bus for write and read operation; when serial interface, D0 and D1 are used as Serial Data bus and D/C Control Signals.
1. In serial interface, D0 is used as SDA, the serial data bus signal.
2. In 4-lines serial interface, D1 is used as command/data indicator signal (D/C).
3. In serial interface, the unused pins of D7-D0 are in state of high impedance, should be connected with “H” or “L” or be floating.</td><td>8</td></tr>
<tr><td colspan="4">Configuration Pins</td></tr>
<tr><td>PS2,
PS1,
PS0</td><td>I</td><td><table><tr><th>PS2</th><th>PS1</th><th>PS0</th><th>State</th></tr><tr><td>L</td><td>H</td><td>L</td><td>3 wire-SPI MPU Interface</td></tr><tr><td>L</td><td>H</td><td>H</td><td>4 wire-SPI MPU Interface</td></tr><tr><td>H</td><td>L</td><td>L</td><td>6800-series 8 bits parallel MPU interface</td></tr><tr><td>H</td><td>H</td><td>L</td><td>8080-series 8 bits parallel MPU interface</td></tr></table>These pins should be fixed to proper “H” or “L”.</td><td>3</td></tr>
<tr><td>CL</td><td>I</td><td>External clock source for test purpose. When CLS = H, TLS8103 use internal clock oscillator, leave CL pin floating; when CLS = L, TLS8103 use external clock, connect CL to external clock source.
Please be noted that CL only for test purpose, for normal LCM design, please connect CLS = H and leave CL floating or connect CL with “L”.</td><td>1</td></tr>
<tr><td>CLS</td><td>I/O</td><td>When CLS = H, TLS8103 use internal clock oscillator, leave CL pin floating; when CLS = L, TLS8103 use external clock, connect CL to external clock source.</td><td>1</td></tr>
</table>

<table>
<tr><td>CSEL</td><td>I</td><td>CSEL = L, COM0~65 is in one side, COM66~131 is in the opposite side.

And it can be set to ‘L’ only.</td><td>1</td></tr>
<tr><td>TE</td><td>I</td><td>Frame sync output for tear affection. Please leave it open when don’t use this function</td><td>1</td></tr>
<tr><td colspan="4">LCD Driver Pins</td></tr>
<tr><td>SEG0 – SEG395</td><td>O</td><td>LCD segment driver outputs.
This display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (internal)</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>Vg</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>H</td><td>VSS</td><td>Vg</td></tr>
<tr><td>L</td><td>L</td><td>Vg</td><td>VSS</td></tr>
<tr><td colspan="2">Sleep-in mode</td><td>VSS</td><td>VSS</td></tr>
</table></td><td>396</td></tr>
<tr><td>COM0 – COM131</td><td>O</td><td>LCD column driver outputs
This internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (internal)</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">Vm</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">Vm</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
</table></td><td>132</td></tr>
<tr><td colspan="4">Test Pins</td></tr>
<tr><td>T1- T8</td><td>I/O</td><td>Test pins, should be left open.</td><td>8</td></tr>
<tr><td>GITOL/ GITOR</td><td>I/O</td><td>GITOL should be connected with GITOR by ITO which run a ring on LCM glass. The TLS8103 can use these two pins and the ITO ring to improve ESD capability. Please leave these two pins open when don’t use this function.</td><td>2</td></tr>
</table>

ITO requirements

Table4 TLS8103 ITO series resistor requirements

Name	Type	Maximum Series Resistors (Ω)
VCC	Power supply	50
VDDIO	Power supply	30
REG_OUT	Power supply	50
VDD	Power supply	20
VCI	Power supply	30
GND	Power supply	30
VSS	Power supply	30
LCDVSS	Power supply	20
VPP	Power supply	50
V0	Capacitor connection	100
XV0	Capacitor connection	100
Vg	Capacitor connection	100
Vm	Capacitor connection	100
PS2, PS1, PS0, CLS, CSEL	Input	1000
/RES	Input	200
D/C(SCK)	Input	200
/CS	Input	200
E(/RD)	Input	200
R/W(/WR)	Input	200
D7~D0	Inout	200
TE	Output	200
CL	Input	200

BLOCK DIAGRAM

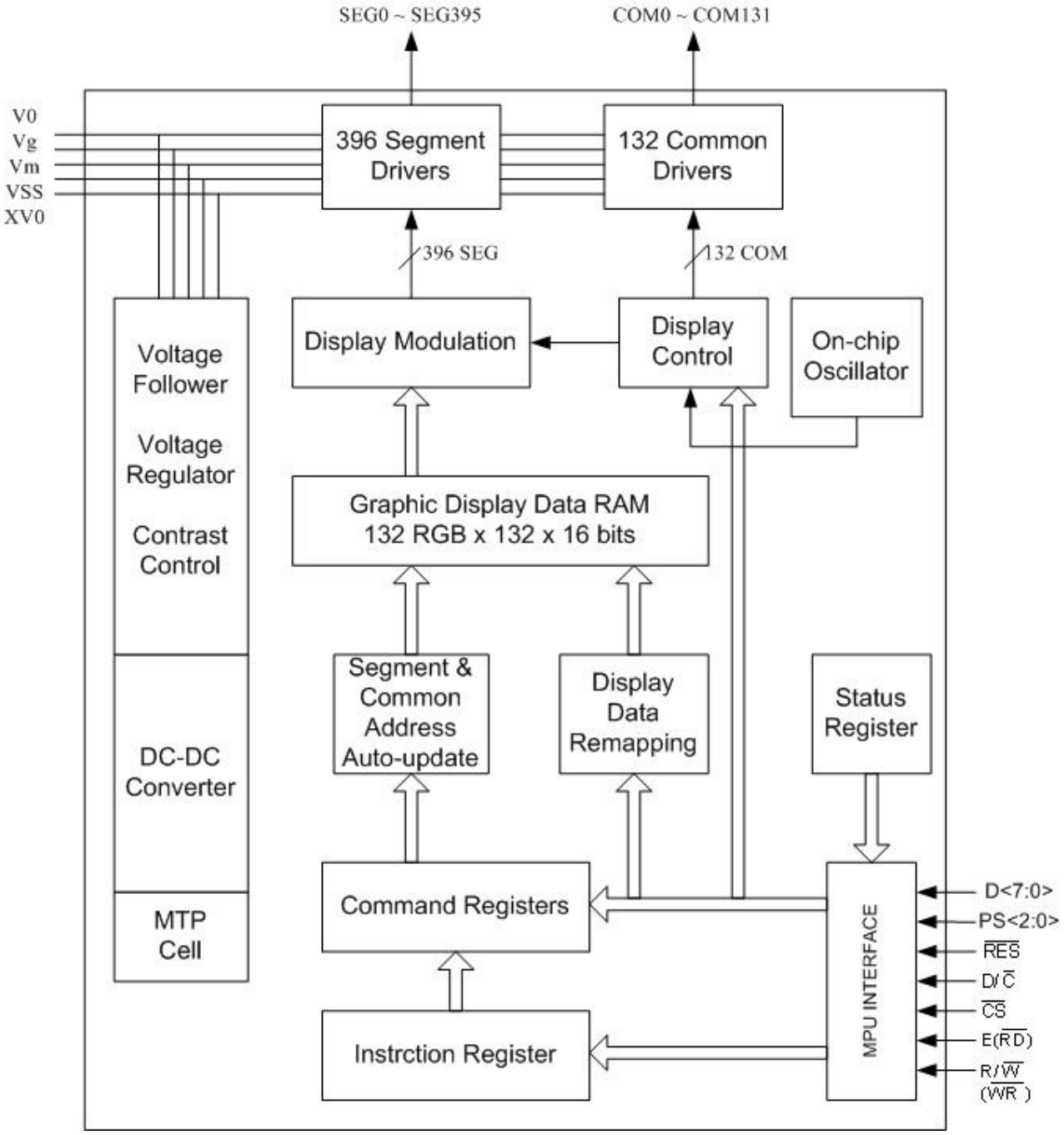


Figure 2 TLS8103 block Diagram

FUNCTION DESCRIPTIONS

MICROPROCESSOR INTERFACE

Chip Select Input

CS pin is chip selection. The TLS8103 is active when CS=L. In serial interface mode, the internal shift register and the counter are reset when CS=H.

Selecting Parallel / Serial Interface

TLS8103 has four types of interfaces with an MPU, which are two serial and two parallel interfaces. These parallel or serial interfaces are determined by PS pin as shown in Table 5.

Table5 Parallel/Serial interface mode selection

PS2	PS1	PS0	State
L	H	L	3 wire-SPI MPU Interface
L	H	H	4 wire-SPI MPU Interface
H	L	L	6800-series 8 bits parallel MPU interface
H	H	L	8080-series 8 bits parallel MPU interface

8-bit Parallel Interface

The TLS8103 identifies the type of the data bus signals according to the combination of D/C, E and R/W signals, as shown in Table 6.

Table6 Parallel data transfer mode selection

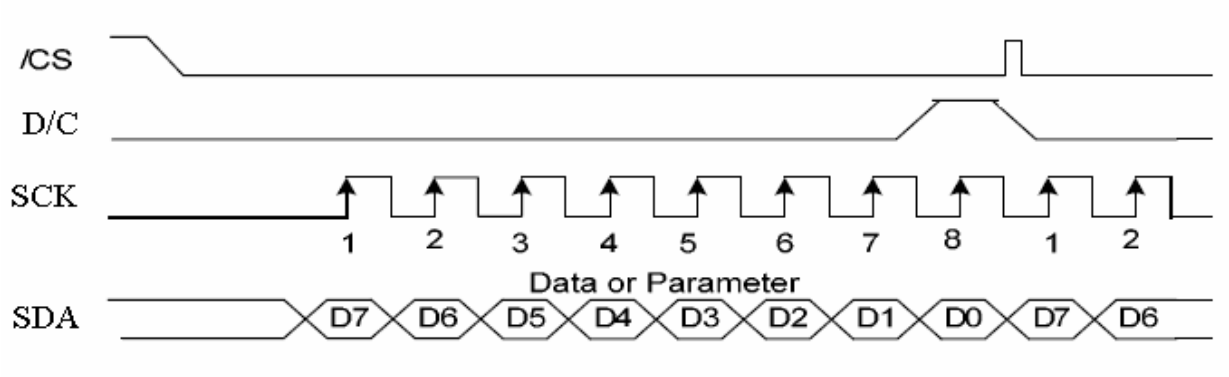
common	6800-series		8080-series		Description
D/C	R/W	E	WR	RD	
H	H	↑	H	↓	Display data read out
H	H	↑	H	↓	Register status read
L	L	↓	↑	H	Instruction write
H	L	↓	↑	H	Display data write

8- and 9-bit Serial Interface

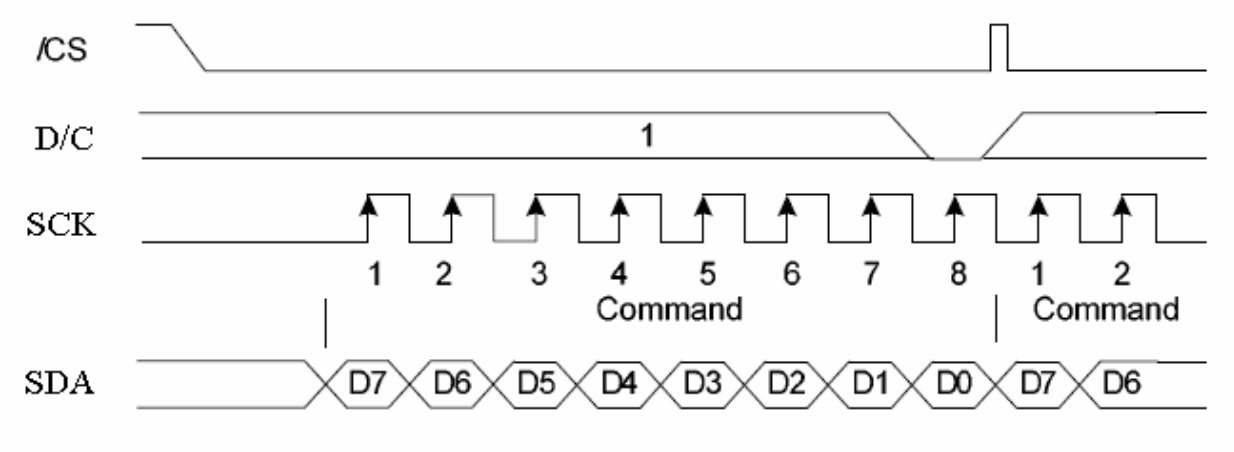
The 8-bit serial interface uses four pins CS, SDA, SCK, and D/C to write in commands and data. Meanwhile, the 9-bit serial interface uses three pins CS, SDA and SCK for the same purpose.

Data read is not available in the serial interface. Data must write to IC with 8 bits for each time. The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4-line)
When entering data (parameters): D/C= HIGH at the rising edge of the 8th SCK.



When entering command: D/C= LOW at the rising edge of the 8th SCK



When entering reading command:

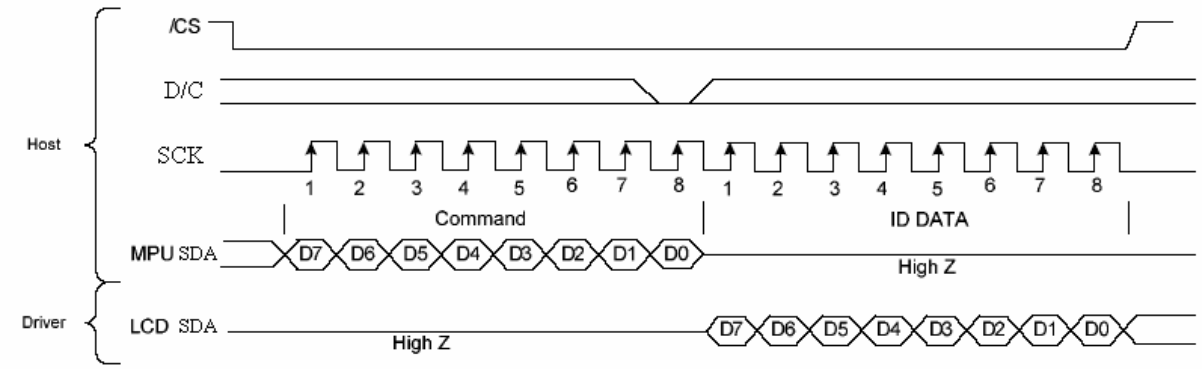
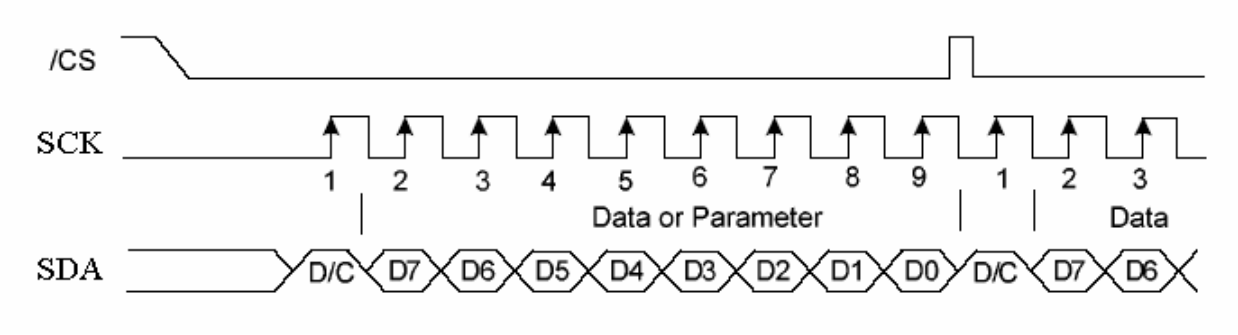
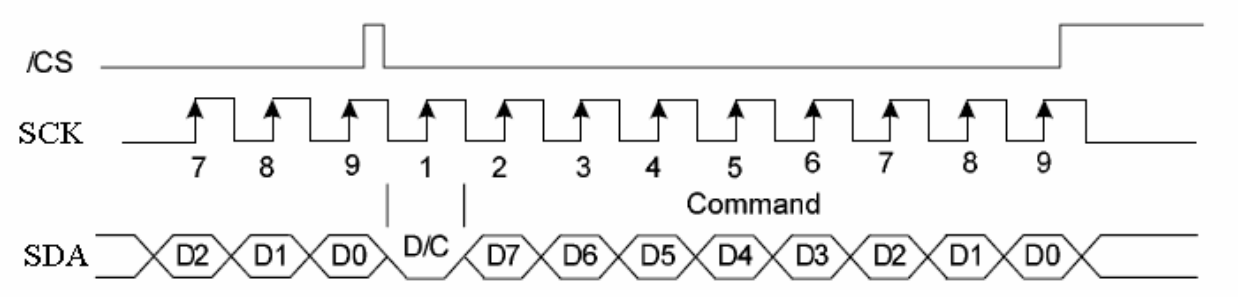


Figure3 4 lines 8 bits serial interface

(2) 9-bit serial interface (3-line)
When entering data (parameters): SDA= HIGH at the rising edge of the 1st SCK



When entering command: SDA= LOW at the rising edge of the 1st SCK



When entering reading command:

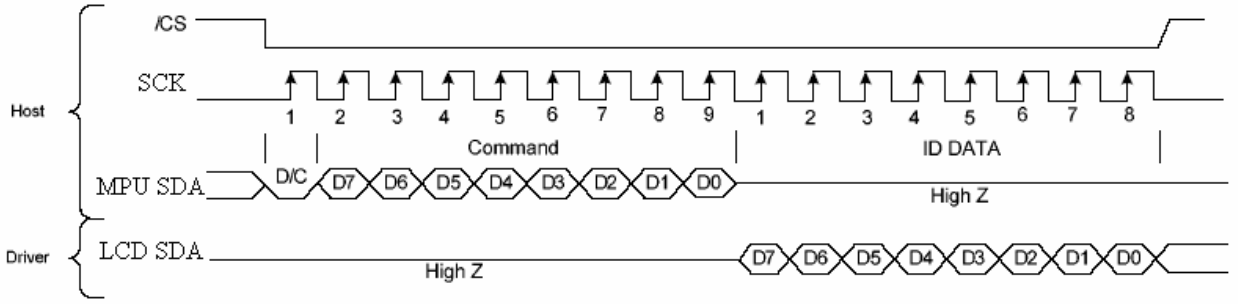


Figure4 3 lines 9 bits serial interface

- If CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.

8-bit and 9-bit Serial Interface Data Color Coding

8-bit serial interface (4-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

There is 1 pixel (1 pixel = 3 sub-pixels) per byte.

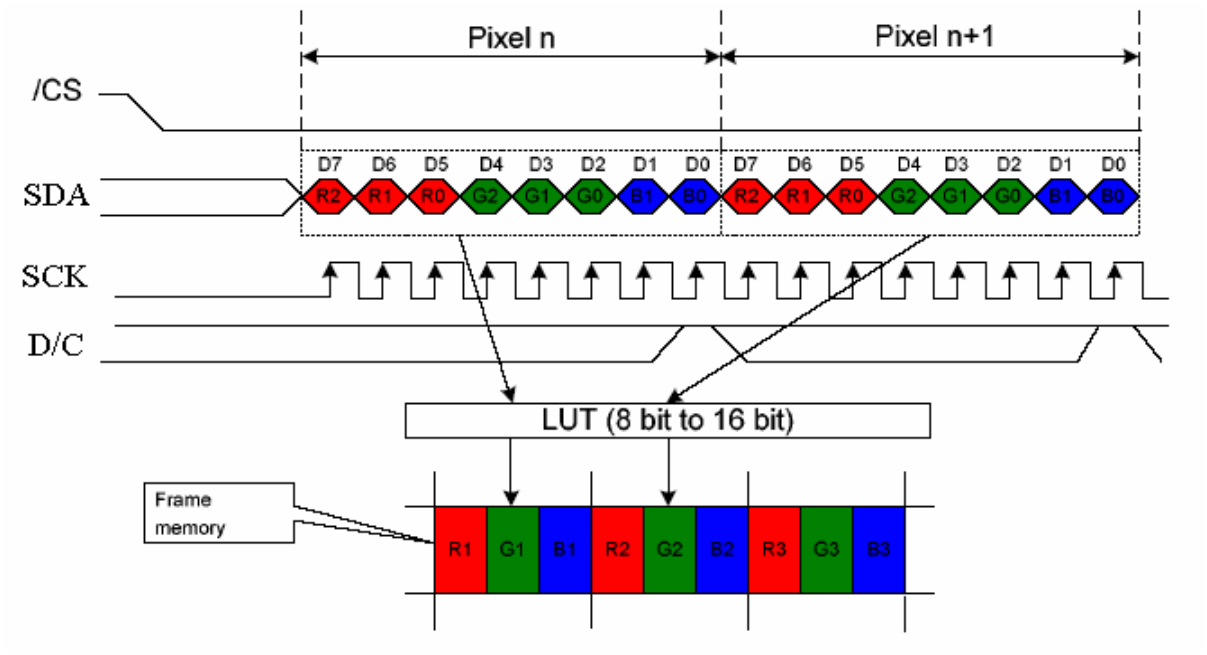


Figure5 8 bits serial interface 256 colors data format

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors — Type A

There are 2 pixel (1 pixel = 3 sub-pixels) per 3 byte.

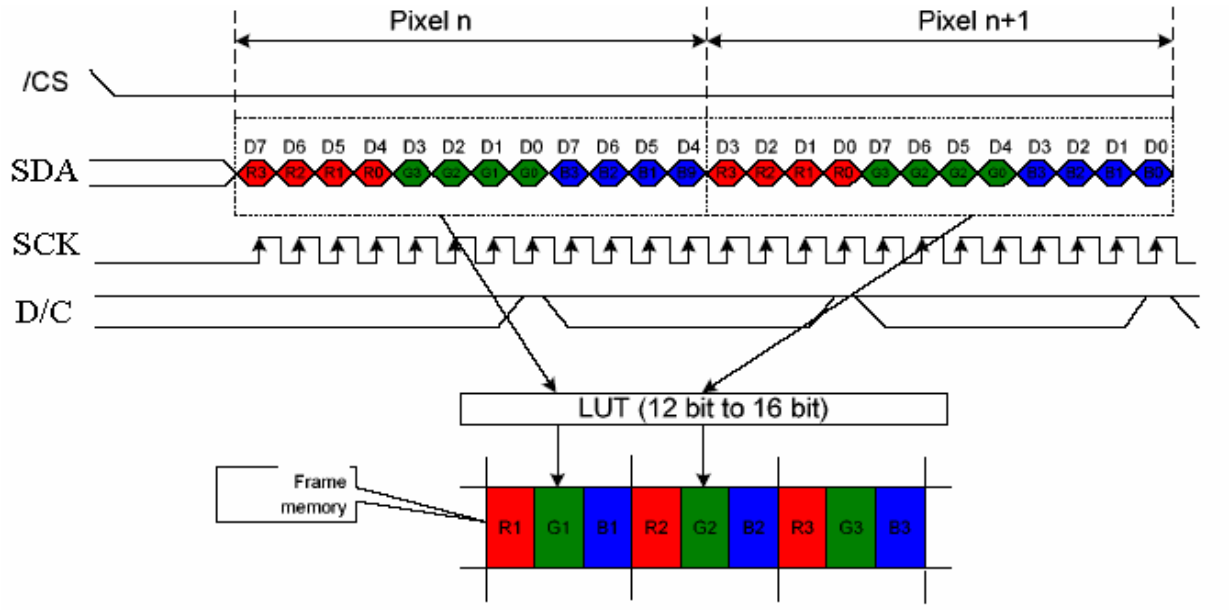


Figure6 8 bits serial interface 4096 colors data format TYPE A

(3) R 4-bit, G 4-bit, B 4-bit, 4,096 colors — Type B

There is 1 pixel (1 pixel = 3 sub-pixels) per 2 bytes.

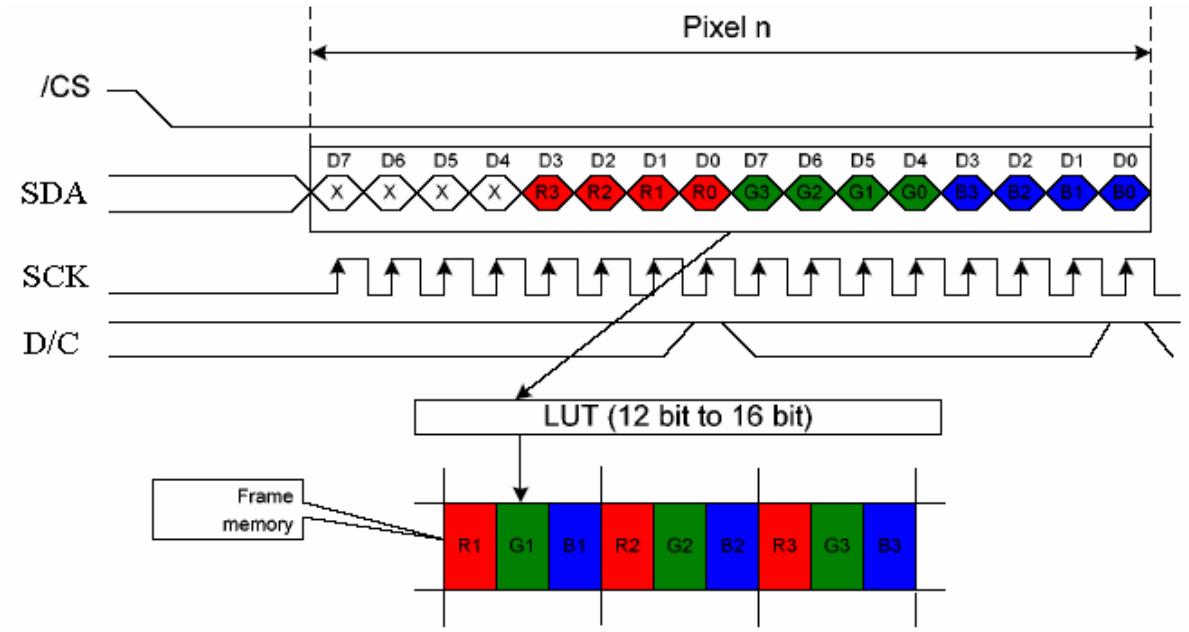


Figure7 8 bits serial interface 4096 colors data format TYPE B

(4) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

There is 1 pixel (1 pixel = 3 sub-pixels) per 2 byte.

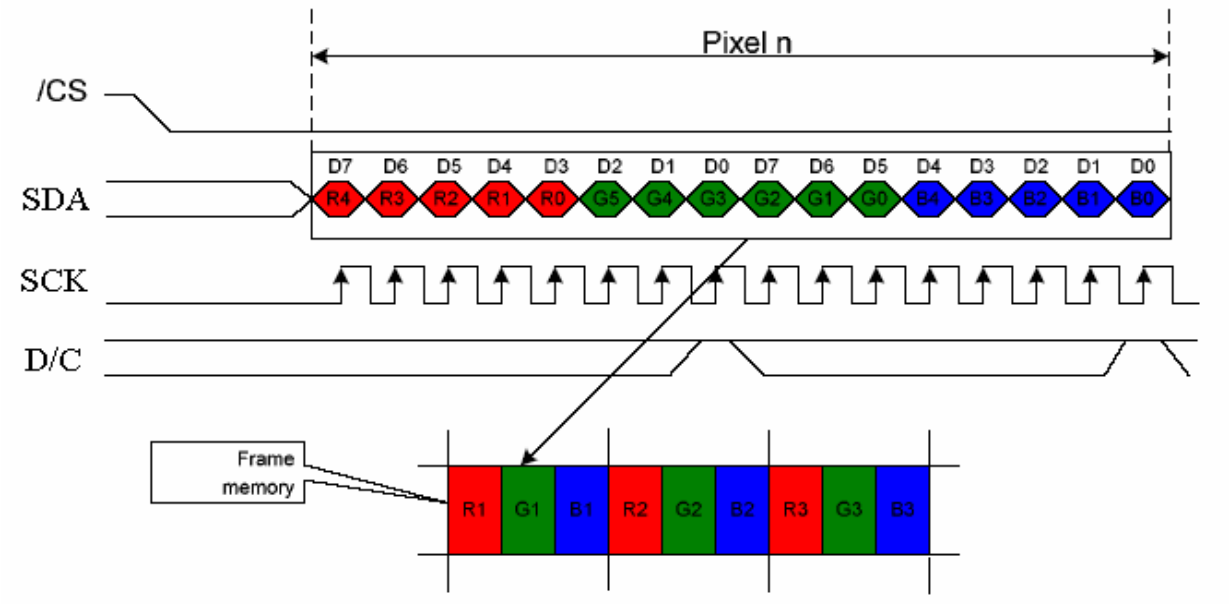


Figure8 8 bits serial interface 65K colors data format

(5) R 6-bit, G 6-bit, B 6-bit, 262K colors

There is 1 pixel (1 pixel = 3 sub-pixels) per 3 byte.

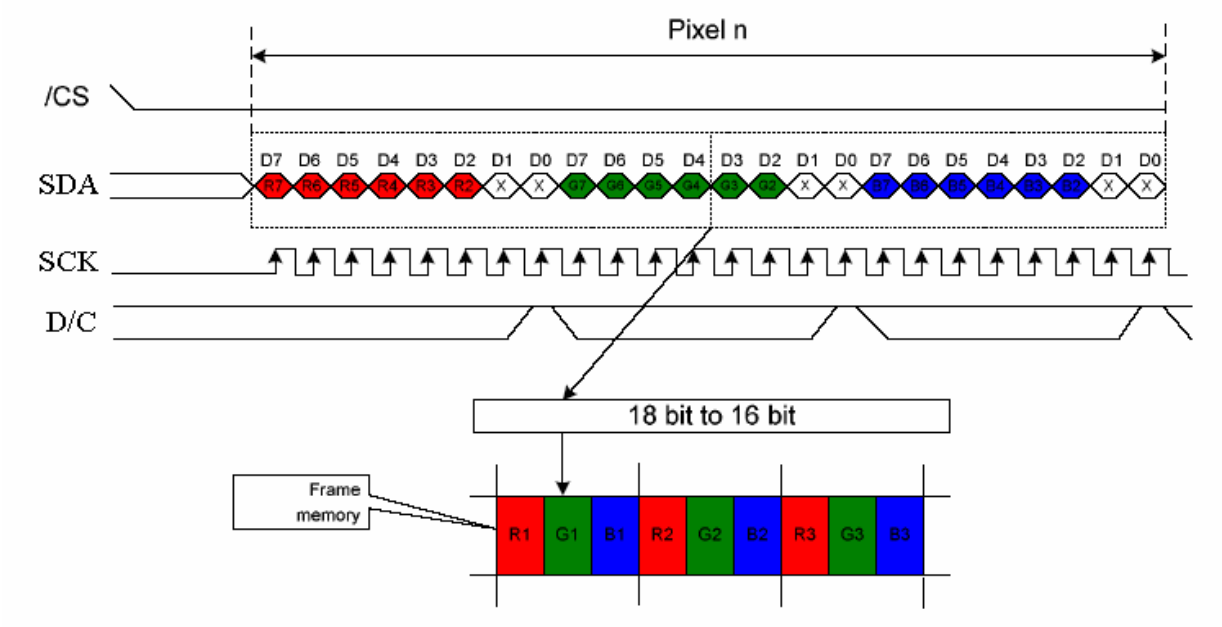


Figure9 8 bits serial interface 262K colors data format

(6) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (1 pixel = 3 sub-pixels) per 3 byte.

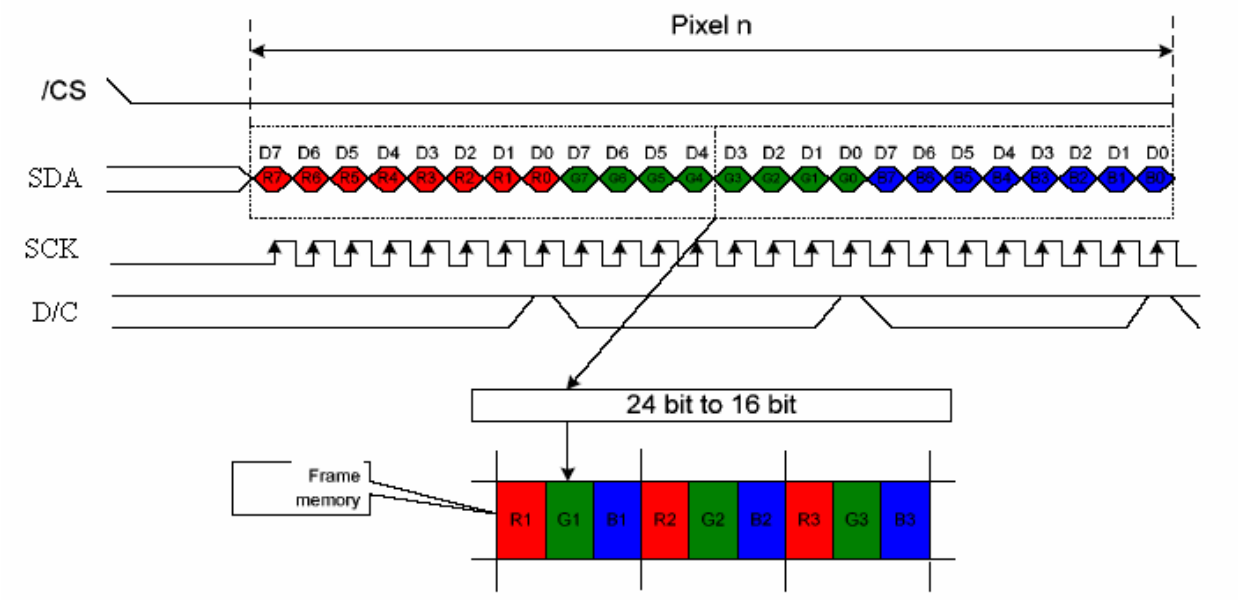


Figure10 8 bits serial interface 16M colors data format

9-bit serial interface (3-line)

(1) R 3-bit, G 3-bit, B 2-bit, 256 colors

There is 1 pixel (1 pixel = 3 sub-pixels) per byte.

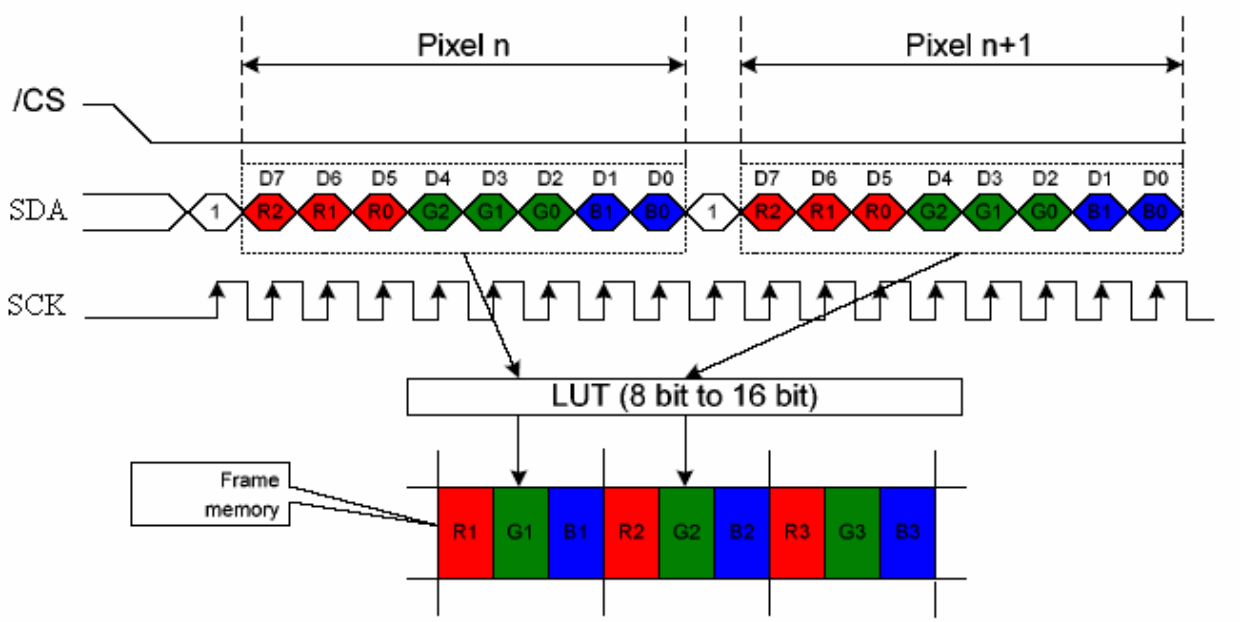


Figure11 9 bits serial interface 256 colors data format

(2) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type A

There are 2 pixel (1 pixel = 3 sub-pixels) per 3 byte.

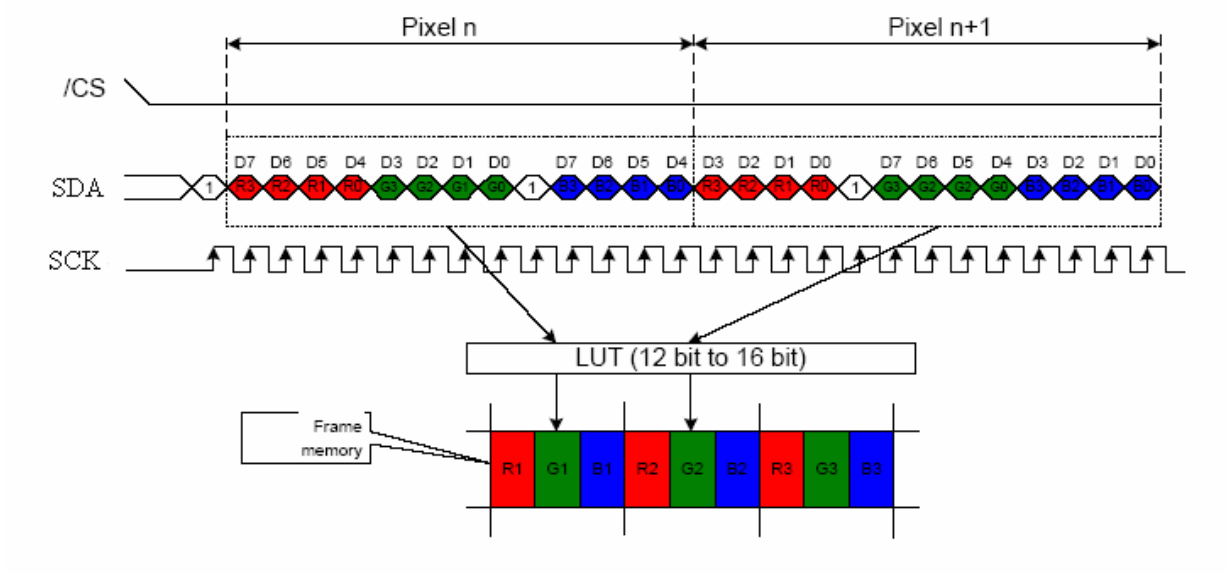


Figure12 9 bits serial interface 4096 colors data format TYPE A

(3) R 4-bit, G 4-bit, B 4-bit, 4,096 colors – Type B

There is 1 pixel (1 pixel = 3 sub-pixels) per 2 bytes.

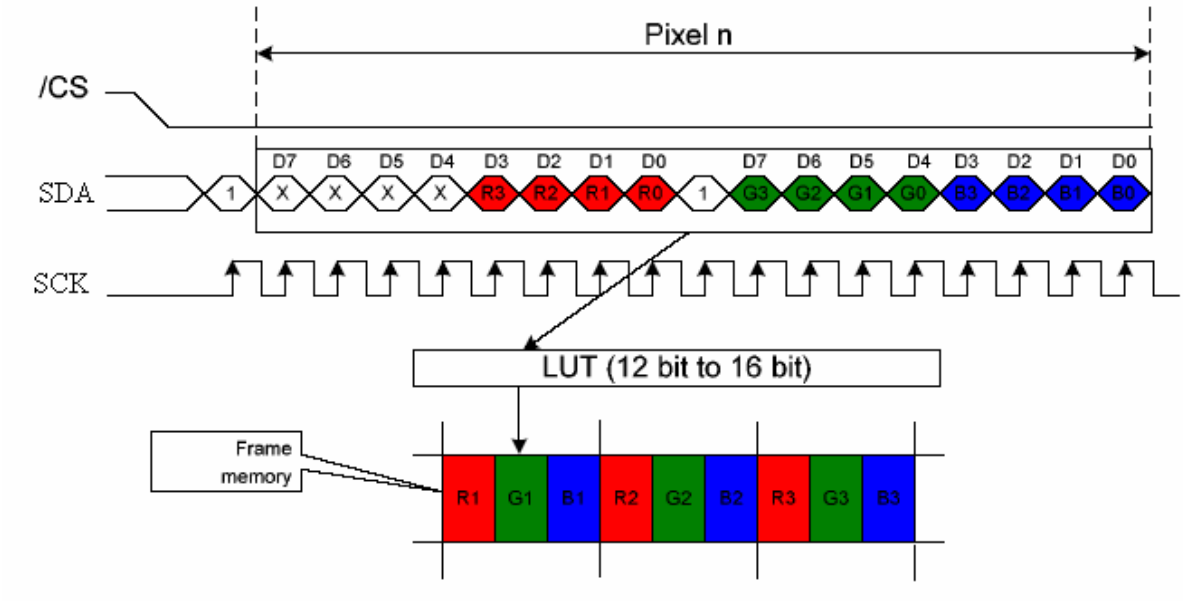


Figure13 9 bits serial interface 4096 colors data format TYPE B

(4) R 5-bit, G 6-bit, B 5-bit, 65,536 colors

There is 1 pixel (1 pixel = 3 sub-pixels) per 2 byte.

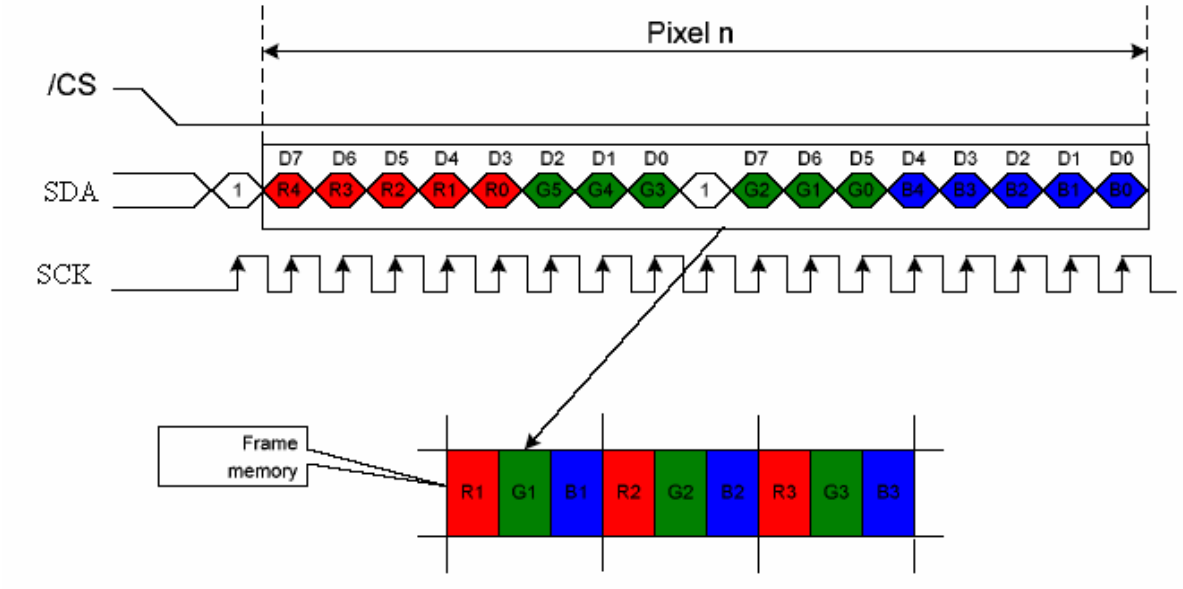


Figure14 9 bits serial interface 65K colors data format

(5) R 6-bit, G 6-bit, B 6-bit, 262K colors

There is 1 pixel (1 pixel = 3 sub-pixels) per 3 byte.

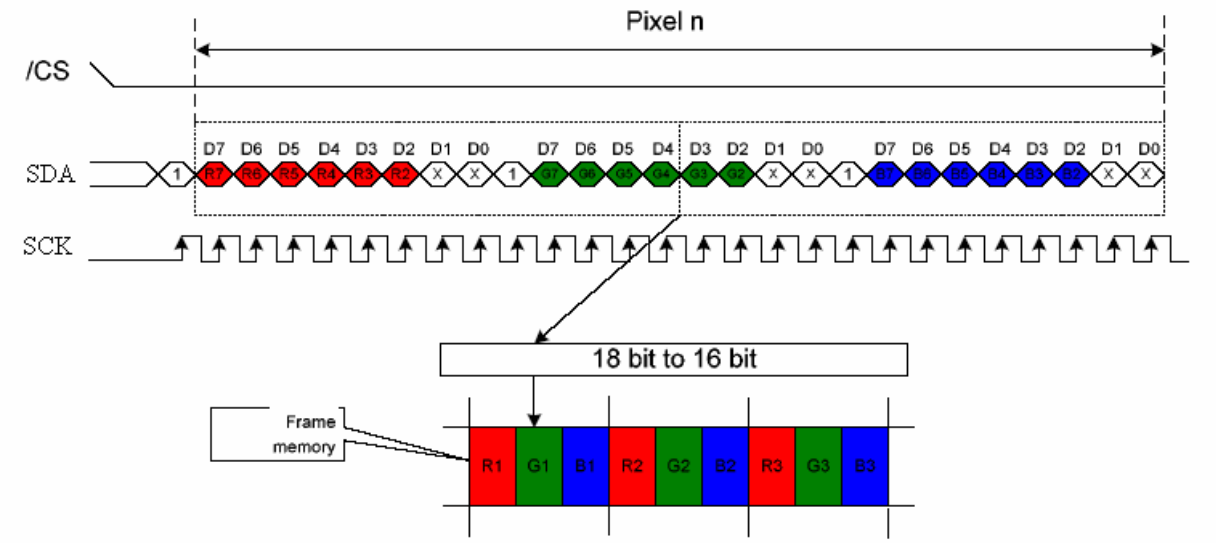


Figure15 9 bits serial interface 262K colors data format

(6) R 8-bit, G 8-bit, B 8-bit, 16M colors

There is 1 pixel (1 pixel = 3 sub-pixels) per 3 byte.

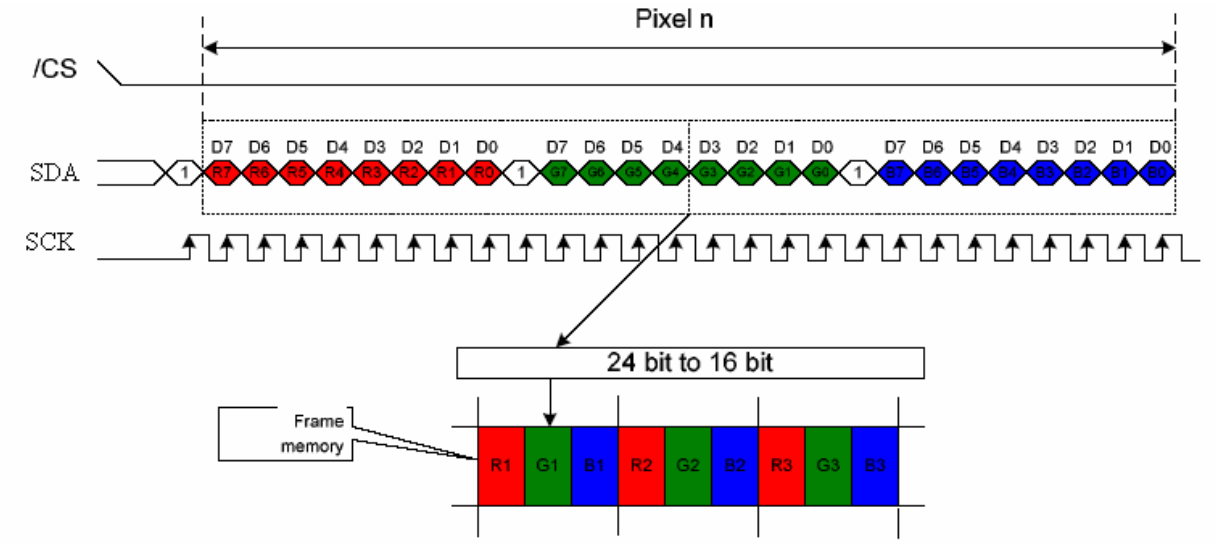


Figure16 9 bits serial interface 16M colors data format

ACCESS TO DDRAM AND INTERNAL REGISTERS

TLS8103 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.
For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle.

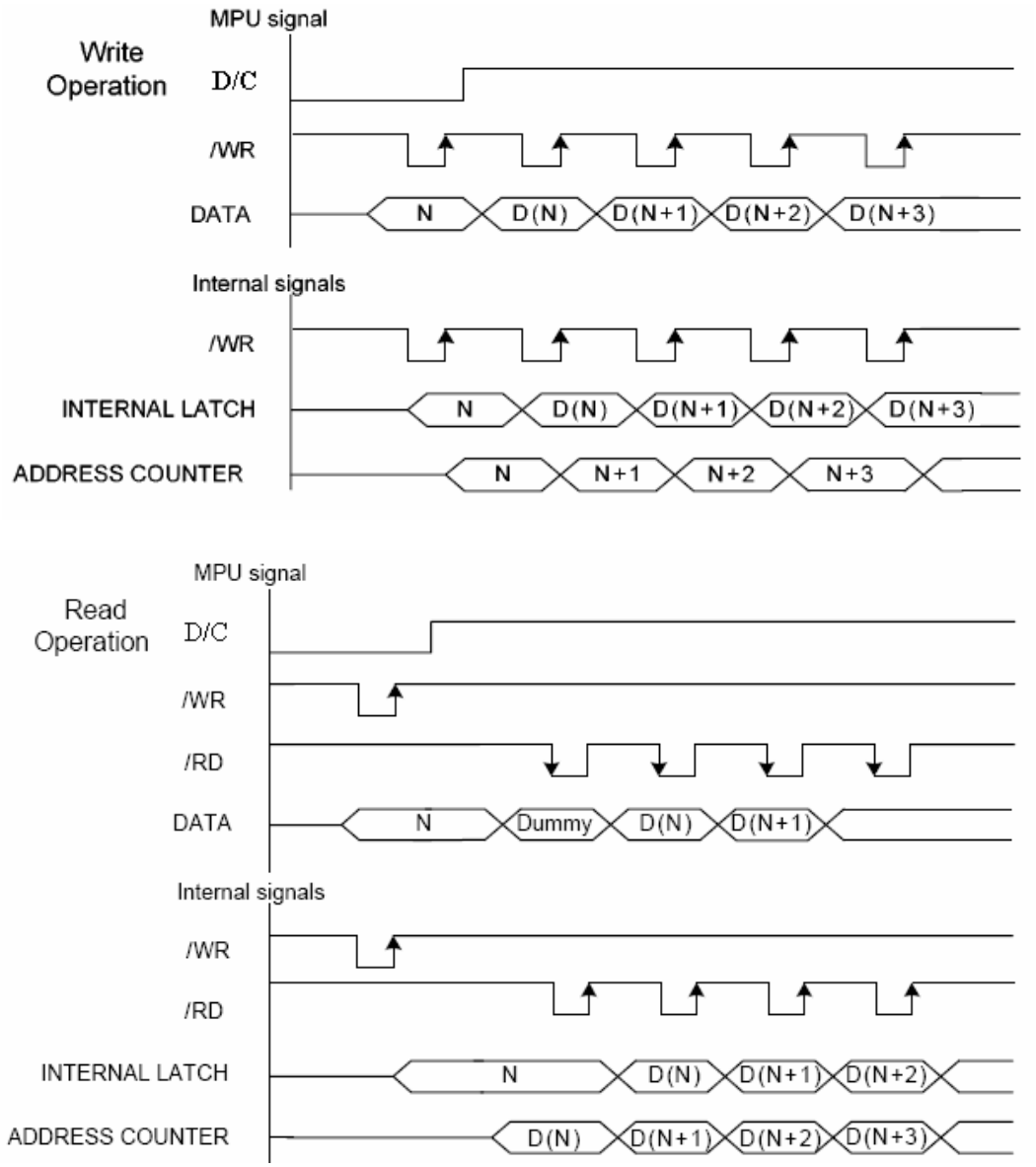


Figure17 Parallel interface pipeline data access

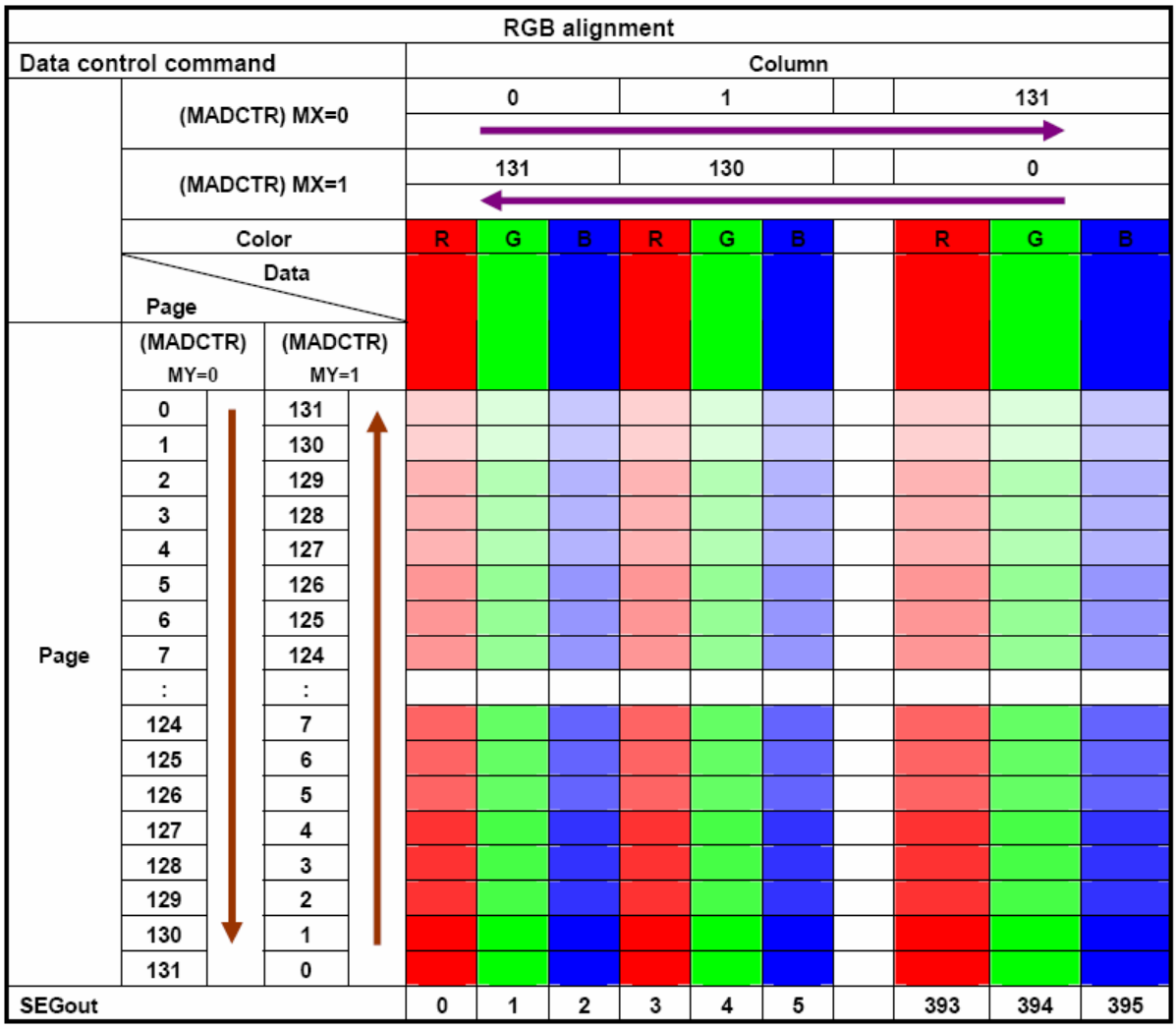
DISPLAY DATA RAM (DDRAM)

DDRAM

It is 132 X 132 X 16 bits capacity RAM prepared for storing dot data. Refer to the following memory map for the RAM configuration.

You can change position of R and B with MADCTR command.

Memory Map

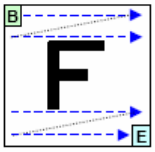
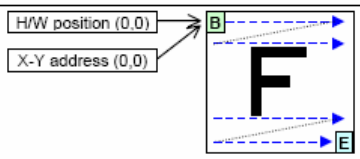
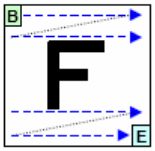
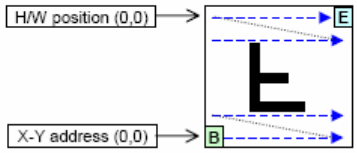
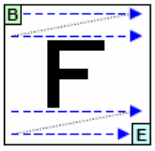
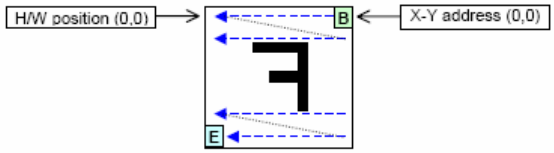
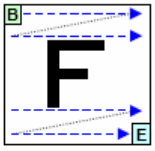
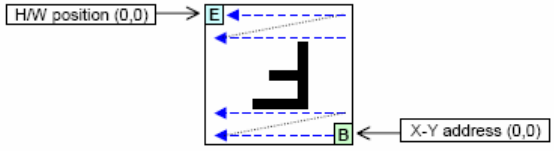
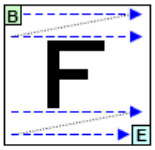
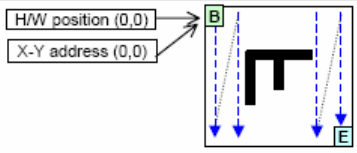
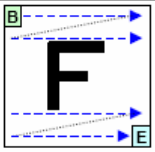
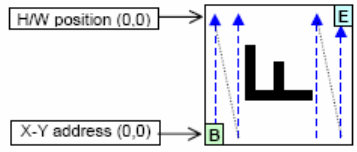
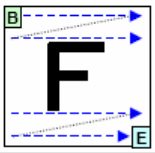
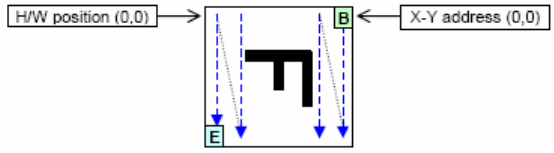
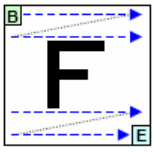
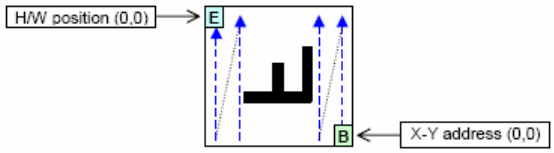


Address Control

The address counter sets the addresses of the display data RAM for writing. Data is written into the pixel RAM matrix of TLS8103. The data for one pixel or two pixels is collected (RGB 565 bit), according to the data formats. As soon as this pixel-data information is complete, the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=131 (83h). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined into which will be written. The window is programmable via the command registers. XS, YS designating the start address and XE, YE designating the end address. For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=131 (83h), YE=131 (83h).
In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (MV=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE), the address pointers wrap around to address (X=XS and Y=YS). For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR”, define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed.

For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

Scroll Address Circuit

The circuit associates lines on DDRAM with COM output. TLS8103 processes signals for the liquid crystal display on 1-line basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in line.

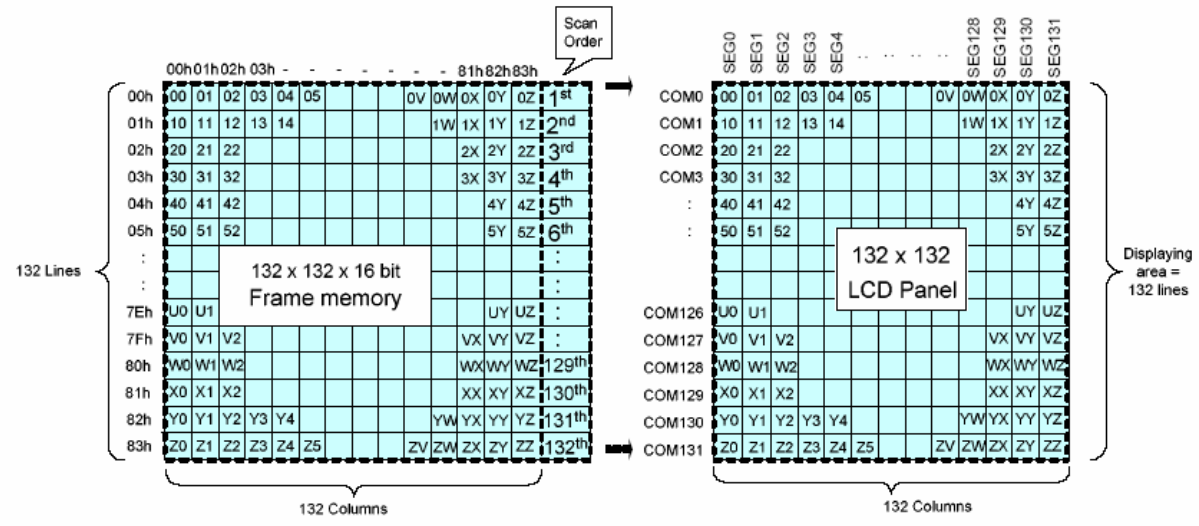
Display data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

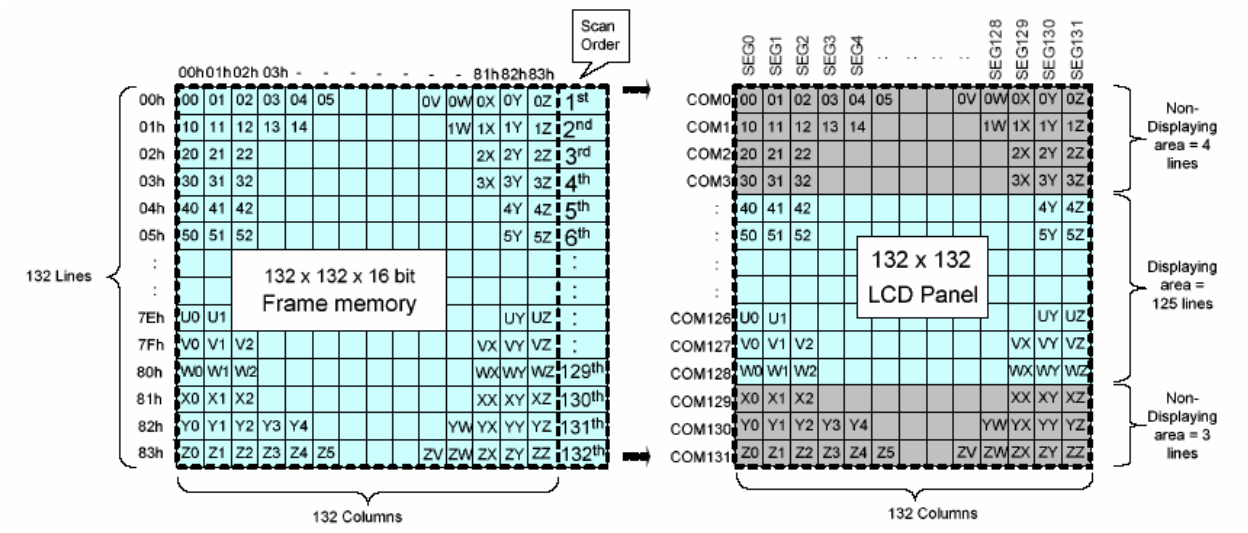
Normal Display On or Partial Mode On, Vertical Scroll Off

In this mode, contents of the frame memory within an area where column address is 00h to 83h and row address is 00h to 83h is displayed. To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



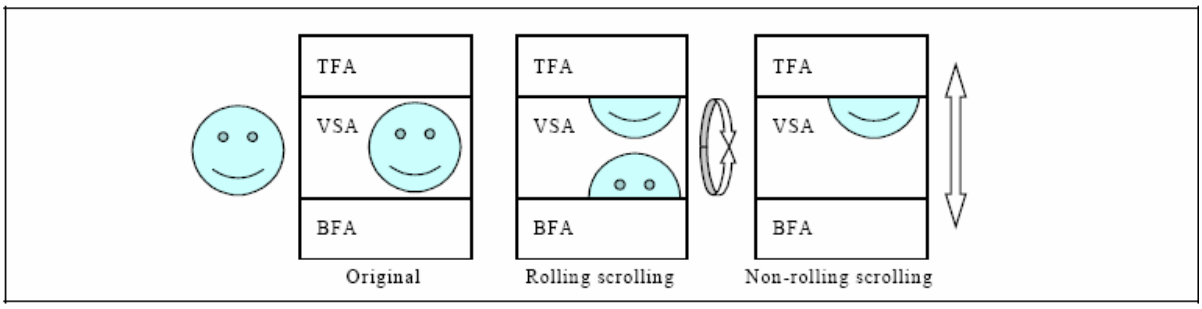
Example2) Partial Display On: PSL[6:0] = 04h, PEL[6:0] = 80h



Vertical Scroll/Rolling Scroll

Rolling Scroll

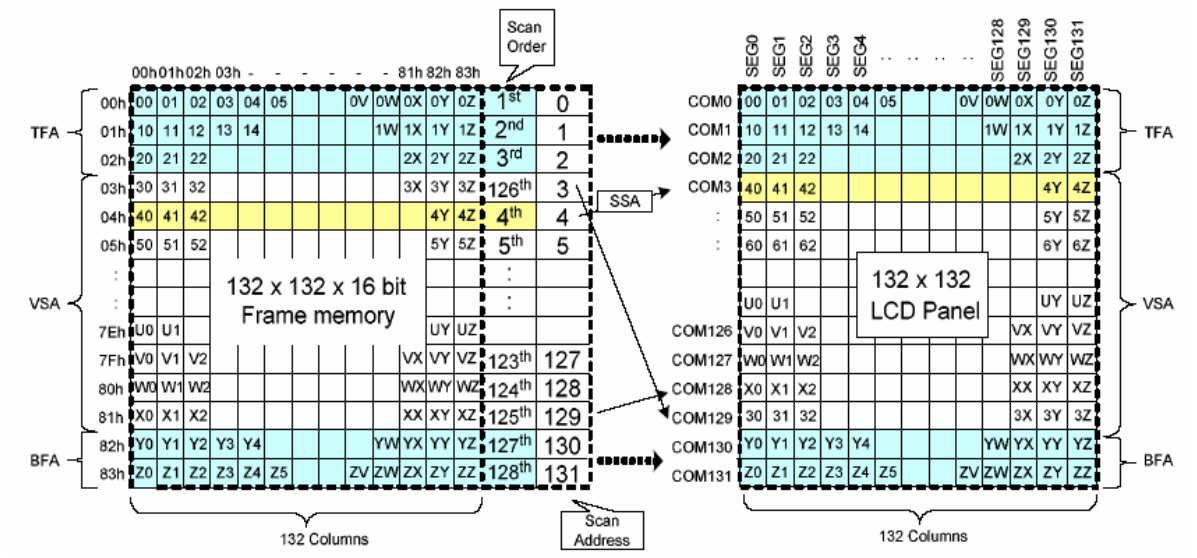
There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).



When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =132. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example)

Panel size=132 x 132, TFA =3, VSA=127, BFA=2, SSA=4: Rolling Scroll



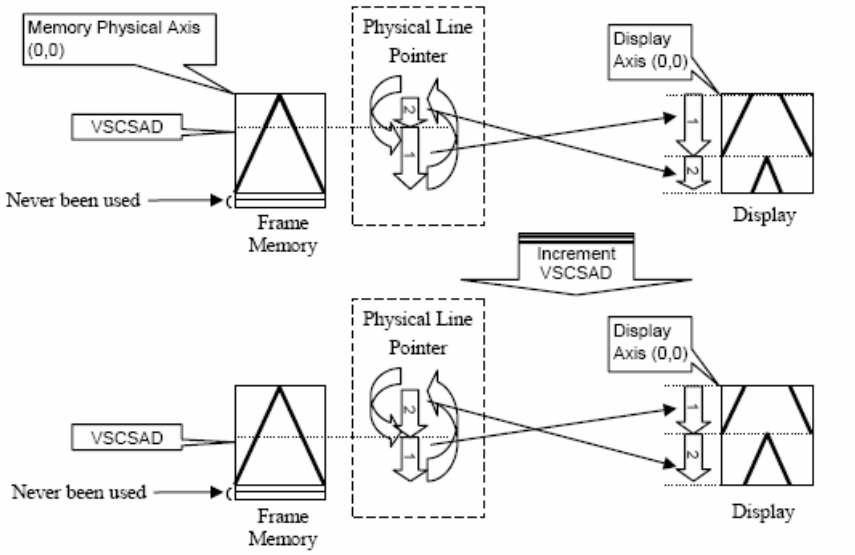
Vertical Scroll Example

There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA<130
N/A. Do not set TFA + VSA + BFA<130. In that case, unexpected picture will be shown.

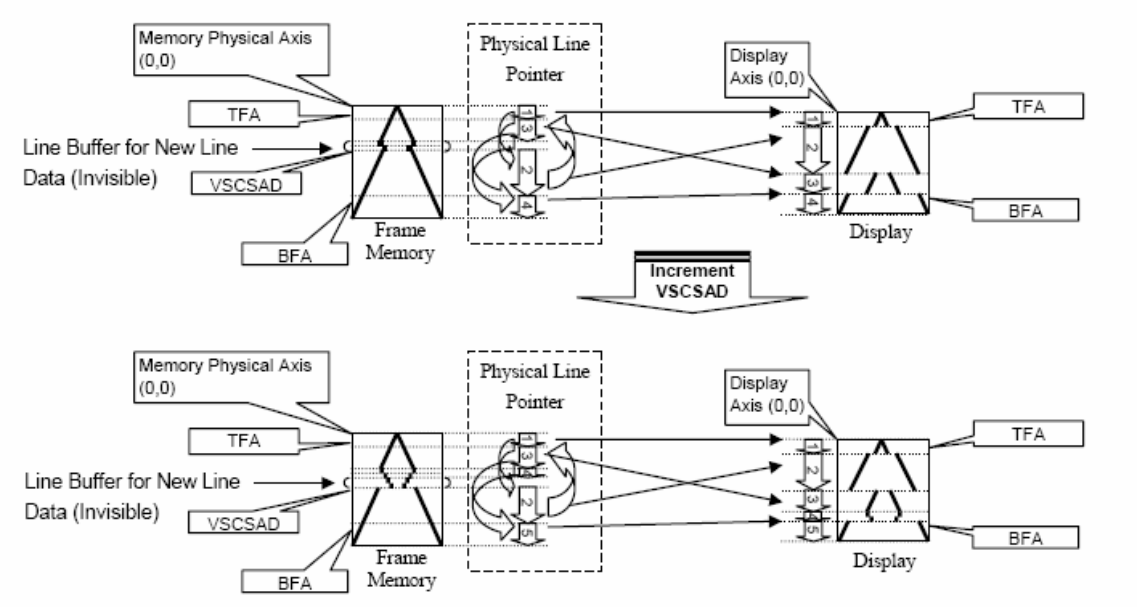
Case 2: TFA + VSA + BFA=130 (Rolling Scrolling)

Example1) TFA=0, VSA=130, BFA=0 and VSCSAD=40.



Case3: TFA + VSA + BFA =132 (Scrolling with 2line buffer)

Example) TFA=20, VSA=82, BFA=30 and VSCSAD=60.



Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

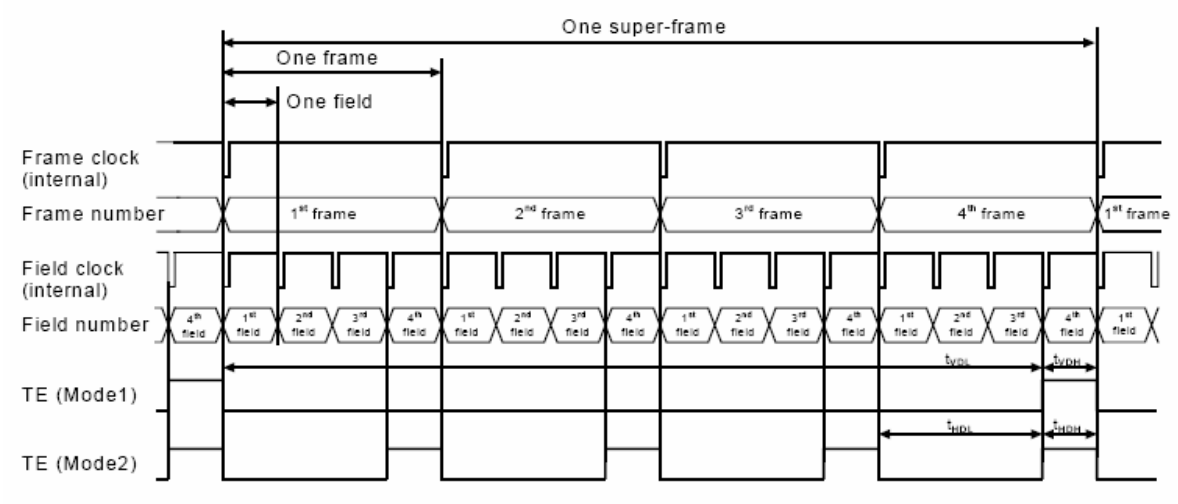
Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync (Tvhd) information only before Super-frame's start (only during every 4th frame and every 4th field).

tvdh = The LCD display is updating the end (4th frame) of the previous Super-frame from the Frame memory
tvdl = The LCD display is updated 1st, 2nd and 3rd frames (It is possible that the begin of the 4th frame is also included for this timing) from the Frame Memory.

Mode 2, the Tearing Effect Output signal consists of only H-Sync (1 frame) information, there is one high pulse and 1 low pulse during every frame.

thdh = The LCD display is updated the end of the frame field from the Frame Memory.
thdl = The LCD display is updated the begin of the frame field from the Frame Memory.



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

Tearing Effect Line Timing

The Tearing Effect signal is described below:

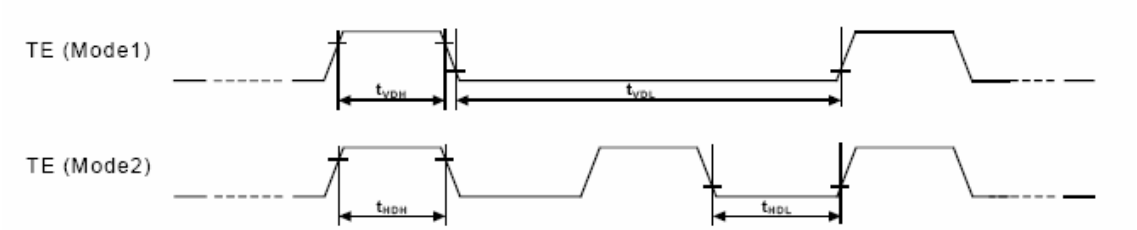


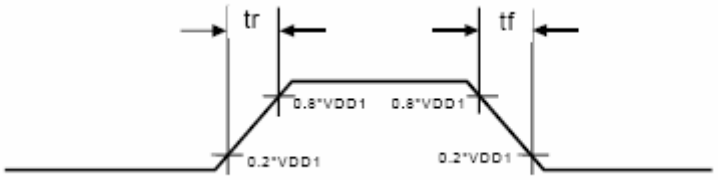
Figure18 Tear affection timing diagram

AC characteristics of Tearing Effect Signal

Idle Mode Off (Frame Rate = 100Hz)

Symbol	Parameter	Min	Max	unit	description
t_{VDL}	Vertical Timing Low Duration	37.5		ms	Mode1
t_{VDH}	Vertical Timing High Duration	2.5		ms	
t_{HDL}	Horizontal Timing Low Duration	7.5		ms	Mode2
t_{HDH}	Horizontal Timing High Duration	2.5		ms	

NOTE: The timings in Table 5.2.5 apply when MADCTL B4=0 and B4=1 . The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



Oscillation circuit

This is on-chip oscillator without external resistor. When the internal oscillator is used, CLS must connect to VDD; when the external oscillator is used, CL could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock CL (internal), which is generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 132-bits display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction.

Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out:

In this mode, the display is able to show maximum 65K colors.

2. Partial Mode On, Idle Mode Off, Sleep Out:

In this mode part of the display is used with maximum 65K colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out:

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out:

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode:

In this mode, the DC-DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with Digital VDD power supply. Contents of the memory are safe.

6. Power Off Mode:

In this mode, both Analog and Digital power supplies are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

POWER FLOW CHART FOR DIFFERENT POWER MODES

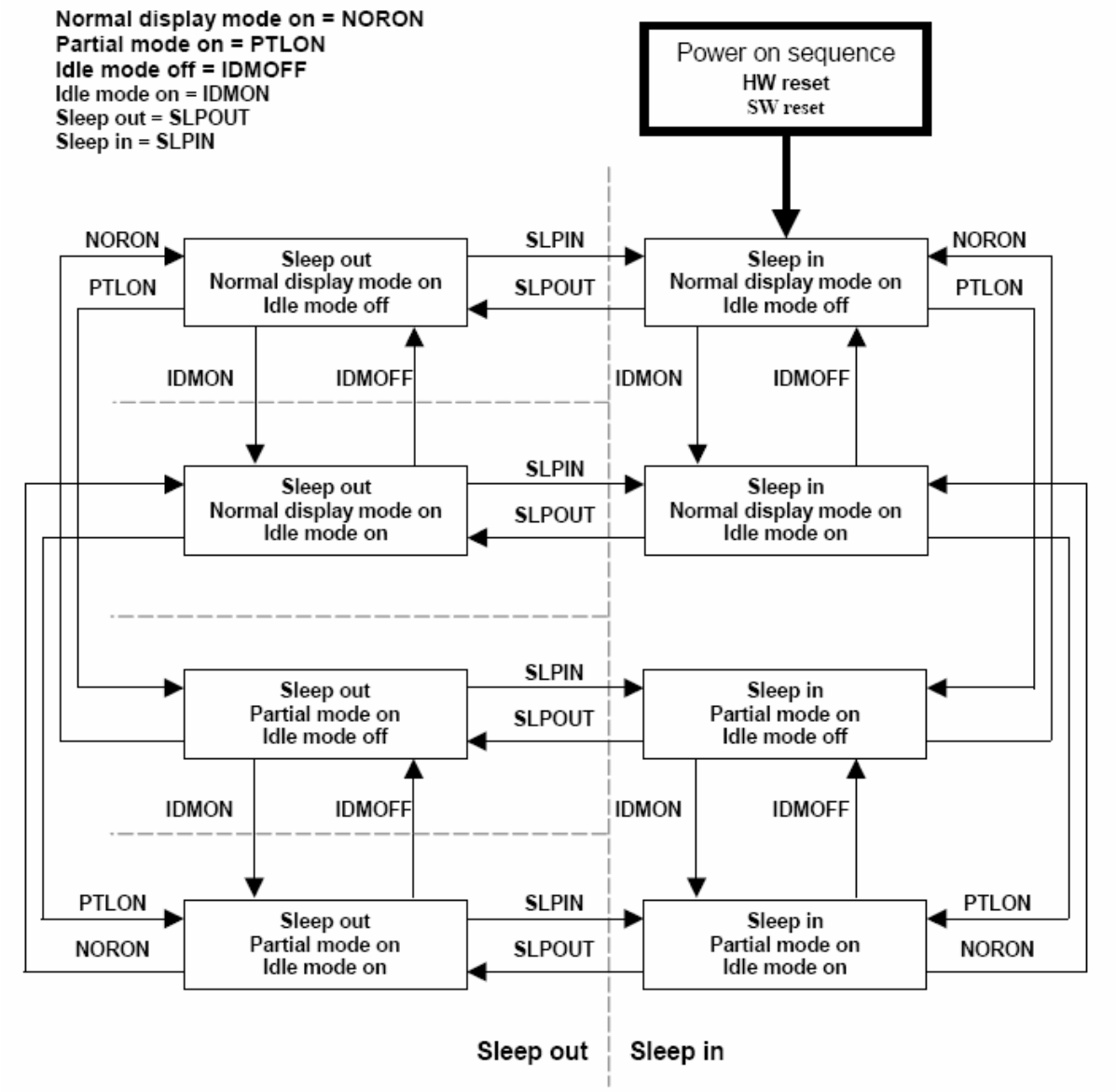


Figure19 TLS8103 Power modes

Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Figure3 shows the referenced combinations in using Power Supply circuits.

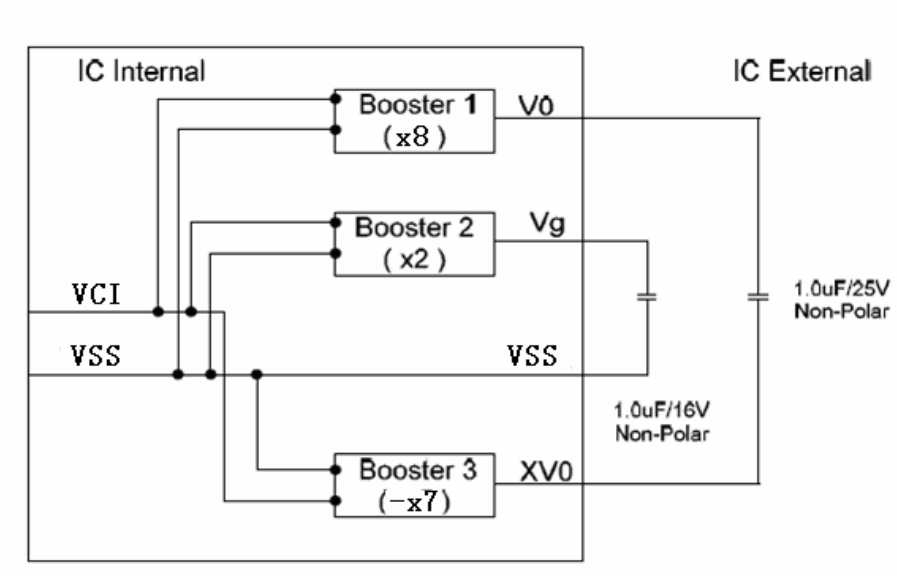


Figure20 TLS8103 LCD Power circuits

Voltage Regulator Circuits

There is a built-in voltage regulator circuits in TLS8103 for generating V0. After internal voltage is regulated by voltage regulator circuit, V0 is generated. Detail explanation of V0 set is listed below:

SET V0 (Temperatue = 24° C)

V0=a+{Vop[8:0] + (EV[6:0]-3Fh)}*b (V)
Example:
Vop[8:0]=011010010
EV[6:0]=0111111
V0=3.6 + { 210 + (63-63) } *0.04 =12 (V)

- a is a fixed constant value (a=3.6V).
- b is a fixed constant value (b=0.04V).
- Vop [8:0] is the programmed VOP value. The programming range for Vop[8:0] is 0 to 410 (19Ahex).
- The range of contrast is 128 steps for MTP to fine tune VOP.

The Vop [8:0] value must be in the V0 programming range as given in Figure 4. Evaluating V0 equation, values outside the programming range indicated in many result. Resulting Vop[8:0] values higher than 410 will be mapped to Vop[8:0] = 410. At room temperature (24° C), we suggests V0 range equals 3.6V to 18V.

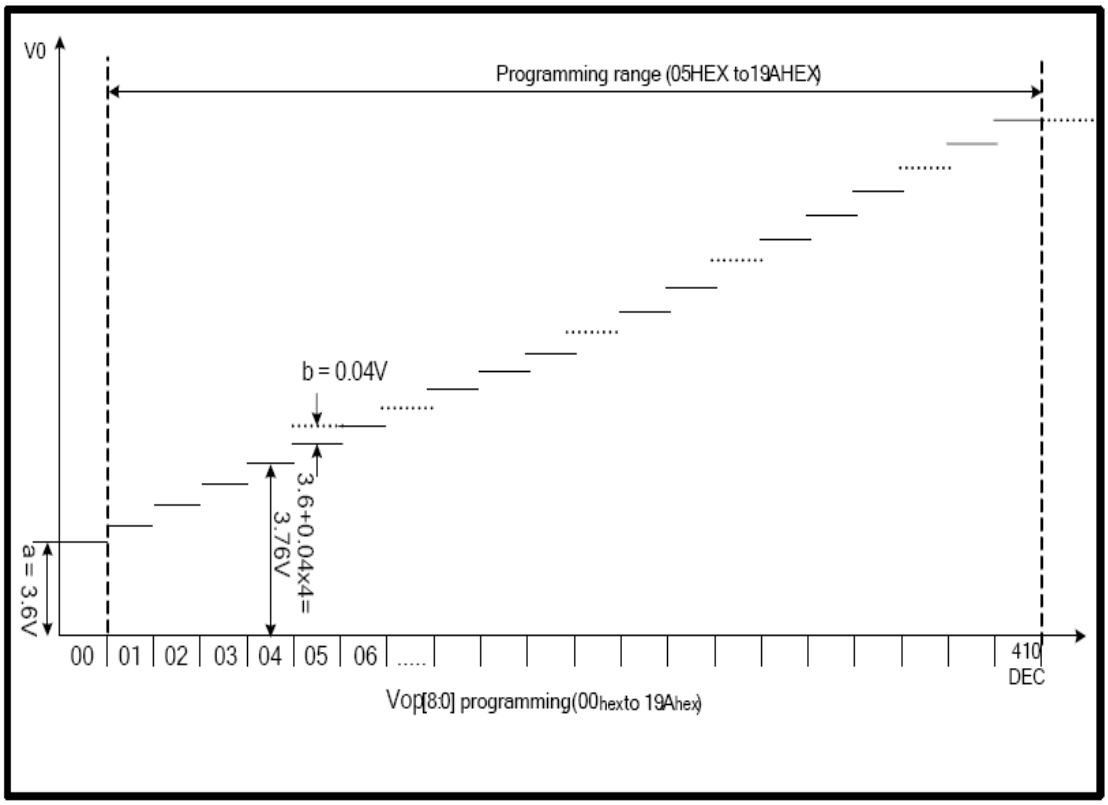


Figure21 TLS8103 LCD Voltage Regulator setting

As the programming range for the internally generated V0 voltage is above the limited V0 (20V), users has to ensure while selecting the temperature compensation that under all conditions and including all tolerances that the V0 voltage remains below 18V.

SET V0 with temperature compensation (Temperature ≠ 24℃)

There are 16-line slope in each temperature steps and customer can select one line slope of temperature compensation coefficiency for each temperature step. Each temperature step is 8° C. Please see Figure 5 as below.

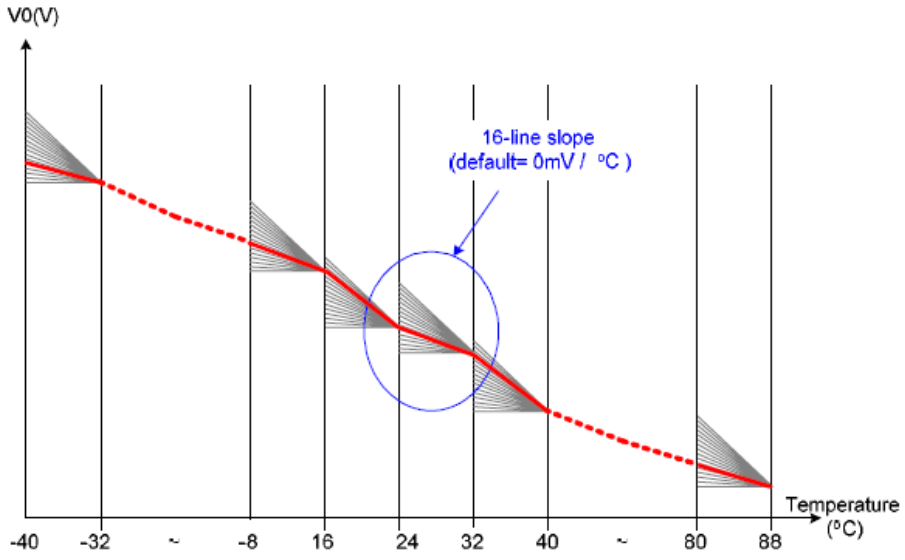


Figure22 TLS8103 LCD temperature compensation curve setting

In command TEMPSEL, each MTx, where x=0, 1, 2,…, E, F, has a value between 0 and 15. MTx= 0 results in 0V increment on V0, MTx = 1 results in Mx=5mV increment, …, MTx = 15 results in Mx=15x5mV=75mV increment. Note that each MTx individually corresponds to a temperature interval; The relations between Mx and V0 quantity due to temperature V0(T) are described in the equations shown as follows:

Temperature range	Equation V0(V) at temperature=T℃
-40℃ ≦ T ＜ -32℃	V0(T) = V0(T_{24})+ (-32-T) · M0 +(M1 + M2 + M3 + M4 + M5 + M6 + M7) · 8
-32℃ ≦ T ＜ -24℃	V0(T) = V0(T_{24})+ (-24-T) · M1 +(M2 + M3 + M4 + M5 + M6 + M7) · 8
-24℃ ≦ T ＜ -16℃	V0(T) = V0(T_{24})+ (-16-T) · M2 +(M3 + M4 + M5 + M6 + M7) · 8
-16℃ ≦ T ＜ -8℃	V0(T) = V0(T_{24})+ (-8-T) · M3 +(M4 + M5 + M6 + M7) · 8
-8℃ ≦ T ＜ 0℃	V0(T) = V0(T_{24})+ (0-T) · M4 +(M5 + M6 + M7) · 8
0℃ ≦ T ＜ 8℃	V0(T) = V0(T_{24})+ (8-T) · M5 +(M6 + M7) · 8
8℃ ≦ T ＜ 16℃	V0(T) = V0(T_{24})+ (16-T) · M6 + M7 · 8
16℃ ≦ T ＜ 24℃	V0(T) = V0(T_{24})+ (24-T) · M7
24℃ ≦ T ＜ 32℃	V0(T) = V0(T_{24})－(T-24) · M8
32℃ ≦ T ＜ 40℃	V0(T) = V0(T_{24})－(T-32) · M9－M8 · 8
40℃ ≦ T ＜ 48℃	V0(T) = V0(T_{24})－(T-40) · M10－(M9 + M8) · 8
48℃ ≦ T ＜ 56℃	V0(T) = V0(T_{24})－(T-48) · M11－(M10 + M9 + M8) · 8
56℃ ≦ T ＜ 64℃	V0(T) = V0(T_{24})－(T-56) · M12－(M11 + M10 + M9 + M8) · 8
64℃ ≦ T ＜ 72℃	V0(T) = V0(T_{24})－(T-64) · M13－(M12 + M11 + M10 + M9 + M8) · 8
72℃ ≦ T ＜ 80℃	V0(T) = V0(T_{24})－(T-72) · M14－(M13 + M12 + M11 + M10 + M9 + M8) · 8
80℃ ≦ T ＜ 88℃	V0(T) = V0(T_{24})－(T-80) · M15－(M14 + M13 + M12 + M11 + M10 + M9 + M8) · 8

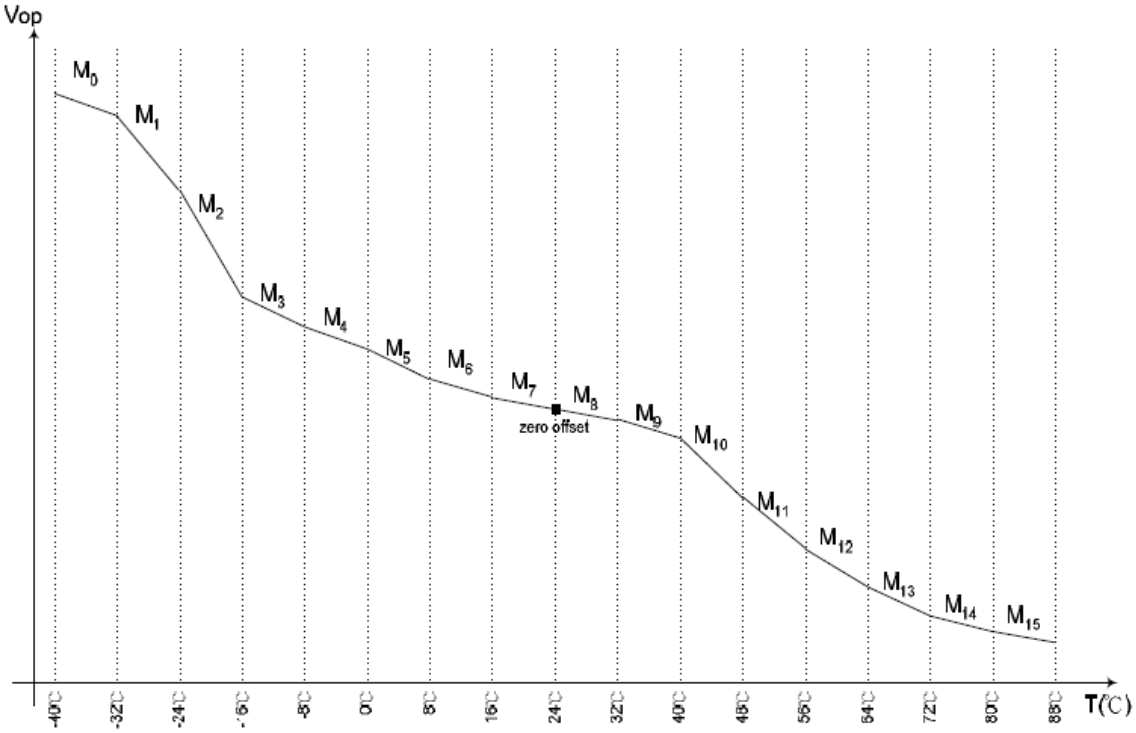


Figure23 TLS8103 LCD temperature compensation curve setting

V0 fine tuning

TLS8103 has 2 commands for fine tuning V0. These commands are VopOfsetInc and VopOfsetDec. When writing VopOfsetInc into IC for each time, V0 would increase 40mV; when writing VopOfsetDec into IC for each time, V0 would decrease 40mV.

Example:
Vop[8:0]=011010010
EV[6:0]=0111111
VopOfsetInc x2
→ V0=3.6 + { 210 + (63-63) } *0.04 + 0.04*2 =12.08 (V)

Voltage Follower Circuits

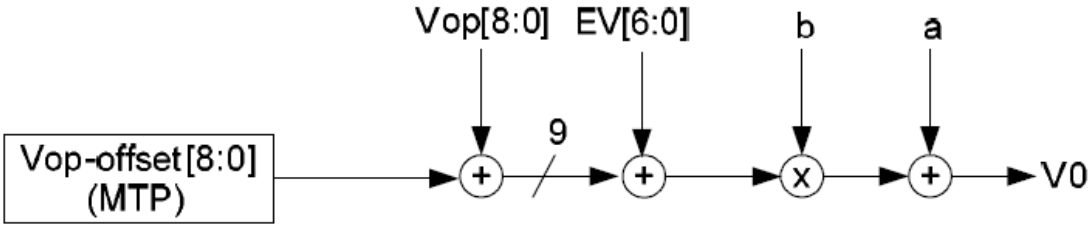
There is a build-in voltage follower circuits in TLS8103 for generating Vg and Vm. These voltages are decided by bias ratio selection circuitry which is set by users with software to control 1/5 to 1/12 bias ratios to match the optimum display performance of LCD panel. Bias driving rule is listed below:

LCD bias	Vg	Vm
1/N bias	(2/N)*V0	(1/N)*V0

N=5~12

MTP Setting Flow

TLS8103 provides the Write and Read function to write the electronic control value and built-in resistance ratio into built-in MTP, and then read them from it. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.



Note1: This setting flow is used for LCM assembler.
Note2: MTP shouldn't be written without preceding loading correctly from MTP in order to avoid some errors during IC operation.
Note3: When writing value to MTP, the voltage of VPP must be more than 7.5V; the current of Ivpp must be more than 4 mA.
Note4: If the MTP is exposed to a high temperature for hours, data in the memory cell may probably be lost before the data retention guarantee period. To retain data in the memory cell, keep the memory cell below 90℃. The data retention guarantee period is specified including the retention period.

Frquency Temperature Gradient Compensation Coefficient

TLS8103 will auto-switch frame rate on different temperature such as Figure 6. TA,TB and TC are frame rate switching temperatures which can be defined by customer with command TMPRNG. FA, FB, FC and FD are switched frame rate which also can be defined by customer with command FRMSEL . The frame rate range is from 37.5Hz to 170Hz.

When the temperature is in increasing state, frame rate changes to the higher step at TA/TB/TC+TH(℃). When the temperature is in decreasing state, frame rate changes to the lower step at TA/TB/TC. For example:

TC=10℃ and TH=5℃, FC switches to FD at 15℃ but FD switches to FC at 10℃. Please take Figure 6 for reference.

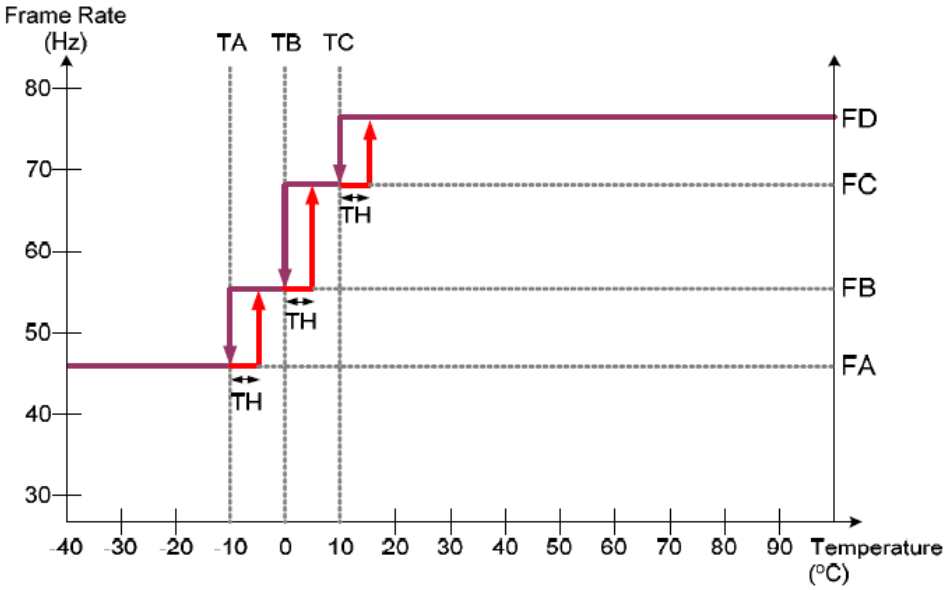


Figure24 TLS8103 LCD auto-adjustment with 4 temperature ranges

COMMAND TABLE

Hex	command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(00H)	NOP	0	1	0	0	0	0	0	0	0	0	0	No operation	1
(01H)	SWRESET	0	1	0	0	0	0	0	0	0	0	1	Software reset	2
(04H)	RDDID	0	1	0	0	0	0	0	0	1	0	0	Read display ID	3
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	ID 17	ID 16	ID 15	ID 14	ID 13	ID 12	ID 11	ID 10	ID1 read (D23-D16)	
		1	0	1	ID 27	ID 26	ID 25	ID 24	ID 23	ID 22	ID 21	ID 20	ID2 read (D15-D8)	
		1	0	1	ID 37	ID 36	ID 35	ID 34	ID 33	ID 32	ID 31	ID 30	ID3 read (D7-D0)	
(09H)	RDDST	0	1	0	0	0	0	0	1	0	0	1	Read display status	4
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	ST 31	ST 30	ST 29	ST 28	ST 27	ST 26	ST 25	ST 24	(D31-D24)	
		1	0	1	ST 23	ST 22	ST 21	ST 20	ST 19	ST 18	ST 17	ST 16	(D23-D16)	
		1	0	1	ST 15	ST 14	ST 13	ST 12	ST 11	ST 10	ST 9	ST 8	(D15-D8)	
		1	0	1	ST 7	ST 6	ST 5	ST 4	ST 3	ST 2	ST 1	ST 0	(D7-D0)	
(0AH)	RDDPM	0	1	0	0	0	0	0	1	0	1	0	Read display power mode	5
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	D7	D6	D5	D4	D3	D2	0	0		
(0BH)	RDDMADCTR	0	1	0	0	0	0	0	1	0	1	1	Read display MADCTR	6
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	D7	D6	D5	D4	D3	0	0	0		
(0CH)	RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	Read display pixel format	7
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	0	0	0	0	0	D2	D1	D0		
(0DH)	RDDIM	0	1	0	0	0	0	0	1	1	0	1	Read display image mode	8
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	D7	0	D5	D4	D3	0	0	0		
(0EH)	RDDSM	0	1	0	0	0	0	0	1	1	1	0	Read display signal mode	9
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	D7	D6	0	0	0	0	0	0		
(10H)	SLPIN	0	1	0	0	0	0	1	0	0	0	0	Sleep in	10
(11H)	SLPOUT	0	1	0	0	0	0	1	0	0	0	1	Sleep out	11
(12H)	PTLON	0	1	0	0	0	0	1	0	0	1	0	Partial mode on	12
(13H)	NORON	0	1	0	0	0	0	1	0	0	1	1	Partial off	13
(20H)	INVOFF	0	1	0	0	0	1	0	0	0	0	0	Display inversion off	14
(21H)	INVON	0	1	0	0	0	1	0	0	0	0	1	Display inversion on	15
(22H)	APOFF	0	1	0	0	0	1	0	0	0	1	0	All pixel off	16
(23H)	APON	0	1	0	0	0	1	0	0	0	1	1	All pixel on	17
(25H)	WRCNTR	0	1	0	0	0	1	0	0	1	0	1	Write contrast	18
		1	1	0	0	EV 6	EV 5	EV 4	EV 3	EV 2	EV 1	EV 0	EV=0 to 127	
(28H)	DISPOFF	0	1	0	0	0	1	0	1	0	0	0	Display off	19
(29H)	DISPON	0	1	0	0	0	1	0	1	0	0	1	Display on	20
(2AH)	CASET	0	1	0	0	0	1	0	1	0	1	0	Column address set	21
		1	1	0	0	XS 6	XS 5	XS 4	XS 3	XS 2	XS 1	XS 0	Column start address (0 to 131)	
		1	1	0	0	XE 6	XE 5	XE 4	XE 3	XE 2	XE 1	XE 0	Column end address (0 to 131)	
(2BH)	RASET	0	1	0	0	0	1	0	1	0	1	1	Row address set	22

		1	1	0	0	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Row start address (0 to 131)	
		1	1	0	0	YE6	YE5	YE4	YE3	YE2	YE1	YE0	Row end address (0 to 131)	
(2CH)	RAMWR	0	1	0	0	0	1	0	1	1	0	0	Memory write operation	23
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to RAM	
(2DH)	RGBSET	0	1	0	0	0	1	0	1	1	0	1	Color set for 256 or 4k color display	24
		1	1	0	-	-	-	R004	R003	R002	R001	R000	Red tone (1st entry)	
		1	1	0	-	-	-	:	:	:	:	:	:	
		1	1	0	-	-	-	R154	R153	R152	R151	R150	Red tone (16th entry)	
		1	1	0	-	-	G005	G004	G003	G002	G001	G000	Green tone (1st entry)	
		1	1	0	-	-	:	:	:	:	:	:	:	
		1	1	0	-	-	G155	G154	G153	G152	G151	GR150	Green tone (16th entry)	
		1	1	0	-	-	-	B004	B003	B002	B001	B000	Blue tone (1st entry)	
		1	1	0	-	-	-	:	:	:	:	:	:	
		1	1	0	-	-	-	B154	B153	B152	B151	B150	Blue tone (16th entry)	
(2EH)	RAMRD	0	1	0	0	0	1	0	1	1	1	0	Memory read	25
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from RAM	
(30H)	PTLAR	0	1	0	0	0	1	1	0	0	0	0	Partial start/end address set	26
		1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	Partial start address (0 to 131)	
		1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	Partial end address (0 to 131)	
(33H)	SCRLAR	0	1	0	0	0	1	1	0	0	1	1	Scroll area set	27
		1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA= 0~132	
		1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA= 0~132	
		1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA= 0~132	
(34H)	TEOFF	0	1	0	0	0	1	1	0	1	0	0	Tearing effect line off	28
(35H)	TEON	0	1	0	0	0	1	1	0	1	0	1	Tearing effect mode set	29
		1	1	0	-	-	-	-	-	-	-	M	"0": mode 1; "1": mode 2	
(36H)	MADCTR	0	1	0	0	0	1	1	0	1	1	0	Memory data access control	30
		1	1	0	MY	MX	MV	-	RGB	-	-	-		
(37H)	VSCSAD	0	1	0	0	0	1	1	0	1	1	1	Scroll start address of SRAM	31
		1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA= 0~131	
(38H)	IDMOFF	0	1	0	0	0	1	1	1	0	0	0	Idle mode off	32
(39H)	IDMON	0	1	0	0	0	1	1	1	0	0	1	Idle mode on	33
(3AH)	COLMOD	0	1	0	0	0	1	1	1	0	1	0	Interface pixel format	34
		1	1	0	-	-	-	-	-	P2	P1	P0	Interface format	
(DAH)	RDID1	0	1	0	1	1	0	1	1	0	1	0	Read ID1	35
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	(D7~D0)	
(DBH)	RDID2	0	1	0	1	1	0	1	1	0	1	1	Read ID2	36
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	(D7~D0)	
(DCH)	RDOD3	0	1	0	1	1	0	1	1	1	0	0	Read ID3	37
		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	(D7~D0)	

(B0H)	DUTYSET	0	1	0	1	0	1	1	0	0	0	0	Display duty setting	38
		1	1	0	DU7	DU6	DU5	DU4	DU3	DU2	DU1	DU0		
(B1H)	FIRSTCOM	0	1	0	1	0	1	1	0	0	0	1	First com. page address	39
		1	1	0	F7	F6	F5	F4	F3	F2	F1	F0		
(B3H)	OSCDIV	0	1	0	1	0	1	1	0	0	1	1	FOSC divider	40
		1	1	0	-	-	-	-	-	-	CLD1	CLD0		
(B5H)	NLINVSET	0	1	0	1	0	1	1	0	1	0	1	N-line control	41
		1	1	0	M	N6	N5	N4	N3	N2	N1	N0		
(B7H)	COMSCANDIR	0	1	0	1	0	1	1	0	1	1	1	Com/Seg scan direction	42
		1	1	0	SMY	SMX	SINV	-	SBGR	-	CSD1	CSD0		
(B8H)	RMWIN	0	1	0	1	0	1	1	1	0	0	0	Read modify in	43
(B9H)	RMWOUT	0	1	0	1	0	1	1	1	0	0	1	Read modify out	44
(C0H)	VOPSET	0	1	0	1	1	0	0	0	0	0	0	Vop setting	45
		1	1	0	VOP7	VOP6	VOP5	VOP4	VOP3	VOP2	VOP1	VOP0		
		1	1	0	-	-	-	-	-	-	-	VOP8		
(C1H)	VOPOFSETINC	0	1	0	1	1	0	0	0	0	0	1	+40mv/step	46
(C2H)	VOPOFSETDEC	0	1	0	1	1	0	0	0	0	1	0	-40mv/step	47
(C3H)	BIASSEL	0	1	0	1	1	0	0	0	0	1	1	Bias selection	48
		1	1	0	-	-	-	-	-	BIAS2	BIAS1	BIAS0		
(C4H)	BSTBMPXSEL	0	1	0	1	1	0	0	0	1	0	0	Booster setting	49
		1	1	0	-	-	-	-	-	BST2	BST1	BST0		
(C5H)	BSTEFFSEL	0	1	0	1	1	0	0	0	1	0	1	Booster efficiency selection	50
		1	1	0	-	-	-	-	-	-	BFT1	BFT0		
(C7H)	VOPOFFSET	0	1	0	1	1	0	0	0	1	1	1	Vop offset fuse bit adjust	51
		1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0		
(D7H)	MTPERS	0	1	0	1	1	0	1	0	1	1	1	MTP erase control	52
		1	1	0	-	-	ERS	0	0	0	0	0		
(E0H)	MTPPROG	0	1	0	1	1	1	0	0	0	0	0	MTP program control	53
(E1H)	MTPPROGE	0	1	0	1	1	1	0	0	0	0	1	MTP program end	54
(E2H)	MTPPROGS	0	1	0	1	1	1	0	0	0	1	0	MTP program start	55
(E4H)	MTPPROGA	0	1	0	1	1	1	0	0	0	1	0	MTP program address	56
		1	1	0	-	-	-	-	-	-	0	0	Always “00”	
(F0H)	FRMSEL	0	1	0	1	1	1	1	0	0	0	0	Frame Freq. in Temp. range A, B, C and D	57
		1	1	0	-	-	-	FA4	FA3	FA2	FA1	-		
		1	1	0	-	-	-	FB4	FB3	FB2	FB1	-		
		1	1	0	-	-	-	FC4	FC3	FC2	FC1	-		
		1	1	0	-	-	-	FD4	FD3	FD2	FD1	-		
(F2H)	TMPRNG	0	1	0	1	1	1	1	0	0	1	0	Delimitation point of Temp. ranges of A, B, C	58
		1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0		
		1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0		
		1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0		
(F3H)	TMPHYS	0	1	0	1	1	1	1	0	0	1	1	Hysteretic value set	59
		1	1	0					TH3	TH2	TH1	TH0		

(F4H)	TMPCOE	0	1	0	1	1	1	1	1	1	1	0	Temp. compensation curve coefficients	60
		1	1	0	MT 13	MT 12	MT 11	MT 10	MT 03	MT 02	MT 01	MT 00		
		1	1	0	MT 33	MT 32	MT 31	MT 30	MT 23	MT 22	MT 21	MT 20		
		1	1	0	MT 53	MT 52	MT 51	MT 50	MT 43	MT 42	MT 41	MT 40		
		1	1	0	MT 73	MT 72	MT 71	MT 70	MT 63	MT 62	MT 61	MT 60		
		1	1	0	MT 93	MT 92	MT 91	MT 90	MT 83	MT 82	MT 81	MT 80		
		1	1	0	MT 113	MT 112	MT 111	MT 110	MT 103	MT 102	MT 101	MT 100		
		1	1	0	MT 133	MT 132	MT 131	MT 130	MT 123	MT 122	MT 121	MT 120		
		1	1	0	MT 153	MT 152	MT 151	MT 150	MT 143	MT 142	MT 141	MT 140		
(FBH)	CLUTR	0	1	0	1	1	1	1	1	0	1	1	CLUT for panel red color gamma correction	61
		1	1	0	-	R 006	R 005	R 004	R 003	R 002	R 001	R 000	Red tone (1st entry)	
		1	1	0	-	:	:	:	:	:	:	:	:	
		1	1	0	-	R 316	R 315	R 314	R 313	R 312	R 311	R 310	Red tone (32th entry)	
(FCH)	CLUTG	0	1	0	1	1	1	1	1	0	1	1	CLUT for panel green color gamma correction	62
		1	1	0	-	G 006	G 005	G 004	G 003	G 002	G 001	G 000	Green tone (1st entry)	
		1	1	0	-	:	:	:	:	:	:	:	:	
		1	1	0	-	G 636	G 635	G 634	G 633	G 632	G 631	G 630	Green tone (64th entry)	
(FDH)	CLUTB	0	1	0	1	1	1	1	1	0	1	1	CLUT for panel blue color gamma correction	63
		1	1	0	-	B 006	B 005	B 004	B 003	B 002	B 001	B 000	Blue tone (1st entry)	
		1	1	0	-	:	:	:	:	:	:	:	:	
		1	1	0	-	B 316	B 315	B 314	B 313	B 312	B 311	B 310	Blue tone (32th entry)	

COMMAND DESCRIPTION

1. NOP (00H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	0	1	0	0	0	0	0	0	0	0	0	00H
parameter	No parameter											
description	This command is an empty command. It does not have effect on the display module. However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write) or RAMRD (Memory Read) and parameter write command.											
restriction	-											
default	Status						Default value					
	Power on sequence						N/A					
	S/W reset						N/A					
	H/W reset						N/A					

2. SWRESET : Software Reset (01H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SWRESET	0	1	0	0	0	0	0	0	0	0	1	01H
parameter	No parameter											
description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameter to their S/W Reset default values and all segment & common output are set to Vm (display off: blank display). Note: the Frame Memory contents are not affected by this command.											
restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during 5msec. If Software Reset is applied during Sleep out mode, it will be necessary to wait 120msec before sending Sleep Out command.											
default	status						Default value					
	Power on sequence						N/A					
	S/W reset						N/A					
	H/W reset						N/A					

3. RDDID : Read Display ID (04H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDID	0	1	0	0	0	0	0	0	1	0	0	04H
Dummy read	1	0	1	-	-	-	-	-	-	-	-	
2nd parameter	1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
3rd parameter	1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
4th parameter	1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
description	This read byte returns 24-bit display identification information. The 1st parameter is dummy data; The 2nd parameter (ID17-ID10): LCD module's manufacturer ID; The 3rd parameter (ID26-ID20): LCD module/driver version ID; The 4th parameter (ID37-ID30): LCD module/driver ID.											
restriction	-											
default	status						Default value					
							ID1		ID2		ID3	
	Power on sequence						55H		80H		00H	
	S/W reset						55H		80H		00H	
	H/W reset						55H		80H		00H	

NOTE: "-" don't care

4. RDDST : Read Display Status (09H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDST	0	1	0	0	0	0	0	1	0	0	1	09H
Dummy read	1	0	1	-	-	-	-	-	-	-	-	
2nd parameter	1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	
3rd parameter	1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	
4th parameter	1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	
5th parameter	1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	

description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on, "0"=Booster Off
ST30	Row Address Order	"1"=Decrement, "0"=Increment
ST29	Column Address Order	"1"=Decrement, "0"=Increment
ST28	Row/Column Order (MV)	"1"=Row/Column exchange (MV=1) "0"=Normal (MV=0)
ST27	Scan Address Order	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order	"1"=BGR, "0"=RGB
ST25	Not Used	"0"
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22 ST21 ST20	Interface Color Pixel Format Definition	"010" = 8-bit/pixel "011" = 12-bit/pixel type A "101" = 16-bit/pixel "110" = 12-bit/pixel type B
ST19	Idle Mode On/Off	"1" = On, "0' = Off
ST18	Partial Mode On/Off	"1" = On, "0' = Off
ST17	Sleep In/Out	"1" = In, "0" = Out
ST16	Display Normal Mode On/Off	"1"=Partial Display, "0"=Normal display
ST15	Vertical Scrolling Status	"1" = Scroll On, '0" = Scroll Off
ST14	Not Used	"0"
ST13	Inversion Status	"1" = On, "0" = Off
ST12	All Pixel On	"1" = Mode On, "0" = Mode Off
ST11	All Pixel Off	"1" = Mode On, "0" = Mode Off
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing Effect Line On/Off	"1" = On, "0" = Off
ST8	Not Used	"0"
ST7	Not Used	"0"
ST6	Not Used	"0"
ST5	Tearing Effect Line Mode	"0" = Mode 1, "1" = Mode 2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"
ST1	Not Used	"0"
ST0	Not Used	"0"

restriction: -

default

status	Default value
Power on sequence	0000_0000_0101_0001_0000_0000_0000
S/W reset	0xxx_xx00_0xxx_0001_0000_0000_0000
H/W reset	0000_0000_0101_0001_0000_0000_0000

NOTE: "-" don't care

5. RDDPM : Read Display Power mode (0AH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDPM	0	1	0	0	0	0	0	1	0	1	0	0AH
Dummy read	1	0	1	-	-	-	-	-	-	-	-	
2nd parameter	1	0	1	D7	D6	D5	D4	D3	D2	0	0	
description	This command indicates the current status of the display as described in the table below:											

Bit	Description	Value
D7	Booster Voltage Status	"1"=Booster On, "0"=Booster Off
D6	Idle Mode On/Off	"1"=Idle Mode On, "0"=Idle Mode Off
D5	Partial Mode On/Off	"1"= Partial Mode On, "0"=Partial Mode Off
D4	Sleep In/Out	"1"=Sleep Out, "0"=Sleep In
D3	Display Normal Mode On/Off	"1"=Normal Display, "0"=Partial Display
D2	Display On/Off	"1"=Display On, "0"=Display Off

restriction	-	
default	status	Default value (D[7:2])
	Power on sequence	08H
	S/W reset	08H
	H/W reset	08H

NOTE: "-" don't care

6. RDDMDCTR : Read Display MADCTR (0BH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDMADCTR	0	1	0	0	0	0	0	1	0	1	1	0BH
Dummy read	1	0	1	-	-	-	-	-	-	-	-	
2nd parameter	1	0	1	D7	D6	D5	D4	D3	0	0	0	
description	This command indicates the current status of the display as described in the table below:											

Bit	Description	Value
D7	Row Address Order	"1"=Decrement, "0"=Increment
D6	Column Address Order	"1"=Decrement, "0"=Increment
D5	Row/Column Order (MV)	"1"=Row/Column exchange (MV=1) "0"=Normal (MV=0)
D4	Scan Address Order	"1"=Decrement, "0"=Increment
D3	RGB/BGR Order	"1"=BGR, "0"=RGB

restriction	-	
default	Status	Default value (D[7:3])
	Power on sequence	00H
	S/W reset	Not Change
	H/W reset	00H

NOTE: "-" don't care

7. RDDCOLMOD : Read Display Pixel Format (0CH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	0CH
Dummy read	1	0	1	-	-	-	-	-	-	-	-	
2nd parameter	1	0	1	0	0	0	0	0	D2	D1	D0	
description	This command indicates the current status of the display as described in the table below:											

Bit	Description	Value

	D2 D1 D0	Interface Color Pixel Format Definition	“010” = 8-bit/pixel “011” = 12-bit/pixel type A “101” = 16-bit/pixel “110” = 12-bit/pixel type B
restriction	-		
default	status	Default value	
	Power on sequence	16-bit/pixel	
	S/W reset	Not Change	
	H/W reset	16-bit/pixel	

NOTE: “-“ don’t care

8. RDDIM : Read Display Image Mode (0DH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDIM	0	1	0	0	0	0	0	1	1	0	1	0DH
Dummy read	1	0	1	-	-	-	-	-	-	-	-	
2nd parameter	1	0	1	D7	0	D5	D4	D3	0	0	0	
description	This command indicates the current status of the display as described in the table below: Bit / Description / Value D7 / Vertical Scrolling Status / “1” = Scroll On, ‘0” = Scroll Off D5 / Inversion Status / “1” = On, “0” = Off D4 / All Pixel On / “1” = Mode On, “0” = Mode Off D3 / All Pixel Off / “1” = Mode On, “0” = Mode Off											
restriction	-											
default	status	Default value										
	Power on sequence	00H										
	S/W reset	00H										
	H/W reset	00H										

NOTE: “-“ don’t care

9. RDDSM : Read Display Signal Mode (0EH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDSM	0	1	0	0	0	0	0	1	1	1	0	0EH
Dummy read	1	0	1	-	-	-	-	-	-	-	-	
2nd parameter	1	0	1	D7	D6	0	0	0	0	0	0	
description	This command indicates the current status of the display as described in the table below: Bit / Description / Value D7 / Tearing Effect Line On/Off / “1” = On, “0” = Off D6 / Tearing Effect Line Mode / “0” = Mode 1, “1” = Mode 2											
restriction	-											
default	status	Default value (D[7:6])										
	Power on sequence	00H										
	S/W reset	00H										
	H/W reset	00H										

NOTE: “-“ don’t care

10. SLPIN: Sleep In (10H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPIN	0	1	0	0	0	0	1	0	0	0	0	10H
parameter	No parameter											
description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. MCU interface and memory are still working and the memory keeps its contents.											
restriction	This command has no effect when module is already in sleep in mode. Sleep In mode can only be exit by the Sleep Out command. It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent. If internal VDD regulator is enable by PIN VDD_EN=H, when power on sequence or S/W reset or H/W reset, the chip is on the sleep in mode and the internal VDD regulator is work, and external MCU can access internal command register and SRAM freely; When the command SLPIN cause the chip into the sleep in mode, the internal VDD regulator is disable to reduce chip power consumption, and only internal command registers can be set but the SRAM access is unavailable.											
default	status						Default value					
	Power on sequence						Sleep in mode					
	S/W reset						Sleep in mode					
	H/W reset						Sleep in mode					

11. SLPOUT: Sleep Out (11H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPOUT	0	1	0	0	0	0	1	0	0	0	1	11H
parameter	No parameter											
description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, internal display oscillator is started. In this mode internal VDD regulator is enable and MCU can access internal command registers and internal SRAM.											
restriction	This command has no effect when module is already in sleep out mode. Sleep Out mode can only be exit by the Sleep In command. It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out Mode) before Sleep Out command can be sent.											
default	status						Default value					
	Power on sequence						Sleep in mode					
	S/W reset						Sleep in mode					
	H/W reset						Sleep in mode					

12. PTLON: Partial Display Mode On (12H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTLON	0	1	0	0	0	0	1	0	0	1	0	12H
parameter	No parameter											
description	This command turns on Partial display mode. The Partial display mode window is described by the Partial Area command. Exit from PTLON by Partial Off command.											

	There is no abnormal visual effect during mode change between Partial Off – Partial On.	
restriction	This command has no effect when Partial mode is active.	
default	status	Default value
	Power on sequence	Partial mode off
	S/W reset	Partial mode off
	H/W reset	Partial mode off

13. NORON: Partial Off (13H)

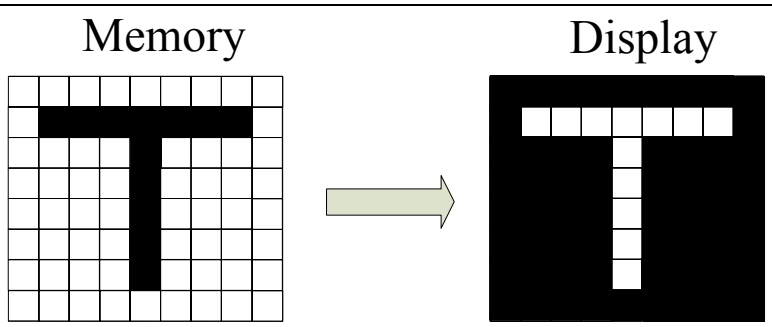
Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NORON	0	1	0	0	0	0	1	0	0	1	1	13H
parameter	No parameter											
description	This command returns the display to normal mode, normal display mode on means Partial mode off, scroll mode off. Exit from NORON by the Partial mode on command (12H).											
restriction	This command has no effect when Partial Off mode is active.											
default	status						Default value					
	Power on sequence						Partial mode off					
	S/W reset						Partial mode off					
	H/W reset						Partial mode off					

14. INVOFF: Display Inversion Off (20H)

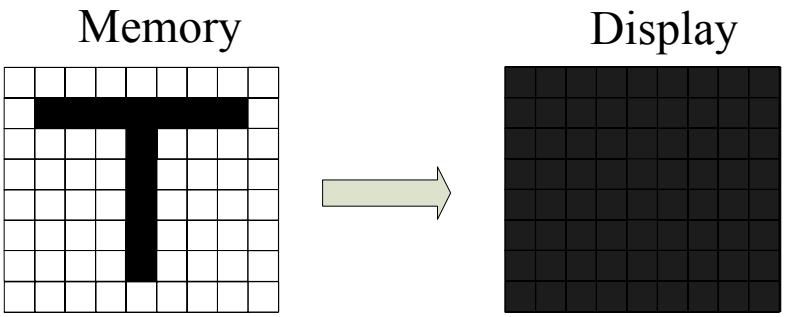
Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVOFF	0	1	0	0	0	1	0	0	0	0	0	20H
parameter	No parameter											
description	This command is used to recover from display inversion mode. This command makes no change of contents of the frame memory. This command does not change any other status.											
restriction	This command has no effect when module is already Inversion Off mode.											
default	status						Default value					
	Power on sequence						Display Inversion Off					
	S/W reset						Display Inversion Off					
	H/W reset						Display Inversion Off					

15. INVON: Display Inversion On (21H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVOFN	0	1	0	0	0	1	0	0	0	0	1	21H
parameter	No parameter											
description	This command is used to enter into display inversion mode. This command makes no change of contents of the frame memory. This command does not change any other status. To exit from display inversion on, the display inversion off command should be written. Example											

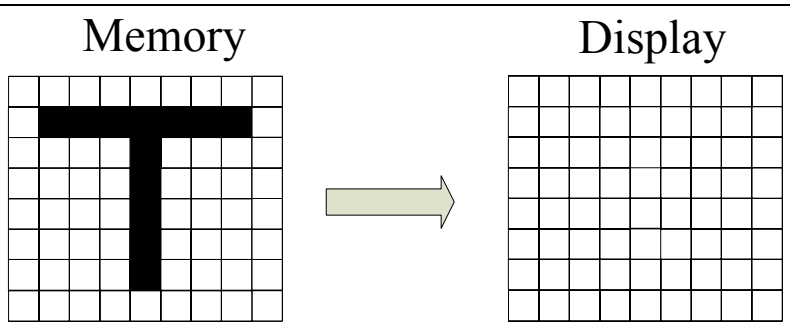
		
restriction	This command has no effect when module is already Inversion On mode.	
default	status	Default value
	Power on sequence	Display Inversion Off
	S/W reset	Display Inversion Off
	H/W reset	Display Inversion Off

16. APOFF: All Pixels Off (22H) (Only for test purpose)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
APOFF	0	1	0	0	0	1	0	0	0	1	0	22H
parameter	No parameter											
description	This command is only used for test purpose. Example 											
restriction	This command has no effect when module is already All Pixels Off mode.											
default	status	Default value										
	Power on sequence	All Pixels Off mode disable										
	S/W reset	All Pixels Off mode disable										
	H/W reset	All Pixels Off mode disable										

17. APON: All Pixels On (23H) (Only for test purpose)

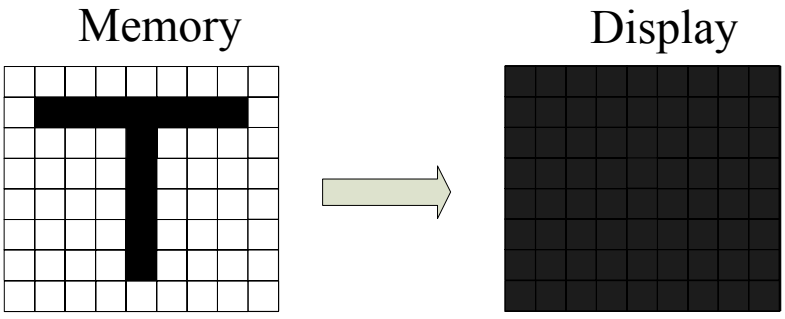
Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
APON	0	1	0	0	0	1	0	0	0	1	1	23H
parameter	No parameter											
description	This command is only used for test purpose. Example											

		
restriction	This command has no effect when module is already All Pixels On mode.	
default	status	Default value
	Power on sequence	All Pixels On mode disable
	S/W reset	All Pixels On mode disable
	H/W reset	All Pixels On mode disable

18. WRCNTR: Write Contrast (25H)

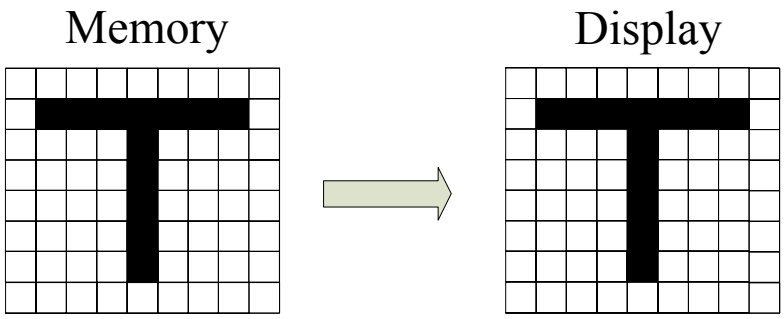
Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRCNTR	0	1	0	0	0	1	0	0	1	0	1	25H
Parameter	1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	-
description	This command is used to fine turning the contrast of the display. Parameter range is 00H-7FH. The contrast is not liner but the contrast adjustment is liner. Luminance is increasing from 00H to 7FH. 00H is presenting dark end and 7FH is presenting bright end.											
restriction	-											
default	status						Default value					
	Power on sequence						3FH					
	S/W reset						3FH					
	H/W reset						3FH					

19. DISPOFF: Display Off (28H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPOFF	0	1	0	0	0	1	0	1	0	0	0	28H
Parameter	No parameter											
description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory disables and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. Exit from this command by Display On. Example 											
restriction	-											

default	status	Default value
	Power on sequence	Display Off
	S/W reset	Display Off
	H/W reset	Display Off

20. DISPON: Display On (29H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPON	0	1	0	0	0	1	0	1	0	0	1	29H
Parameter	No parameter											
description	Turn on the display screen according to the current display data RAM content and the display timing and setting. This command is used to recover from DISPLAY OFF mode. Output from the frame memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. Example 											
restriction	This command has no effect when module is already in Display On mode.											

default	Status	Default value
	Power on sequence	Display Off
	S/W reset	Display Off
	H/W reset	Display Off

21. CASET: Column Address Set (2AH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CASET	0	1	0	0	0	1	0	1	0	1	0	2AH
1st Parameter	1	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
2nd Parameter	1	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other drive status. The value of XS[7:0] and XE[7:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.											
restriction	XS[7:0] always must be equal to less than XE[7:0] When XS[7:0] or XE[7:0] is greater than 83H (when MV=0) or 83H (when MV=1),data of out of range will be ignored. Parameter range: 0 <= XS[7:0] <= XE[7:0] <= 131											

default	Status	Default value	
		XS[7:0]	XE[7:0]
	Power on sequence	00H	83H
	S/W reset	00H	83H
	H/W reset	00H	83H

22. RASET: Row Address Set (2BH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RASET	0	1	0	0	0	1	0	1	0	1	1	2BH
1st Parameter	1	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
2nd Parameter	1	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other drive status. The value of YS[7:0] and YE[7:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.											
restriction	YS[7:0] always must be equal to less than YE[7:0] When YS[7:0] or YE[7:0] is greater than 83H (when MV=0) or 83H (when MV=1),data of out of range will be ignored. Parameter range: 0 <= YS[7:0] <= YE[7:0] <= 131											
default	Status						Default value					
							YS[7:0]				YE[7:0]	
	Power on sequence						00H				83H	
	S/W reset						00H				83H	
	H/W reset						00H				83H	

23. RAMWR: Memory Write (2CH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RAMWR	0	1	0	0	0	1	0	1	1	0	0	2CH
Write D1[7:0]	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
…	1	1	0	…	…	…	…	…	…	…	…	
Write Dn[7:0]	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
description	This command is used to transfer data MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the start Column/Start Row address. Frame Write can be canceled by sending any other command.											
restriction	In all color modes. There is no restriction on length of parameters.											
default	Status						Default value					
	Power on sequence						Contents of memory is set randomly					
	S/W reset						Contents of memory is remained					
	H/W reset						Contents of memory is remained					

24. RGBSET: Color Set For 256-color Display (2DH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGBSET	0	1	0	0	0	1	0	1	1	0	1	2DH
1st parameter	1	1	0	-	-	-	R004	R003	R002	R001	R000	
…	1	1	0	-	-	-	:	:	:	:	:	
16th parameter	1	1	0	-	-	-	R154	R153	R152	R151	R150	
17th parameter	1	1	0	-	-	G005	G004	G003	G002	G001	G000	
…	1	1	0	-	-	:	:	:	:	:	:	
32th parameter	1	1	0	-	-	G155	G154	G153	G152	G151	G150	
33th parameter	1	1	0	-	-	-	B004	B003	B002	B001	B000	
…	1	1	0	-	-	-	:	:	:	:	:	
48th parameter	1	1	0	-	-	-	B154	B153	B152	B151	B150	
description	This command is used to define the LUT for 8bit-to-16bit / 12bit-to-16bit color depth conversions. 48 bytes must be written to the LUT regardless of the color mode.											

R input (3bits) 256 colors 8 bit/pixel mode	R input (4bits) 4096 colors 12 bit/pixel mode	R output (5bits) 65,536 colors 16 bit/pixel mode	RGBSET Parameter
000	0000	R004 R003 R002 R001 R000	1
001	0001	R014 R013 R012 R011 R010	2
010	0010	R024 R023 R022 R021 R020	3
011	0011	R034 R033 R032 R031 R030	4
100	0100	R044 R043 R042 R041 R040	5
101	0101	R054 R053 R052 R051 R050	6
110	0110	R064 R063 R062 R061 R060	7
111	0111	R074 R073 R072 R071 R070	8
	1000	R084 R083 R082 R081 R080	9
	1001	R094 R093 R092 R091 R090	10
	1010	R104 R103 R102 R101 R100	11
	1011	R114 R113 R112 R111 R110	12
	1100	R124 R123 R122 R121 R120	13
	1101	R134 R133 R132 R131 R130	14
	1110	R144 R143 R142 R141 R140	15
	1111	R154 R153 R152 R151 R150	16
G input (3bits) 256 colors 8 bit/pixel mode	G input (4bits) 4096 colors 12 bit/pixel mode	G output (6bits) 65,536 colors 16 bit/pixel mode	
000	0000	G005G004 G003 G002 G001 G000	17
001	0001	G015G014 G013 G012 G011 G010	18
010	0010	G025G024 G023 G022 G021 G020	19
011	0011	G035G034 G033 G032 G031 G030	20
100	0100	G045G044 G043 G042 G041 G040	21
101	0101	G055G054 G053 G052 G051 G050	22
110	0110	G065G064 G063 G062 G061 G060	23
111	0111	G075G074 G073 G072 G071 G070	24
	1000	G085G084 G083 G082 G081 G080	25
	1001	G095G094 G093 G092 G091 G090	26
	1010	G105G104 G103 G102 G101 G100	27
	1011	G115G114 G113 G112 G111 G110	28
	1100	G125G124 G123 G122 G121 G120	29
	1101	G135G134 G133 G132 G131 G130	30
	1110	G145G144 G143 G142 G141 G140	31
	1111	G155G154 G153 G152 G151 G150	32
B input (3bits) 256 colors 8 bit/pixel mode	B input (4bits) 4096 colors 12 bit/pixel mode	B output (5bits) 65,536 colors 16 bit/pixel mode	
000	0000	B004 B003 B002 B001 B000	33
001	0001	B014 B013 B012 B011 B010	34
010	0010	B024 B023 B022 B021 B020	35
011	0011	B034 B033 B032 B031 B030	36
100	0100	B044 B043 B042 B041 B040	37
101	0101	B054 B053 B052 B051 B050	38
110	0110	B064 B063 B062 B061 B060	39
111	0111	B074 B073 B072 B071 B070	40
	1000	B084 B083 B082 B081 B080	41
	1001	B094 B093 B092 B091 B090	42
	1010	B104 B103 B102 B101 B100	43
	1011	B114 B113 B112 B111 B110	44
	1100	B124 B123 B122 B121 B120	45
	1101	B134 B133 B132 B131 B130	46
	1110	B144 B143 B142 B141 B140	47
	1111	B154 B153 B152 B151 B150	48

restriction	-	
default	Status	Default value
	Power on sequence	Random values
	S/W reset	Not change
	H/W reset	Random values

25. RAMRD: Memory Read (2EH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RAMRD	0	1	0	0	0	1	0	1	1	1	0	2EH
1st parameter	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0	
2nd parameter	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0	
…	1	0	1	…	…	…	…	…	…	…	…	
(N+1)th parameter	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0	
description	This command is used to transfer data from frame memory to MCU. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the start Column/Start Row address. Frame Read can be canceled by sending any other command.											
restriction	In all color modes, the Frame Read is always 16bit so there is no restriction on length of parameter. Note: Memory Read is only possible via the Parallel Interface.											
default	Status						Default value					
	Power on sequence						Contents of memory is set randomly					
	S/W reset						Contents of memory is remained					
	H/W reset						Contents of memory is remained					

26. PTLAR: Partial Area (30H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTLAR	0	1	0	0	0	1	1	0	0	0	0	30H
1st parameter	1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	
2nd parameter	1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	
description	This command defines the partial mode's display area. There are two parameters associated with the command, the first defines the Start Line (PS) and the second the End Line (PE). PS and PE refer to the Frame Memory Line counter.											
restriction	PS and PE are based on line unit.											
default	Status						Default value					
							PS[7:0]				PE[7:0]	
	Power on sequence						00H				83H	
	S/W reset						00H				83H	
	H/W reset						00H				83H	

27. SCRLAR: Scroll Area (33H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SCRLAR	0	1	0	0	0	1	1	0	0	1	1	33H
1st parameter	1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	
2nd parameter	1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
3rd parameter	1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	
description	This command just defines the Vertical Scrolling Area of the display and not performances vertical scroll.											

	The 1st parameter TFA[7:0] describes the TOP Fixed Area (in No. of lines from Top of the Frame Memory and display). The 2nd parameter VSA[7:0] describes the height of the vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) the first line appears immediately after the bottom most line of the Top Fixed Area. The 3rd parameter BFA[7:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).			
restriction	The condition is (TFA + VSA + BFA) = 132, otherwise Scroll mode is undefined.			
default	Status	Default value		
		TFA[7:0]	VSA[7:0]	BFA[7:0]
	Power on sequence	00H	84H	00H
	S/W reset	00H	84H	00H
	H/W reset	00H	84H	00H

28. TEOFF: Tearing Effect Line Off (34H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEOFF	0	1	0	0	0	1	1	0	1	0	0	34H
Parameter	No parameter											
description	This command is used to turn off (Active Low) the Tearing Effect output signal from the TE signal line.											
restriction	This command has no effect when Tearing Effect output is already OFF.											
default	status						Default value					
	Power on sequence						Tearing effect Off					
	S/W reset						Tearing effect Off					
	H/W reset						Tearing effect Off					

29. TEON: Tearing Effect Line On (35H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEON	0	1	0	0	0	1	1	0	1	0	1	35H
Parameter	1	1	0	-	-	-	-	-	-	-	M	-
description	This command is used to turn on the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTR bit. When M=0: The Tearing Effect Output Line consists of V-Blanking information only:  When M=1: The Tearing Effect Output Line consists of both V-Blanking information.  											
restriction	This command has no effect when Tearing Effect output is already OFF.											
default	status						Default value					
	Power on sequence						Tearing effect Off & M=0					
	S/W reset						Tearing effect Off & M=0					
	H/W reset						Tearing effect Off & M=0					

30. MADCTR: Memory Data Access Control (36H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MADCTR	0	1	0	0	0	1	1	0	1	1	0	36H
Parameter	1	1	0	MY	MX	MV	-	RGB	-	-	-	-

description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit Assignment

Bit	Name	Description
MY	Row Address Order	These 3bits controls MCU to memory write/read direction
MX	Column Address Order	
MV	Row/Column Address Order	
RGB	RGB – BGR Order	Color selector switch control The content of the Frame Memory are

restriction: -

default

status	Default value
Power on sequence	MY=0, MX=0, MV=0, RGB=0
S/W reset	Not changed
H/W reset	MY=0, MX=0, MV=0, RGB=0

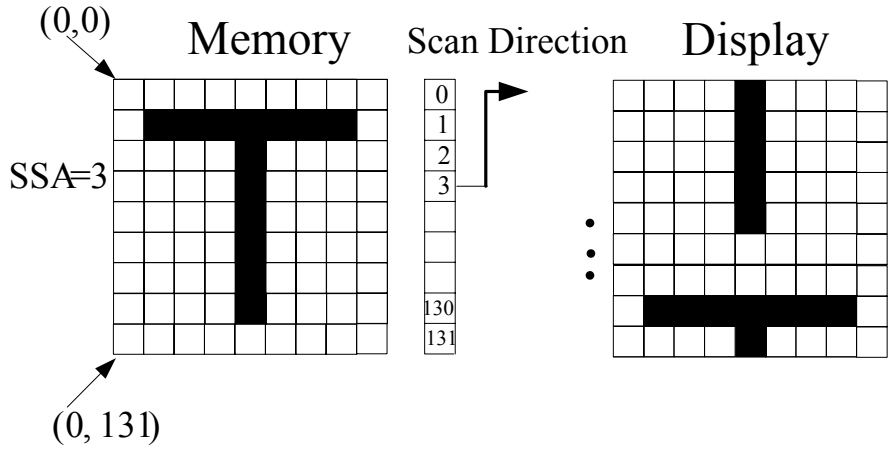
31. VSCSAD: Vertical Scroll Start Address of RAM (37H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VSCSAD	0	1	0	0	0	1	1	0	1	1	1	37H
Parameter	1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	-

description

This command is used together with Vertical Scrolling Definition (33H). These two commands describe the scrolling area and scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last of the Top Fixed Area on the display as illustrated below:
This command start scrolling.
Exit from Vertical Scrolling mode by commands Partial On (12H) or Partial Off (13H).

Example: when Top Fixed Area = Bottom Fixed Area = 00H, Vertical Scrolling Area = 132 and Vertical Scrolling Pointer SSA=3.



restriction: Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33H) otherwise undesirable image will be displayed on the panel.

default

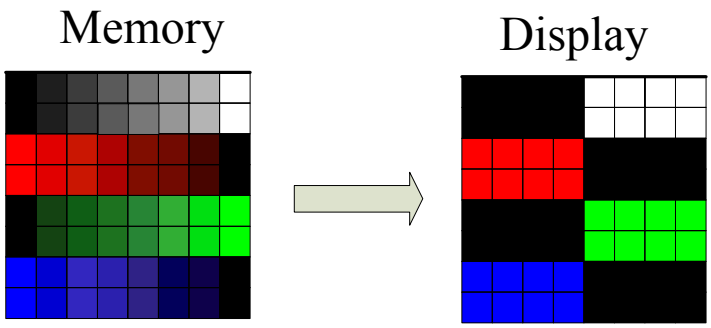
status	Default value

	Power on sequence	00H
	S/W reset	00H
	H/W reset	00H

32. IDMOFF: Idle Mode Off (38H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMOFF	0	1	0	0	0	1	1	1	0	0	0	38H
Parameter	No Parameter											
description	This command is used to recover from idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle off mode: 1. LCD can display maximum 65536 colors. 2. Normal frame frequency is applied.											
restriction	This command has no effect when module is already in idle off mode.											
default	status						Default value					
	Power on sequence						Idle mode off					
	S/W reset						Idle mode off					
	H/W reset						Idle mode off					

33. IDMON: Idle Mode On (39H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
IDMON	0	1	0	0	0	1	1	1	0	0	1	39H
Parameter	No Parameter											
description	This command is used to enter into idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle on mode: 1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the frame memory, 8 color depth data is displayed. 2. 8-color mode frame frequency is applied. 3. Exit from IDMON by idle off mode (38H) command. 											
restriction	This command has no effect when module is already in idle off mode.											
default	status						Default value					
	Power on sequence						Idle mode off					
	S/W reset						Idle mode off					
	H/W reset						Idle mode off					

34. COLMOD: Interface Pixel Format (3AH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
COLMOD	0	1	0	0	0	1	1	1	0	1	0	3AH
Parameter	1	1	0	-	-	-	-	-	P2	P1	P0	
description	This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:											

Interface format	P2	P1	P0
Not defined	0	0	0
Not defined	0	0	1
8-Bit/Pixel	0	1	0
12-Bit/Pixel (Type **A**)	0	1	1
12-Bit/Pixel (Type **B**)	1	0	0
16-Bit/Pixel	1	0	1
18-Bit/Pixel	1	1	0
24-Bit/Pixel	1	1	1

restriction	There is no visible effect until the Frame Memory is written to.	
default	status	Default value
	Power on sequence	05H (16-Bit/Pixel)
	S/W reset	Not change
	H/W reset	05H (16-Bit/Pixel)

35. RDID1: Read ID1 Value (DAH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID1	0	1	0	1	1	0	1	1	0	1	0	DAH
Dummy read	1	1	0	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
description	This read byte returns 8-bit LCD module's manufacturer ID.											
restriction	-											
default	status						Default value					
	Power on sequence						55H					
	S/W reset						55H					
	H/W reset						55H					

36. RDID2: Read ID2 Value (DBH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID1	0	1	0	1	1	0	1	1	0	1	1	DBH
Dummy read	1	1	0	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
description	This read byte returns 8-bit LCD module/driver ID.											
restriction	-											
default	status						Default value					
	Power on sequence						80H					
	S/W reset						80H					
	H/W reset						80H					

37. RDID3: Read ID3 Value (DCH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID1	0	1	0	1	1	0	1	1	1	0	0	DCH
Dummy read	1	1	0	-	-	-	-	-	-	-	-	-
2nd parameter	1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-
description	This read byte returns 8-bit LCD module/driver ID.											
restriction	-											
default	status						Default value					
	Power on sequence						00H					
	S/W reset						00H					
	H/W reset						00H					

38. DUTYSET: Display Duty Setting (B0H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DUTYSET	0	1	0	1	0	1	1	0	0	0	0	B0H
Parameter	1	1	0	DU7	DU6	DU5	DU4	DU3	DU2	DU1	DU0	-
description	This command is used to set display duty, command set = display duty – 1.											
restriction	Display duty must > 4 (1/4 duty)											
default	Status						Default value					
	Power on sequence						83H					
	S/W reset						83H					
	H/W reset						83H					

39. FIRSTCOM: First Com. Page address (B1H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DUTYSET	0	1	0	1	0	1	1	0	0	0	1	B1H
Parameter	1	1	0	F7	F6	F5	F4	F3	F2	F1	F0	-
description	This command defines the first output COM number that mapping to the RAM page address 0.											
restriction	-											
default	Status						Default value					
	Power on sequence						00H					
	S/W reset						00H					
	H/W reset						00H					

40. OSCDIV: FOSC Divider (B3H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
OSCDIV	0	1	0	1	0	1	1	0	0	1	1	B3H
Parameter	1	1	0	-	-	-	-	-	-	CLD1	CLD0	-
description	This command is used to specify the CL dividing ratio. CLD1 CLD0: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.											

CLD1	CLD0	CL dividing ratio
0	0	Not divide
0	1	2 divisions
1	0	4 division
1	1	8 division

restriction	-	
default	Status	Default value
	Power on sequence	00b

	S/W reset	00b
	H/W reset	00b

41. NLINVSET: N-Line control (B5H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NLINVSET	0	1	0	1	0	1	1	0	1	0	1	B5H
Parameter	1	1	0	M	N6	N5	N4	N3	N2	N1	N0	-
description	This command is used to set the inverted line number with range of 2 to 128 to improve display quality. When M=0, inversion occurs in every frame; when M=1, inversion is independent from frame. If N[6:0]=0, N-Line inversion function is disable. Line inversion numbers = N[6:0] +1;											
restriction	-											
default	Status						Default value					
	Power on sequence						80H					
	S/W reset						80H					
	H/W reset						80H					

42. COMSCANDIR: Com/Seg Scan Direction for glass layout (B7H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
COMSCANDIR	0	1	0	1	0	1	1	0	1	1	1	B7H
Parameter	1	1	0	SMY	SMX	SINV	SML	SBGR	-	CSD1	CSD0	-
description	This command is used to specify the common output direction in the pin of CSEL=L. this command helps to improve Common ITO layout tolerance on the LCM. When CSEL=L configuration is selected, pins and common outputs are scanned in the order shown below.											
restriction	-											
default	Status						Default value (CSD1 CSD0)					
	Power on sequence						00b					
	S/W reset						00b					
	H/W reset						00b					

	Function	0	1
SMY	Inverse the MY setting	Keep MY	Inverse MY
SMX	Inverse the MX setting	Keep MX	Inverse MX
SINV	Inverse the INVON setting	Keep INVON	Inverse INVON
SBGR	Inverse the BGR setting	Keep BGR	Inverse BGR

CSD1	CSD0	Common scan direction			
		COM0	COM65	COM66	COM131
0	0	0 →	65	66 →	131
0	1	0 →	65	131 →	66
1	0	65 →	0	66 →	131

43. RMWIN: Read Modify In (B8H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RMWIN	0	1	0	1	0	1	1	1	0	0	0	B8H
Parameter	No parameter											
description	Read Modify In											
restriction	-											
default	Status						Default value					

	Power on sequence	Read modify out
	S/W reset	Read modify out
	H/W reset	Read modify out

44. RMWOUT: Read Modify Out (B9H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RMWIN	0	1	0	1	0	1	1	1	0	0	1	B9H
Parameter	No parameter											
description	Read Modify Out											
restriction	-											
default	Status						Default value					
	Power on sequence						Read modify out					
	S/W reset						Read modify out					
	H/W reset						Read modify out					

45. VOPSET: Vop SET (C0H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VOPSET	0	1	0	1	1	0	0	0	0	0	0	C0H
1st Parameter	1	1	0	VOP7	VOP6	VOP5	VOP4	VOP3	VOP2	VOP1	VOP0	-
2nd Parameter	1	1	0	-	-	-	-	-	-	-	VOP8	-
description	This command is used to program the optimum LCD supply voltage V0.											
restriction	-											
default	Status						Default value					
	Power on sequence						1_1110_1011b(EBH)					
	S/W reset						1_1110_1011b(EBH)					
	H/W reset						1_1110_1011b(EBH)					

46. VOPOFSETINC: Vop Increase 1 (C1H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VOPOFSETINC	0	1	0	1	1	0	0	0	0	0	1	C1H
Parameter	No parameter											
description	With the VOPOFSETDEC and VOPOFSETINC command the Vlcd voltage and there with the contrast of the LCD can be adjusted. This command increases the value of Vop offset register by 1. If you set the electronic control value to 1111111, the control value is set to 0000000 after this command has been executed.											
restriction	-											
default	Status						Default value					
	Power on sequence						--					
	S/W reset						--					
	H/W reset						--					

47. VOPOFSETDEC: Vop Decrease 1 (C2H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VOPOFSETDEC	0	1	0	1	1	0	0	0	0	1	0	C2H
Parameter	No parameter											
description	With the VOPOFSETDEC and VOPOFSETINC command the Vlcd voltage and there with the contrast of the LCD can be adjusted. This command decreases the value of Vop offset register by 1. If you set the electronic control value to 0000000, the control value is set to 1111111 after this command has been executed.											

restriction	-	
default	Status	Default value
	Power on sequence	--
	S/W reset	--
	H/W reset	--

48. BIASSEL: Bias selection (C3H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BIASSEL	0	1	0	1	1	0	0	0	0	1	1	C3H
Parameter	1	1	0	-	-	-	-	-	BIAS2	BIAS1	BIAS0	-

description: Select LCD bias ratio of the voltage required for driving the LCD.

BIAS2	BIAS1	BIAS0	LCD bias
0	0	0	1/12
0	0	1	1/11
0	1	0	1/10
0	1	1	1/9
1	0	0	1/8
1	0	1	1/7
1	1	0	1/6
1	1	1	1/5

restriction	-	
default	Status	Default value (BIAS[2:0])
	Power on sequence	110b
	S/W reset	110b
	H/W reset	110b

49. BSTBMPXSEL: Booster setting (C4H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BSTPMPXSEL	0	1	0	1	1	0	0	0	1	0	0	C4H
Parameter	1	1	0	-	-	-	-	-	BST2	BST1	BST0	-

description: Booster Setting

BST2	BST1	BST0	
0	0	0	X1 (boosting off)
0	0	1	X2 boosting circuit
0	1	0	X3 boosting circuit
0	1	1	X4 boosting circuit
1	0	0	X5 boosting circuit
1	0	1	X6 boosting circuit
1	1	0	X7 boosting circuit
1	1	1	X8 boosting circuit

restriction	-	
default	Status	Default value (BST[2:0])
	Power on sequence	110b
	S/W reset	110b
	H/W reset	110b

50. BSTEFFSEL: Booster Efficiency Selection (C5H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
BSTEFFSEL	0	1	0	1	1	0	0	0	1	0	1	C5H
Parameter	1	1	0	-	-	-	-	-	-	BTF1	BTF0	-
description	Booster Efficiency Setting											

	BTF1	BTF0	Frequency (Hz)	
	0	0	Level 1	
	0	1	Level 2	
	1	0	Level 3	
	1	1	Level 4	
	By Booster Stages (2x, 3x, 4x, 5x, 6x, 7x, 8x) and Booster Efficiency (Level 1-4) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (Level 4 is higher than Level 1). The Booster Efficiency is better than lower level, and it just need few more power consumption current.			
restriction	-			
default	Status	Default value (BTF[1:0])		
	Power on sequence	01b		
	S/W reset	01b		
	H/W reset	01b		

51. VOPOFFSET: Vop offset fuse adjust (C7H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VOPOFFSET	0	1	0	1	1	0	0	0	1	1	1	C7H
Parameter 1	1	1	0	VOS7	VOS6	VOS5	VOS4	VOS3	VOS2	VOS1	VOS0	-
description	This command is used to the Vop offset for V0, which is also the value programmed into MTP											
restriction	-											
default	Status						Default value (VOS[8:0])					
	Power on sequence						7FH					
	S/W reset						7FH					
	H/W reset						7FH					

52. MTPERS (D7H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MTPERS	0	1	0	1	1	0	1	0	1	1	1	D7H
Parameter	1	1	0	-	-	ERS	0	0	0	0	0	1
description	MTP erase command. This command is used to indicate MTP erase operation. After MTP erase, MTP can be programmed again and can be set to new value.											
restriction	-											

53. MTPPROG (E0H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MTPPROG	0	1	0	1	1	1	0	0	0	0	0	E0H
description	MTP program command. This command is used to indicate MTP program operation.											
restriction	Before set MTPPROG, the VPP must be connect with external VPP supply (7.5V), and VDD must be connected with external VDD supply (1.8V).											

54. MTPPROGE (E1H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MTPPROGE	0	1	0	1	1	1	0	0	0	0	1	E1H
description	This command is used indicate the end of the MTP operation, whatever program or erase											
restriction	-											

55. MTPPROGS (E2H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MTPPROGS	0	1	0	1	1	1	0	0	0	1	0	E2H
description	This command is used indicate the start of the MTP operation, whatever program or erase											
restriction	-											

56. MTPPROGA (E4H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MTPPROGA	0	1	0	1	1	1	0	0	1	0	0	E4H
description	MTP program and erase address											
restriction	please always set to 2'b00											
default	Status						Default value					
	Power on sequence						00b					
	S/W reset						00b					
	H/W reset						00b					

57. FRMSEL: Frame Freq. in Temperature range (F0H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
FRMSEL	0	1	0	1	1	1	1	0	0	0	0	F0H
1stparameter	1	1	0	-	-	-	-	FA4	FA3	FA2	FA1	RangeA
2ndparameter	1	1	0	-	-	-	-	FB4	FB3	FB2	FB1	RangeB
3rdparameter	1	1	0	-	-	-	-	FC4	FC3	FC2	FC1	RangeB
4thparameter	1	1	0	-	-	-	-	FD4	FD3	FD2	FD1	RangeB

description

Select Frame Freq. in normal display mode.
1st parameter : Frame freq. value set in temperature range 10(-30℃) to TA
2nd parameter : Frame freq. value set in temperature P range TA to TB
3rd parameter : Frame freq. value set in temperature range TB to TC
4th parameter : Frame freq. value set in temperature range TC to 130(90℃)
For command setting to frame rate value look-up-table, please see the following table:

Reg(hex)	Frame Rate (Hz)
00	50
01	55
02	60
03	65
04	70
05	75
06	80
07	85
08	90
09	95
0A	100
0B	105
0C	110
0D	115
0E	120
0F	125

restriction: -

default

Status	Default value
Power on sequence	00H
S/W reset	00H

	H/W reset	00H

58. TMPRNG: Temp. range set for Frame Freq. Adj. (F2H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TMPRNG	0	1	0	1	1	1	1	0	0	1	0	F2H
1st parameter	1	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	Range A
2nd parameter	1	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	Range B
3rd parameter	1	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	Range C
description	Temp. Range set for automatic frame freq. adj. operation according the current temp. value. 1st parameter: Temp. range A value set 2nd parameter: Temp. range B value set 3rd parameter: Temp. range C value set **TA/TB/TC Temperature(℃) + 40 = TA/TB/TC[6:0]** Example: If TA wants to be set at 24℃, TA[6:0]=24+40=64(40h),											
restriction	-40℃≦TA≦TA+TH≦TB≦TB+TH≦TC≦87℃											
default	Status							Default value				
	Power on sequence							00H				
	S/W reset							00H				
	H/W reset							00H				

59. TMPHYS: Temp. Hysteresis Set for Frame Freq. Adj. (F3H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TMPHYS	0	1	0	1	1	1	1	0	0	1	1	F3H
1st parameter	1	1	0	-	-	-	-	-	TH2	TH1	TH0	
description	Temp. hysteresis range set for frame freq. adj. Parameter TH[3:0] is used to set Temp. hysteresis range. The relationship between temp. state and temp. range value is shown below. TBD **TH Temperature(℃) - 1 = TH[3:0]** Example: If TH wants to set 5℃, TH[3:0]=5-1=4.											
restriction	Temp. hysteresis value should be smaller than the gap of temp. Range.											
default	Status							Default value				
	Power on sequence							00H				
	S/W reset							00H				
	H/W reset							00H				

60. TEMPSEL: Temperature Gradient Compensation Coefficient Set (F4H)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEMPSEL	0	1	0	1	1	1	1	0	1	0	0	F4H
1st parameter	1	1	0	MT 13	MT 12	MT 11	MT10	MT03	MT02	MT01	MT00	(-24 ₀C to -32 ₀C) (-32 ₀C to -40 ₀C)
2nd parameter	1	1	0	MT 33	MT 32	MT 31	MT30	MT23	MT22	MT21	MT20	(-8 ₀C to -16 ₀C) (-16 ₀C to -24 ₀C)
3rd parameter	1	1	0	MT 53	MT 52	MT 51	MT50	MT43	MT42	MT41	MT40	(8 ₀C to 0 ₀C) (0 ₀C to -8 ₀C)
4th parameter	1	1	0	MT 73	MT 72	MT 71	MT70	MT63	MT62	MT61	MT60	(24 ₀C to16 ₀C) (16 ₀C to 8 ₀C)

5th parameter	1	1	0	MT 93	MT 92	MT 91	MT90	MT83	MT82	MT81	MT80	(40 oC to 32oC) (32 oC to 24oC)
6th parameter	1	1	0	MT 113	MT 112	MT 111	MT11 0	MT10 3	MT10 2	MT10 1	MT10 0	(56 oC to 48oC) (48 oC to 40oC)
7th parameter	1	1	0	MT 133	MT 132	MT 131	MT13 0	MT12 3	MT12 2	MT12 1	MT12 0	(72 oC to 64 oC) (64 oC to 56 oC)
8th parameter	1	1	0	MT 153	MT 152	MT 151	MT15 0	MT14 3	MT14 2	MT14 1	MT14 0	(87 oC to 80 oC) (80 oC to 72 oC)

description

This command defines temperature gradient compensation coefficient. For this command detail description and opearation, please see Section 7.11.

MTn3	MTn2	MTn1	MTn0	Voltage/℃
0	0	0	0	0mv/℃
0	0	0	1	-5mv/℃
0	0	1	0	-10mv/℃
0	0	1	1	-15mv/℃
0	1	0	0	-20mv/℃
0	1	0	1	-25mv/℃
0	1	1	0	-30mv/℃
0	1	1	1	-35mv/℃
1	0	0	0	-40mv/℃
1	0	0	1	-45mv/℃
1	0	1	0	-50mv/℃
1	0	1	1	-55mv/℃
1	1	0	0	-60mv/℃
1	1	0	1	-65mv/℃
1	1	1	0	-70mv/℃
1	1	1	1	-75mv/℃

restriction: -

default

Status	Default value
Power on sequence	00H
S/W reset	00H
H/W reset	00H

61. CLUTR (FBH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CLUTR	0	1	0	1	1	1	1	1	0	1	1	FBH
1st parameter	1	1	-	P17	P16	P15	P14	P13	P12	P11	P10	-
2nd parameter	1	1	-	P27	P26	P25	P24	P23	P22	P21	P20	
3rd parameter	1	1	-	P37	P36	P35	P34	P33	P32	P31	P30	
4th parameter	1	1	-	P47	P46	P45	P44	P43	P42	P41	P40	
---	1	1	-	:	:	:	:	:	:	:	:	
---	1	1	-	:	:	:	:	:	:	:	:	
31st parameter	1	1	-	P317	P316	P315	P314	P313	P312	P311	P310	
32nd parameter	1	1	-	P327	P326	P325	P324	P323	P322	P321	P320	
description	This command is used to set gamma curve for color gray R											
restriction	The 1st parameter P1 must be set to 0, and 32nd parameter must be set to 127. N+1 parameter's value – N parameter's value <16.											

default

Status	Default value
Power on sequence	P1=0, P2=6, P3=10, P4=14, P5=18, P6=22, P7=26, P8=30, P9=34, P10=38, P11=42, P12=46, P13=50, P14=54, P15=58, P16=62,
H/W reset	

		P17=66, P18=70, P19=74, P20=78, P21=82, P22=86, P23=90, P24=94, P25=98, P26=102, P27=106, P28=110, P29=114, P30=118, P31=122, P32=127
	SW reset	Not changed

62. CLUTG (FCH)

Command	D/C	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CLUTR	0	1	0	1	1	1	1	1	1	0	0	FCH
1st parameter	1	1	0	-	P16	P15	P14	P13	P12	P11	P10	-
2nd parameter	1	1	0	-	P26	P25	P24	P23	P22	P21	P20	
3rd parameter	1	1	0	-	P36	P35	P34	P33	P32	P31	P30	
4th parameter	1	1	0	-	P46	P45	P44	P43	P42	P41	P40	
---	1	1	0	-	:	:	:	:	:	:	:	
---	1	1	0	-	:	:	:	:	:	:	:	
63rd parameter	1	1	0	-	P636	P635	P634	P633	P632	P631	P630	
64th parameter	1	1	0	-	P646	P645	P644	P643	P642	P641	P640	
description	This command is used to set color gray G											
restriction	The 1st parameter P1 must be set to 0, and 64nd parameter must be set to 127. N+1 parameter's value – N parameters value < 8.											
default	Status						Default value					
	Power on sequence						P1=0, P2=3, P3=5, P4=7, P5=9, P6=11, P7=13, P8=15, P9=17 P10=19, P11=21, P12=23, P13=25, P14=27, P15=29, P16=31, P17=33, P18=35, P19=37, P20=39, P21=41, P22=43, P23=45, P24=47, P25=49, P26=51, P27=53, P28=55, P29=57, P30=59, P31=61, P32=63, P33=65, P34=67, P35=69, P36=71, P37=73, P38=75, P39=77, P40=79, P41=81, P42=83, P43=85, P44=87, P45=89, P46=91, P47=93, P48=95, P49=97, P50=99, P51=101, P52=103, P53=105, P54=107, P55=109, P56=111, P57=113, P58=115, P59=117, P60=119, P61=121, P62=123, P63=125, P64=127					
	H/W reset											
	SW reset						Not changed					

63. CLUTB (FDH)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
CLUTR	0	1	0	1	1	1	1	1	1	0	1	FDH
1st parameter	1	1	0	-	P16	P15	P14	P13	P12	P11	P10	-
2nd parameter	1	1	0	-	P26	P25	P24	P23	P22	P21	P20	
3rd parameter	1	1	0	-	P36	P35	P34	P33	P32	P31	P30	
4th parameter	1	1	0	-	P46	P45	P44	P43	P42	P41	P40	
---	1	1	0	-	:	:	:	:	:	:	:	
---	1	1	0	-	:	:	:	:	:	:	:	
31st parameter	1	1	0	-	P316	P315	P314	P313	P312	P311	P310	
32nd parameter	1	1	0	-	P326	P325	P324	P323	P322	P321	P320	
description	This command is used to set color gray B											
restriction	The 1st parameter P1 must be set to 0, and 32nd parameter must be set to 127. N+1 parameter's value – N parameter's value <16.											
default	Status						Default value					
	Power on sequence						P1=0, P2=6, P3=10, P4=14, P5=18, P6=22, P7=26, P8=30, P9=34, P10=38, P11=42, P12=46, P13=50, P14=54, P15=58, P16=62, P17=66, P18=70, P19=74, P20=78, P21=82,					
	H/W reset											

		P22=86, P23=90, P24=94, P25=98, P26=102, P27=106, P28=110, P29=114, P30=118, P31=122, P32=127
	SW reset	Not changed

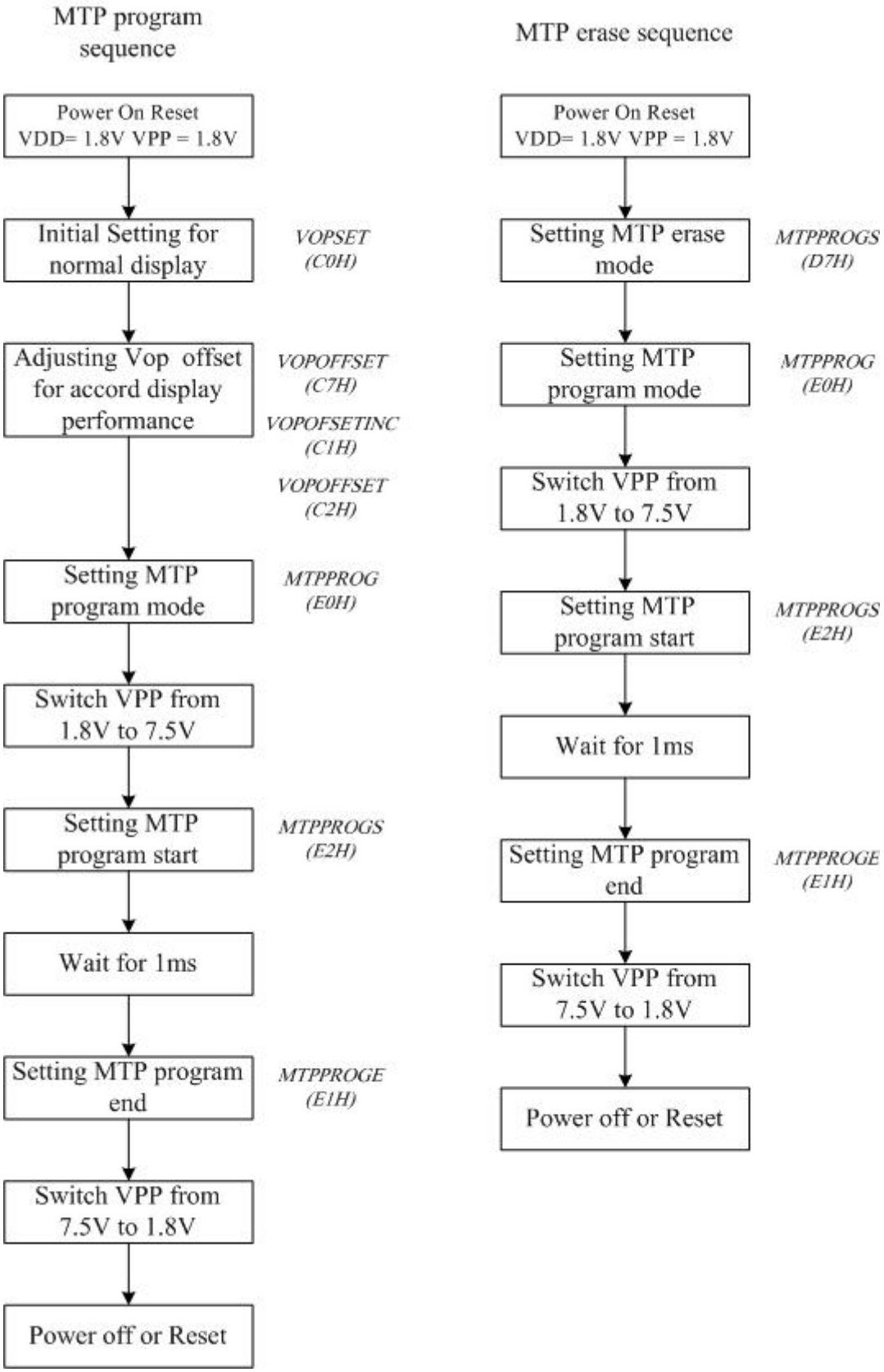
INITIALIZATION SEQUENCE

The registers that are initialized are listed below.

Item	After power on	After software reset	After hardware reset
Frame memory (RAM data)	random	No change	No change
RDDID	55H	80H	00H
RDDPM	08h	08h	08h
RDDMADCTR	00h	No change	00h
RDDCOLMOD	05h (16bit/pixel)	No change	05h (16bit/pixel)
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
Sleep in/out	in	in	in
Display mode	Normal	Normal	normal
Display inversion on/off	off	off	off
All pixel off mode	disable	disable	disable
All pixel on mode	disable	disable	disable
Contrast (EV)	3Fh	3Fh	3Fh
Display on/off	off	off	off
Column: start address(XS)	00h	00h	00h
Column: end address (XE)	83h	83h	83h
Row: start address (YS)	00h	00h	00h
Row: end address (YE)	83h	83h	83h
Color set	random	Contents of the look-up table protected	random
Partial: Start Address (PS)	00h	00h	00h
Partial: End Address (PE)	83h	83h	83h
Scroll: Top Fixed Area (TFA)	00h	00h	00h
Scroll: Scroll Area (VSA)	84h	84h	84h
Scroll: Bottom Fixed Area (BFA)	00h	00h	00h
TE On/Off	off	off	Off
TE Mode	0	0	0
Memory Data Access Control (MY/MX/MV/RGB)	0/0/0/0/0	No change	No change
Scroll Start Address (SSA)	00h	00h	00h
Idle Mode On/Off	off	off	off
Interface Color Pixel Format (P)	05h (16bit/pixel)	No change	05h (16bit/pixel)
ID1	TBD	TBD	TBD
ID2	TBD	TBD	TBD
ID3	TBD	TBD	TBD
Drive Duty	83h	83h	83h
First Common	00h	00h	00h
FOSC Divider	No division	No division	No division
Common scan direction	0->65,66->131	0->65,66->131	0->65,66->131
Vop	0EBh	0EBh	0EBh
Vop Offset increase/decrease	disable	disable	disable
Bias	1/6	1/6	1/6
Booster setting	7x	7x	7x
Booster Efficiency	01	01	01
EPCTIN	0	0	0
MTP selection	disable	disable	disable
Frame Frequency in Normal Color (FA/FB/FC/FD)	00H	00H	00H

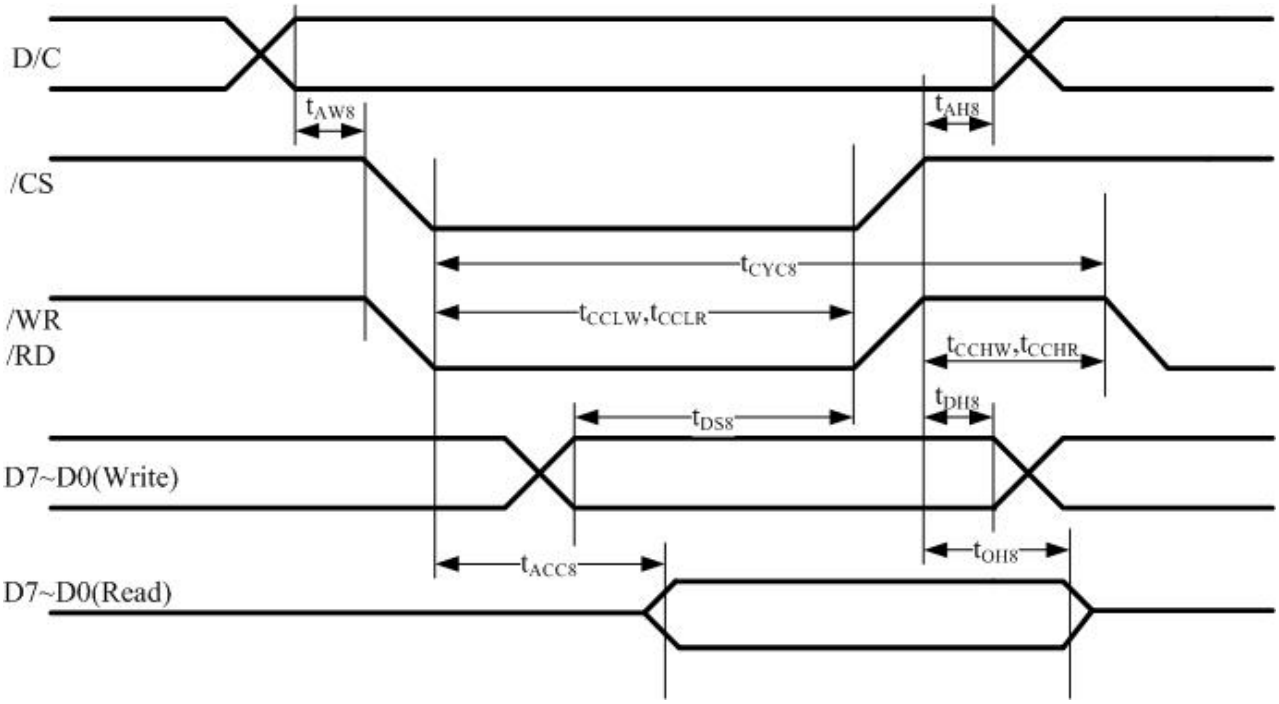
Frame Frequency in 8-Color (Idle) (F8A/F8B/F8C/F8D)	00H	00H	00H
Temperature Range (TA/TB/TC)	00H	00H	00H
Temperature Hysteresis (TH)	00H	00H	00H
TEMPSEL	00H	00H	00H

Vop CALIBRATION



AC CHARACTERISTICS

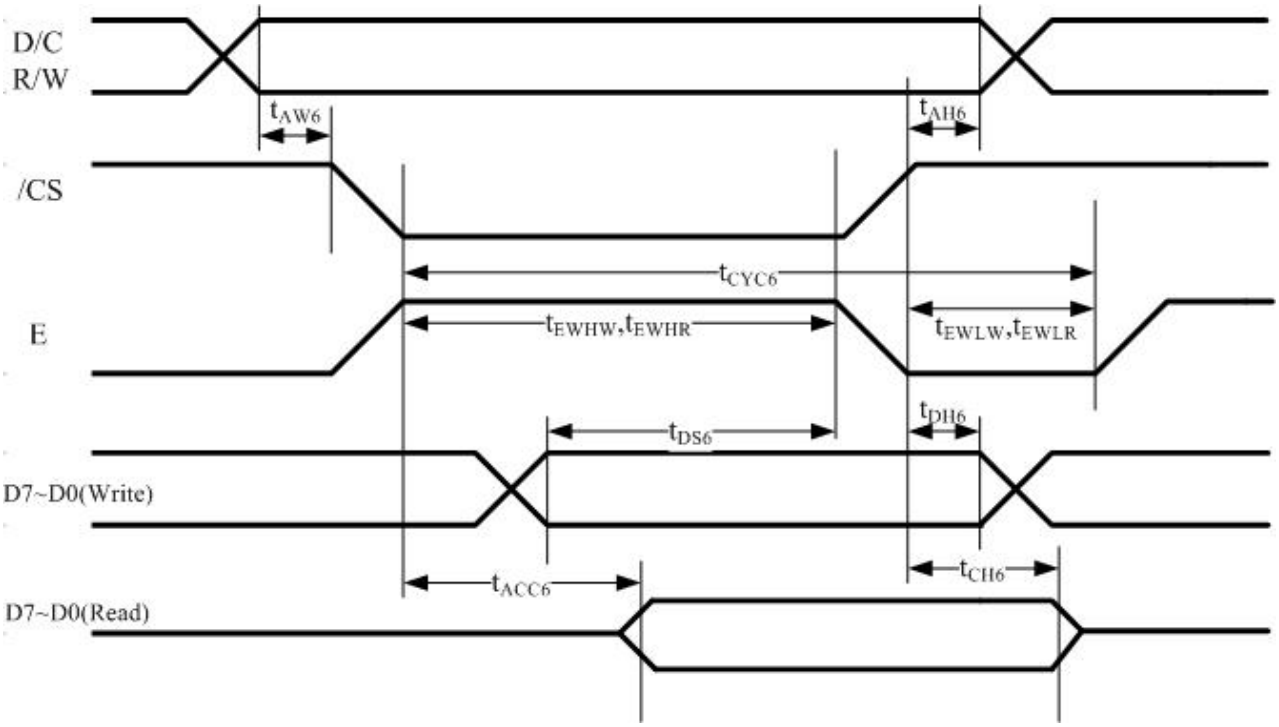
System Buses Read/Write Timing Characteristics For 8080 Series MPU



(VDD = 1.65V~1.95V,Ta = –30 to 70℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	D/C	t_{AH8}		10	--	ns
Address setup time		t_{AW8}		10	--	
Enable L pulse width (WRITE)	/CS /WR	t_{CCLW}		40	--	
Enable H pulse width (WRITE)		t_{CCHW}		40	--	
System cycle time		t_{CYC8}		140		
Enable L pulse width (READ)	/CS /RD	t_{CCLR}		40	--	
Enable H pulse width (READ)		t_{CCHR}		40	--	
System cycle time		t_{CYC8}		160		
WRITE Data setup time	D7 to D0	t_{DS8}		15	--	
WRITE Address hold time		t_{DH8}		15	--	
READ access time		t_{ACC8}	CL = 30 pF max	--	--	
READ Output disable time		t_{OH8}	CL = 30 pF max	20	60	

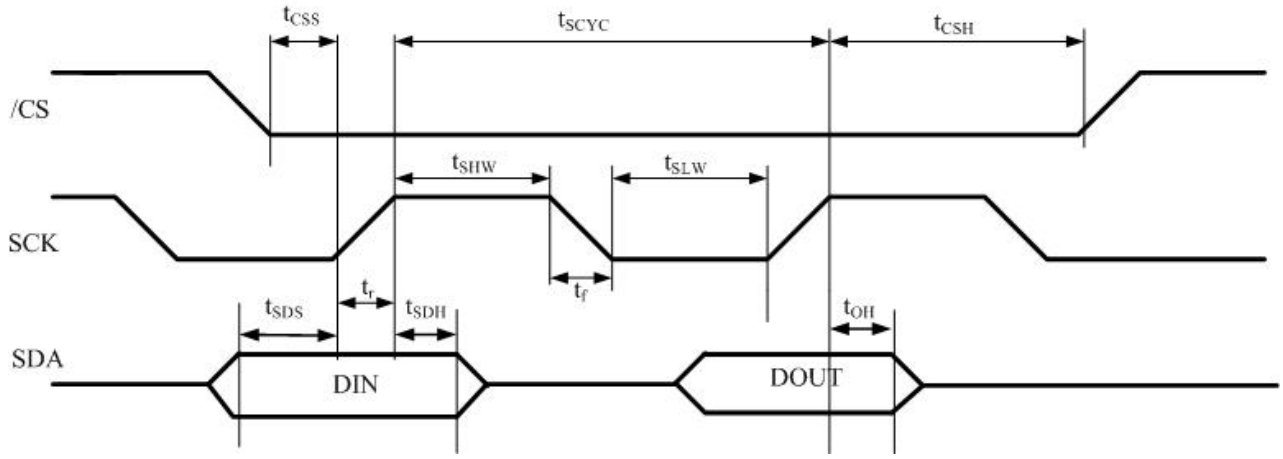
System Bus Read/Write Timing Characteristics For the 6800 Series MPU



(VDD = 1.65V~1.95V,Ta = –30 to 70℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address hold time	D/C	t_{AH6}		10	--	ns
Address setup time		t_{AW6}		10	--	
Enable L pulse width (WRITE)	/CS E	t_{EWLW}		40	--	
Enable H pulse width (WRITE)		t_{EWHW}		40	--	
System cycle time		t_{CYC6}		140	--	
Enable L pulse width (READ)	/CS E	t_{EWLR}		40	--	
Enable H pulse width (READ)		t_{EWHR}		40	--	
System cycle time		t_{CYC6}		160	--	
WRITE Data setup time	D7 to D0	t_{DS6}		15	--	
WRITE Address hold time		t_{DH6}		15	--	
READ access time		t_{ACC6}	CL = 30 pF max	--	--	
READ Output disable time		t_{OH6}	CL = 30 pF max	20	60	

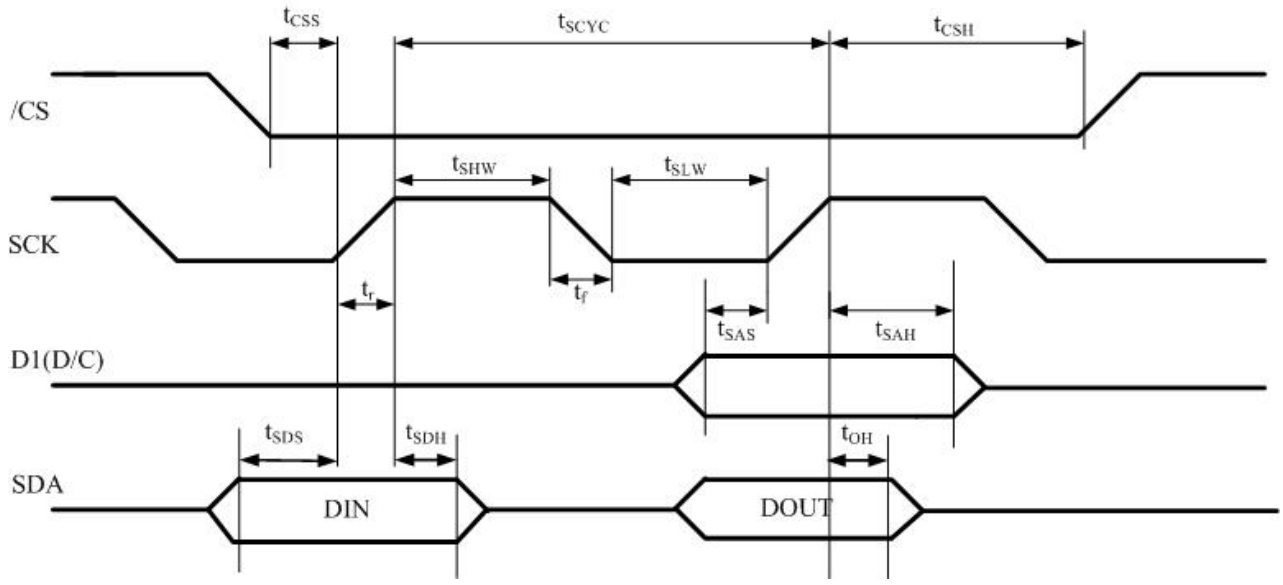
3-line Serial Interface Timing



(VDD = 1.65V~1.95V,Ta = –30 to 70℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
3-line SPI Clock Period	SCK	t_{SCYC}		70	--	ns
SCK “H” pulse width		t_{SHW}		30	--	
SCK “L” pulse width		t_{SLW}		30	--	
Data setup time	SDA	t_{SDS}		15	--	
Data hold time		t_{SDH}		15	--	
Data output hold time		t_{OH}		20	60	
CS-SCK time	/CS	t_{CSS}		60	--	
CS-SCK time		t_{CSH}		60	--	

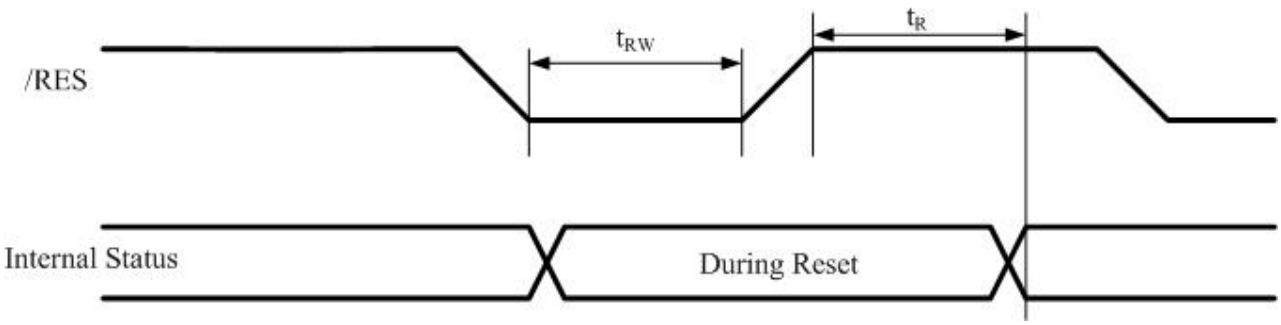
4-line Serial Interface Timing



(VDD = 2.8V,Ta = –30 to 85℃)

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
4-line SPI Clock Period	SCK	t_{SCYC}		70	--	ns
SCK “H” pulse width		t_{SHW}		30	--	
SCK “L” pulse width		t_{SLW}		30	--	
Address setup time	D/C	t_{SAS}		10	--	
Address hold time		t_{SAH}		10	--	
Data setup time	SDA	t_{SDS}		15	--	
Data hold time		t_{SDH}		15	--	
Data output hold time		t_{OH}		20	60	
CS-SCK time	/CS	t_{CSS}		60	--	
CS-SCK time		t_{CSH}		60	--	

Reset Timing



(VDD = 1.8 ~ 3.3V, Ta = 25℃)

Item	Symbol	Condition	Rating		Unit
			Min.	Max.	
Reset cancel time	tR		--	5.0	ms
Reset low pulse width	tRW	/RES	10.0	--	us
Reset insensible pulse width	tNS			3.0	us

Note1: The reset cancel includes also required time for chip internal initialization, which need reset cancel time tR within 5ms after a rising edge of /RES.
Note2: A reset pulse width less than tNS is rejected by TLS8103 for noise prevention .

DC CHARACTERISTICS

(Unless otherwise specified, V_{DD}=1.8V,VSS=0, TA = -30 to 85 ºC)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{DD}	Logic Supply Voltage		1.65	-	1.95	V
V_{CI}	Analog Supply Voltage		2.5	-	3.3	V
V_{LCD}	LCD Operating Voltage		-	-	18	V
V_{OH}	High Logic Output Level		0.8*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level		0	-	0.2*V_{DD}	V
V_{IH}	High Logic Input Level	I_{OH} = -0.5mA	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	I_{OL} = 0.5mA	0	-	0.2*V_{DD}	V
I_{LI}	Input leakage Current		-1.0	-	1.0	uA
I_{LO}	Output leakage Current		-3.0	-	3.0	uA
I_{DD}	Dynamic Current Consumption	Power down mode	-	3	TBD	uA
		V_{CC}=V_{CI}=2.8V, internal V_{DD} Regulator enable, V_0-V_{SS}=15 V, bias=1/9, boosting level 6x, displaying all ON pattern, Ta =25 ºC, with out panel	-	TBD	TBD	uA
		V_{CC}=V_{CI}=2.8V, internal V_{DD} Regulator enable, V_0-V_{SS}=15 V, bias=1/9, boosting level 6x, displaying checker pattern, Ta=25 ºC, with out panel	-	TBD	TBD	uA
R_{ON}	Liquid Crystal Driver ON Resistance	Ta=25℃ (Relative to V_{SS}) V_0=15V	-	TBD	TBD	KΩ
		Ta=25℃ (Relative to V_{SS}) $V_{0=}$15V	-	TBD	TBD	KΩ
FR	Frame frequency		TBD	73	TBD	Hz

ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
Power Supply voltage	V_{DD}	-0.3 to 2.0	V
	V_{CC}	-0.3 to 3.6	
	V_{CI}	-0.3 to 3.6	V
	V_{LCD} (V0-VSS, Vg-XV0, V0-XV0)	-0.3 to 18	V
	Vg, Vm	-0.3 to V_{LCD}	V
Operating Temperature	T_A	-30 to +85	ºC
Storage Temperature(Bare chip)	T_{stg}	-65 to +150	ºC

APPLICATION NOTES

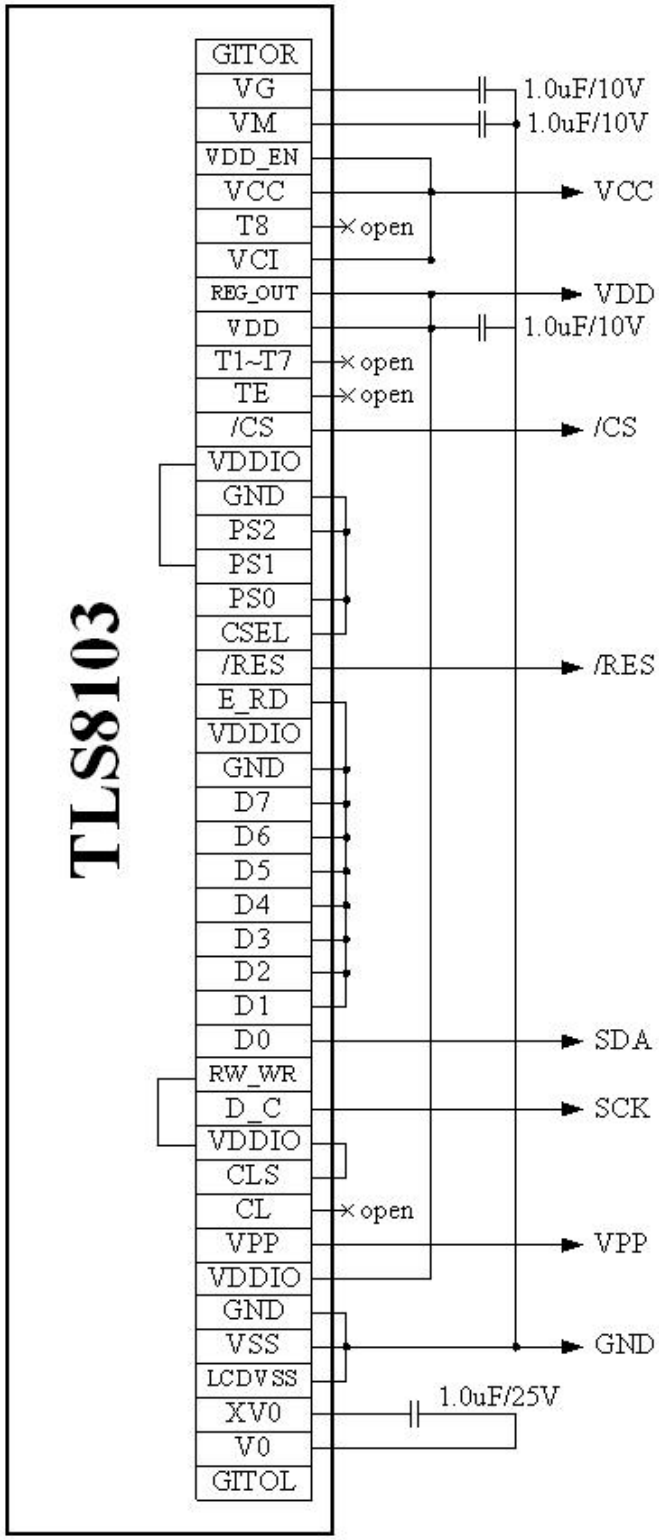
Application Information for LCD Panel (Reference Example)

TBD

Application Information for Pin Connection to MPU (Reference Example)

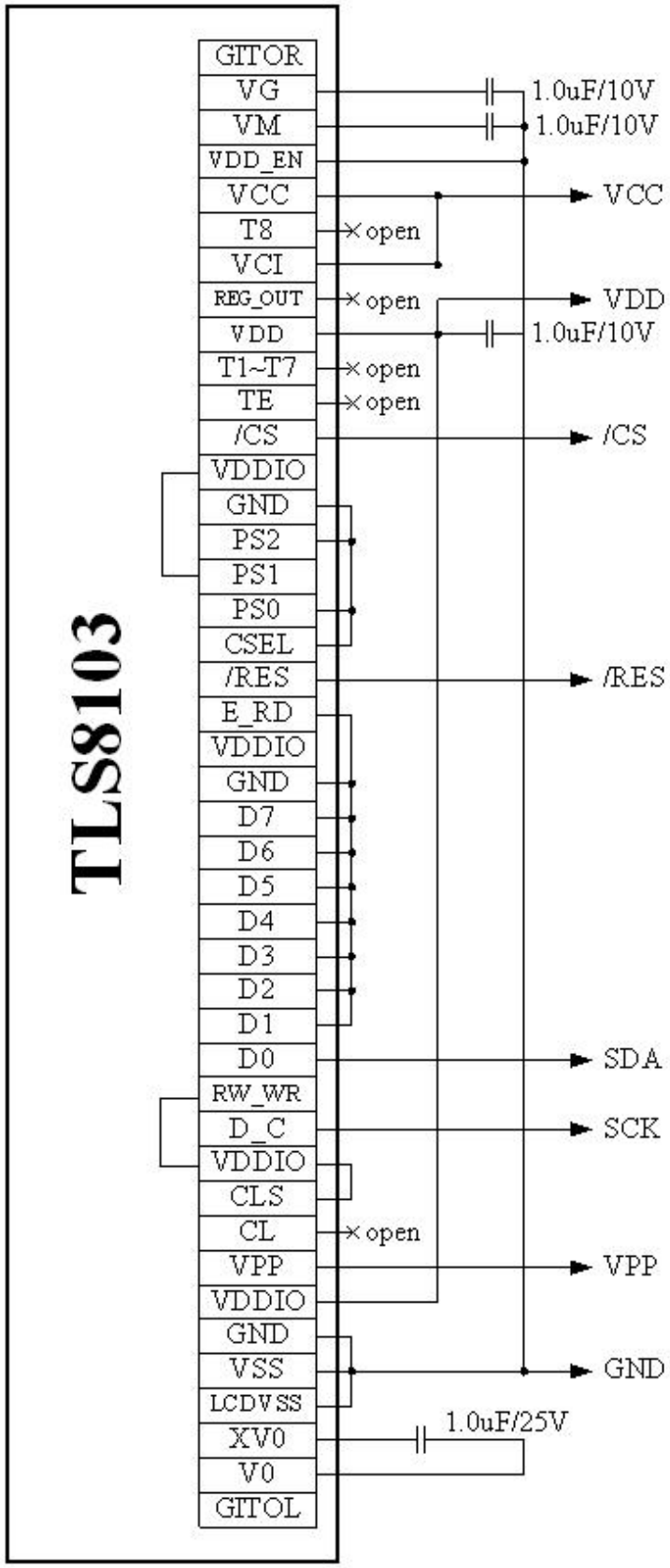
3 wires SPI interface

Internal VDD regulator enable, VDD pin only for external supply when MTP program. Please left VDD pin open when connect with mobile phone. VCC is power supply for analog and internal VDD regulator.
VPP pin only for external supply (7.5V) when MTP program.
VDDIO connect with VDD for 1.8V I/O application.
Internal oscillator enable



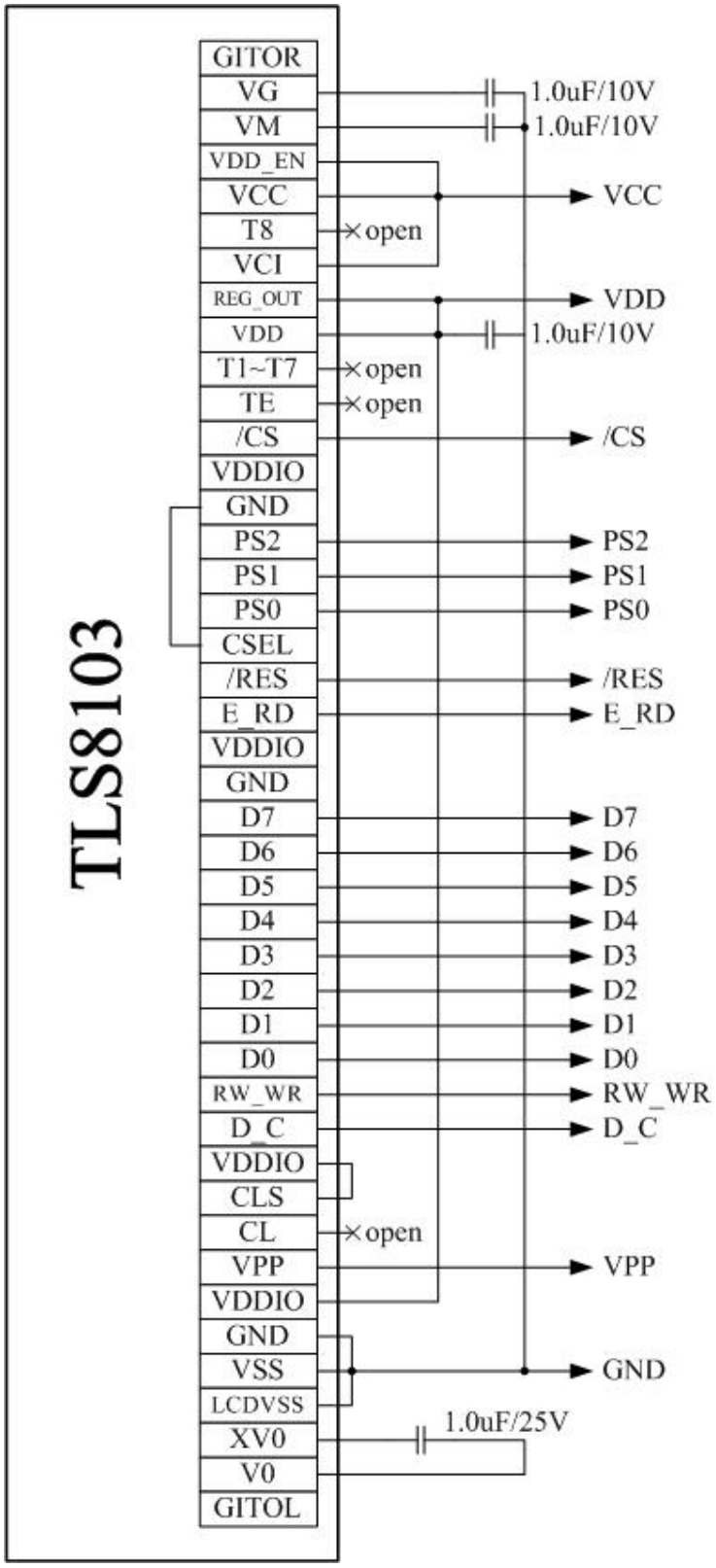
3 wires SPI interface

Internal VDD regulator disable, VDD is external VDD (1.8V) power supply input, VCC is only for analog.
VPP pin only for external supply (7.5V) when MTP program.
VDDIO connect with VDD for 1.8V I/O application.
Internal oscillator enable



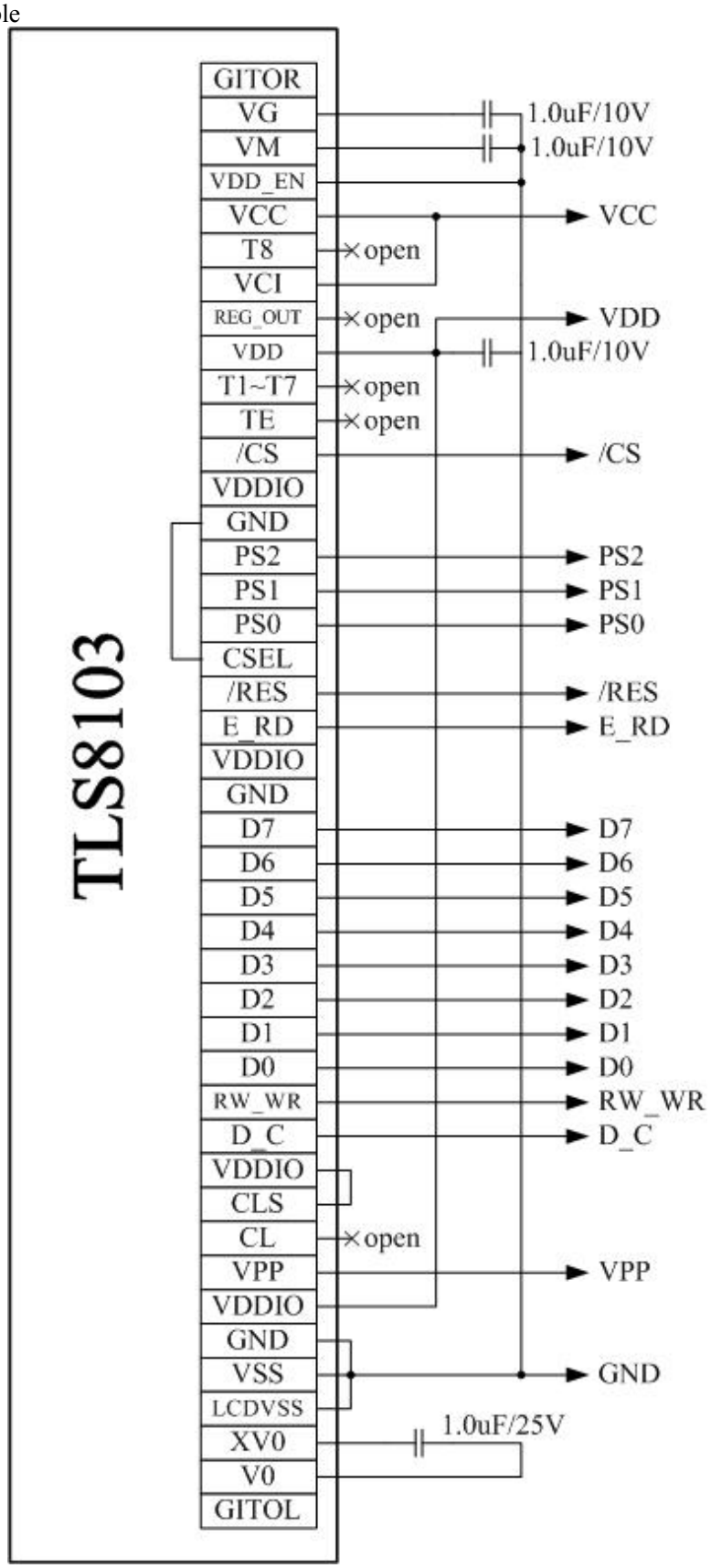
Parallel interface

Internal VDD regulator enable, VDD pin only for external supply when MTP program. Please left VDD pin open when connect with mobile phone. VCC is power supply for analog and internal VDD regulator.
VPP pin only for external supply (7.5V) when MTP program. VDDIO connect with VDD for 1.8V I/O application, or for 3V I/O application VDDIO should be connected with VCI.
Internal oscillator enable



Parallel interface

Internal VDD regulator disable, VDD is external VDD (1.8V) power supply input, VCC is only for analog.
VPP pin only for external supply (7.5V) when MTP program. VDDIO connect with VDD for 1.8V I/O application, or for 3V I/O application VDDIO should be connected with VCI.
Internal oscillator enable



Revision History

TLS8103 Datasheet Revision History		
Version	Content	Date
1.0	Original	Jun., 2007
2.0	1) modify the VDD ITO requirement from <50Ω to 20Ω, page 25 2) Add internal VDD regulator state description in the command SLPIN/SLPOUT, page 60 3) Add command description 4) Add parallel interface demo diagram 5) Add Vop CALIBRATION description, page 83.	Jul., 2007
2.1	1) Modify the CSEL PIN description, page24. 2) Delete command 'ML' description	Jul., 2007
2.2	1) modify the RW_WR connection error in the parallel interface demo diagram, page 93 and 94 2) modify max tNS parameter form 3ms to 5ms, page 55 3) modify the Vop calibration sequence diagram, page 83 4) modify the N-line inverse setting default value to 0x80H, page72 5) modify some error or confusing description, page 84, page75, page 76, page 30, page 24, page 21, page4, page 3	Jul., 2007
2.3	Modify the ITO requirements of power PADs of VDD/VDDIO/GND/VSS/LCDVSS/VCC/REG_OUT /VCC/VPP, page 25	Aug., 2007