TLV2217 Low-Dropout Fixed-Voltage Regulators

1 Features

- Fixed 1.8-V, 2.5-V, and 3.3-V Outputs
- ±1% Maximum Output Voltage Tolerance at T_J = 25°C
- 500-mV Maximum Dropout Voltage at 500 mA (3.3-V Option)
- ±2% Output Voltage Variation Across Load and Temperature
- Internal Overcurrent Limiting
- Internal Thermal-Overload Protection
- Internal Overvoltage Protection

2 Applications

- Electronic Points of Sale
- Medical, Health, and Fitness Applications
- Printers
- Appliances and White Goods
- TV Set-Top Boxes

3 Description

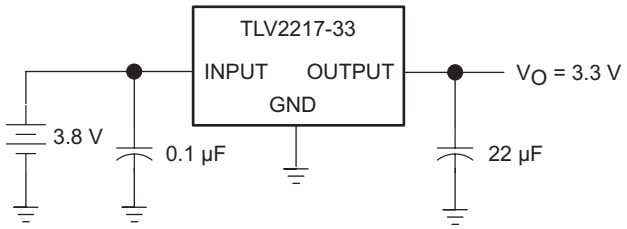
The TLV2217 family of low-dropout regulators offers a variety of fixed-voltage options that offer a maximum continuous input voltage of 16 V, making them more versatile than CMOS regulators. Utilizing a PNP pass element, these regulators are capable of sourcing 500 mA of current, with a specified maximum dropout of 500 mV (3.3-V and 2.5-V options), making these regulators ideal for low-voltage applications. Additionally, the TLV2217 regulators offer very tight output accuracy of ±2% across operating load and temperature ranges. Other convenient features the regulators provide are internal overcurrent limiting, thermal-overload protection, and overvoltage protection. The TLV2217 family of regulators is available in fixed voltages of 1.8 V, 2.5 V, and 3.3 V.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV2217-xxPW	TSSOP (20)	6.50 mm × 4.40 mm
TLV2217-xxKVU	TO-252 (2)	6.04 mm × 6.15 mm
TLV2217-xxKCS	TO-220 (3)	10.16 mm × 9.15 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Copyright © 2016, Texas Instruments Incorporated

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

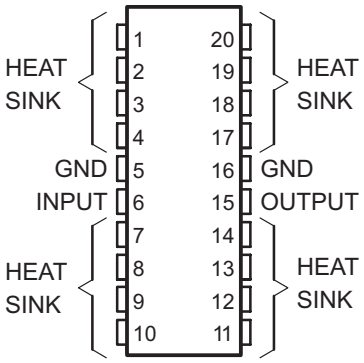
Changes from Revision L (April 2005) to Revision M **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see *Package Ordering Addendum* at the end of the data sheet ... 1
- Changed Junction-to-ambient thermal resistance, $R_{\theta JA}$, values in *Thermal Information* table From: 83°C/W To: 81.6°C/W (PW), From: 28°C/W To: 31°C/W (KVU), and From: 19°C/W To: 22.5°C/W (KCS) ... 4
- Changed Junction-to-case (top) thermal resistance, $R_{\theta JC(top)}$, values in *Thermal Information* table From: 32°C/W To: 22.1°C/W (PW), From: 19°C/W To: 37.5°C/W (KVU), and From: 17°C/W To: 34.6°C/W (KCS) ... 4
- Changed Junction-to-case (bottom) thermal resistance, $R_{\theta JC(bot)}$, values in *Thermal Information* table From: 1.4°C/W To: 0.6°C/W (KVU) and From: 3°C/W To: 0.8°C/W (KCS) ... 4

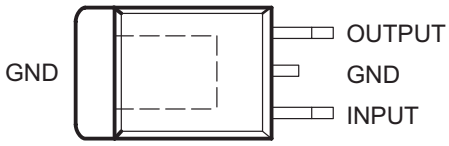
Copyright © 1992–2016, Texas Instruments Incorporated

5 Pin Configuration and Functions

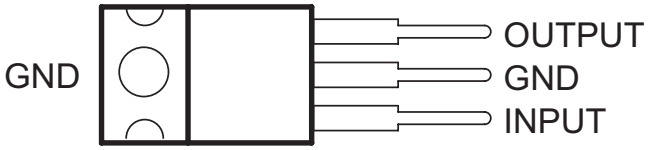
PW Package
20-Pin TSSOP
Top View



KVU Package
3-Pin TO-252
Top View



KCS Package
3-Pin TO-220
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	PW	KVU	KCS		
INPUT	6	1	1	I	Voltage input
OUTPUT	15	3	3	O	Voltage output
GND	5, 16	2	2	—	Ground
HEAT SINK	1, 2, 3, 4, 7, 8, 9, 10, 11, 12, 13, 14 17, 18, 19, 20	—	—	—	Connection for improved thermal dissipation. These terminals have an internal resistive connection to ground and must be grounded or electrically isolated.

Copyright © 1992–2016, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Continuous input voltage, V_I		16	V
Operating virtual junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage	3(1)	12	V
I_O	Output current	0	500	mA
T_J	Operating virtual junction temperature	0	125	°C

(1) Minimum V_I is equal to 3.0 V or V_O(max) + 0.5 V, whichever is greater.

6.4 Thermal Information

THERMAL METRIC(1)(2)		TLV2217			UNIT
		PW (TSSOP)	KVU (TO-252)	KCS (TO-220)	
		20 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.6	31	22.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.1	37.5	34.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32	11.3	8.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	1.9	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.5	11.2	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	0.6	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Copyright © 1992–2016, Texas Instruments Incorporated

6.5 Electrical Characteristics: TLV2217-33

V_I = 4.5 V, I_O = 500 mA, T_J = 25°C, and over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	T_J = 25°C	3.267	3.3	3.333	V
		T_J = 0°C to 125°C	3.234		3.336	
Input voltage regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP} V_I = 4.5 V			–62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0 mA			2	5	mA
	I_O = 500 mA			19	49	

(1) Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω, on the output.

6.6 Electrical Characteristics: TLV2217-25

V_I = 3.3 V, I_O = 500 mA, T_J = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	T_J = 25°C	2.475	2.4	2.525	V
		T_J = 0°C to 125°C	2.45		2.55	
Input voltage regulation	V_I = 3.8 V to 5.5 V			4	12	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP} V_I = 4.5 V			–62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			4	23	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA				400	mV
	I_O = 500 mA				500	
Bias current	I_O = 0 mA			2	5	mA
	I_O = 500 mA			19	49	

(1) Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω, on the output.

6.7 Electrical Characteristics: TLV2217-18

V_I = 3.3 V, I_O = 500 mA, T_J = 25°C, and over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	T_J = 25°C	1.782	1.8	1.818	V
		T_J = 0°C to 125°C	1.764		1.836	
Input voltage regulation	V_I = 3.8 V to 5.5 V			3	9	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{PP} V_I = 4.5 V			–62		dB
Output voltage regulation	I_O = 20 mA to 500 mA			3	17	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA			See(2)		mV
	I_O = 500 mA			See(2)		
Bias current	I_O = 0 mA			2	5	mA
	I_O = 500 mA			19	49	

(1) Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor, with equivalent series resistance of 1.5 Ω, on the output.
(2) Dropout voltage is limited by the input voltage range, with minimum V_I = 3 V.

Copyright © 1992–2016, Texas Instruments Incorporated

6.8 Typical Characteristics

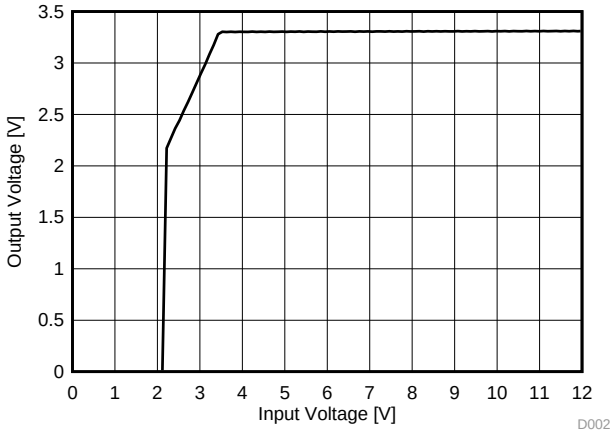


Figure 1. TLV2217-33 Output Voltage vs Input Voltage

Copyright © 1992–2016, Texas Instruments Incorporated

7 Detailed Description

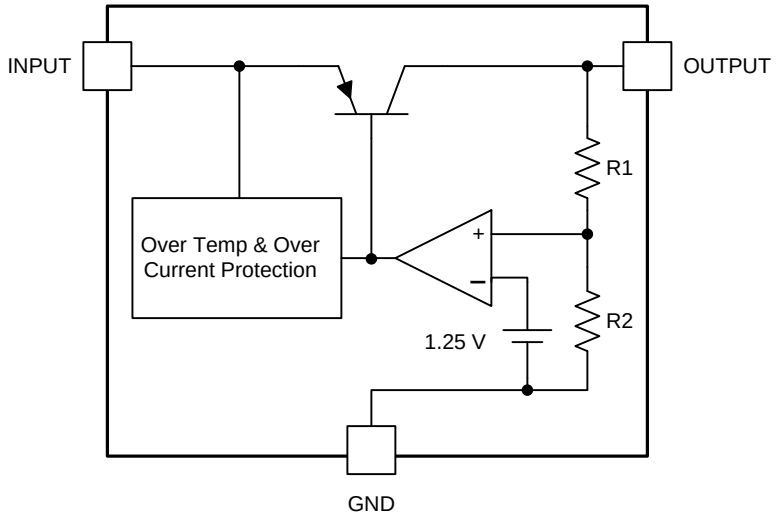
7.1 Overview

The TLV2217 device is a positive low-dropout voltage regulator designed to provide up to 500 mA of output current. The device is available in 1.8-V, 2.5-V, and 3.3-V options. All internal circuitry is designed to operate down to 0.5-V input-to-output differential, with the minimum input voltage of 3 V for all voltage options.

The TLV2217 device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.4 Ω and 2 Ω.

The TLV2217 device is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Overload Block

Current limiting and overtemperature shutdown protects against overload by turning off the PNP pass element.

7.4 Device Functional Modes

7.4.1 Operation With Low Input Voltage

The TLV2217 device requires 0.5-V headroom ($V_I – V_O$) to operate in regulation. With less headroom, the device may drop out and OUTPUT voltage is INPUT voltage minus dropout voltage.

7.4.2 Operation at Light Loads

The load or feedback must consume the minimum bias current defined in *Electrical Characteristics: TLV2217-33* for regulation, or the output may be too high.

7.4.3 Operation in Self Protection

When an overload occurs, the device shuts down the output stage or reduce the output current to prevent device damage. The device automatically resets from the overload. The output may be reduced or alternate between on and off until the overload is removed.

8 Application and Implementation

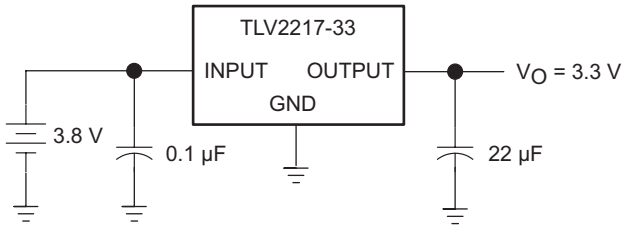
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV2217 is a low-dropout linear regulator and can be used as a fixed output voltage supply for a wide variety of applications up to 500 mA. The TLV2217 has multiple output voltage options including 1.8 V, 2.5 V, and 3.3 V. The TLV2217 requires a minimum of 3 V or ($V_{O(max)}$ + 0.5 V) input to ensure regulation and is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

8.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

Figure 2. Typical Application Schematic

8.2.1 Design Requirements

The input voltage must be high enough so that there is enough headroom for the output to regulate. This specification is defined as the dropout voltage in the *Electrical Characteristics: TLV2217-33*.

A 0.1-µF capacitor must be place on the input to stabilize the input supply, especially if the TLV2217 is not placed near the source of supply.

Output capacitor selection is critical for regulator stability. Larger C_{OUT} values benefit the regulator by improving transient response and loop stability. This device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.4 Ω and 2 Ω. See *Compensation-Capacitor Selection Information* for additional details regarding capacitor selection.

8.2.2 Detailed Design Procedure

8.2.2.1 Compensation-Capacitor Selection Information

The TLV2217 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figure 3 and Figure 4 can be used to establish the capacitance value and ESR range for the best regulator performance.

Copyright © 1992–2016, Texas Instruments Incorporated

Typical Application (continued)

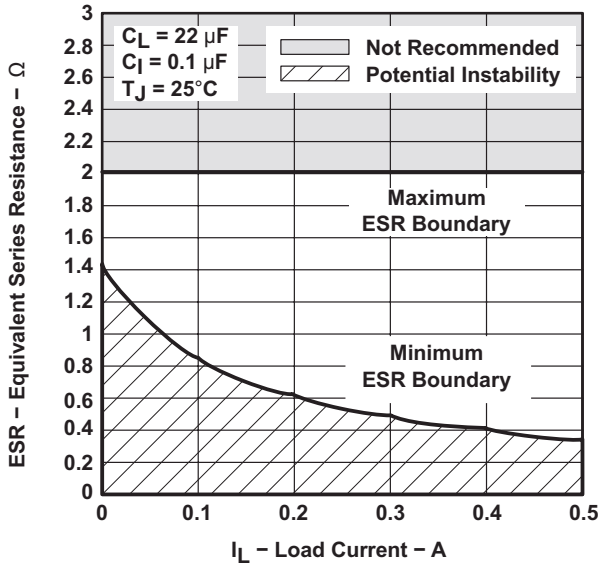


Figure 3. TLV2217 ESR of Output Capacitor vs Load Current

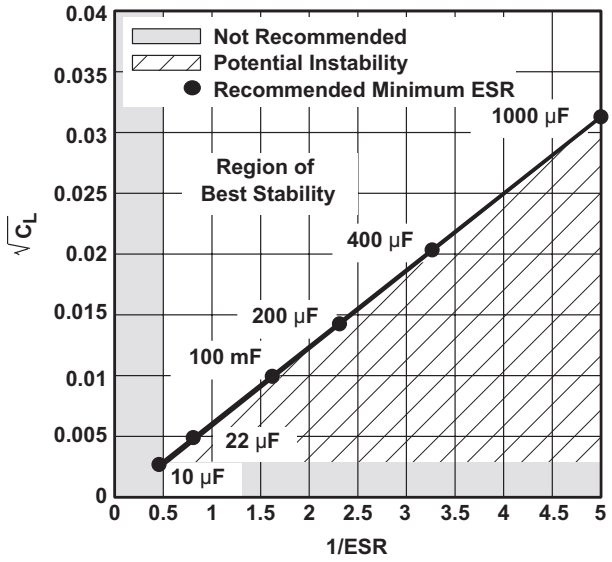


Figure 4. TLV2217 Stability vs ESR

8.2.2.2 High Start-up Current

Due to the structure of the TLV2217, a high peak current is required on start-up. See Figure 5 for the input current characteristic.

NOTE

When the TLV2217 is starting up, it has to overcome the peak current to start regulating at the output. Due to the peak current required for the TLV2217, a resistor connected in series with the input is not recommended, as the I*R drop across the resistor may cause the input voltage to drop below the required headroom for the device.

8.2.3 Application Curves

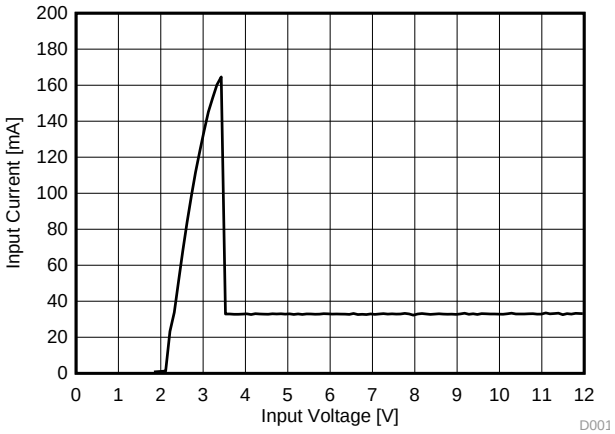


Figure 5. Input Current vs Input Voltage

9 Power Supply Recommendations

See *Recommended Operating Conditions* for the recommended supply voltage range.

10 Layout

10.1 Layout Guidelines

See Figure 6 for an example layout for the TLV2217 using the TO-220 package. Input and output bypass capacitors must be placed as close to the device pins as possible. The output capacitor must have a specified ESR in the range defined by Figure 4. Additionally, the ground pin and thermal tab must be well connected to a ground plane to aid in thermal dissipation.

10.2 Layout Example

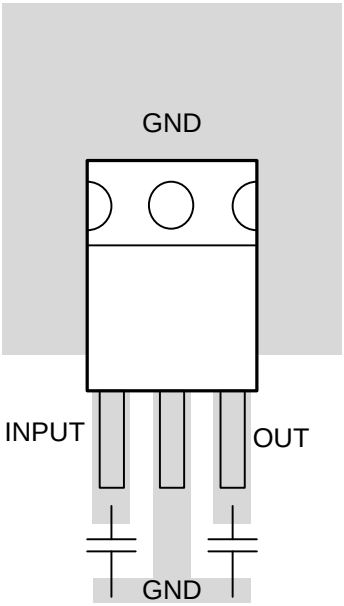


Figure 6. TO-220 Package Example Layout

Copyright © 1992–2016, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 1992–2016, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2217-18KCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TLV2217-18	Samples
TLV2217-18KCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TLV2217-18	Samples
TLV2217-18KVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	2217-18	Samples
TLV2217-25KCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TLV2217-25	Samples
TLV2217-25KVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	2217-25	Samples
TLV2217-25PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	2217-25	Samples
TLV2217-33KCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	TLV2217-33	Samples
TLV2217-33KVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	2217-33	Samples
TLV2217-33PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 125	2217-33	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

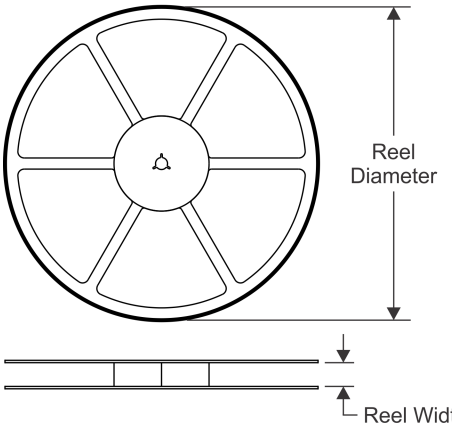
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

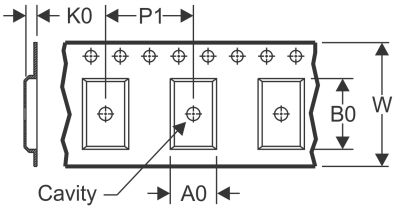
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

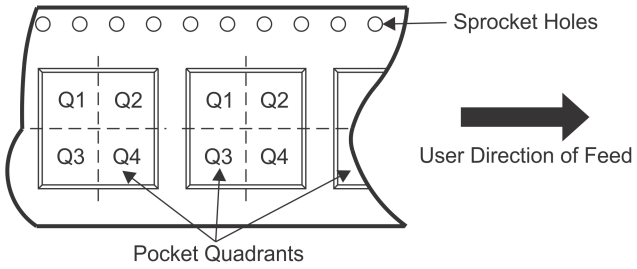


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

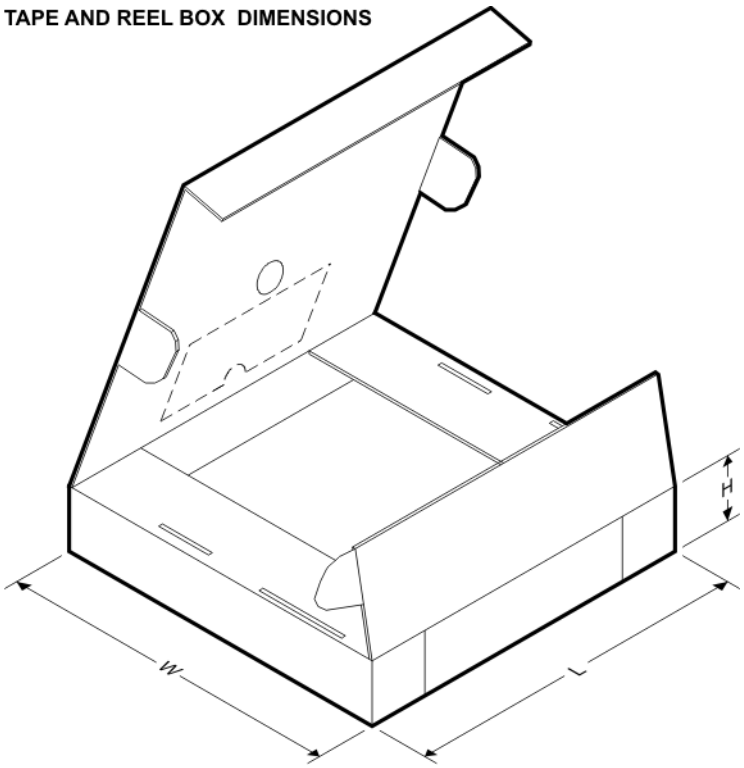
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2217-18KVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV2217-25KVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV2217-25PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLV2217-33KVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TLV2217-33PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

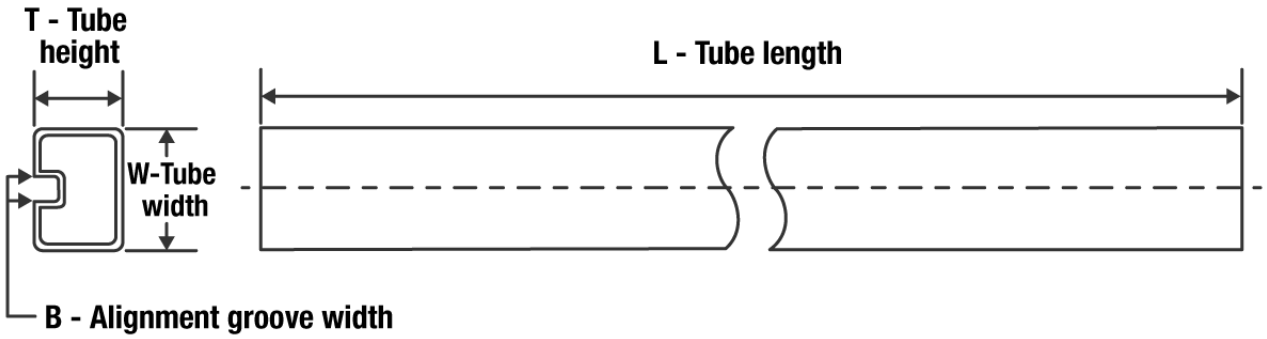
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2217-18KVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV2217-25KVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV2217-25PWR	TSSOP	PW	20	2000	853.0	449.0	35.0
TLV2217-33KVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
TLV2217-33PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

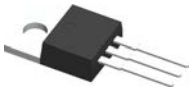
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2217-18KCS	KCS	TO-220	3	50	532	34.1	700	9.6
TLV2217-18KCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
TLV2217-25KCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
TLV2217-33KCSE3	KCS	TO-220	3	50	532	34.1	700	9.6

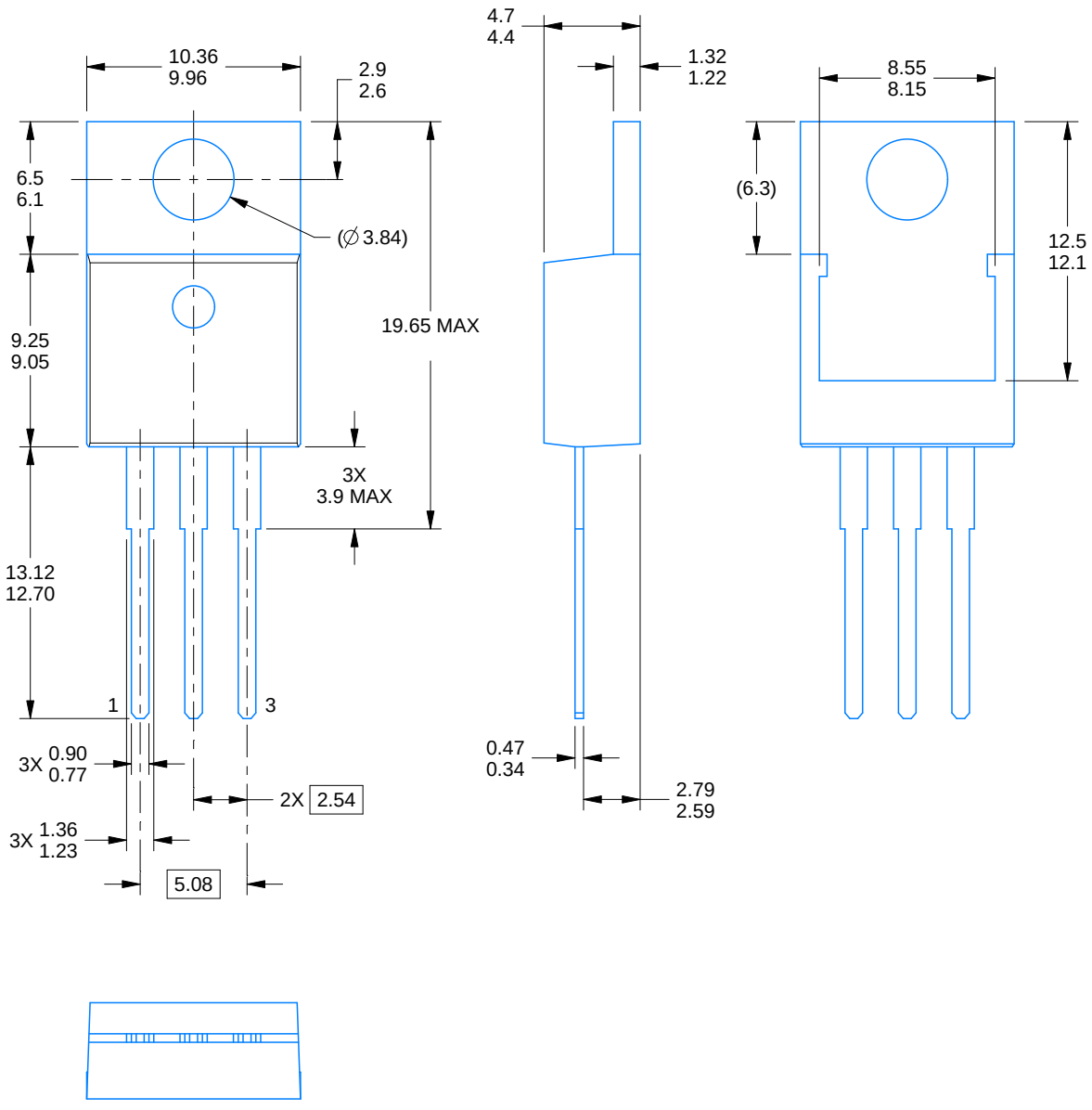
KCS0003B



PACKAGE OUTLINE

TO-220 - 19.65 mm max height

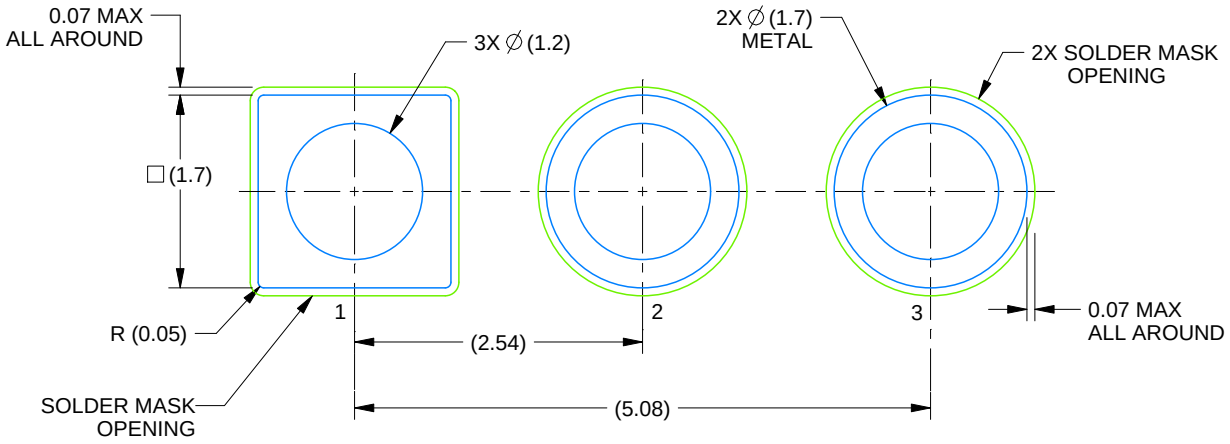
TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

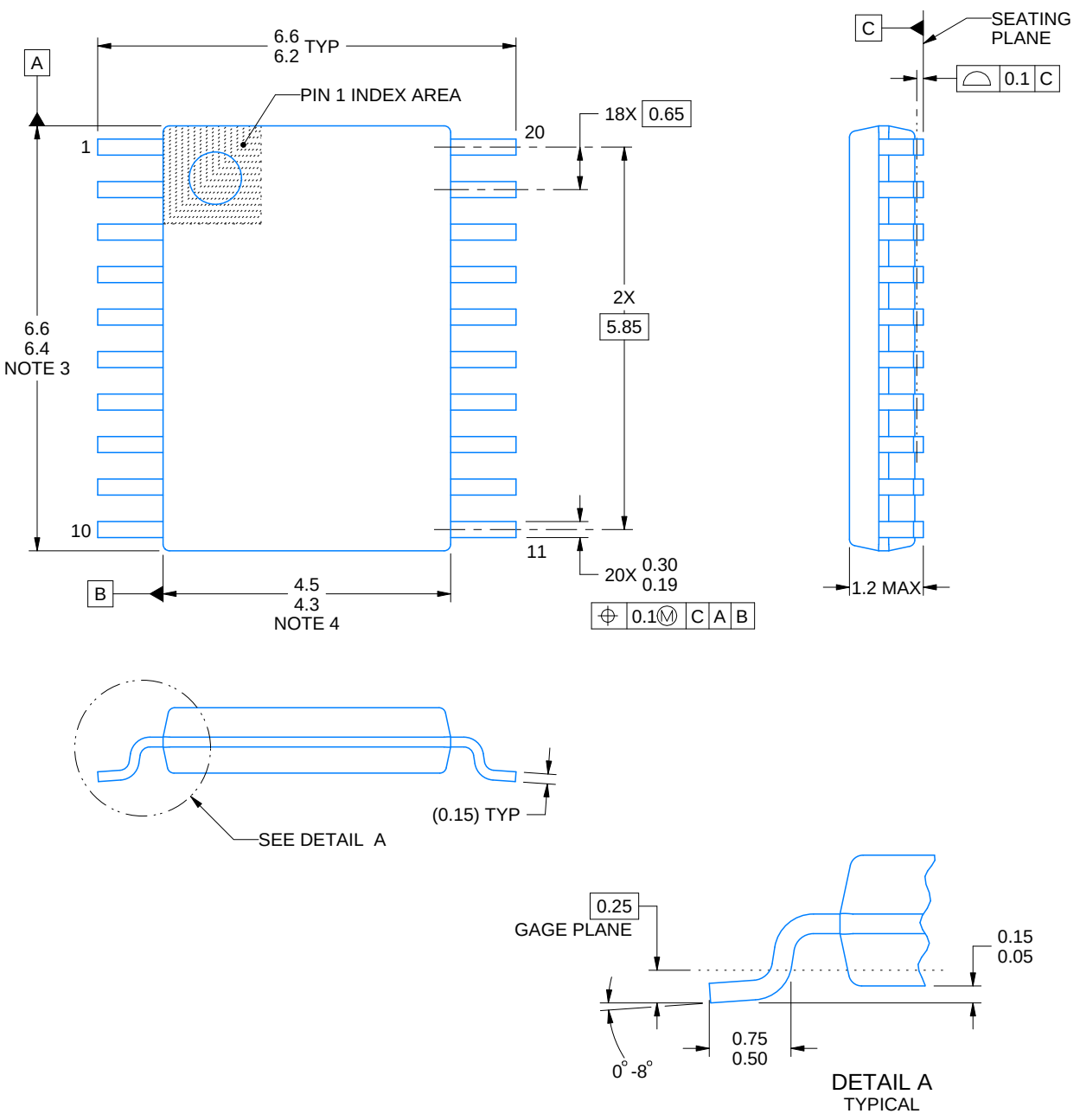
4222214/B 08/2018

PACKAGE OUTLINE

PW0020A

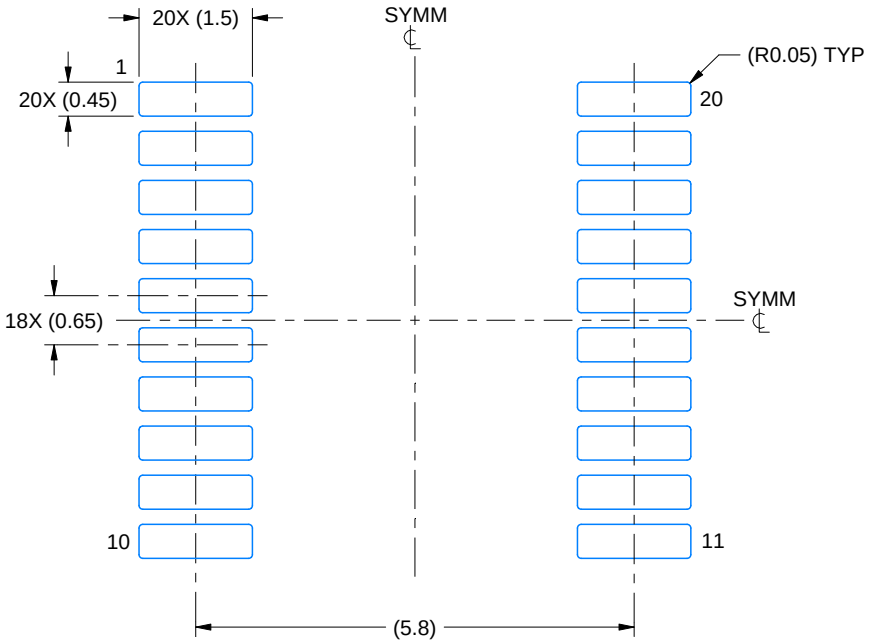
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



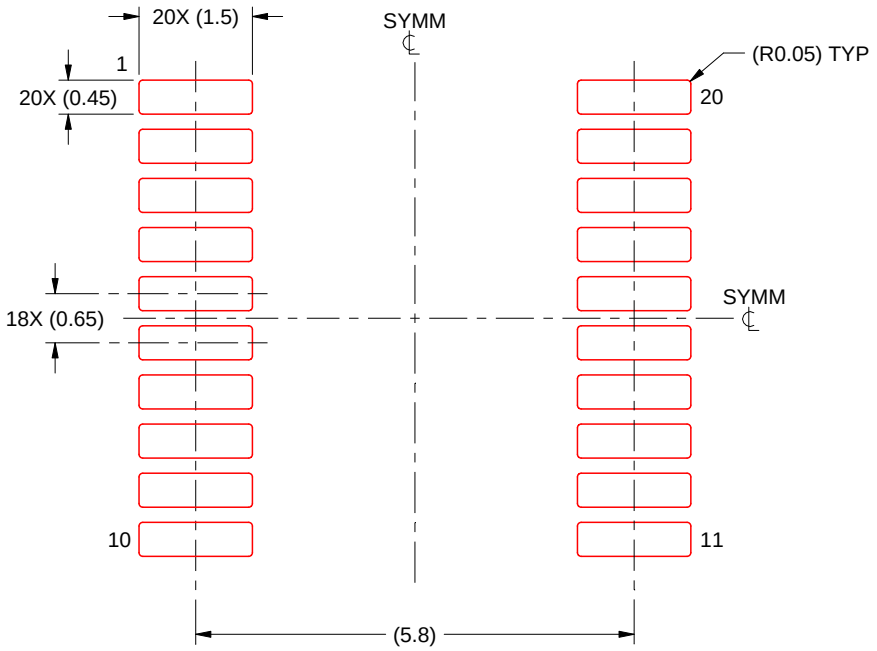
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

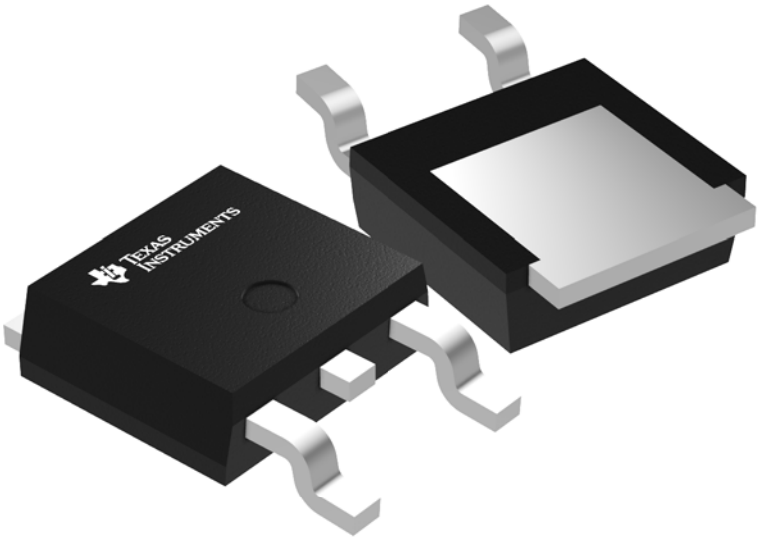
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

KVU 3

TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



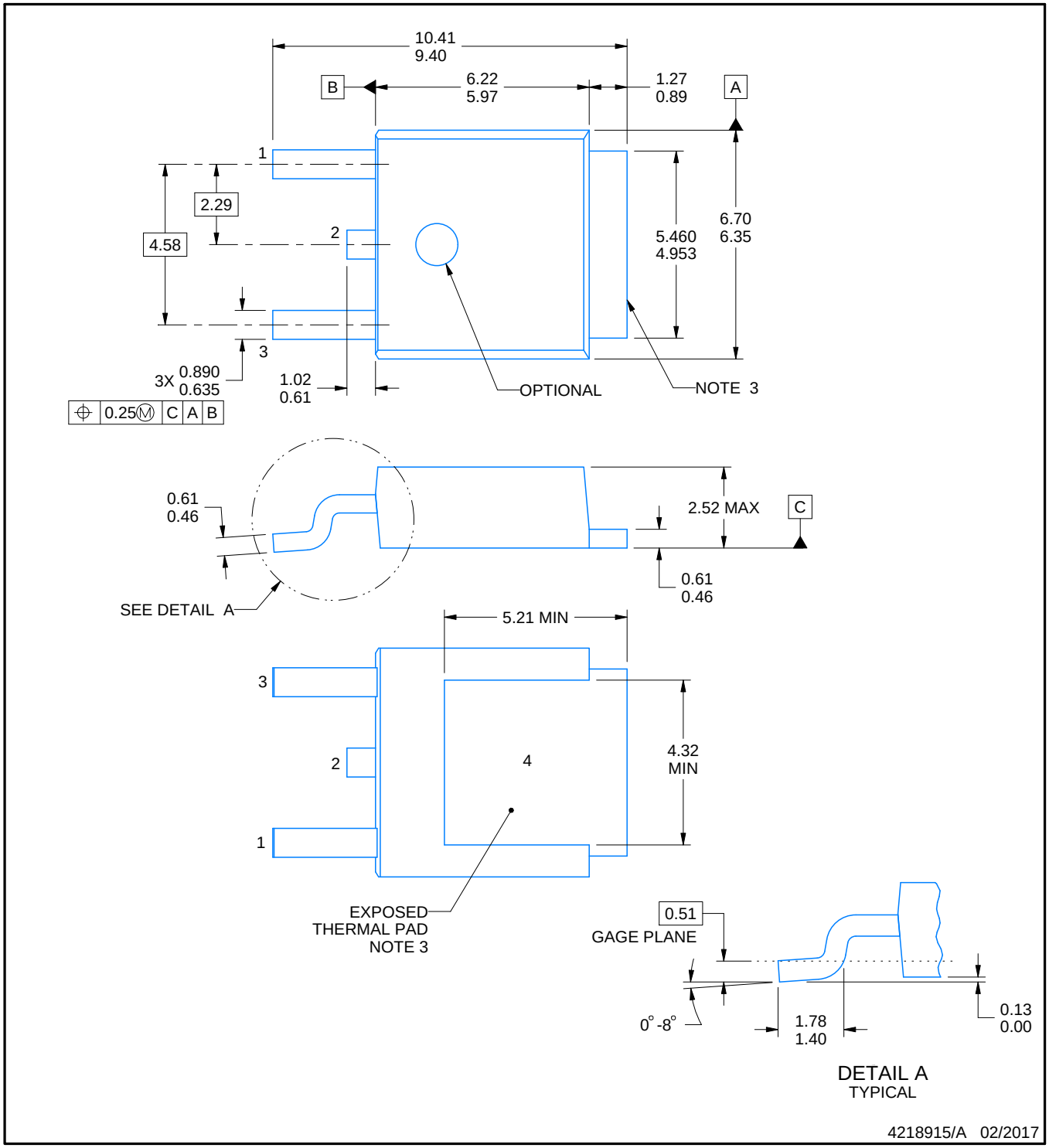
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

KVU0003A

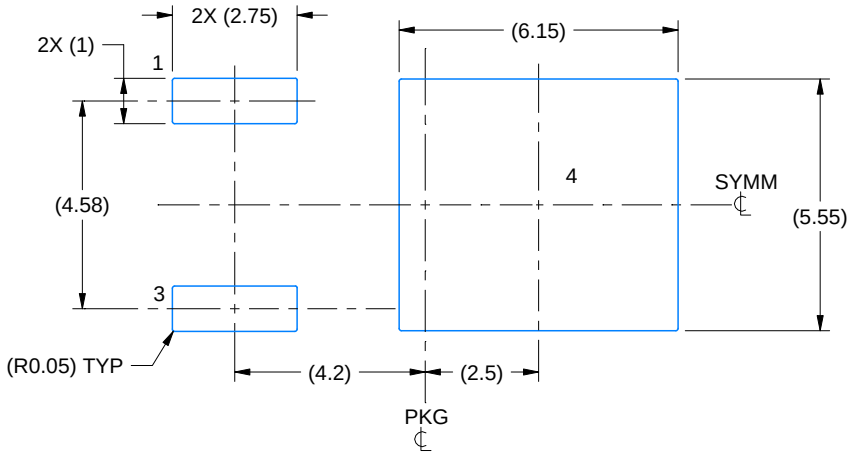
TO-252 - 2.52 mm max height

TO-252

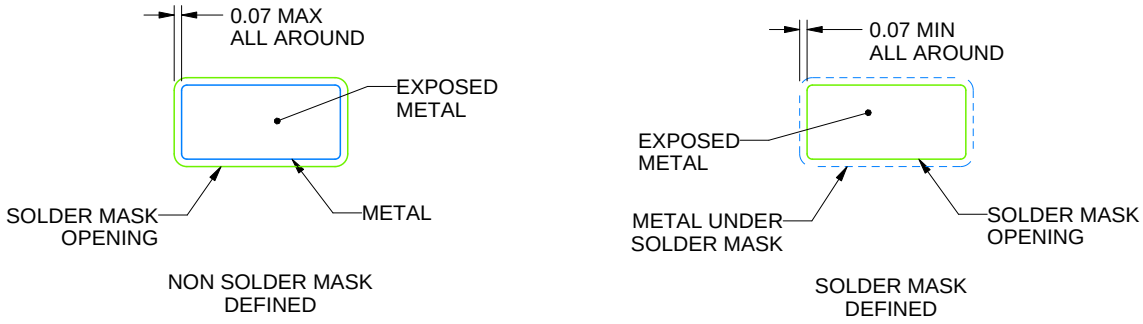


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

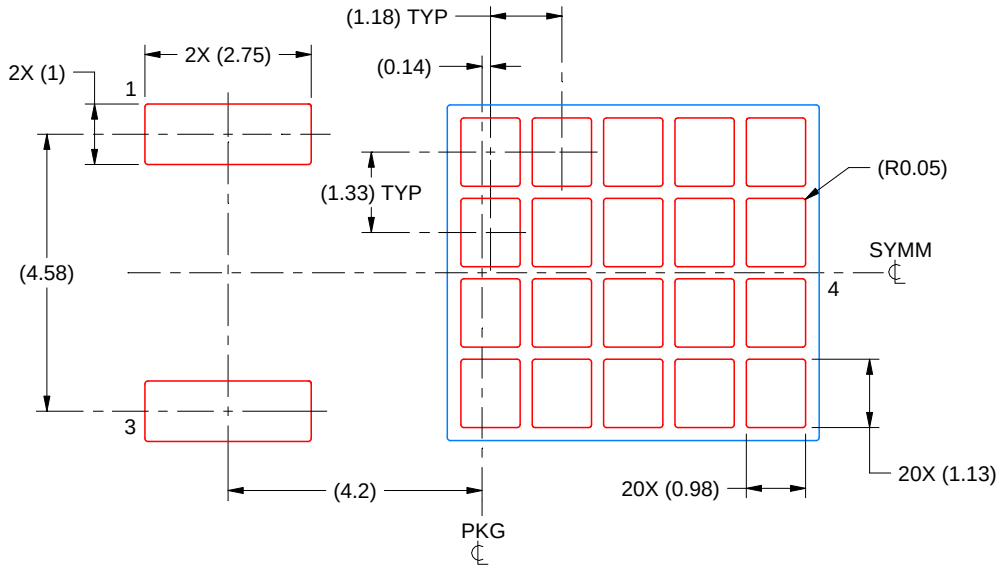
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KVU0003A

TO-252 - 2.52 mm max height

TO-252



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated