TLV62065-Q1 3-MHz 2-A Step-Down Converter in 2-mm × 2-mm WSON Package

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- V_{IN} Range from 2.9 to 5.5 V
- Up to 97% Efficiency
- Power-Save Mode or Fixed Frequency PWM Mode
- Output Voltage Accuracy in PWM Mode ±2%
- Output Capacitor Discharge Function
- Typical 18-µA Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Available in a 2-mm × 2-mm × 0.75-mm WSON

2 Applications

- Automotive Infotainment and Cluster
- Advanced Driver Assistance System (ADAS)
- Automotive Display

3 Description

The TLV62065-Q1 device is a highly-efficient synchronous step-down DC-DC converter with adjustable output voltage. The device operates at a switching frequency of 3 MHz and provides up to 2 A of output current.

With an input voltage range of 2.9 to 5.5 V, the device is a perfect fit for power conversion from a 5-V or 3.3-V system supply rail. The TLV62065-Q1 device enters power-save mode operation at light-load currents to maintain high efficiency over the entire load current range. For low-noise applications, the TLV62065-Q1 device can be forced into fixed-frequency PWM mode by pulling the MODE pin high.

In the shutdown mode, the current consumption is reduced to less than 1 µA and an internal circuit discharges the output capacitor.

The TLV62065-Q1 device operates with a 1-µH inductor and 10-µF output capacitor.

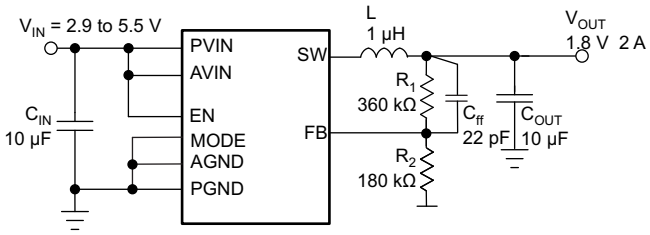
The TLV62065-Q1 device is available in a small 2-mm × 2-mm × 0.75-mm 8-pin WSON package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV62065-Q1	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



Efficiency vs. Load Current

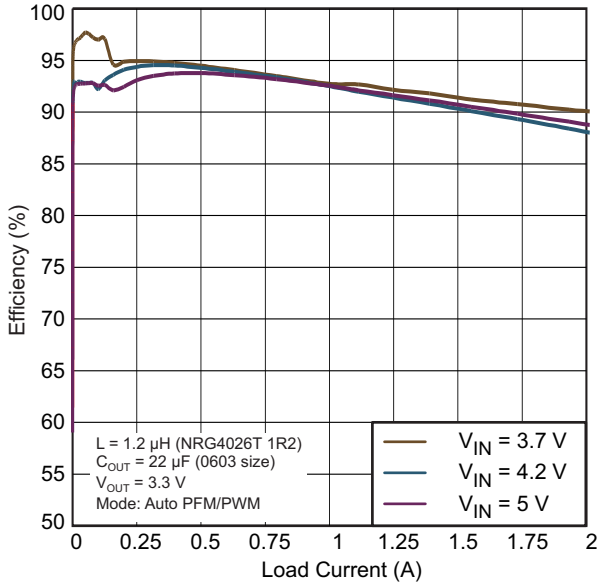


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2012) to Revision B **Page**

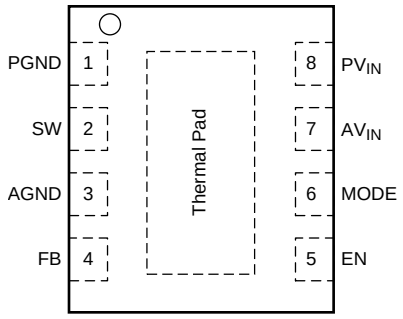
- Changed the *Description* section to state that the TLV62065-Q1 device has an adjustable output voltage. ... 1
- Added the *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed the *Thermal Information* values ... 4
- Deleted the *Parameter Measurement Information* section because the circuit is similar to the application circuit in the *Typical Application* section ... 11
- Changed f_c to f_z and R_2 to R_1 in the feed-forward capacitor equations in the *Output Voltage Setting* section ... 15
- Deleted the *List of Inductors* and *List of Capacitors* tables ... 16

Changes from Original (January 2012) to Revision A **Page**

- Update automotive qualitifcation description and add temperature grade ... 1
- Update Absolute Maximum Ratings ... 4
- Update Electrical Characteristics - Shutdown current max rating ... 5

5 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	3	IN	Analog GND supply pin for the control circuit.
AV_{IN}	7	IN	Analog V_{IN} power supply for the control circuit. This pin must be connected to the PV_{IN} pin and the input capacitor.
EN	5	IN	EN is the enable pin of the device. Pulling this pin low forces the device into shutdown mode. Pulling this pin high enables the device. This pin must be terminated.
FB	4	IN	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In the case of fixed output voltage option, connect this pin directly to the output capacitor.
MODE	6	IN	When the MODE pin is high, the device is forced to operate in fixed-frequency PWM mode. When the MODE pin is low , the device enters the power-save mode with automatic transition from PFM mode to fixed-frequency PWM mode. This pin must be terminated.
PGND	1	PWR	GND supply pin for the output stage
PV_{IN}	8	PWR	V_{IN} power-supply pin for the output stage
SW	2	OUT	SW is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this pin and the output capacitor.
Thermal pad		—	For good thermal performance, this pad must be soldered to the land pattern on the PCB. This pad should be used as device GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	AVIN, PVIN	–0.3	7	V
	EN, MODE, FB	–0.3	V_{IN} + 0.3 < 7	
	SW	–0.3	7	
Current (source)	Peak output	Internally limited		A
Junction temperature, T_J		–40	140	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
	Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	±750	
		Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
AV_{IN} , PV_{IN}	Supply voltage	2.9		5.5	V
	Output current capability			2000	mA
	Output voltage range for adjustable voltage	0.8		V_{IN}	V
L	Effective inductance range	0.7	1	1.6	µH
C_{OUT}	Effective output-capacitance range	4.5	10	22	µF
T_A	Operating ambient temperature(1)	–40		105	°C
T_J	Operating junction temperature	–40		140	°C

(1) In applications where high power dissipation, poor package thermal resistance, or both are present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the device or package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (R_{\theta JA} \times P_{D(max)})$

6.4 Thermal Information

THERMAL METRIC(1)		TLV62065-Q1 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	67.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	7.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 10 µF 0603, C_{OUT} = 10 µF 0603, L = 1 µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.9		5.5	V
I_Q	Operating quiescent current	I_{OUT} = 0 mA, device operating in PFM mode and not device not switching		18		µA
I_{SD}	Shutdown current	EN = GND, current into AVIN and PVIN combined		0.1	5	µA
V_{UVLO}	Undervoltage lockout threshold	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.99	
ENABLE, MODE						
V_{IH}	High-level input voltage	2.9 V ≤ V_{IN} ≤ 5.5 V	1		5.5	V
V_{IL}	Low-level input voltage	2.9 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
I_{IN}	Input bias current	EN, MODE tied to GND or AVIN		0.01	1	µA
POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 3.6 V (1)		120	180	mΩ
		V_{IN} = 5 V (1)		95	150	
$r_{DS(on)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6 V (1)		90	130	mΩ
		V_{IN} = 5 V (1)		75	100	
I_{LIMF}	Forward current limit MOSFET high-side and low-side	3 V ≤ V_{IN} ≤ 3.6 V	2300	2750		mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		10		
OUTPUT						
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage, PWM mode	PWM operation, MODE = V_{IN} , 2.9 V ≤ V_{IN} ≤ 5.5 V, 0-mA load	–2%	0%	2%	
$V_{FB(PFM)}$	Feedback voltage, PFM mode, voltage positioning	Device in PFM mode, voltage positioning active (2)		1%		
V_{FB}	Load regulation			–0.5		%/A
	Line regulation			0		%/V
$R_{(Discharge)}$	Internal discharge resistor	Activated with EN = GND, 2.9 V ≤ V_{IN} ≤ 5.5 V, 0.8 V ≤ V_{OUT} ≤ 3.6 V		200		Ω

(1) Maximum value applies for T_J = 85°C.
(2) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the *Application and Implementation* section.

6.6 Switching Characteristics

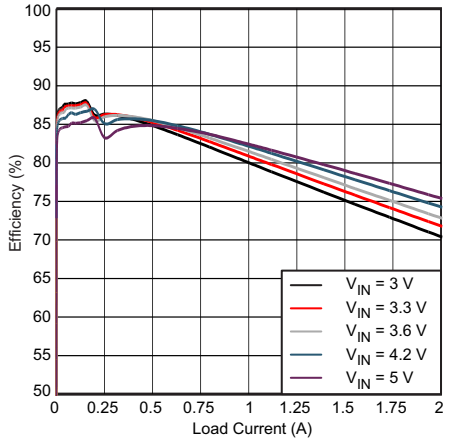
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_{SW}	Oscillator frequency	2.9 V ≤ V_{IN} ≤ 5.5 V	2.6	3	3.4	MHz
OUTPUT						
t_{START}	Startup time	Time from active EN to reach 95% of V_{OUT}		500		µs

6.7 Typical Characteristics

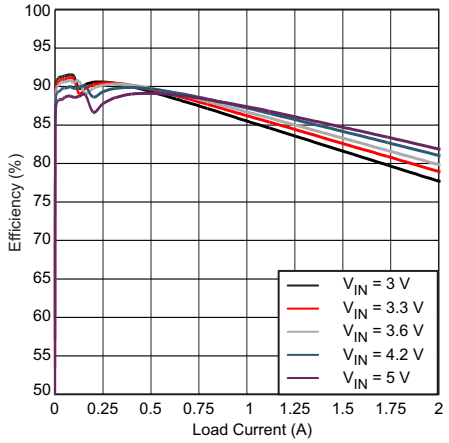
Table 1. Table of Graphs

		FIGURE
η Efficiency	Load Current, V_{OUT} = 1.2 V, Auto PF//PWM Mode, Linear Scale	Figure 1
	Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode, Linear Scale	Figure 2
	Load Current, V_{OUT} = 3.3 V, PFM/PWM Mode, Linear Scale	Figure 3
	Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode vs. Forced PWM Mode, Logarithmic Scale	Figure 4
Output Voltage Accuracy	Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode	Figure 5
	Load Current, V_{OUT} = 1.8 V, Forced PWM Mode	Figure 6
Shutdown Current	Input Voltage and Ambient Temperature	Figure 7
Quiescent Current	Input Voltage	Figure 8
Oscillator Frequency	Input Voltage	Figure 9
Static Drain-Source On-State Resistance	Input Voltage, Low-Side Switch	Figure 10
	Input Voltage, High-Side Switch	Figure 11
$R_{DISCHARGE}$	Input Voltage vs. V_{OUT}	Figure 12
Typical Operation	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 500 mA, L = 1.2 µH, C_{OUT} = 10 µF	Figure 13
	PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 20 mA, L = 1.2 µH, C_{OUT} = 10 µF	Figure 14
Load Transient	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 0.2 mA to 1 A	Figure 15
	PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 20 mA to 250 mA	Figure 16
	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 200 mA to 1500 mA	Figure 17
Line Transient	PWM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	Figure 18
	PFM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	Figure 19
Startup into Load	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, Load = 2.2-Ω	Figure 20
Output Discharge	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, No Load	Figure 21



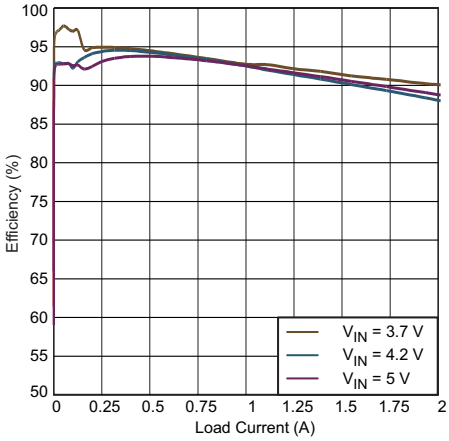
V_{OUT} = 1.2 V Linear Scale
L = 1.2 µH (NRG4026T 1R2) C_{OUT} = 10 µF (0603 size)

Figure 1. Efficiency vs Load Current Auto PFM and PWM MODE



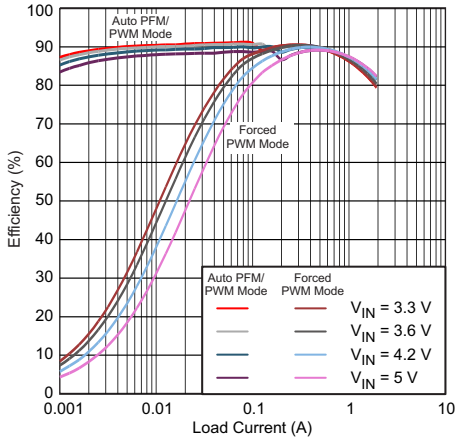
V_{OUT} = 1.8 V Linear Scale
L = 1.2 µH (NRG4026T 1R2) C_{OUT} = 10 µF (0603 size)

Figure 2. Efficiency vs Load Current Auto PFM and PWM MODE



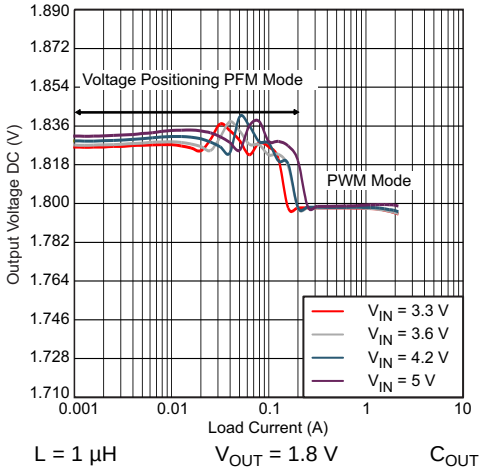
V_{OUT} = 3.3 V Linear Scale
L = 1.2 µH (NRG4026T 1R2) C_{OUT} = 22 µF (0603 size)

Figure 3. Efficiency vs Load Current Auto PFM and PWM MODE



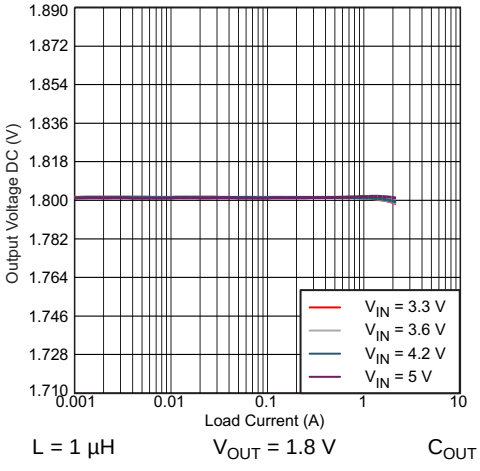
V_{OUT} = 1.8 V Logarithmic Scale
C_{OUT} = 10 µF (0603 size) L = 1.2 µH (NRG4026T 1R2)

Figure 4. Efficiency vs Load Current Auto PFM and PWM Mode vs. Forced PWM Mode



L = 1 µH V_{OUT} = 1.8 V C_{OUT} = 10 µF

Figure 5. Output Voltage Accuracy vs Load Current Auto PFM and PWM MODE



L = 1 µH V_{OUT} = 1.8 V C_{OUT} = 10 µF

Figure 6. Output Voltage Accuracy vs Load Current Forced PWM MODE

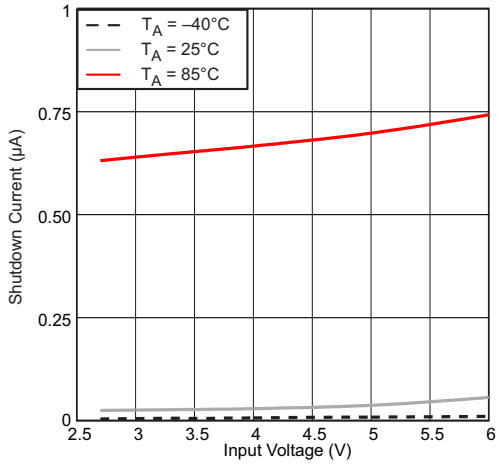


Figure 7. Shutdown Current vs Input Voltage and Ambient Temperature

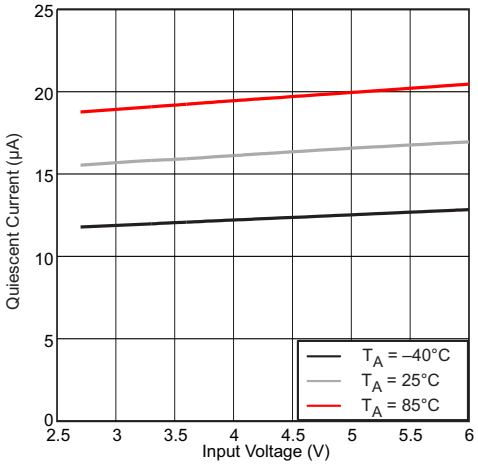


Figure 8. Quiescent Current vs Input Voltage

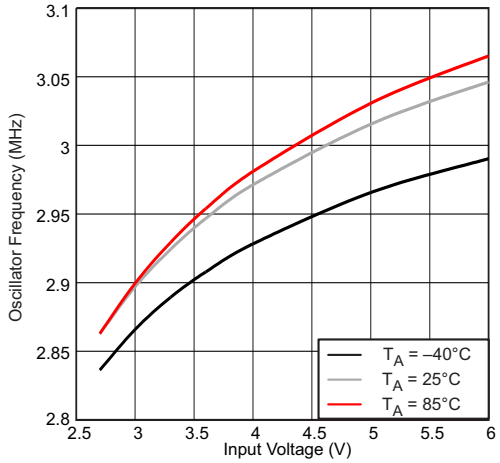
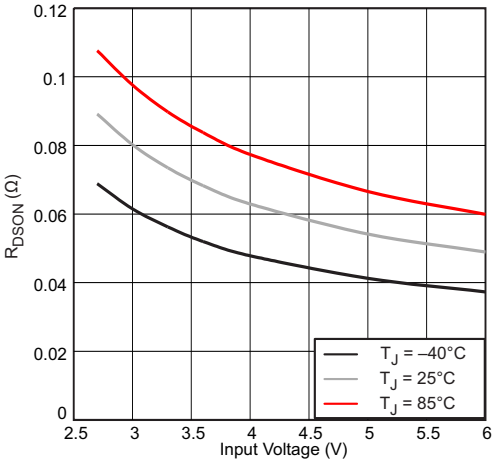
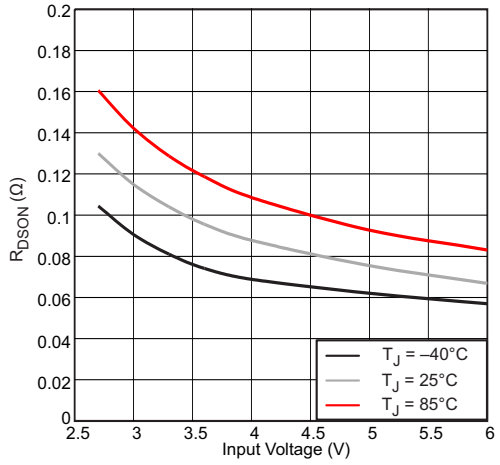


Figure 9. Oscillator Frequency vs Input Voltage



Low-Side Switch

Figure 10. Static Drain-Source On-State Resistance vs Input Voltage



High-Side Switch

Figure 11. Static Drain-Source On-State Resistance vs Input Voltage

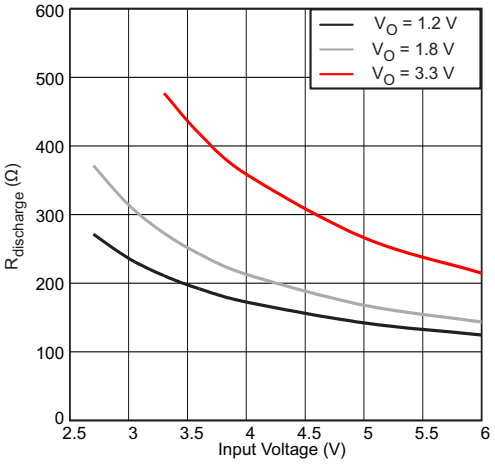
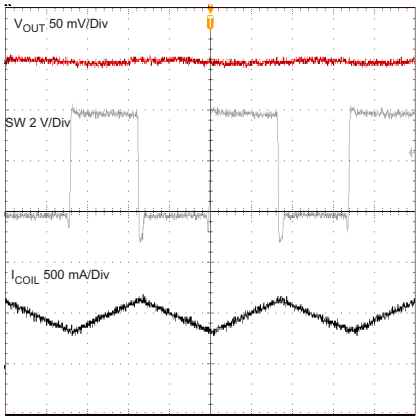
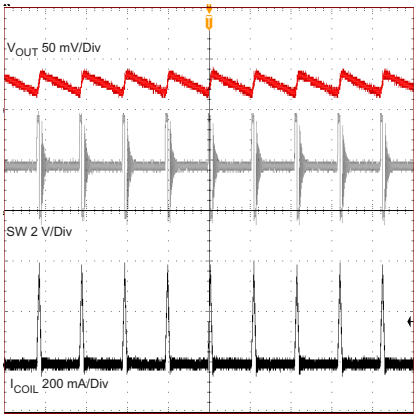


Figure 12. $R_{DISCHARGE}$ vs Input Voltage



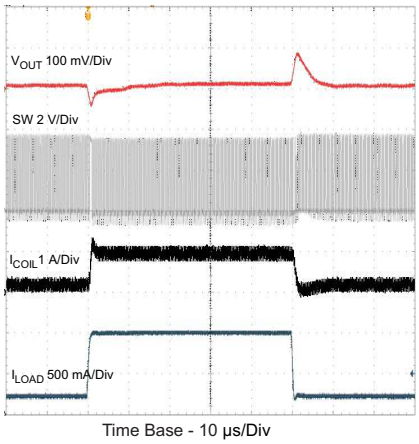
V_{IN} = 3.6 V V_{OUT} = 1.8 V MODE = GND
C_{OUT} = 10 µF L = 1.2 µH I_{OUT} = 500 mA

Figure 13. Typical Operation (PWM Mode)



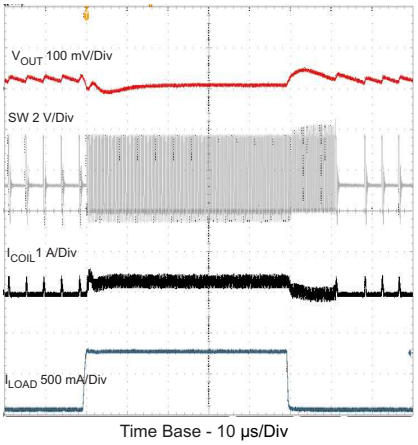
V_{IN} = 3.6 V V_{OUT} = 1.8 V MODE = GND
C_{OUT} = 10 µF L = 1.2 µH I_{OUT} = 20 mA

Figure 14. Typical Operation (PFM Mode)



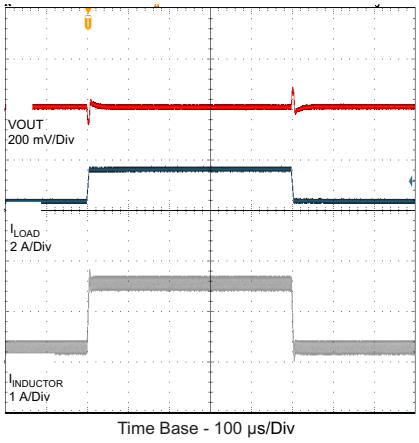
V_{IN} = 3.6 V V_{OUT} = 1.2 V I_{OUT} = 0.2 to 1 A

Figure 15. Load Transient Response, MODE = V_{IN} PWM Mode 0.2 A To 1 A



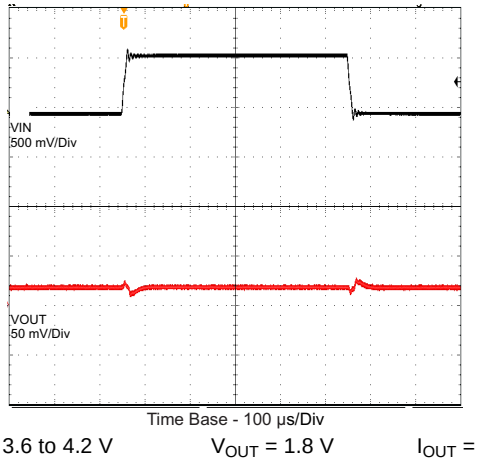
V_{IN} = 3.6 V V_{OUT} = 1.2 V I_{OUT} = 20 to 250 mA

Figure 16. Load Transient PFM Mode 20 mA to 250 mA



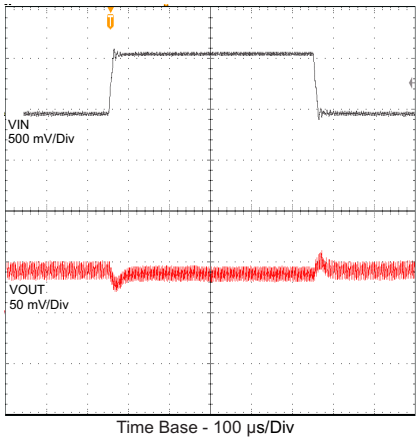
V_{IN} = 3.6 V V_{OUT} = 1.8 V L = 1.2 µH
C_{OUT} = 10 µF I_{OUT} = 200 to 1500 mA

Figure 17. Load Transient Response 200 mA To 1500 mA



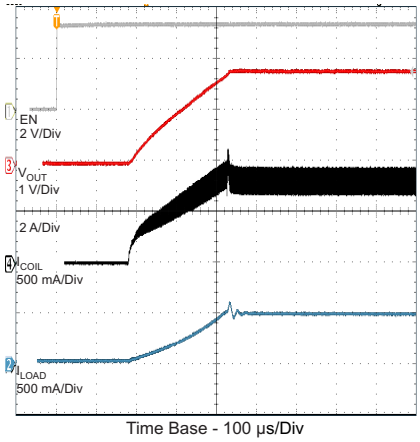
V_{IN} = 3.6 to 4.2 V V_{OUT} = 1.8 V I_{OUT} = 500 mA
C_{OUT} = 10 µF L = 1.2 µH

Figure 18. Line Transient Response PWM Mode



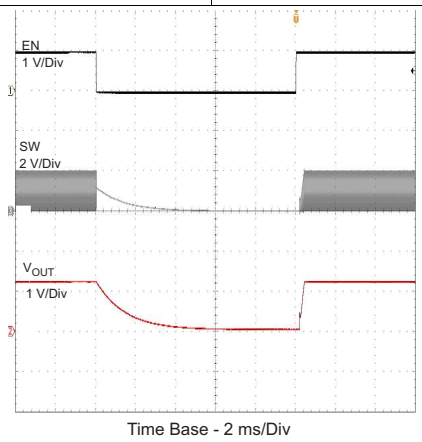
V_{IN} = 3.6 to 4.2 V V_{OUT} = 1.8 V I_{OUT} = 500 mA
C_{OUT} = 10 µF L = 1.2 µH

Figure 19. Line Transient PFM Mode



V_{IN} = 3.6 V V_{OUT} = 1.8 V Load = 2.2 Ω
C_{OUT} = 10 µF L = 1.2 µH

Figure 20. Startup Into Load



V_{IN} = 3.6 V V_{OUT} = 1.8 V No load
C_{OUT} = 10 µF

Figure 21. Output Discharge

7 Detailed Description

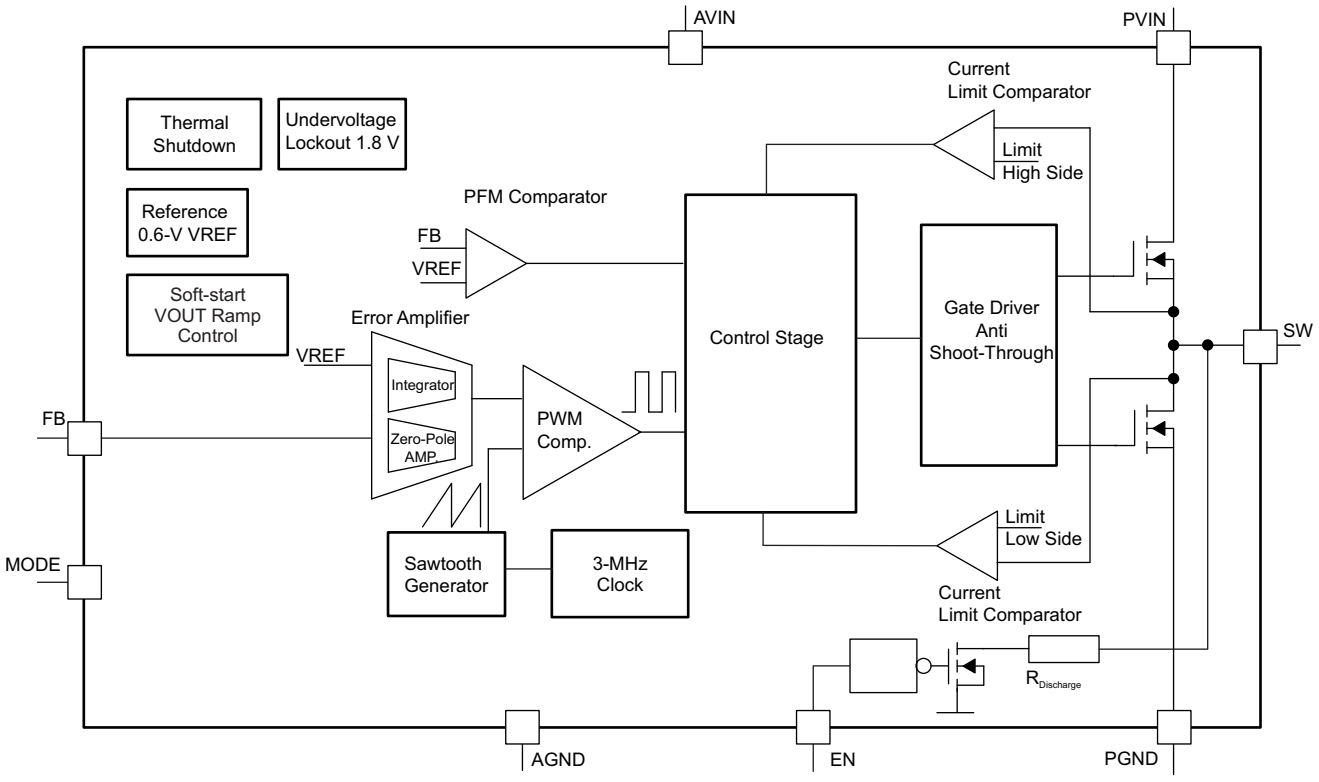
7.1 Overview

The TLV62065-Q1 step-down converter operates with a typical 3-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power-save mode, and then operates in pulse-frequency mode (PFM).

During PWM operation, the converter uses a unique fast-response voltage-mode controller scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current now flows from the input capacitor through the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch in case the current-limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current now flows from the inductor to the output capacitor and to the load. The current returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable

The device is enabled by setting the EN pin high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltages reaches 95% of the nominal value within t_{START} of typically 500 µs after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC-DC converters. To drive the EN pin high and get a sequencing of supply rails, connect the EN pin to the output of another converter. With EN = GND, the device enters shutdown mode. In this mode, all circuits are disabled and the SW pin is connected to PGND through an internal resistor to discharge the output.

7.3.2 Mode Selection

The MODE pin allows mode selection between forced PWM mode and power-save mode.

Connecting this pin to GND enables the power-save mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed-frequency PWM mode even at light load currents which allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

7.3.3 Soft-Start Functionality

The TLV62065-Q1 device has an internal soft-start circuit that controls the ramp-up of the output voltage. When the converter is enabled and the input voltage is above the undervoltage lockout threshold, V_{UVLO}, the output voltage ramps up from 5% to 95% of the nominal value within a t_{Ramp} of 250 µs (typical).

This ramping limits the inrush current in the converter during startup and prevents possible input-voltage drops when a battery or high-impedance power source is used.

During soft start, the switch current limit is reduced to 1/3 of the nominal value, I_{LIMF}, until the output voltage reaches 1/3 of the nominal value. When the output voltage trips this threshold, the device operates with the nominal current-limit, I_{LIMF}.

7.3.4 Internal Current-Limit and Foldback Current-Limit For Short-Circuit Protection

During normal operation, the high-side and low-side MOSFET switches are protected by the current limits, I_{LIMF}. When the high-side MOSFET switch reaches the current limit, it is turned off and the low-side MOSFET switch is turned on. The high-side MOSFET switch can only turn on again when the current in the low-side MOSFET switch decreases below the current-limit, I_{LIMF}. The device is capable of providing peak inductor currents up to the internal-current limit $_{ILIMF}$.

As soon as the switch-current limits are hit and the output voltage falls below 1/3 of the nominal output voltage because of an overload or short-circuit condition, the foldback current limit is enabled. In this case, the switch-current limit is reduced to 1/3 of the nominal value, I_{LIMF}.

Because the short-circuit protection is enabled during startup, the device does not deliver more than 1/3 of the nominal current-limit, I_{LIMF}, until the output voltage exceeds 1/3 of the nominal output voltage. This must be considered when a load which acts as a current sink is connected to the output of the converter.

Feature Description (continued)

7.3.5 100% Duty Cycle Low-Dropout Operation

The device begins to enter 100% duty cycle mode as the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN}, the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage differential. This differential voltage is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and is calculated using Equation 1.

$$V_{IN}min = V_O max + I_O max \times (R_{DS(on)}max + R_L) \quad (1)$$

where

- $I_O$max = maximum output current
- $R_{DS(on)}$max = maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_O$max = nominal output voltage plus maximum output voltage tolerance

7.3.6 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. The UVLO circuit disables the output stage of the converter once the falling V_{IN} trips the undervoltage lockout threshold V_{UVLO}. The undervoltage lockout threshold V_{UVLO} for falling V_{IN} is typically 1.78 V. The device begins operation when the rising V_{IN} trips the undervoltage lockout threshold V_{UVLO} again at 1.95 V (typical).

7.3.7 Output Capacitor Discharge

With EN = GND, the device enters shutdown mode and disables all internal circuits. An internal resistor connects the SW pin is to PGND to discharge the output capacitor. This feature ensures startup with a discharged output capacitor when the converter is enabled again and prevents a *floating* charge on the output capacitor. The output voltage ramps up monotonic, starting from 0 V.

7.3.8 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues operation with a soft-start when the junction temperature falls below the thermal shutdown hysteresis.

7.4 Device Functional Modes

7.4.1 Power Save Mode

Pulling the TLV62065-Q1 MODE pin low enables power-save mode. If the load current decreases, the converter enters power-save mode operation automatically. In power-save mode, the converter skips switching and operates with reduced frequency in the PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage 1% (typical) above the nominal output voltage. This voltage-positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs when the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

In power-save mode, a PFM comparator monitors the output voltage. As the output voltage falls below the PFM comparator threshold of $V_{OUTnominal}$ + 1%, the device begins a PFM current pulse. For this pulse, the high-side MOSFET switch turns on and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with 18-µA current consumption (typical).

Device Functional Modes (continued)

In case the output voltage is still below the PFM comparator threshold, further PFM current pulses are generated until the PFM comparator threshold is reached. The converter begins switching again when the output voltage drops below the PFM comparator threshold because of the load current.

The device leaves PFM mode and goes to PWM mode in case the output current can no longer be supported in PFM mode.

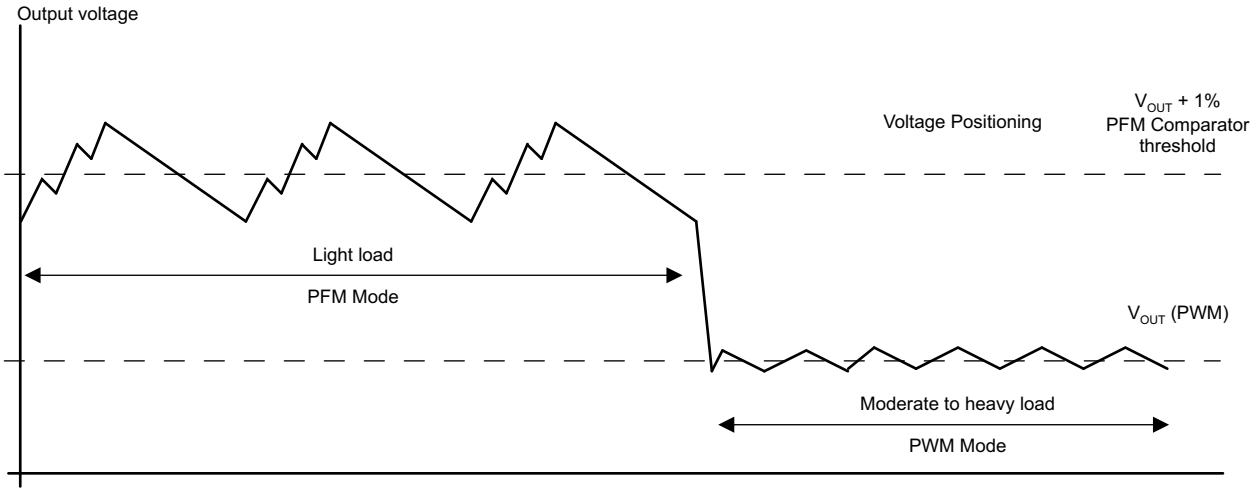


Figure 22. Power Save Mode Operation With Automatic Mode Transition

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV62065-Q1 device is a highly efficient, synchronous step-down, DC-DC converter with an adjustable output voltage and an output current of up to 2 A. The device can be used in buck converter applications with an input range from 2.9 to 5.5 V.

8.2 Typical Application

The typical application circuit (see Figure 23) is optimized for an output voltage of 1.8 V and a load current of 2 A maximum for an input voltage from 2.9 to 5.5 V.

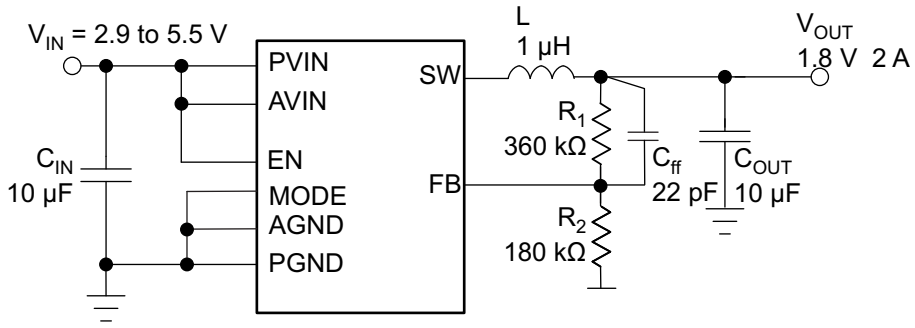


Figure 23. TLV62065-Q1 1.8-V Adjustable Output Voltage Configuration

8.2.1 Design Requirements

The input voltage for this device must be from 2.9 V to 5.5 V. The output voltage must be set using an external voltage divider. The internal compensation network of the device is optimized for an LC output filter that is composed of a 1-µH inductor and a 10-µF ceramic capacitor with a suitable external feed-forward capacitor calculated based on the voltage divider resistor. The *Recommended Operating Conditions* table specifies the allowed range for input voltages, output voltages, output current, inductance, and capacitance. The values listed in this table must be followed when designing the regulator. Low-ESR ceramic capacitors should be used at the input and output for better filtering and ripple performance. The *Detailed Design Procedure* section provides the necessary equations and guidelines for selecting external components for this regulator.

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Setting

Use Equation 2 to calculate the output voltage.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

A typical an internal reference voltage, V_{REF}, is 0.6 V.

To minimize the current through the feedback divider network, R_2, should be within the range of 120 kΩ to 360 kΩ. To keep the network robust against noise the sum of R_1 and R_2 should not exceed approximately 1 MΩ. An external feed-forward capacitor, C_{ff}, is required for optimum regulation performance. Lower resistor values can be used. R_1 and C_{ff} place a zero in the loop. Use Equation 4 to calculate the value of C_{ff} .

Typical Application (continued)

$$f_Z = \frac{1}{2 \times \pi \times R_1 \times C_{ff}} = 25\ \text{kHz} \quad (3)$$

$$C_{ff} = \frac{1}{2 \times \pi \times R_1 \times 25\ \text{kHz}} \quad (4)$$

8.2.2.2 Output Filter Design (inductor And Output Capacitor)

The internal compensation network of the TLV62065-Q1 device is optimized for an LC output filter with a corner frequency that is calculated with Equation 5

$$f_c = \frac{1}{2 \times \pi \times \sqrt{(1\,\mu\text{H} \times 10\,\mu\text{F})}} = 50\ \text{kHz} \quad (5)$$

The device operates with nominal inductors of 1 µH to 1.2 µH and with 10 µF to 22 µF small X5R and X7R ceramic capacitors. The device is optimized for a 1-µH inductor and 10-µF output capacitor.

8.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for the DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

Use Equation 6 to calculate the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 7. This value is recommended because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f}$$

where

- ΔI_L = Peak-to-peak inductor ripple current
- L = Inductor value
- f = Switching frequency (3 MHz typical) (6)

$$I_{L\,max} = I_{OUT\,max} + \frac{\Delta I_L}{2}$$

where

- I_{Lmax} = Maximum inductor current (7)

A more conservative approach is to select the inductor current rating just for the switch-current limit $I_{LIMF}$of the converter.

The total losses of the coil have a strong impact on the efficiency of the DC-DC conversion and consist of both the losses in the DC resistance $R_{(DC)}$ and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Typical Application (continued)

8.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the TLV62065-Q1 device allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output-voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V- and Z5U-dielectric capacitors, aside from a wide variation in capacitance over temperature, become resistive at high frequencies and may not be used. For most applications, a nominal 10-µF or 22-µF capacitor is suitable. In small ceramic capacitors, the DC-bias effect decreases the effective capacitance. Therefore a 22-µF capacitor can be used for output voltages higher than 2 V.

In case additional ceramic capacitors in the supplied system are connected to the output of the DC-DC converter, the output capacitor C_{OUT} must be decreased in order not to exceed the recommended effective capacitance range. In this case, a loop-stability analysis must be performed as described in the *Checking Loop Stability* section.

Use Equation 8 to calculate the RMS ripple current at the nominal load current and while the device is in PWM mode.

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

8.2.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and minimizing interference with other circuits caused by high input voltage spikes. For most applications a 10-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability, or could even damage the part by exceeding the maximum ratings.

8.2.2.3 Checking Loop Stability

The first step of circuit and stability evaluation is to look at the following signals from a steady-state perspective:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These signals are the basic signals that must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter, or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This instability is often a result of board layout, wrong L-C output filter combinations, or both. As a next step in the evaluation of the regulation loop, the transient response of the load is tested. During the time between the application of the load transient and the turnon of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta_{I(LOAD)} \times ESR$, where ESR is the effective series resistance of C_{OUT}. $\Delta_{I(LOAD)}$ begins to charge or discharge C_O, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode at medium-to-high load currents.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing; that helps evaluate stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin.

Typical Application (continued)

8.2.3 Application Curves

For the application curves, see the graphs listed in Table 2.

Table 2. Table of Graphs

		FIGURE
Output Voltage Accuracy	Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode	Figure 5
	Load Current, V_{OUT} = 1.8 V, Forced PWM Mode	Figure 6

9 Power Supply Recommendations

The TLV62065-Q1 device is designed to operate from an input voltage up to 5.5 V. For the input pins (PVIN and AVIN), a small ceramic capacitor with a typical value of 10 µF is recommended for most applications. Capacitance derating for aging, temperature, and DC bias must be taken into account while determining the capacitor value.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line regulator, load regulation or both and have stability issues as well as EMI and thermal problems. Providing a low-inductance, low-impedance ground path is critical. Therefore, use wide and short traces for the main current paths. The input capacitor as well as the inductor and output capacitor should be placed as close as possible to the IC pins.

Connect the AGND and PGND pins of the device to the thermal pad land of the PCB and use this pad as a star point. To minimize the effects of ground noise use a common power node (PGND), and a different node (AGND) for the signal. The FB divider network should be connected directly to the output capacitor and the FB line must be routed away from noisy components and traces (for example, the SW line).

Because of the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. For good thermal performance, PCB design of at least four layers is recommended. The thermal pad of the IC must be soldered on the power pad area on the PCB to achieve proper thermal connection. Additionally, for good thermal performance, the thermal pad on the PCB must be connected to an inner GND plane with sufficient via connections.

10.2 Layout Example

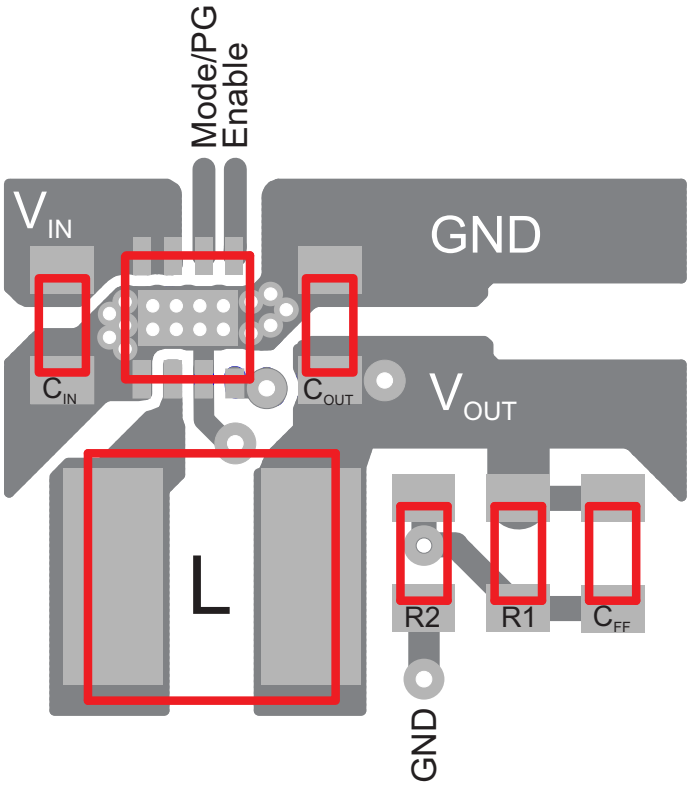


Figure 24. PCB Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

TLV62065EVM-719 User's Guide (SLVU424)

11.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62065TDSGRQ1	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SCD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV62065-Q1 :

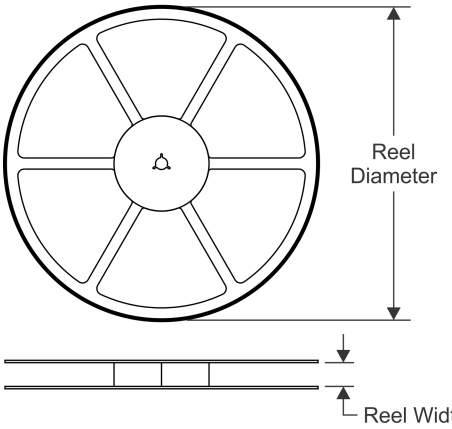
- Catalog: TLV62065

NOTE: Qualified Version Definitions:

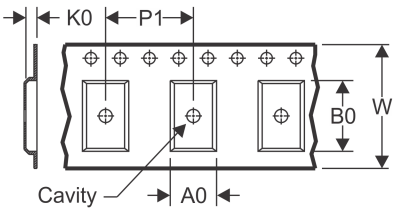
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

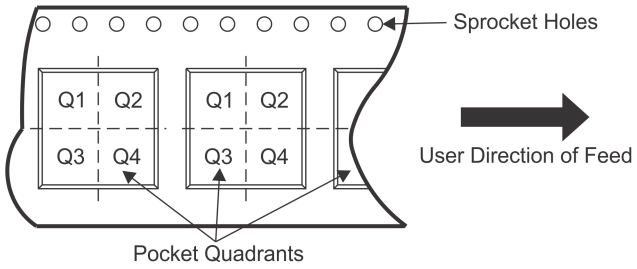


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

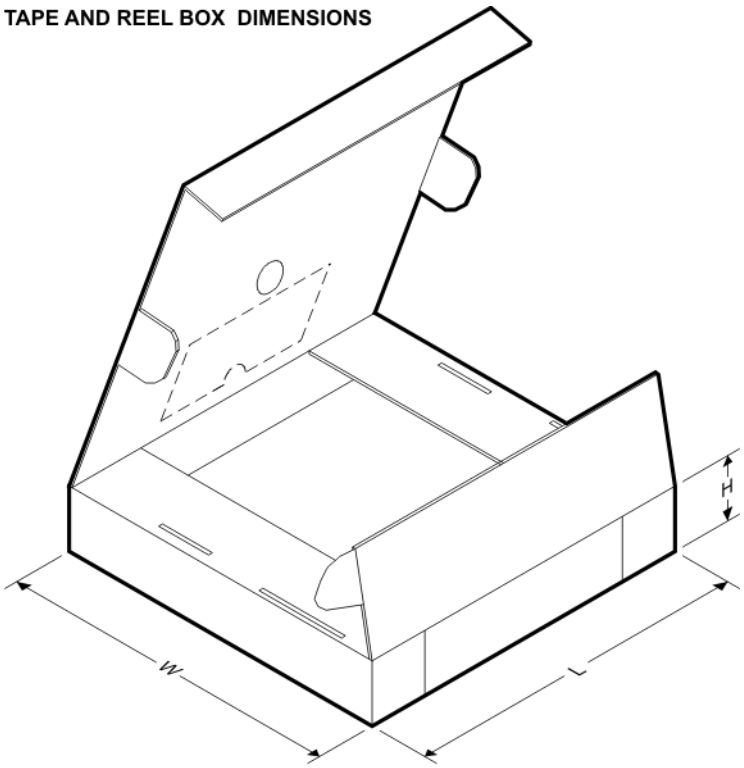
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62065TDSGRQ1	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

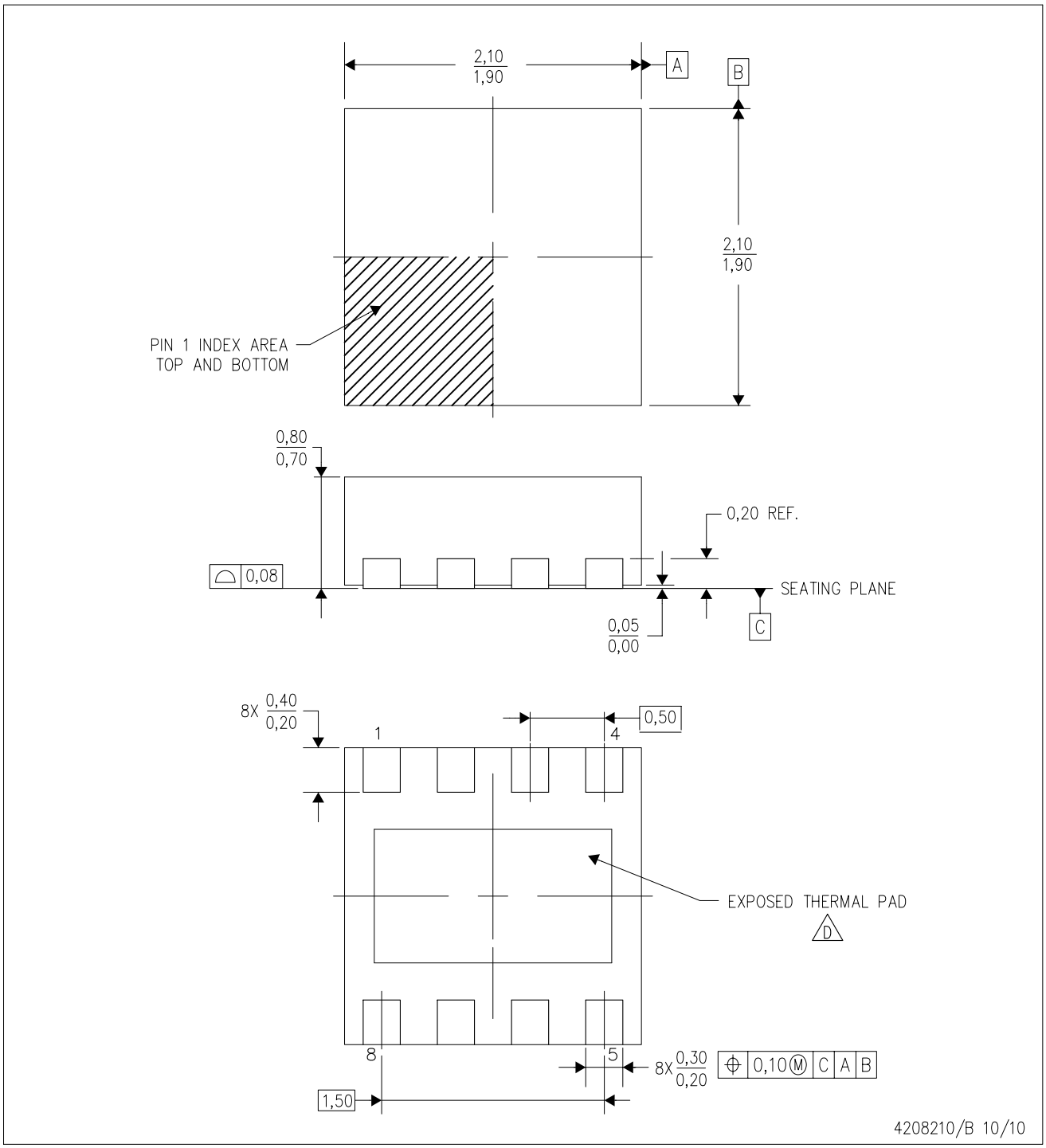
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62065TDSGRQ1	WSON	DSG	8	3000	195.0	200.0	45.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

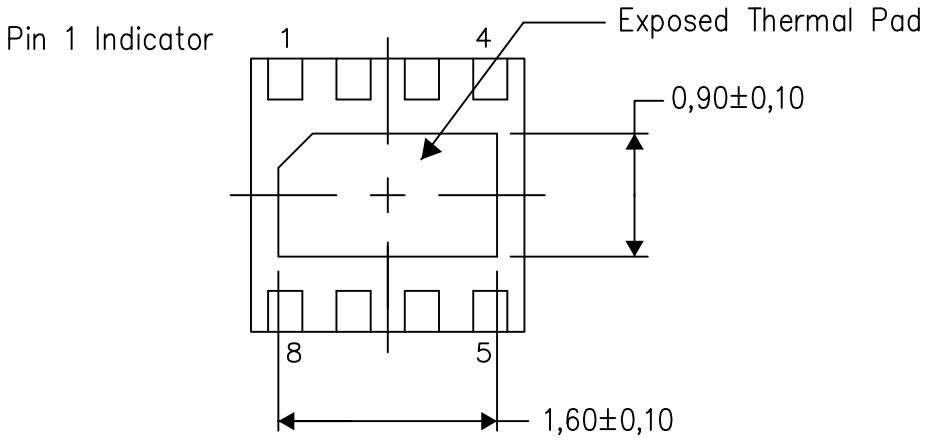
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



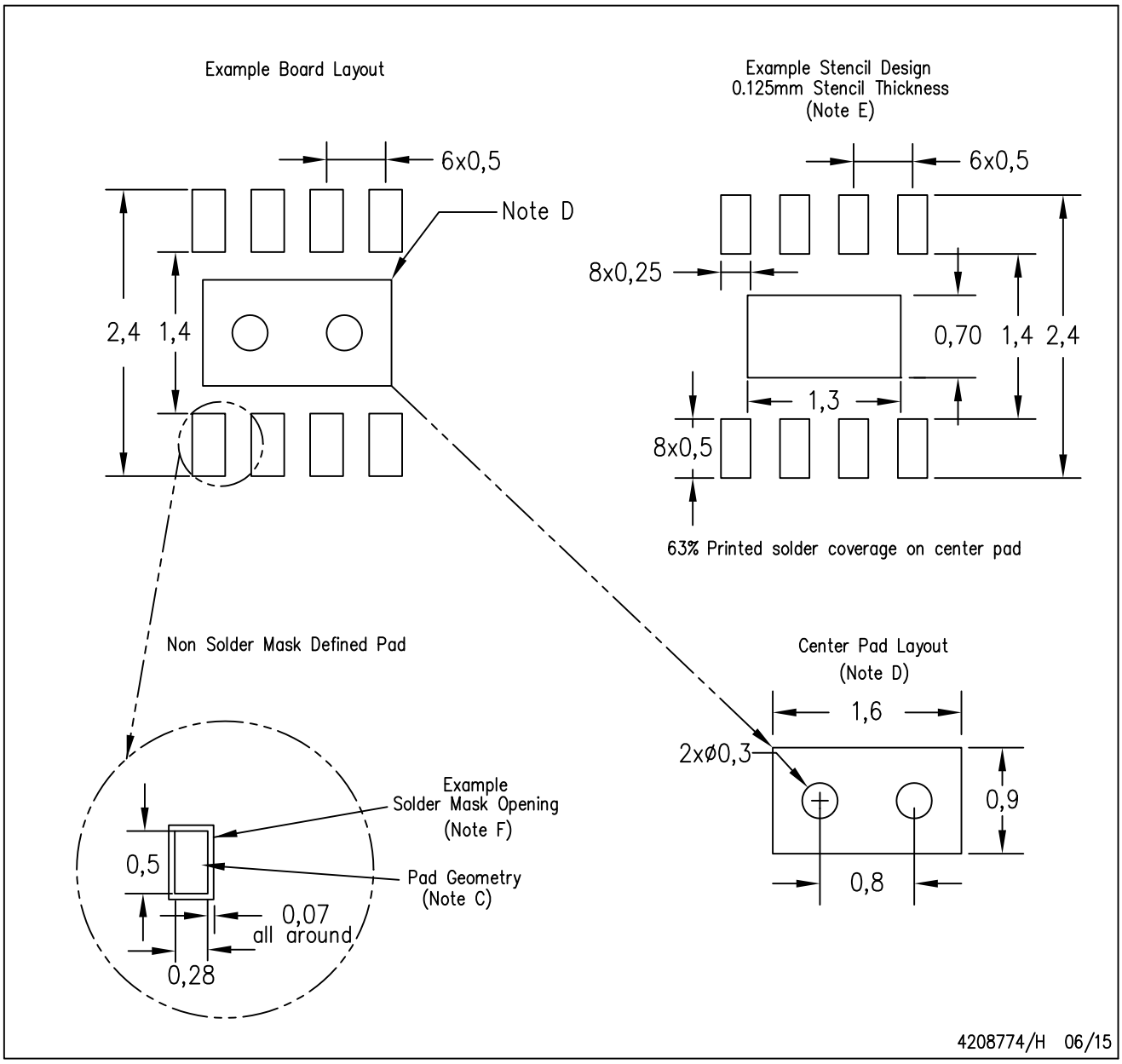
Bottom View

Exposed Thermal Pad Dimensions

4208347/I 06/15

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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