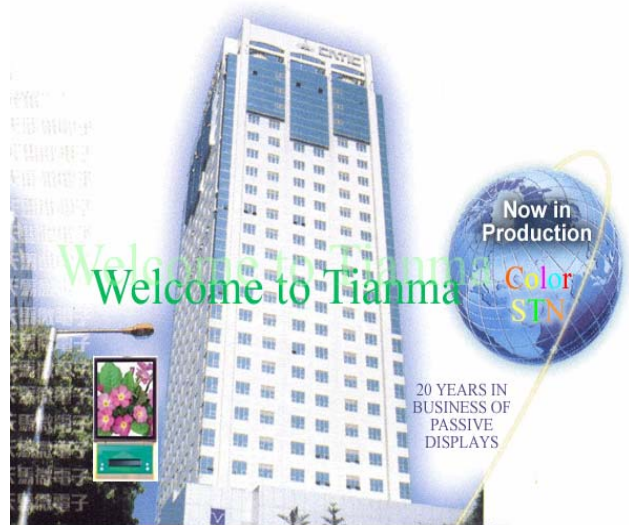# SPECIFICATION FOR COLOR STN LCD MODULE

MODEL NO: TM128128A4KFWG4
CUSTOMER:

TIANMA MICROELETRONIC CO., LTD
22/F HANGDU BUILDING, CATIC ZONE,
SHEN NAN ROAD CENTRAL
SHENZHEN, CHINA
TEL: (86-755) 83790774
FAX: (86-755) 83790431
WEB: WWW.TIANMA.COM

PREPARED	CHECKED	VERIFIED BY R&D DEPT	VERIFIED BY QC DEPT	APPROVED

REVISION RECORD

Date	Rev.No.	Revision Items	Prepared	Checked	Approved
2007.1.26	**V1.0**	**The first version**			

CONTENTS

Page

1.General Specifications

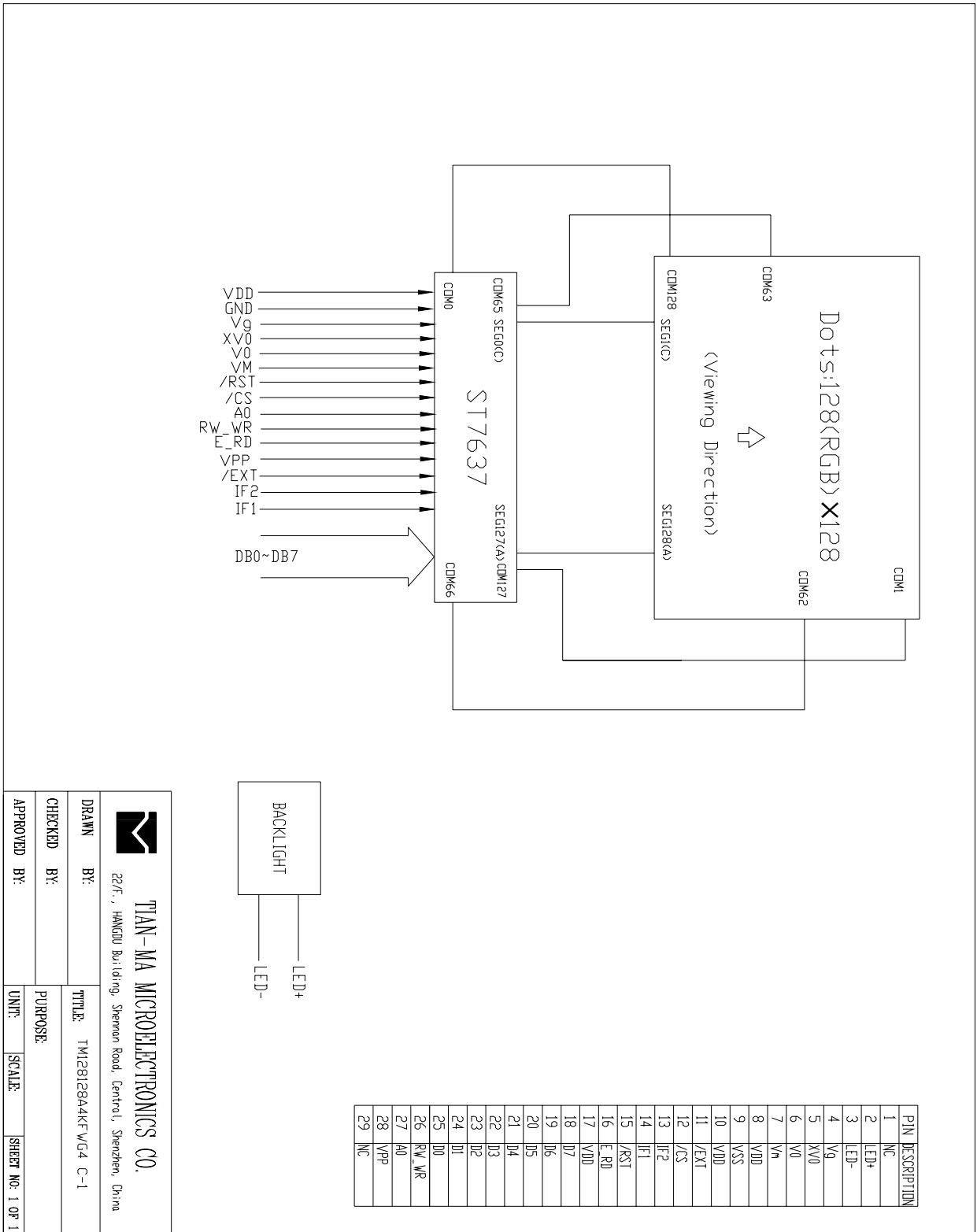| Item	Contents	Unit	Note
LCD Type	CSTN	-	
Display color	65K		1
LCD Duty	1/128	-	
LCD Bias	1/12	-	
Viewing Direction	6:00	O'Clock	
Active Area(W×H)	25.488×26.486	mm	
Number of Dots	128(RGB)×128	mm	
Dote Size(W×H)	0.0564×0.197	mm	
Dot Pitch(W×H)	0.1992×0.207	mm	
Controller	ST7637	-	
V_{DD}	2.8	V	
Vop	14	V	
Outline Dimensions	Refer to outline drawing on next page		
Backlight	1-LED (white)	-	
Operating Temperature	-20～+70℃	-	
Storage Temperature	-30～+80℃	-	
Weight	TBD	g	2
Data Transfer	8 bits parallel	-	
Polarizer Mode	Transmissive/negative	-	

Note 1: Color tune is slightly changed by temperature and driving voltage.
Note 2:   TBD- To Be Determined.

2. Outline Drawing

NOTES:
1. DISPLAY TYPE: CSTN (65K COLOR)
2. VIEWING DIRECTION: 6:00
3. POLARIZER MODE: TRANSMISSIVE/NEGATIVE
4. LCD CONTROLLER: ST7637
5. DRIVE METHOD: 1/128 DUTY 1/12 BIAS
6. VDD: 2.8V
7. OPERATING VOLTAGE:14V
8. BACKLIGHT: 1CHIP-WHITE LED
9. OPERATING TEMP.:   -20°C~70°C
10. STORAGE TEMP.:   -30°C~80°C
11. UNMARKED TOLERANCE:±0.3
12. ☐ MEANS IMPORTANT DIMENSION

DDIS:128(XRGB)X128

DOUBLE SIDE TAPE

FRONT
CONTACT SIDE
DOUBLE SIDE TAPE
CONTACT SIDE

DOUBLE SIDE GLUE TAPE
3M444
T=0.1

VER	DESCRIPTION	DATE
	NEW ISSUE	07-1-26

TIAN-MA MICROELECTRONICS CO.
22/F., HANGDU Building, Shennan Road, Central, Shenzhen, China

DRAWN BY:		
CHECKED BY:		
APPROVED BY:		
CONFIRMED BY:		

TITLE: TM128128A4KFWG4 G-1
DWG NO:
DWG NAME:
SHEET NO: 1 OF 1
SCALE:
UNIT: mm

PIN	DESCRIPTION
1	NC
2	LED+
3	LED-
4	Vg
5	XV0
6	XV0
7	V0
8	Vm
9	VSS
10	VDD
11	VDD
12	/EXT
13	/CS
14	IF2
15	IF1
16	/RST
17	E_RD
18	VDD
19	D7
20	D6
21	D5
22	D4
23	D3
24	D2
25	D1
26	D0
27	RW_WR
28	A0
29	VPP
	NC

3. Circuit Block Diagram

4. Absolute Maximum Ratings(Ta=25℃)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	-0.5	3.3	V	
Power Supply Voltage for LCD	Vop	-	-	V	
Logic Signal Input Voltage	V_I	-0.3	V_{DD}+0.3	V	1,2
Operating Temperature	Top	-20	+70	℃	
Storage Temperature	Tst	-30	+80	℃	

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.

2. V_{DD} >V_{SS} must be maintained.

5. Electrical Specifications and Instruction Code

5.1 Electrical characteristics (Ta=25℃)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Operation voltage		V_{OP}	Ta=25℃	13.7	14	14.3	V	1
Input Voltage	'H'	V_{IH}	V_{DD}=2.8V	$0.8V_{DD}$	-	V_{DD}	V	
	'L'	V_{IL}	V_{DD}=2.8V	Vss	-	$0.2V_{DD}$	V	
Output Voltage	'H'	V_{OH}	-	$0.8V_{DD}$	-	V_{DD}	V	
	'L'	V_{OL}	-	Vss	-	$0.2V_{DD}$	V	
Current Consumption		I_{CC1}	Normal mode	-	-	23	mA	2
		I_{CC2}	Stand-by mode	-	-	-	mA	3
		I_{CC3}	dimming mode	-	-	-	mA	4

Note:

　　1: IC default setting, Duty:1/128.

　　2: Display full white. Backlight on state.

　　3: IC on standby mode.

　　4: Display full white. Backlight dimming state

5.2 LED backlight specification

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Forward voltage		V_f	I_f=20mA	3.1	3.3	3.5	V	
Reverse voltage		V_r	I_r=15uA		-		V	
Forward current	Normal	I_{pn}	1-chip		20		mA	
	Dimming	I_{pd}						
Reverse Current		I_r	V_r=?V		15		μA	
Uniformity			I_f=20mA	80				

5.3 Interface Signals

Pin No.	Symbol	I/O	Function
1	NC	I	Not connected
2	LED+	P	+3.3V for backlight
3	LED-	P	Supply ground for backlight
4	Vg	I/O	Bias LCD driver supply voltage
5	XV0	I/O	Negative LCD driver supply voltage
6	V0	I/O	Positve LCD driver supply voltage
7	Vm	I/O	Bias LCD driver supply voltage
8	VDD	P	Power Supply Voltage
9	VSS	P	Ground
10	VDD	P	Power Supply Voltage
11	EXT	I	MTP burn-in control pin
12	CS	I	Chip select: Low active
13	IF2	I	Parallel data interface select pin
14	IF1	I	
15	RST	I	Reset pin: Low active
16	RD	I	Read enable clock input pin
17	VDD	P	Power Supply Voltage
18	D7	I/O	8 bit data bus
19	D6	I/O	
20	D5	I/O	
21	D4	I/O	
22	D3	I/O	
23	D2	I/O	
24	D1	I/O	
25	D0	I/O	
26	WR	I	Write enable clock input pin
27	A0	I	Data / Instruction select input pin
28	VPP	I	MTP power supply voltage 7.5~7.75V input pin

5.4 Interface Timing Chart
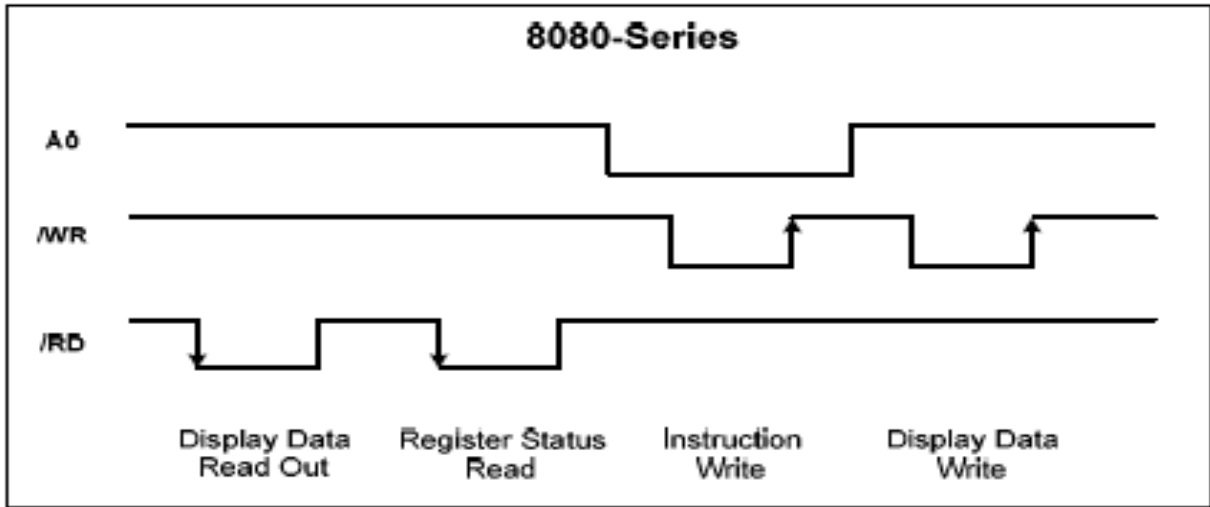
Note: Please refer to SITRONIX's ST7637 data sheet for more details.

5.5 Instruction table

	Command Table-1 , /EXT= H , L, or floating													
Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(00h)	NOP	0	1	0	0	0	0	0	0	0	0	0	No Operation	9.1.1
(01h)	SWRESET	0	1	0	0	0	0	0	0	0	0	1	Software reset	9.1.2
(04h)	RDDID	0	1	0	0	0	0	0	0	1	0	0	Read Display ID	9.1.3
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	ID1 read (D23-D16)	
-		1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID2 read (D15-D8)	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	ID3 read (D7-D0)	
(09h)	RDDST	0	1	0	0	0	0	0	1	0	0	1	Read Display Status	9.1.4
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	(D31-D24)	
-		1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	(D23-D16)	
-		1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	(D15-D8)	
-		1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	(D7-D0)	
(0Ah)	RDDPM	0	1	0	0	0	0	0	1	0	1	0	Read Display Power Mode	9.1.5
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	D2	0	0	-	
(0Bh)	RDDMADCTR	0	1	0	0	0	0	0	1	0	1	1	Read Display MADCTR	9.1.6
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	0	0	0	-	
(0Ch)	RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	Read Display Pixel Format	9.1.7
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	0	0	0	0	0	D2	D1	D0	-	
(0Dh)	RDDIM	0	1	0	0	0	0	0	1	1	0	1	Read Display Image Mode	9.1.8
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	0	D5	D4	D3	0	0	0	-	
(0Eh)	RDDSM	0	1	0	0	0	0	0	1	1	1	0	Read Display Image Mode	9.1.9
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	0	0	0	0	0	0	-	
(0Fh)	RDDSDR	0	1	0	0	0	0	0	1	1	1	1	Read Display Self-diagnostic result	9.1.10
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
		1	0	1	D7	D6	0	D4	0	0	0	0	-	

(10h)	SLPIN	0	1	0	0	0	0	1	0	0	0	0	Sleep in & booster off	9.1.11
(11h)	SLPOUT	0	1	0	0	0	0	1	0	0	0	1	Sleep out & booster on	9.1.12
(12h)	PTLON	0	1	0	0	0	0	1	0	0	1	0	Partial mode on	9.1.13
(13h)	NORON	0	1	0	0	0	0	1	0	0	1	1	Partial off (Normal)	9.1.14
(20h)	INVOFF	0	1	0	0	0	1	0	0	0	0	0	Display inversion off (normal)	9.1.15
(21h)	INVON	0	1	0	0	0	1	0	0	0	0	1	Display inversion on	9.1.16
(22h)	APOFF	0	1	0	0	0	1	0	0	0	1	0	All pixel off (Only for test purpose)	9.1.17
(23h)	APON	0	1	0	0	0	1	0	0	0	1	1	All pixel on (Only for test purpose)	9.1.18
(25h)	WRCNTR	0	1	0	0	0	1	0	0	1	0	1	Write contrast	9.1.19
-		1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	EV = 0 to 127	
(28h)	DISPOFF	0	1	0	0	0	1	0	1	0	0	0	Display off	9.1.20
(29h)	DISPON	0	1	0	0	0	1	0	1	0	0	1	Display on	9.1.21
(2Ah)	CASET	0	1	0	0	0	1	0	1	0	1	0	Column address set	9.1.22
		1	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	X_ADR start: 0≤XS≤83h	
		1	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	X_ADR end: XS≤XE ≤83h	
(2Bh)	RASET	0	1	0	0	0	1	0	1	0	1	1	Row address set	9.1.23
		1	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Y_ADR start: 0≤YS≤83h	
		1	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	Y_ADR end: YS≤YE≤83h	
(2Ch)	RAMWR	0	1	0	0	0	1	0	1	1	0	0	Memory write	9.1.24
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data	
(2Dh)	RGBSET	0	1	0	0	0	1	0	1	1	0	1	Color set for 256 or 4k color display	9.1.25
-		1	1	0	-	-	-	R4	R3	R2	R1	R0	Red tone (00000)	
-		1	1	0	:	:	:	:	:	:	:	:	: -	
-		1	1	0	-	-	-	R4	R3	R2	R1	R0	Red tone (11111)	
-		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (000000)	
		1	1	0	:	:	:	:	:	:	:	:	: -	
		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (111111)	
		1	1	0	-	-	-	B4	B3	B2	B1	B0	Blue tone (00000)	
		1	1	0	:	:	:	:	:	:	:	:	: -	
		1	1	0	-	-	-	B4	B3	B2	B1	B0	Blue tone (11111)	
(2Eh)	RAMRD	0	1	0	0	0	1	0	1	1	1	0	Memory Read	9.1.26
		1	1	0	-	-	-	-	-	-	-	-	Dummy read	
		1	1	0	D7	D6	D5	D4	D3	D2	D1	D0		
(30h)	PTLAR	0	1	0	0	0	1	1	0	0	0	0	Partial start/end address set	9.1.27

					D7	D6	D5	D4	D3	D2	D1	D0	Description	
-		1	1	0	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	Start address (0~131)	
-		1	1	0	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	End address (0~131)	
(33h)	SCRLAR	0	1	0	0	0	1	1	0	0	1	1	Scroll Area	9.1.28
-		1	1	0	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA=0~132	
-		1	1	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA=0~132	
-		1	1	0	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA=0~132	
(34h)	TEOFF	0	1	0	0	0	1	1	0	1	0	0	Tearing effect line off	9.1.29
(35h)	TEON	0	1	0	0	0	1	1	0	1	0	1	Tearing effect mode set & on	9.1.30
-		1	1	0	-	-	-	-	-	-	-	M	"0": mode1, "1": mode2	
(36h)	MADCTR	0	1	0	0	0	1	1	0	1	1	0	Memory data access control	9.1.31
-		1	1	0	MY	MX	MV	ML	RGB	-	-	-	-	
(37h)	VSCSAD	0	1	0	0	0	1	1	0	1	1	1	Scroll start address of RAM	9.1.32
		1	1	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA = 0~131	
(38h)	IDMOFF	0	1	0	0	0	1	1	1	0	0	0	Idle mode off	9.1.33
(39h)	IDMON	0	1	0	0	0	1	1	1	0	0	1	Idle mode on	9.1.34
(3Ah)	COLMOD	0	1	0	0	0	1	1	1	0	1	0	Interface pixel format	9.1.35
-		1	1	0	-	-	-	-	-	P2	P1	P0	Interface format	
(DAh)	RDID1	0	1	0	1	1	0	1	1	0	1	0	Read ID1	9.1.36
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	(D7-D0)	
(DBh)	RDID2	0	1	0	1	1	0	1	1	0	1	1	Read ID2	9.1.37
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	(D7-D0)	
(DCh)	RDID3	0	1	0	1	1	0	1	1	1	0	0	Read ID3	9.1.38
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	(D7-D0)	

Note 1: When /EXT connects to H or floating, commands which are not defined in "Command Table-1" are treated as NOP (00H) command.

Note 2: Commands 10H, 12H, 13H, 20H, 21H, 25H, 28H, 29H, 30H, 36H (Bit ML only), 38H and 39H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects.

During Sleep In mode, these commands are updated immediately.

Read status (09H), Read Display Power Mode (0AH), Read Display MADCTR (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) and Read Display Self Diagnostic Result (0FH) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

6. Optical Characteristics

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		$\Phi_1=0°$ $\Phi_2=0°$	150	180		Cd/m^2	1
Uniformity	$\triangle$Bp			80%				1,2
Viewing Angle	Φ_1(up down)		Cr≥2	-40～+20			Deg	3
	Φ_2(left right)			-45～+45				
Contrast Ratio	Cr		$\Phi_1=0°$ $\Phi_2=0°$	25	40	-	-	4
Response Time	Tr			-	-	-	ms	5
	T_f			-	-	-		
Color of CIE Coordinate	W	x	$\Phi_1=0°$ $\Phi_2=0°$	-	-	-	-	1,6
		y		-	-	-	-	
	R	x		-	-	-	-	
		y		-	-	-	-	
	G	x		-	-	-	-	
		y		-	-	-	-	
	B	x		-	-	-	-	
		y		-	-	-	-	
NTSC Ratio	S				25.0%			

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ10mm)
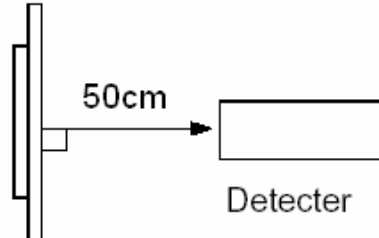
Note 2: $\triangle Bp = Bp$ (Min.) / Bp (Max.)×100 (%)

   Bp (Max.) = Maximum brightness in 9 measured spots

   Bp (Min.) = Minimum brightness in 9 measured spots.

3~5mm
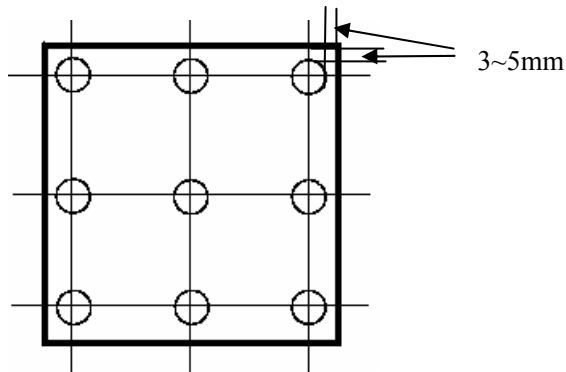
Measurement equipment PR-705 (Φ10mm)

Note 3: Definition of Viewing Angle(Test LCD using DMS501)
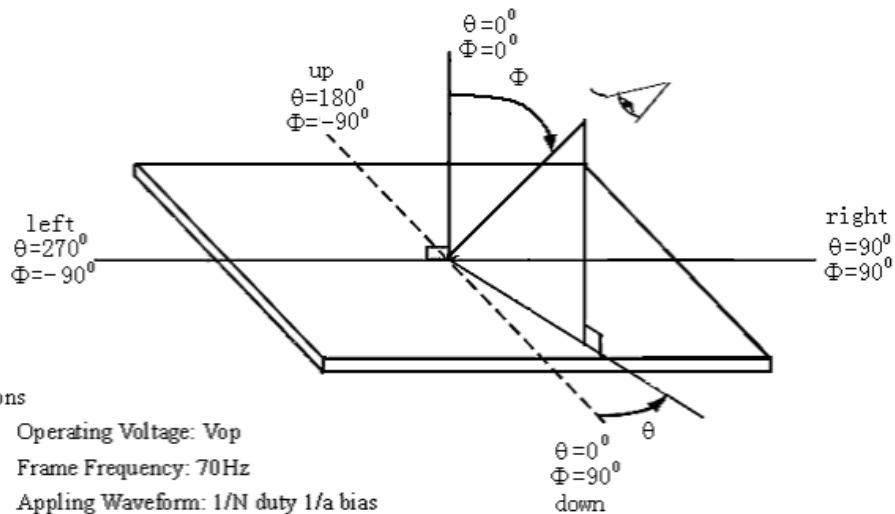
*Conditions

   Operating Voltage: Vop
   Frame Frequency: 70Hz
   Appling Waveform: 1/N duty 1/a bias
   Contrast ratio: ≥ 2

Note 4: Definition of contrast ratio.(Test LCD using DMS501)
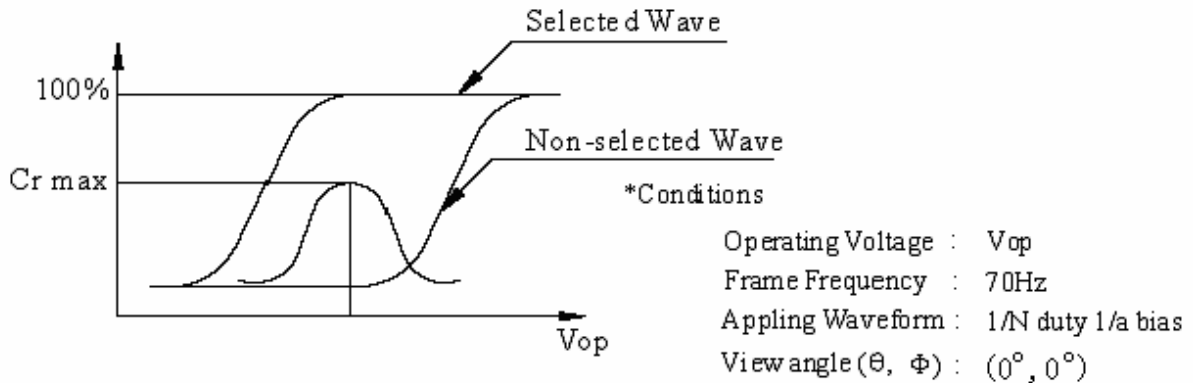
$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

Note 5: Definition of Response time(Test LCD using DMS501)
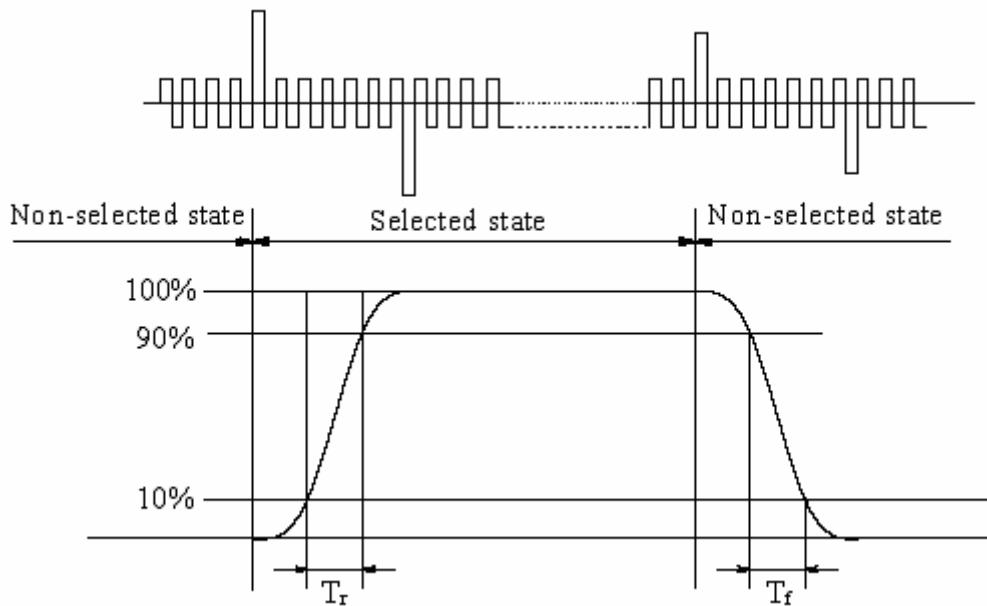
Operating Voltage: Vop

Frame Frequency: 70Hz

Appling Waveform: 1/N duty 1/a bias

View angle (θ, Φ): $(0^0, 0^0)$

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.

1931 CIE Chromaticity Diagram
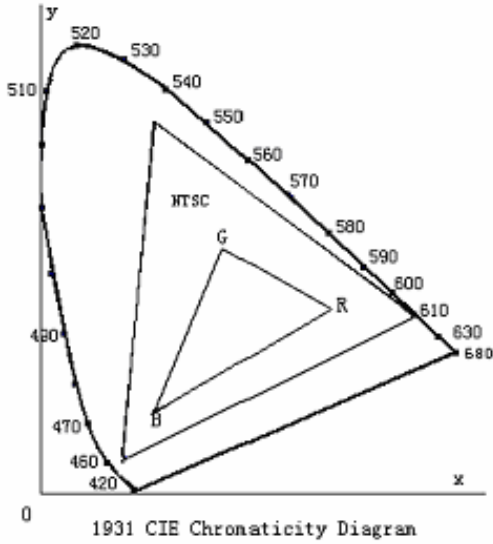
Color gamut:
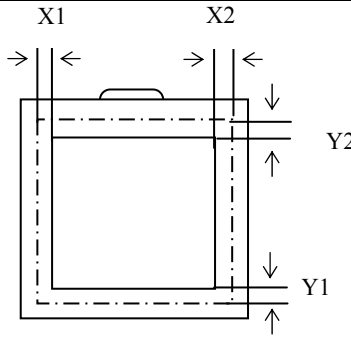
$$S = \frac{area\ of\ RGB\ triangle}{area\ of\ NTSC\ triangle} \times 100\%$$

7. Reliability
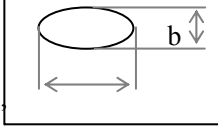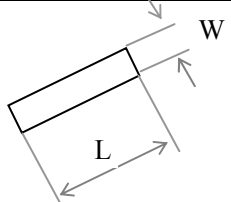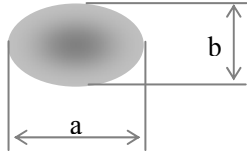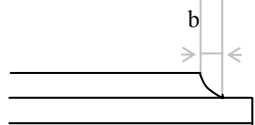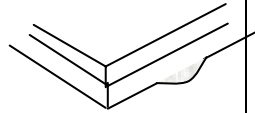
No.	Test Item	Test condition	Criterion
1	High Temperature Storage	80℃±2℃96H Restore 4H at 25℃	
2	Low Temperature Storage	-30℃±2℃ 96H Restore 4H at 25℃	
3	High Temperature Operation	70℃±2℃ 48H Restore 4H at 25℃	
4	Low Temperature Operation	-20℃±2℃ 48H Restore 4H at 25℃	1. After testing, cosmetic defects should not happen. 2.Total current consumption should not be over 10% of initial value.
5	High Temperature /Humidity Operation	40℃±2℃ 90%RH 48H	
6	Temperature Cycle	-30℃⟷25℃⟷80℃ 5min 30min ⟷25℃ , 5min after 10cycle, Restore 4H at 25℃	
7	Vibration Test (package state)	10Hz~150Hz, 100m/s2, 120min	
8	Shock Test (package state)	Half- sine wave, 300m/s2, 18ms	Not allowed cosmetic and electrical defects.
9	Atmospheric Pressure Test	25kPa 16H Restore 2H	
10	Cable Bending Test		More than 50000 times

8 Quality level

8.1 Notes for quality standard

	Note		
General	1. Should any defects which are not specified in this standard happen, additional standard shall be determined by mutual agreement between customer and Tianma. 2. Viewing Area should be the area which Tianma guarantees. 3. Limited sample should be prior to this Inspection standard. 4. Viewing Judgement should be under static pattern. 5. Inspection conditions 　　Inspection distance　　: 250 mm (from the sample) 　　Temperature　　: 25±5℃ 　　Inspection angle　　: 45degrees in 3,6,9,12 o′clock direction		
Definitions of Inspection items	Pinhole, Bright spot, Black spot, White spot, Black line, White Line, Foreign particle, Bubble	The color of a small area is different from the remainder. The phenomenon dose not change with voltage.	
	Contrast variation	The color of a small area is different from the remainder. The phenomenon changes with voltage.	
	Polarizer defect	Scratch, Dirt, Particle, Bubble on polarizer or between polarizer and glass.	
	Glass defect	Glass crack, Shaved corner of glass, Surplus glass	
Definitions of Inspection ranges		Dividing A zone and B zone proceed to make a judgment. A zone : Inside Viewing area B zone : Outside Viewing area X1(A.A~V.A): mm X2(A.A~V.A): mm Y1(A.A~V.A): mm Y2(A.A~V.A): mm	
Outgoing Inspection standard	Inspection level Ⅱ Normal Inspection		
	Rank	Inspection Item	AQL(Number of defective LCMs counted)
	Major defect	All Functional defects(Such as No display, Display abnormally, Open or missing segment, Short circuit，Missing component, No sound, Blight abnormally and so on),Outline dimension beyond the drawing， progressive defects and those affecting reliability	0.65
	Minor defect	Appearance defects, such as Black/White spot, Bright spot, Pinhole, Black/White line, Contrast variation, Bubble(Bubble in the cell is not included),Glass defect, Polarizer defect, Soldering defect and so on. Details of the standard as follows.	1.50

8.2Standards of inspection items

Inspection item			Judgement standard			
			Category		Acceptable number	
					A zone	B zone
1	Black spot, White spot Bright Spot, Pinhole Foreign Particle, Bubble and Particle Between polarizer and glass, Scratch on polarizer	$\Phi=(a+b)/2(mm)$	A B C D	$\Phi \leqq 0.15$ $0.15<\Phi \leqq 0.20$ $0.20<\Phi \leqq 0.30$ $0.30<\Phi$	Neglected 2 1 0	Neglected
			Total defective point(B,C)		3	
2	Black line, White line, Bubble and Particle Between Polarizer and glass, Scratch on polarizer	W:Width, L:Length(mm)	A	$W \leqq 0.10$	Neglected	Neglected
			B	$0.01<W \leqq 0.03$ $L \leqq 3.0$	2	
			C	$0.03<W \leqq 0.05$ $L \leqq 3.0$	1	
			D	$0.05<W$	0	
			Total defective point(B,C)		2	
3	Contrast variation	$\Phi=(a+b)/2(mm)$	A	$\Phi \leqq 0.2$	Neglected	Neglected
			B	$0.2<\Phi \leqq 0.3$	2	
			C	$0.3<\Phi \leqq 0.4$	1	
			D	$0.4<\Phi$	0	
			Total defective point(B,C)		3	
4	Bubble inside cell		any size		none	none
5	Polarizer defect (if Polarizer is used)	Scratch and damage on polarizer, Particle on polarizer or between polarizer and glass.	Refer to item 1 and item 2.			
		Bubble, dent and convex	A	$\Phi \leqq 0.3$	Neglected	Neglected
			B	$0.3<\Phi \leqq 0.7$	2	
			C	$0.7<\Phi$	0	
			Total defective point(B,C)		2	
6	Surplus glass	①Stage surplus glass	$b \leqq 0.3mm$			
		②Surrounding surplus glass	Should not influence outline dimension and assembling.			

Inspection item			Judgment standard	
			Category(application: B zone)	
7	Glass defect crack	①The front of lead terminals	A	If a $\leqq$ t and b $\leqq$1.0, c is not limited
			B	a $\leqq$ t, 1$\leqq$b$\leqq$2mm, c$\leqq$3mm
			C	If glass crack cover alignment mark, b$\leqq$0.5mm.
			D	Crack at two sids of lead terminals should not cover patterns and alignment mark
		②Surrounding crack—non-contact side		b < Inner borderline of the seal
		③ Surrounding crack— contact side		b < Outer borderline of the seal
		④Corner	A	a $\leqq$ t, b $\leqq$ 3.0, c $\leqq$ 3.0
				*Glass crack should not cover patterns used for

	Inspection item		Judgement standard
8	PCB defect	Component soldering: No cold soldering、short、open circuit、burr、tin ball The flat encapsulation component position deviation must be less than 1/3 width of the pin (Pic.1); the sheet component deviation: Pin deviates from the pad and contact with the near components is not permitted（Pic.2）	
		lead defect: The lead lack must be less than 1/3 of its width; The lead burr must be less than 1/3 of the seam; Impurities connect with the near leads is not permitted	
		Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted	
		Glue on root of the speaker receiver and motor lead: The insulative coat of the lead must join into the PCB; the protected glue must envelop to the insulative coat.	

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

　　　— Isopropyl alcohol

　　　— Ethyl alcohol

　Solvents other than those mentioned above may damage the polarizer.　　Especially, do not use the following:

　　　— Water

　　　— Ketone

　　　— Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

　a. Be sure to ground the body when handling the LCD Modules.

　b. Tools required for assembly, such as soldering irons, must be properly ground.

　c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature :   0℃ ～ 40℃

Relatively humidity: ≤80%

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.