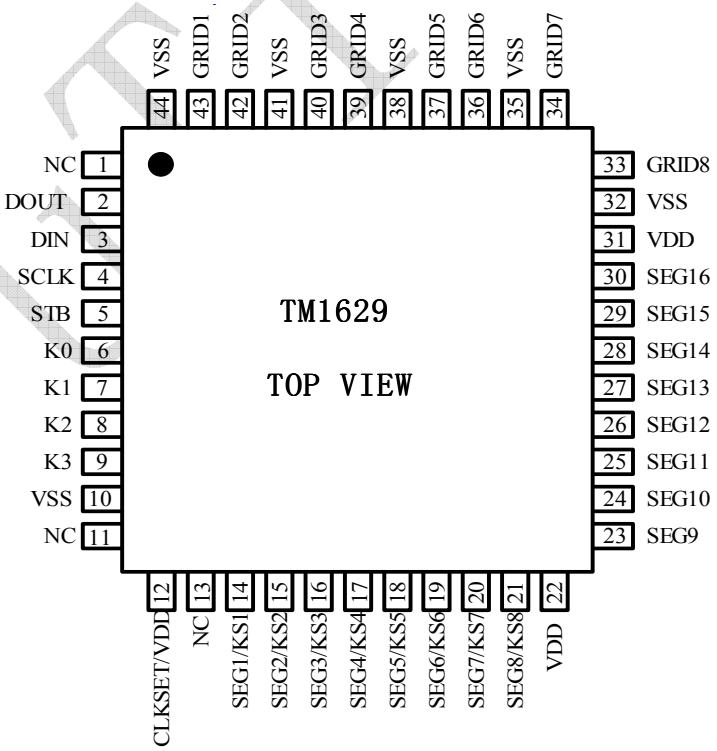
Overview

TM1629 is a special circuit for LED (light-emitting diode) driver control with keyboard scanning port. It integrates with different circuits such as MCU digital port, data latch, LED high-voltage drive, keyboard scanning, etc. The product has good performance and reliable quality, and is mainly applied in display drive of VCR, VCD, DVD, home theater and other similar products.

Features

- Low power consumption CMOS workmanship
- Display mode（16segment×8positions）
- Key scanning（8×4bit）
- Luminance adjustment circuit (8-level adjustable duty cycle)
- Serial port (CLK, STB, DIN DOUT)
- Oscillation mode: built-in RC oscillation（450KHz±5%）
- Built-in power-on reset circuit
- Packaging:QFP44

Pin definitions



Pin definitions

Sign	Name	Description
DIN	Data input	I/O serial data at rising edge of clock, starting from low order .can use with DOUT to DIO
DOUT	Date output	On the rising edge of the clock output serial data, from a low starting. With DIN shorted for DIO to use
STB	Chip selection	Initialize serial port at rising/falling edge, and then wait for receiving command. The first byte after the STB becomes low is taken as the command. When treating the command, other current treatments are stopped. When STB is high, CLK is ignored.
CLK	Clock input	I/O serial data at rising edge of clock
K0～K3	Key scanning data input	The data to this pin are latched after display cycle
SEG1/KS1~SEG8/KS8	Output (segment)	Segment output (also used for key scanning), P pipe open-drain output
SEG9~SEG16	Output (segment)	Segment output (also used for key scanning), P pipe open-drain output
GRID1～GRID8	Output (position)	Position output, N pipe open-drain output
VDD	Logical power supply	5V±10%
VSS	Logic ground	Ground system
NC	Space	No connection

Note: During data output, DIO port is N-pipe open-drain output, and when reading keys, an external pull-up resistor of 1K – 10K is required. We recommend a 10K pull-up resistor. DIO controls the action of the N-pipe at the falling edge of the clock, and at this time the reading is not stable, please refer to figure (6). It becomes stable only when reading at the rising edge of the clock.

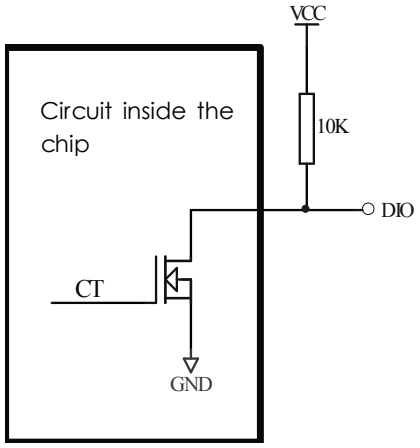


Figure (1)

Display register address and display mode

The storage of this register is transferred from external component to TM1629 through serial port, with an address of 16 bytes unit in total from 00H-ODH, corresponding to the LED lamps connected to the chip' s SGE and GRID pin respectively. The distribution is shown as the following figure:

When writing LED display data, operate in the order from lower position to higher position of the display address and the data byte.

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	
xHL (four low positions)				xxHU (four high positions)				xxHL (four low positions)				xxHU (four high positions)				
B0	B1	B2	B3	B4	B5	B6	B	B0	B1	B2	B3	B4	B5	B6	B	
00HL				00HU				01HL				01HU				GRID1
02HL				02HU				03HL				03HU				GRID2
04HL				04HU				05HL				05HU				GRID3
06HL				06HU				0 HL				0 HU				GRID4
08HL				08HU				09HL				09HU				GRID5
0 HL				0 HU				0BHL				0BHU				GRID6
0CHL				0CHU				0DHL				0DHU				GRID
0EHL				0EHU				0FHL				0FHU				GRID8

Figure (2)

Write LED display data when, according to from the low address to address, from low to high byte operation in the use of no use to the SEG output port, in the corresponding BIT address bits to write 0.

Key scanning and key scanning register

The key scanning matrix is 8×4bit, shown as below:

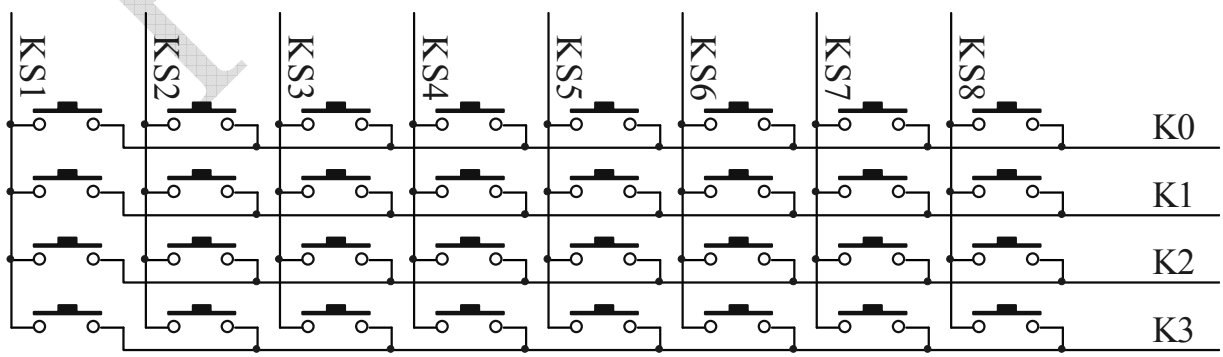


Figure (3)

Key scan data storage address figure (4) shows, first read key commands, began to read the key data of B TE1 - B TE4 bytes, reading data from the low output, K chip and KS pins corresponding key is pressed, the corresponding bytes within the BIT bit 1.

B0	B1	B2	B3	B4	B5	B6	B	
K3	K2	K1	K0	K3	K2	K1	K0	
KS1				KS2				B TE1
KS3				KS4				B TE2
KS5				KS6				B TE3
KS				KS8				B TE4

Figure (4)

NOTE: 1. TM1629 can read 4 bytes in total, and no more is allowed.

2. Order of reading can only be from B TE1 to B TE4, no trans-byte reading is allowed. For instance, when the keys corresponding to K2 and KS8 on the hardware are pressed, the data in such keys can only be read when reading to 4BIT of the fifth byte When the three keys K1 and KS8, K2 and KS8, K3 and KS8 are pressed at the same time, the reading of B TE4 at B4, B5 and B6 are all 1 .

3. The compound key can only be the same KS, and only different K pins can form a compound key the same K and different KS pins can not from a compound key.

Description to commands

Commands are used to set display mode and state of LED driver.

The first byte input by DIO at the falling edge of STB is taken as the first command. Through decoding, take the highest two bits B and B6 to distinguish different commands.

B	B6	Command
0	1	Data reading/writing setting command
1	0	Display control command
1	1	ddress setting command

If STB is set to high level during command or data transmission, the serial communication will be initialized, and the command or data being transmitted are invalid (previously transmitted commands or data are still valid).

1.Display mode setting command

The command is used to set the data write and read, B1 and B0 bit is set to 01 or 11 is not allowed.

MSB LSB

B	B6	B5	B4	B3	B2	B1	B0	Function	Description

0	1	0			0	0	Data reading/writing mode setting	Write data to display register
0	1				1	0		Read key scanning data
0	1			0			ddress increase mode setting	uto increase of address
0	1			1				Fixed address
0	1		0				Test mode setting (for internal use only)	Normal mode
0	1		1					Test mode

2. ddress command setting

MSB LSB

B	B6	B5	B4	B3	B2	B1	B0	Display address
1	1	N/ , fill in 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	0 H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0 H
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH

This command is used to set the address of display register.
When the address is set as 0EH or higher, the data are ignored until a valid address is set.
When powered, the address is set as 00H.

3.Display control

MSB LSB

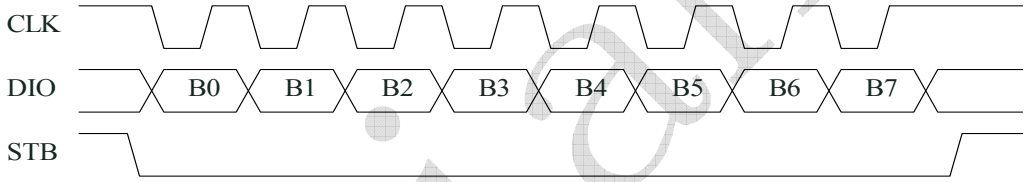
B	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	N/ , fill in 0			0	0	0	Extinction number setting	Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1		Set the pulse width to

								10/16
1	0			1	0	0		Set the pulse width to 11/16
1	0			1	0	1		Set the pulse width to 12/16
1	0			1	1	0		Set the pulse width to 13/16
1	0			1	1	1		Set the pulse width to 14/16
1	0		0				Display switch setting	Display is off
1	0		1					Display is on

Serial data transmission format

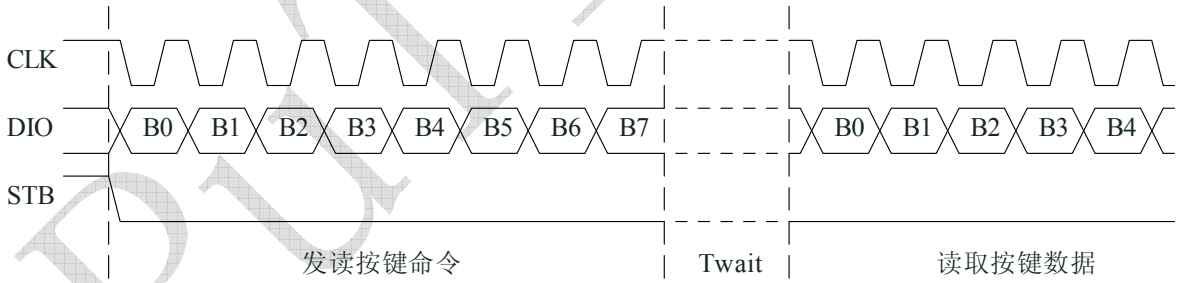
Reading and receiving 1 BIT are both happened at the rising edge of the clock.

1. Data receiving (writing data)



Figure（5）

2.Data reading (reading data)



Figure（6）

▲ **Note**: when reading data, it requires for a waiting time Twait (min. 1 S) to set the command to the falling edge of CLK for data reading starting from the eighth rising edge of the serial clock CLK.

Display and keys

1. Drive common cathode digital tub

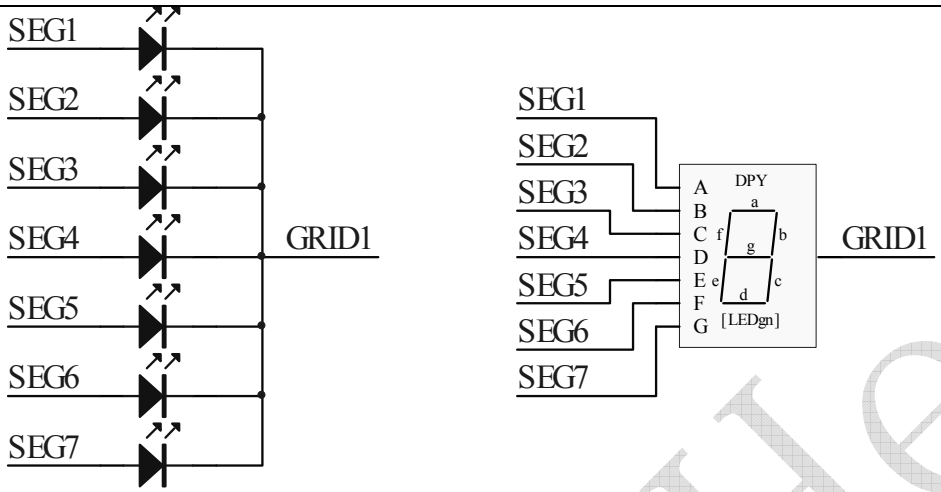


Figure ( )

Figure ( ) shows the connection diagram of common cathode digital tube to make the digital tube display 0 , set SEG1, SEG2, SEG3, SEG4, SEG5 and SEG6 to high level and SEG to low level when GRID1 is low level, view the address table shown in Figure (2), and write data 3FH in 00H address unit.

SEG8	SEG	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
0	0	1	1	1	1	1	1	00H
B	B6	B5	B4	B3	B2	B1	B0	

2. Drive common anode digital tube

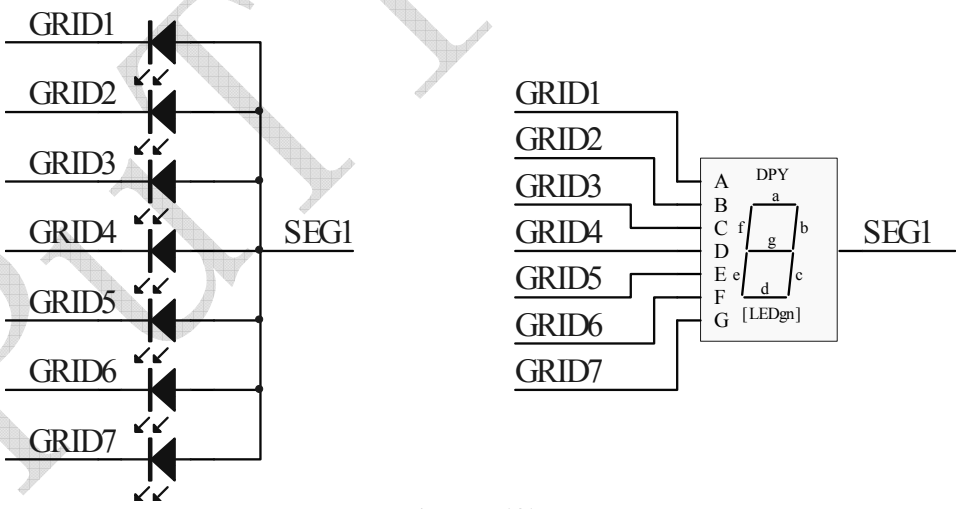


Figure (8)

Shows the connection diagram of common anode digital tube to make the digital tube display 0 , set SEG1 to high level when GRID1, GRID2, GRID3, GRID4, GRID5 and GRID6 are low level, and set SEG1 to low level when GRID is low level, write data 01H to address unit 00H, 02H, 04H, 06H, 08H and 0 H respectively and write data 00H to other address units.

SEG8	SEG	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	

0	0	0	0	0	0	0	1	00H
0	0	0	0	0	0	0	1	02H
0	0	0	0	0	0	0	1	04H
0	0	0	0	0	0	0	1	06H
0	0	0	0	0	0	0	1	08H
0	0	0	0	0	0	0	1	0 H
0	0	0	0	0	0	0	0	0CH
B	B6	B5	B4	B3	B2	B1	B0	

NOTE SEG1-11 is P pipe open-drain output, and GRID1- is N pipe open-drain output while operating, SEG1-11 only can be connected to LED anode, GRID only can be connected to LED cathode, and shouldn't be connected reversely.

3.Keys

Key scanning is completed by TM1629 automatically and cannot be controlled by user. Users only have to read the key value according to the time sequence. It requires two display circles to complete a key scanning, and one display circle requires about T 8x500US. Two different keys are pressed one after another, and the two readings are both the key value of the key firstly pressed.

ccording to figure (9), observe the output key scanning waveforms of SEG1/KS1 and SEG2/KS2 with an oscilloscope, as shown in figure (10).

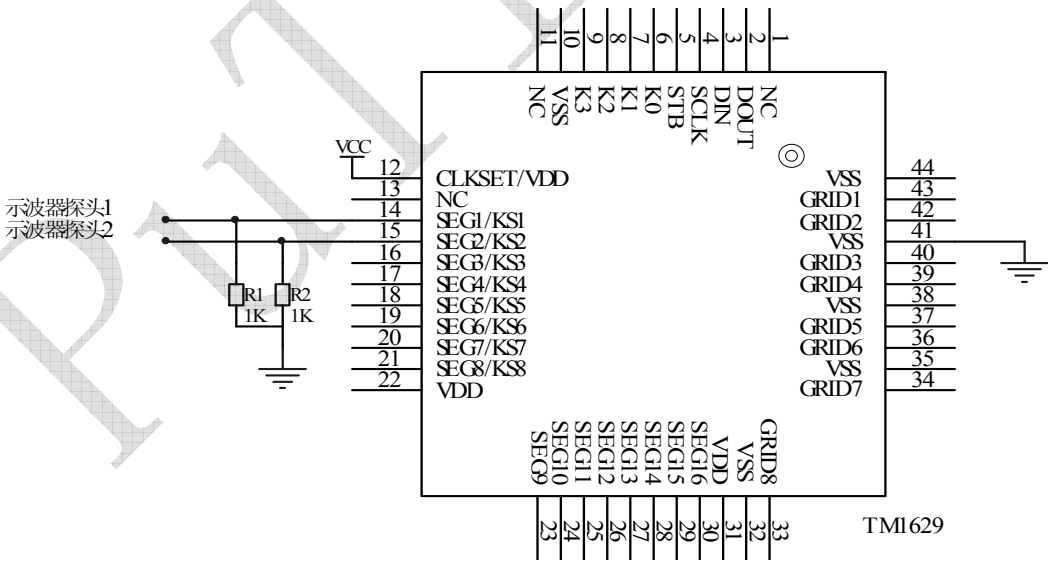


Figure (9)

Waveforms of SEGN/KSN when IC is scanning keyboard:

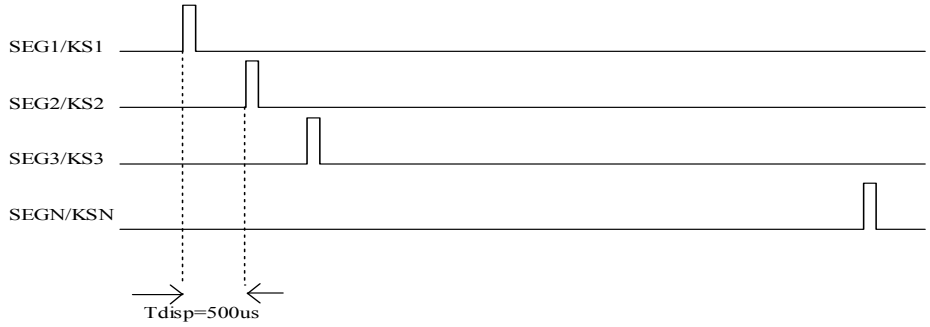


Figure (10)

Tdisp relates to the working oscillation frequency of the IC. s the improvements of TM1629 provided by our company, the oscillation may differ. 500US is only for reference and the actual measurements shall prevail .Generally, Figure (11) can meet the requirements of key design.

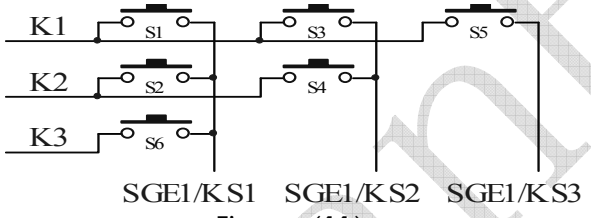


Figure (11)

When S1 is pressed down, B0 of the first byte reads 1 . If several keys are pressed down, several 1 will be read when S2 and S3 are pressed down, B1 and B3 of the first byte will read 1 .

Note: Precautions for composite key note:

SEG1/KS1-SEG10/KS10 is for display and key scanning multiplexing. Figure (12) for example, to make D1 on, D2 off, please set SEG1 to 1 , SEG2 to 0 if S1 and S2 are pressed at the same time, equivalent to SEG1 and SEG2 short circuit, D1 and D2 are lit.

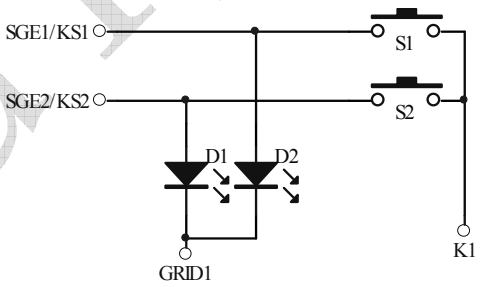


Figure (12)

Solution

1. On hardware, set the keys that should be pressed simultaneously to different K lines, as shown in.

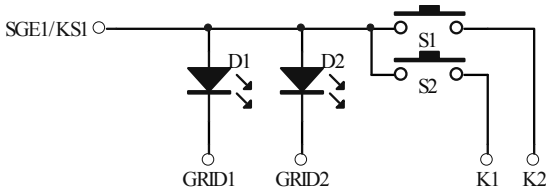


Figure (13)

2. Connect the resistors in series on SEG1 SEG N, as shown in Figure (14) the resistance should be 510 too large resistance will cause key invalid, and too low resistance can't solve the problem of display interference.

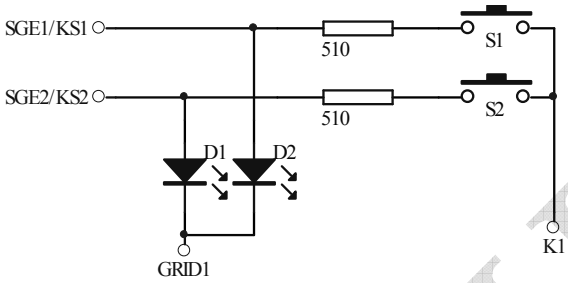


Figure (14)

3. Or connect the diodes in series, as shown in Figure (15).

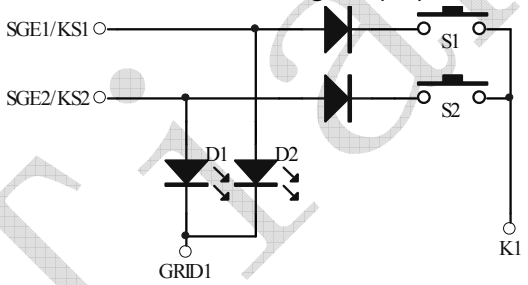
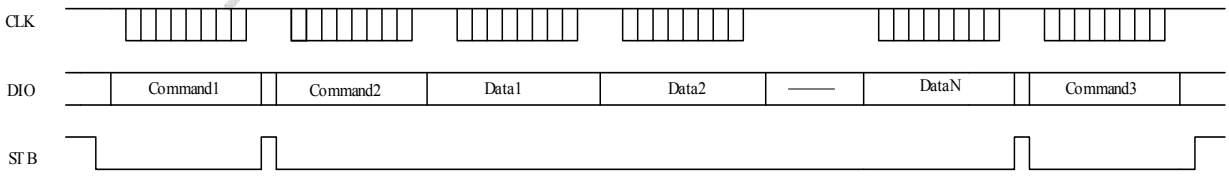


Figure (15)

Transmission of serial data in application

1. ddress increase mode

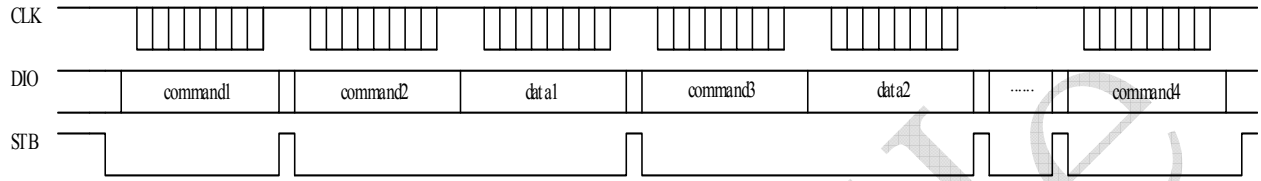
In the address auto +1 mode, to set an address actually means to set the initial address stored in the transferred data flow. When the initial address command is completely sent, send the data (16B TE at most) immediately without having to set STB to high position, and only do it when data sending completes.



Command1: display mode setting command
Command2: data reading/writing setting command
Command3: display address setting command

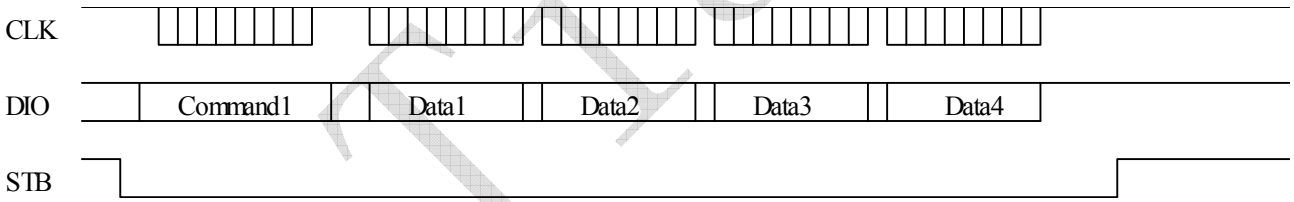
2.Fixed address mode

In the fixed address mode, to set the address actually means to set the address stored in the to-be-transferred 1B TE data. When the address is sent completely, send the 1B TE data immediately without having to set STB to high position (only do it when data sending completes) then, set the address to be stored in the second data, and when the data (16B TE at most) sending completes, set STB to high position.



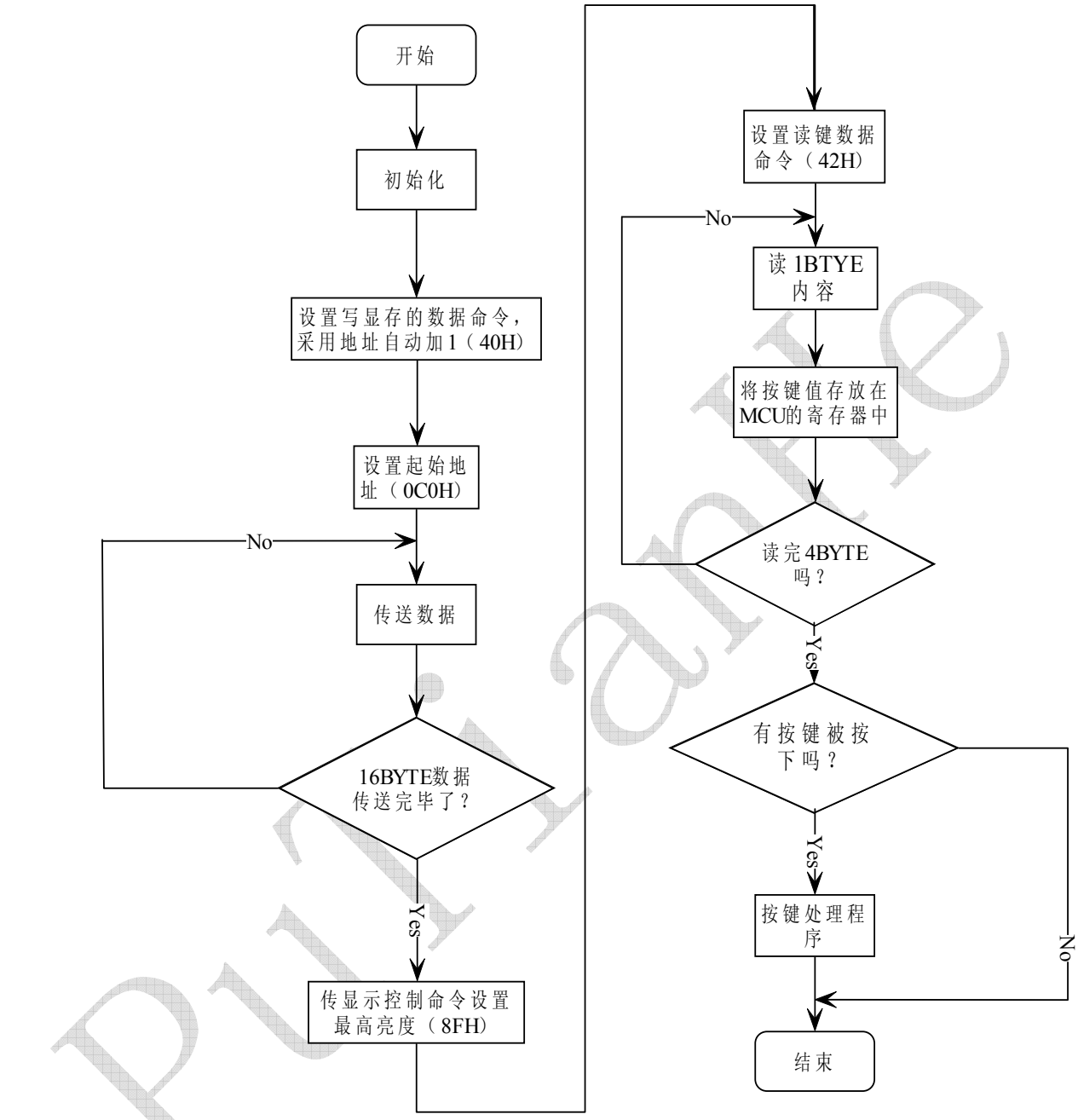
Command1: display mode setting command
Command2: data reading/writing setting command
Command3: display address setting command, to set display address 1
Data1: display data 1, save to the address unit specified by Command3
Command4: display address setting command, to set display address 2
Data2: display data 2, save to the address unit specified by Command4
Command5: display control command

3.Read time sequence of keys

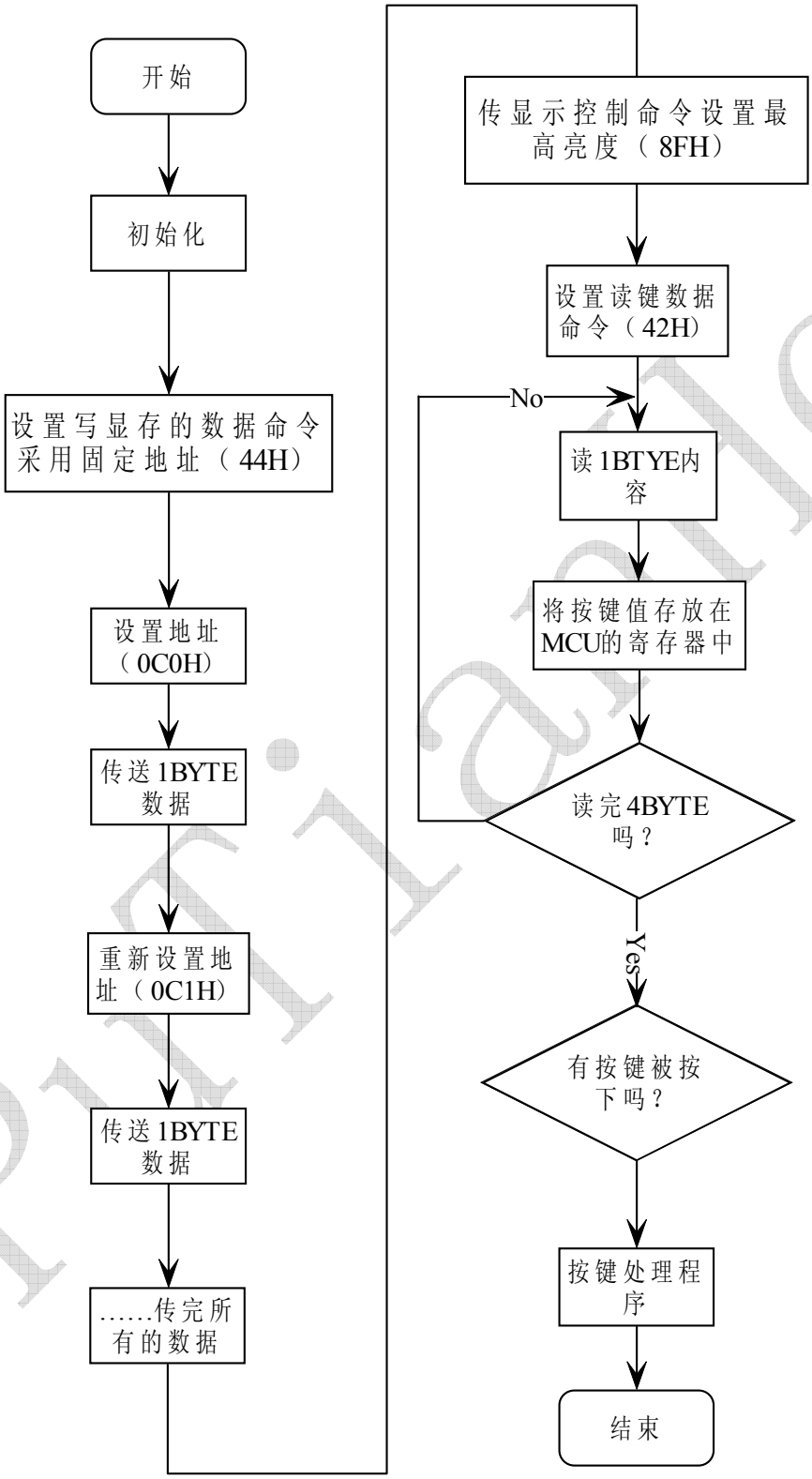


Command1: reading key command
Data1~5: reading key data

4.The flow chart adopting utomatic increase of address mode

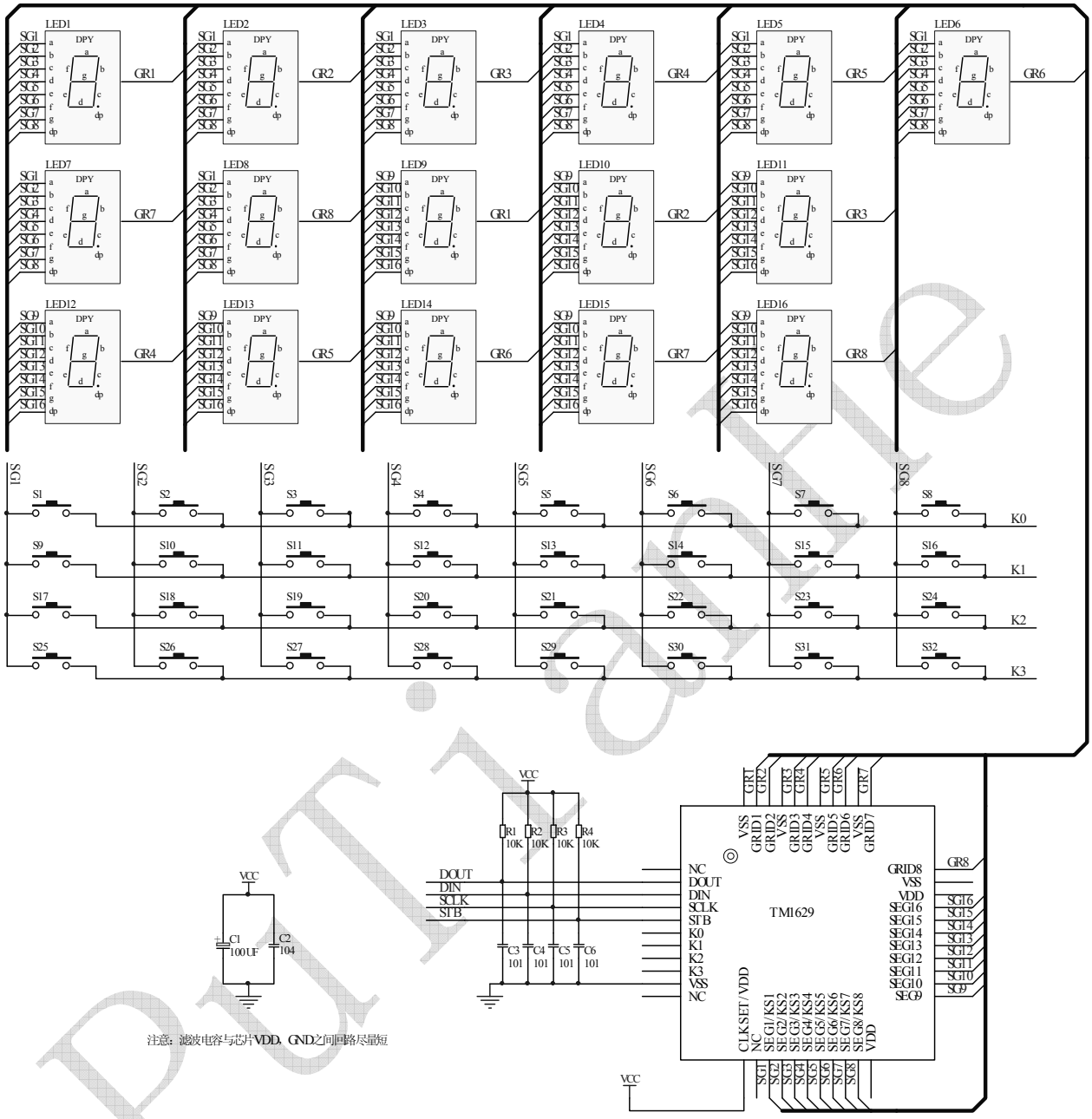


The flow chart adopting Fixed address mode



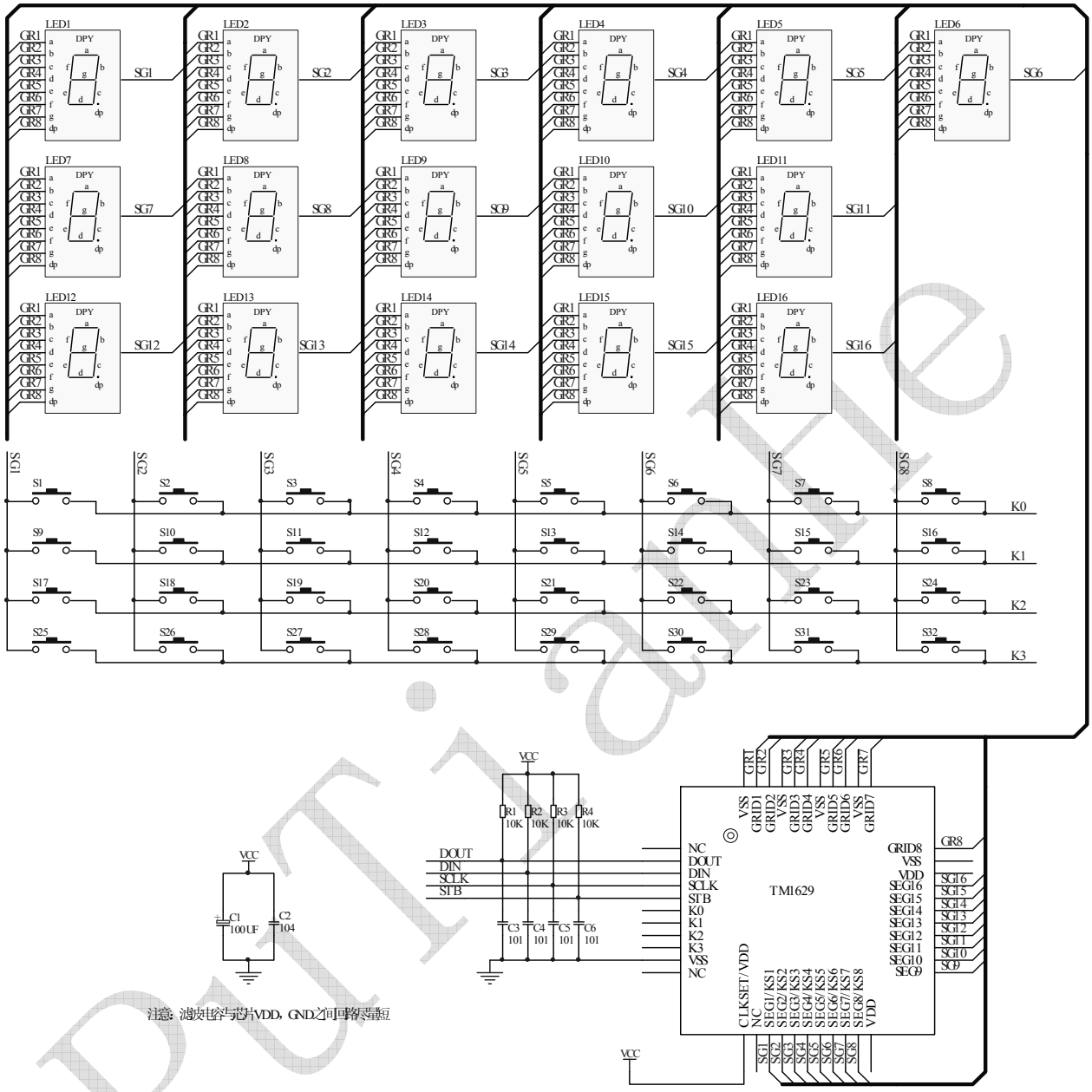
Schematic diagram

1.Connecting diagram of TM1629 driver common cathode digital screen is shown in Figure (18):



Figure（18）

2.Connecting diagram of TM1629 driver common anode digital screen is shown in Figure(19)



NOTE 1. The wiring of the filter capacitor between VDD and GND on PCB should be close to the chip of TM1629 to enhance filtering effect.

2. The three 100P capacitors connecting to DIO, CLK and STB communication ports can reduce interferences to such ports.

3. Since the conduction pressure drop of Blu-ray digital tube is 3V, the power supply of TM1629 is 5V.

Electrical parameters

1.Limit parameters (Ta 25 , Vss 0 V)

Parameter	Sign	Range	Unit
Logic supply voltage	VDD	-0.5 ～+ .0	V
Logic input voltage	VI1	-0.5 ～ VDD + 0.5	V
LED Seg driver output current	IO1	-50	m
LED Grid driver output current	IO2	+200	m
Power consumption	PD	400	mW
Operating temperature	Topt	-40 ～ +80	
Storage temperature	Tstg	-65 ～+150	

2.Normal operating range (Ta -20 ～ + 0 Vss 0 V)

Parameter	Sign	Min.	Typical	Max.	Unit	Testing condition
Logic supply voltage	VDD		5		V	-
High level input voltage	VIH	0. VDD	-	VDD	V	-
Low level input voltage	VIL	0	-	0.3 VDD	V	-

3.Electrical characteristics (Ta -20 ～ + 0 VDD 4.5 ～ 5.5 V Vss 0 V)

Parameter	Sign	Min.	Typical	M	Unit	Testing condition
High level input voltage	Ioh1	-20	-25	-40	m	Seg1~Seg11 Vo vdd-2V
	Ioh2	-20	-30	-50	m	Seg1~Seg11 Vo vdd-3V
Low level input voltage	IOL1	80	140	-	m	Grid1~Grid6 Vo 0.3V
Low level input voltage	Idout	4	-	-	m	VO 0.4V dout
High level output current tolerance	Itolsg	-	-	5	%	VO VDD – 3V Seg1～Seg11

The output pulldown resistor	RL		10		K	K1~K3
Input current	II	-	-	±1		VI VDD / VSS
High level input voltage	VIH	0. VDD	-		V	CLK DIN STB
Low level input voltage	VIL	-	-	0.3 VDD	V	CLK DIN STB
Lagging voltage	VH	-	0.35	-	V	CLK DIN STB
Dynamic current loss	IDDdyn	-	-	5	m	No load, show off

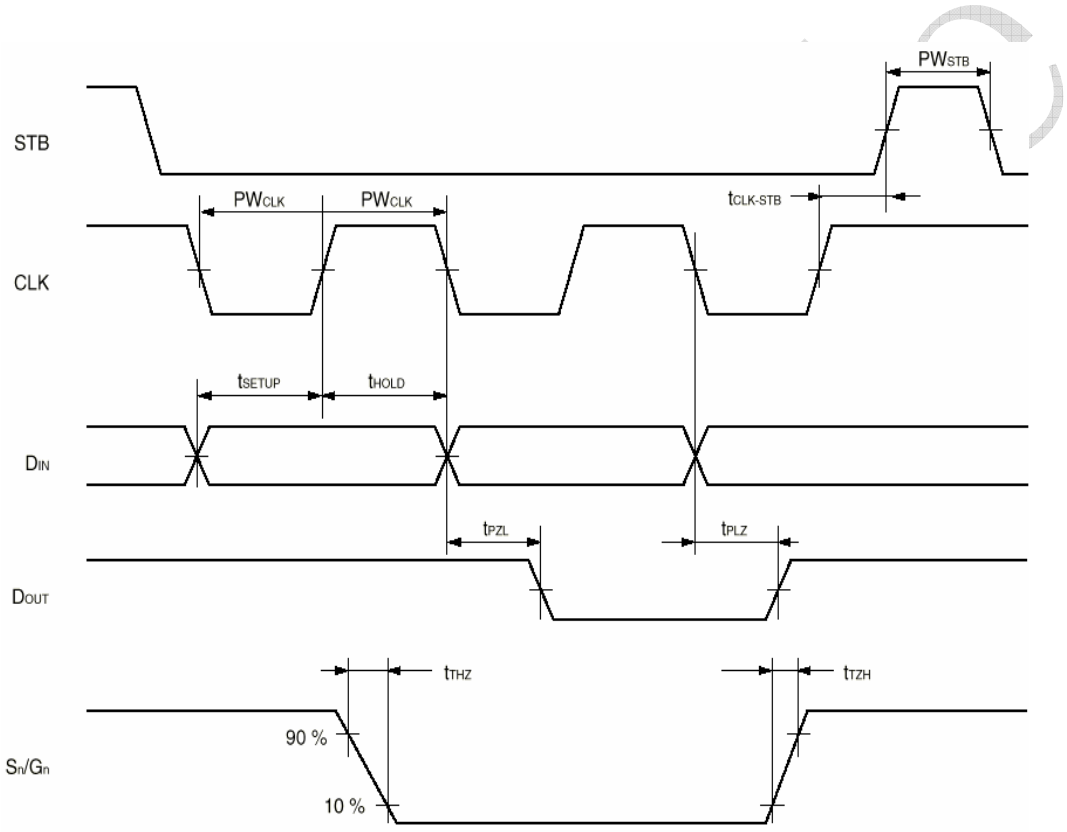
4.Switching characteristics (Ta -20 ～ + 0 VDD 4.5 ～ 5.5 V)

Parameter	Symbol	Min	Typical	Max	unit	Test condition	
Oscillation frequency	fosc	-	500	-	KHz	R 16.5 K	
Propagation delay time	tPL	-	-	300	ns	CLK DOUT	
	tP L	-	-	100	ns	CL 15pF, RL 10K	
Rise time	TT H 1	-	-	2	s	CL 300p F	Seg1～Seg11
	TT H 2	-	-	0.5	s		Grid1～Grid4 Seg12/Grid ～ Seg14/Grid5
Dome time	TTH	-	-	120	s	CL 300pF Segn Gridn	
Maximum clock frequency	Fmax	1	-	-	MHz	50%	
Input capacitance	CI	-	-	15	pF	-	

5.Timing characteristics (Ta -20 ～ + 0 VDD 4.5 ～ 5.5 V)

Parameter	Symbol	MIN	Typical	M	unit	Test conditon
Clock pulse width	PWCLK	400	-	-	ns	-
Pulse width	PWSTB	1	-	-	s	-

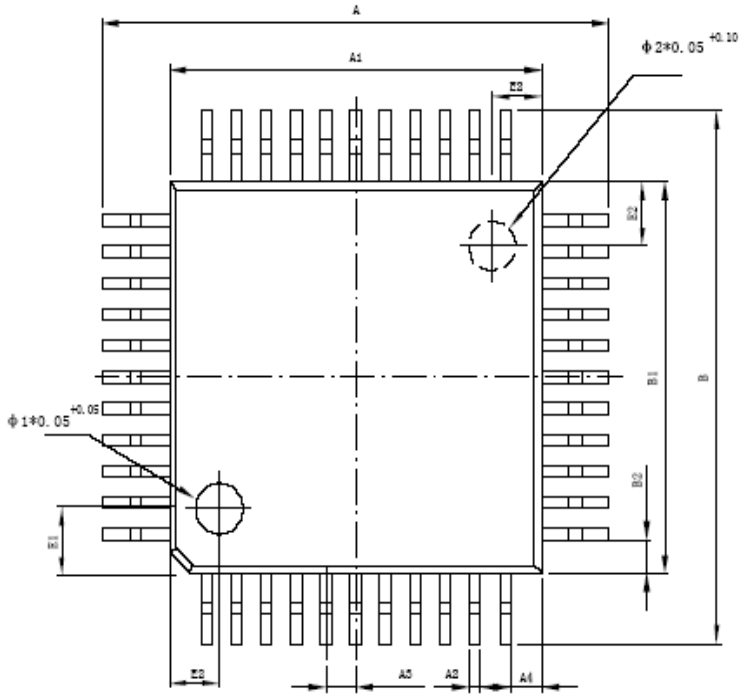
Data setup time	tSETUP	100	-	-	ns	-
Data hold time	tHOLD	100	-	-	ns	-
CLK STB TIEM	tCLK STB	1	-	-	s	CLK STB
Waiting time	tW IT	1	-	-	s	CLK CLK

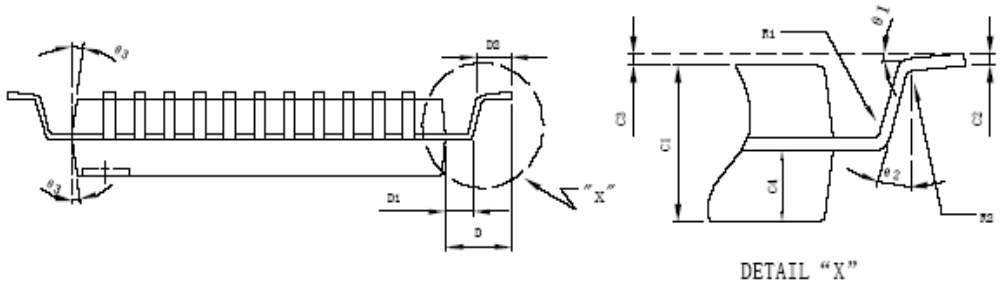


Packing Size

QFP44

尺寸 / 标注	最 小（mm）	最 大（mm）	尺寸 / 标注	最 小（mm）	最 大（mm）
A	13.20	14.00	D	1.8 TYP	
A（短脚）	12.90	13.50	D(短脚)	1.6 TYP	
A1	9.90	10.10	D1	0.80 TYP	
A2	0.30	0.375	D2	0.60	1.00
A3	0.67	0.93	E1	1.34	1.42
A4	0.85TYP		E2	1.37	1.45
B	13.20	14.00	R1	0.13MIN	
B（短脚）	12.90	13.50	R2	0.13	0.3
B1	9.90	10.10	φ1	1.5TYP	
B2	0.85TYP		φ2	1.5TYP	
C1	1.90	2.10	θ1	4° TYP	
C2	0.11	0.23	θ2	20° TYP	
C3	0.05	0.20	θ3	8° TYP	
C4	0.904	0.944			





History

Edition	Date of issue	Introduction
V1.0	2010-02-29	Trial version
V1.1	2012-0 -13	Revised edition