REV:1.0

SPECIFICATION FOR COLOR LCD MODULE

MODEL NO: TM240320BNFWG

CUSTOMER:_____

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PREPARED	CHECKED	VERIFIED BY R&D DEPT	VERIFIED BY QC DEPT	APPROVED

REVISION RECORD

Date	Rev.No.	Revision Items	Prepared	Checked	Approved
2005-12-23	1.0	FIRST RELEASE			

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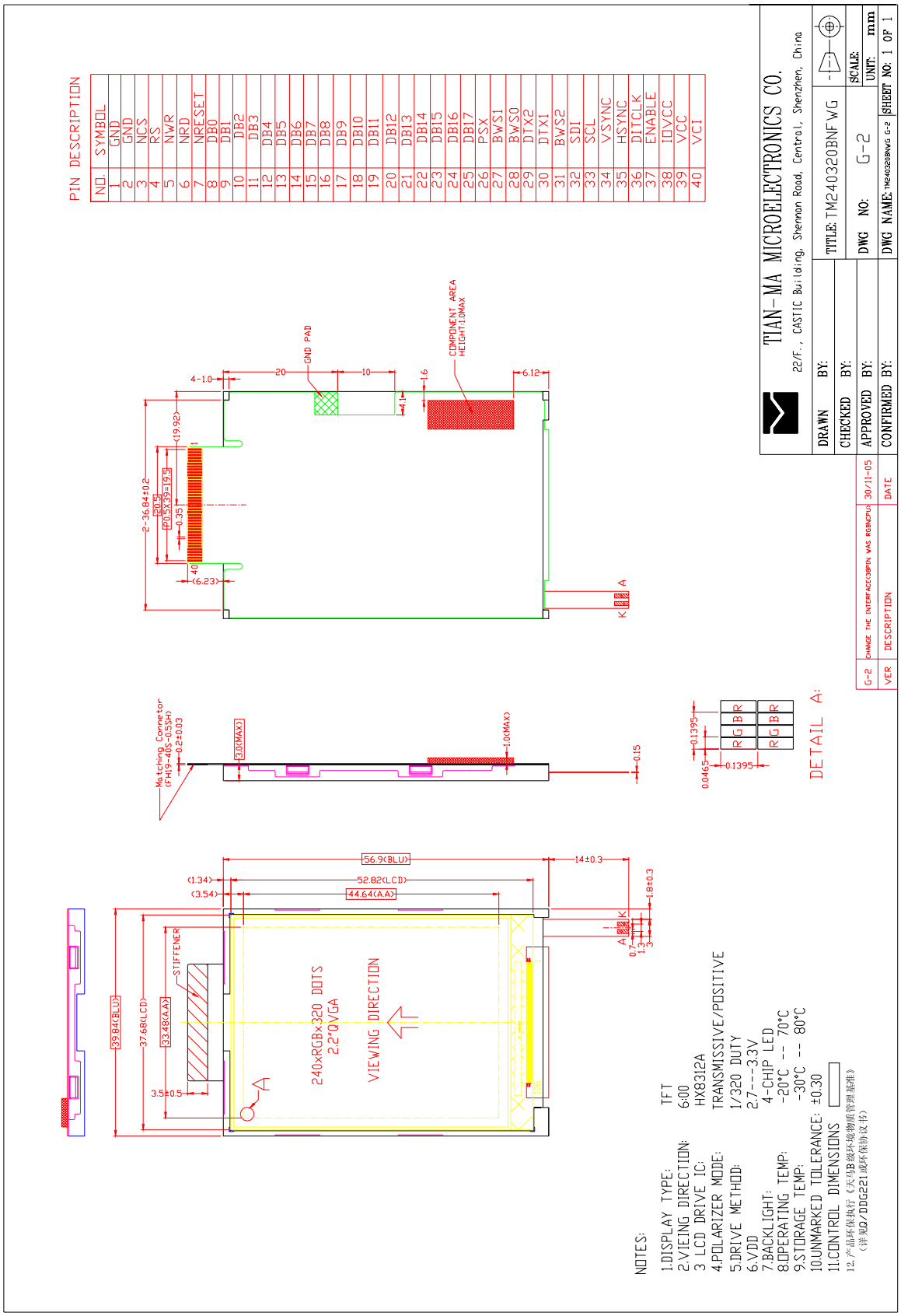
1.General Specifications

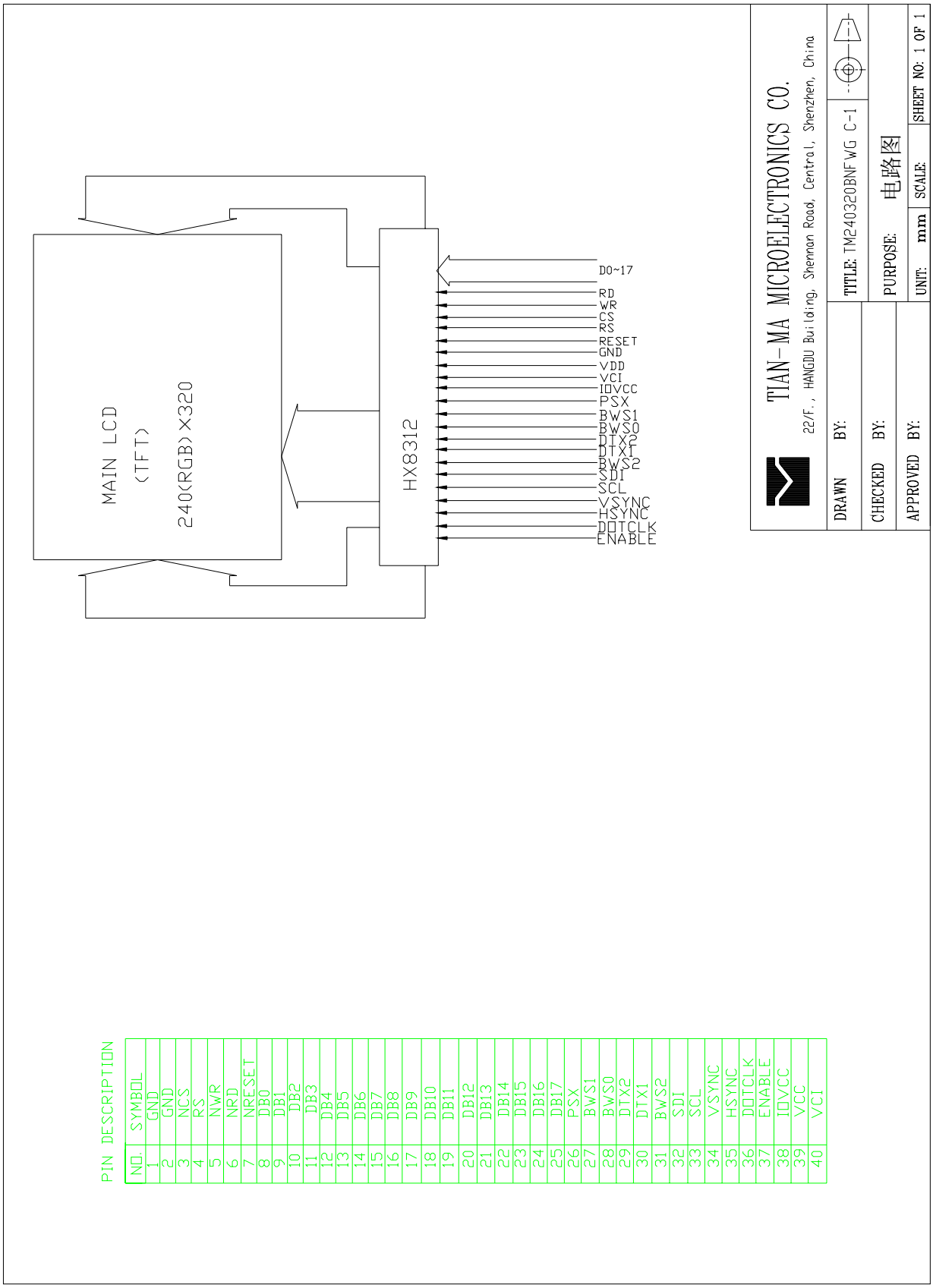
Item	Main LCD	Unit	Note
LCD Type	TFT(LTPS)	-	
Display color	262K		1
LCD Duty	1/320	-	
LCD Bias	-	-	
Viewing Direction	6:00	O'Clock	
Viewing Area(W×H)	-	mm	
Active Area(W×H)	33.48X44.64	mm	
Number of Dots	240(RGB)×320	mm	
Dot Size(W×H)	-	mm	
Dot Pitch(W×H)	0.0465X0.1395	mm	
Controller	HX8312-A	-	
V_{DD}	2.7~3.3V	V	
Outline Dimensions	Refer to outline drawing on next page		
Backlight	LED(white)	-	
Operating Temperature	-20～+70℃	-	
Storage Temperature	-30～+80℃	-	
Weight	TBD	g	2
Data Transfer	18 bits parallel	-	
Polarizer Mode	Transmissive/Positive	-	

Note 1: Select by software, and color tune is slightly changed by temperature and driving voltage.
Note 2: TBD- To Be Determined.

2. Outline Drawing



3. Circuit Block Diagram



PIN DESCRIPTION

NO.	SYMBOL
1	GND
2	GND
3	NCS
4	RS
5	NWR
6	NRD
7	NRESET
8	DB0
9	DB1
10	DB2
11	DB3
12	DB4
13	DB5
14	DB6
15	DB7
16	DB8
17	DB9
18	DB10
19	DB11
20	DB12
21	DB13
22	DB14
23	DB15
24	DB16
25	DB17
26	PSX
27	BWS1
28	BWS0
29	DTX2
30	DTX1
31	BWS2
32	SDI
33	SCL
34	VSYNC
35	HSYNC
36	DOTCLK
37	ENABLE
38	IOVCC
39	VCC
40	VCI

4. Absolute Maximum Ratings(Ta=25℃)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage(1)	V_{BAT}	-	-	V	1,2
Power Supply Voltage(2)	V_{DD}	2.4	3.3	V	
Power Supply Voltage for Mail LCD	Vop	-	-	V	
Logic Signal Input Voltage	V_I	-0.3	V_{DD}+0.3	V	
Operating Temperature	Top	-20	+70	℃	
Storage Temperature	Tst	-30	+80	℃	

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.

2. V_{DD} >V_{SS} must be maintained.

5. Electrical Specifications and Instruction Code

5.1 Electrical characteristics (Ta=25℃)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Operation voltage for Main LCM		V_{DD}	Ta=25℃	2.4	2.8	3.3	V	1
Input voltage	'H'	V_{IH}	IOVCC=1.6 ~3.3V	0.8IOVCC	-	IOVCC	V	
	'L'	V_{IL}	IOVCC=1.6 ~3.3V	-0.3V	-	0.2IOVCC	V	
Output Voltage	'H'	V_{OH}	I_{OH}=-0.1mA	0.8IOVCC	-	-	V	
	'L'	V_{OL}	I_{OL} =0.1mA	-	-	0.2IOVCC	V	
Current Consumption		I_{CC1}	Normal mode	-	70	80	mA	2
		I_{CC2}	Stand-by mode	-	2.5	4	mA	3
		I_{CC3}	Dimming mode	-	-	-	mA	4

Note:

1: IC default setting, Duty:1/320

2: Display full white. Backlight on state.

3: IC on standby mode, VBAT=3.8V.

4: Display full white. Backlight dimming state.

5.2 Interface Signal

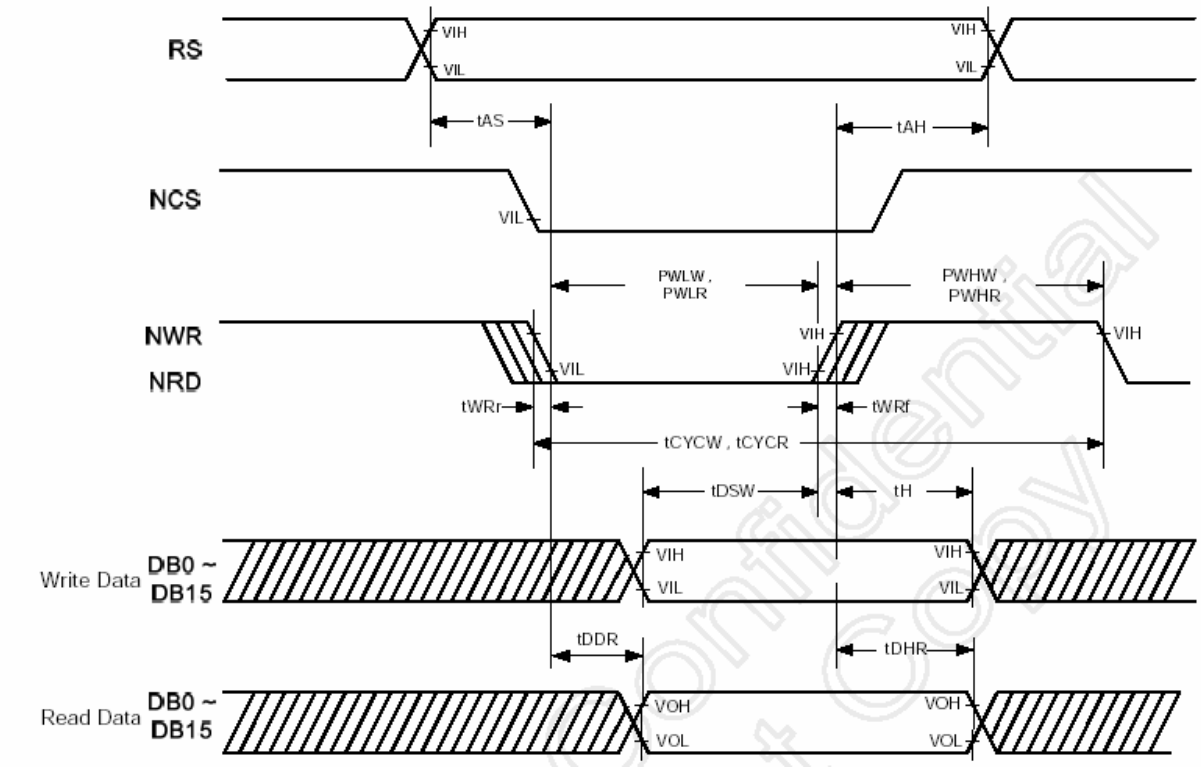
Pin No.	Symbol	I/O	Function
1	GND	I	Power Ground
2	GND	I	Power Ground
3	CS	I	Chip select input pin
4	RS	I	Instruction /data select input pin
5	WR	I	Write execution control pin
6	RD	I	Read execution control pin
7	RESET	I	System reset
8	D0	I/O	DATA BUS
9	D1	I/O	
10	D2	I/O	
11	D3	I/O	
12	D4	I/O	
13	D5	I/O	
14	D6	I/O	
15	D7	I/O	
16	D8	I/O	
17	D9	I/O	
18	D10	I/O	
19	D11	I/O	
20	D12	I/O	
21	D13	I/O	
22	D14	I/O	
23	D15	I/O	
24	D16	I/O	
25	D17	I/O	
26	PSX	I	The parallel and serial bus interface selection in system interface circuit
27	BWS1	I	The bus width selection in system interface circuit
28	BWS0	I	

29	DTX2	I	Specify the transferring method of one pixel data in system interface
30	DTX1	I	
31	BWS2		The bus width selection in RGB interface circuit
32	SDI		Serial bus interface data input pin
33	SCL		Serial bus interface clock input pin
34	VSYNC		Vertial synchronization signal input pin
35	HSYNC		Horizontal synchronization signal input pin
36	DOTCLK		Dot clock singal input used in the RGB interface circuit
37	ENABLE		Enable singal pin used in the RGB interface circuit
38	IOVCC		A Power supply for I/O circuit
39	VCC		A Power supply for the internal logic circuit
40	VCI		A Power supply for set-up circuit and power supply circuit

Note: Please refer to HIMAX HX8312-A data sheet for more details.

5.3 Interface Timing Chart

80-system Bus Operation

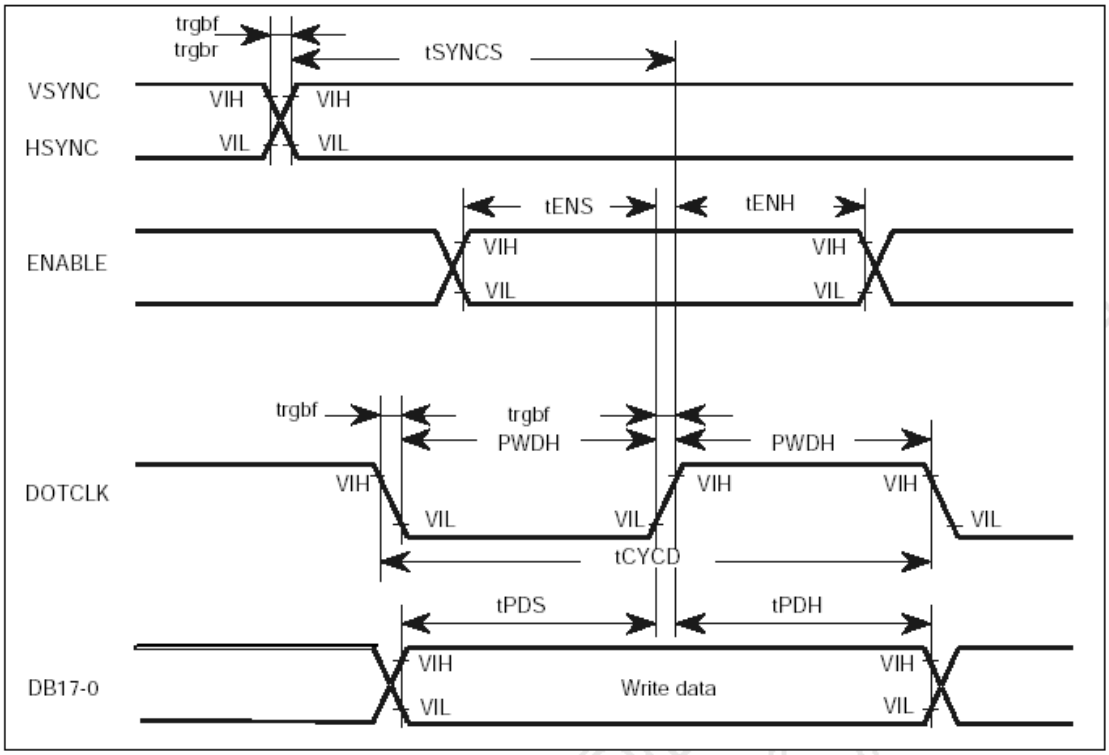


80-system Bus Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	200	-	-	Figure 17.1
	Read	t_{CYCR}	ns	300	-	-	Figure 17.1
Write low-level pulse width		PW_{LW}	ns	40	-	-	Figure 17.1
Read low-level pulse width		PW_{LR}	ns	150	-	-	Figure 17.1
Write high-level pulse width		PW_{HW}	ns	70	-	-	Figure 17.1
Read high-level pulse width		PW_{HR}	ns	150	-	-	Figure 17.1
Write / Read rise / fall time		t_{WRr} , t_{WRf}	ns	-	-	25	Figure 17.1
RS Setup time	(RS to NCS, NWR)	t_{AS}	ns	5	-	-	Figure 17.1
RS hold time	(NCS, NWR to RS)	t_{AH}	ns	5	-	-	Figure 17.1
Write data set up time		t_{DSW}	ns	20	-	-	Figure 17.1
Write data hold time		t_{H}	ns	15	-	-	Figure 17.1
Read data delay time		t_{DDR}	ns	-	-	100	Figure 17.1
Read data hold time		t_{DHR}	ns	5	-	-	Figure 17.1

Table 17. 3. 1 Normal Write Mode (IOVCC = 1.65 ~ 2.4V) / (VCC = 2.4V~3.3V)

RGB Interface Operation

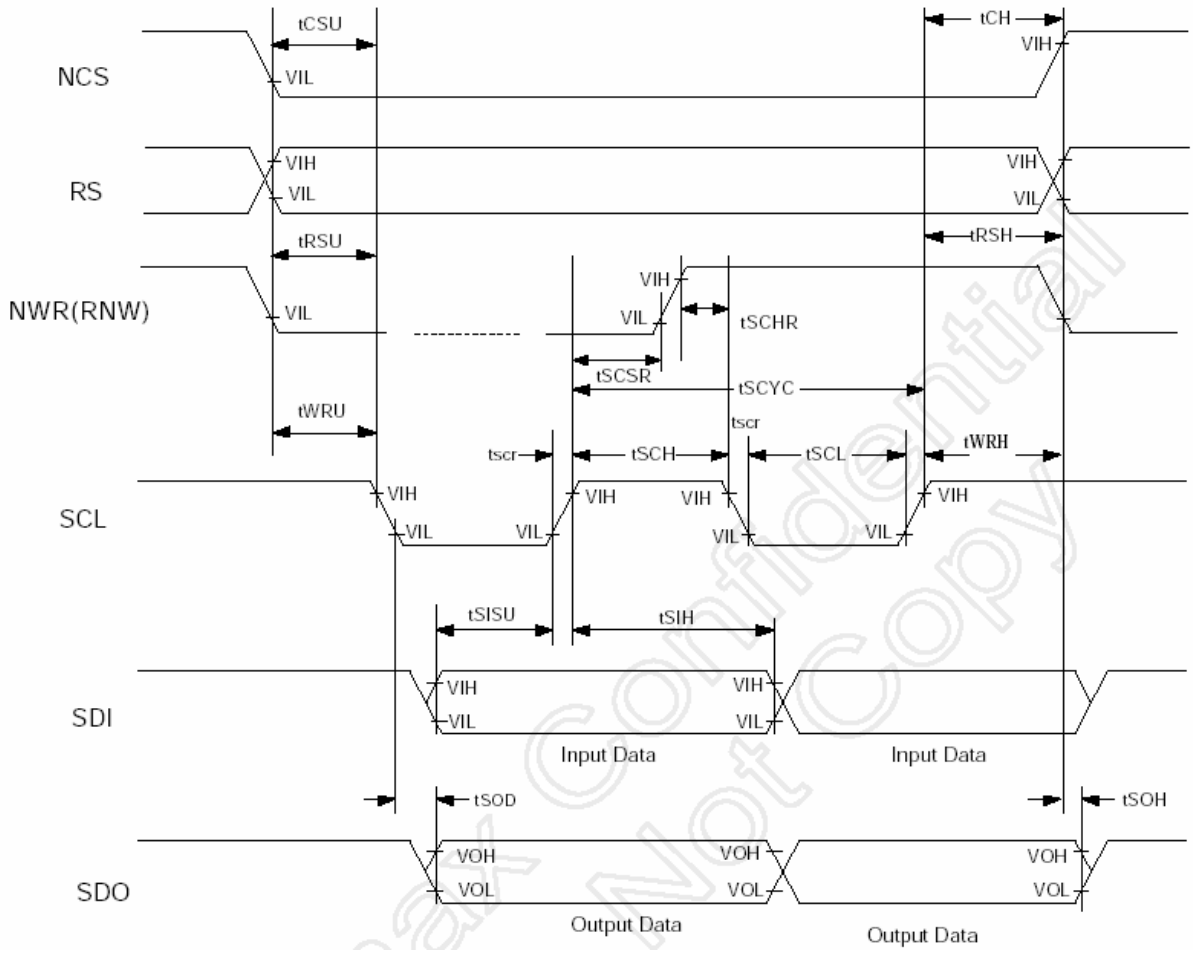


RGB Interface Timing Characteristics

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	t_{SYNCS}	ns	10	-	-	Figure 17.4
ENABLE set up time	t_{ENS}	ns	10	-	-	Figure 17.4
ENABLE hold time	t_{ENH}	ns	10	-	-	Figure 17.4
DOTCLK “low” level pulse width	PW_{DL}	ns	40	-	-	Figure17.4
DOTCLK “high” level pulse width	PW_{DH}	ns	40	-	-	Figure17.4
DOTCLK cycle time	t_{CYCD}	ns	200	-	-	Figure17.4
DATA set up time	t_{PDS}	ns	20	-	-	Figure17.4
DATA hold time	t_{PDH}	ns	20	-	-	Figure17.4
DOTCLK , VSYNC , HSYNC rising and falling time	t_{rgbr} , t_{rgbf}	ns	-	-	25	Figure17.4

Table 17. 6. 1 RGB interface mode, Normal Write Mode (IOVCC=1.65~2.4V) / (VCC = 2.4V~3.3V)

Clock Synchronized Serial Data Transfer Interface Operation



Serial Data Transfer Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	ns	100	-	-	Figure 17.3
	Read (transmitted)	t_{SCYC}	ns	200	-	-	Figure 17.3
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	Figure 17.3
	Read (transmitted)	t_{SCH}	ns	150	-	-	Figure 17.3
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	Figure 17.3
	Read (transmitted)	t_{SCL}	ns	150	-	-	Figure 17.3
Serial clock rise / fall time		t_{scr} , t_{scf}	ns	-	-	20	Figure 17.3
Chip select (NCS) set up time		t_{CSU}	ns	20	-	-	Figure 17.3
Chip select (NCS) hold time		t_{CH}	ns	60	-	-	Figure 17.3
RS set up time		t_{RSU}	ns	10			Figure 17.3
RS hold time		t_{RSH}	ns	10			Figure 17.3
Read/write select (RNW) set up time		t_{WRU}	ns	10			Figure 17.3
Read/write select (RNW) hold time		t_{WRH}	ns	10			Figure 17.3
Read clock set up time		t_{SCSR}	ns	10			Figure 17.3
Read clock hold time		t_{SCHR}	ns	10			Figure 17.3
Serial input data set up time		t_{SISU}	ns	30	-	-	Figure 17.3
Serial input data hold time		t_{SIH}	ns	30	-	-	Figure 17.3
Serial output data delay time		t_{SOD}	ns	-	-	100	Figure 17.3
Serial output data hold time		t_{SOH}	ns	5	-	-	Figure 17.3

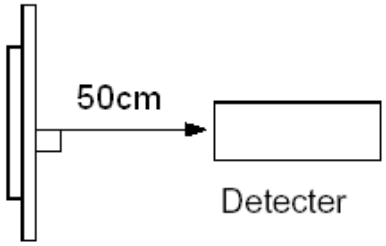
Table 17. 5. 1 (IOVCC=1.65~3.3V) / (VCC = 2.4V~3.3V)

6. Optical Characteristics

6.1 Main LCD

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		Φ_1=0° Φ_2=0°	150			Cd/m^2	1
Uniformity	△Bp			70%				1,2
Viewing Angle	Φ_1(up down)		Cr≥2	-15～+35			Deg	3
	Φ_2(left right)			-45～+45				
Contrast Ratio	Cr		Φ_1=0° Φ_2=0°	40	50	70	-	4
Response Time	Tr+ T_f			-	40	60	ms	5
Color of CIE Coordinate	W	x	Φ_1=0° Φ_2=0°	0.26	0.30	0.34	-	1,6
		y		0.26	0.30	0.34	-	
	R	x		0.46	0.50	0.54	-	
		y		0.29	0.33	0.37	-	
	G	x		0.27	0.31	0.35	-	
		y		0.47	0.51	0.55	-	
	B	x		0.12	0.16	0.20	-	
		y		0.14	0.18	0.22	-	
NTSC Ratio	S				50%			

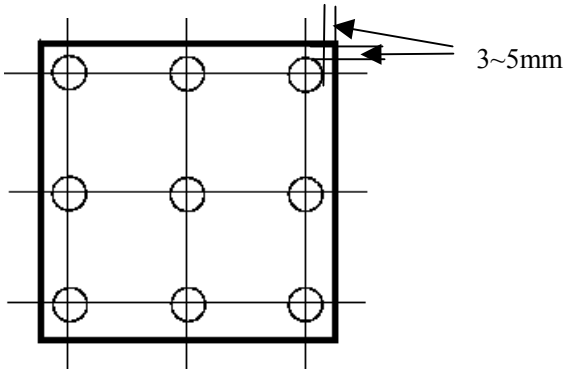
Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ10mm)



Note 2: △Bp = Bp (Min.) / Bp (Max.)×100 (%)

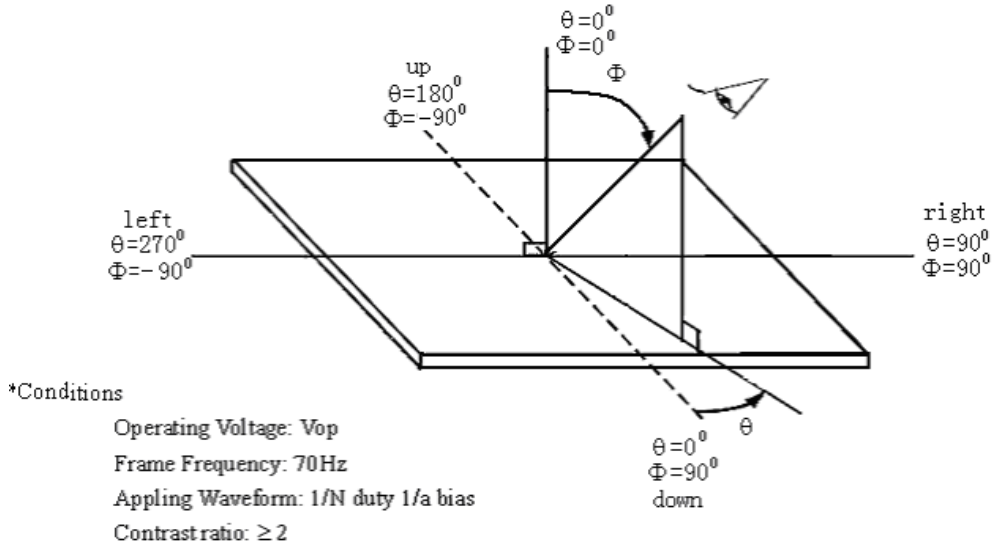
Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.



Measurement equipment PR-705 (Φ10mm)

Note 3: Definition of Viewing Angle(Test LCD using DMS501)



*Conditions

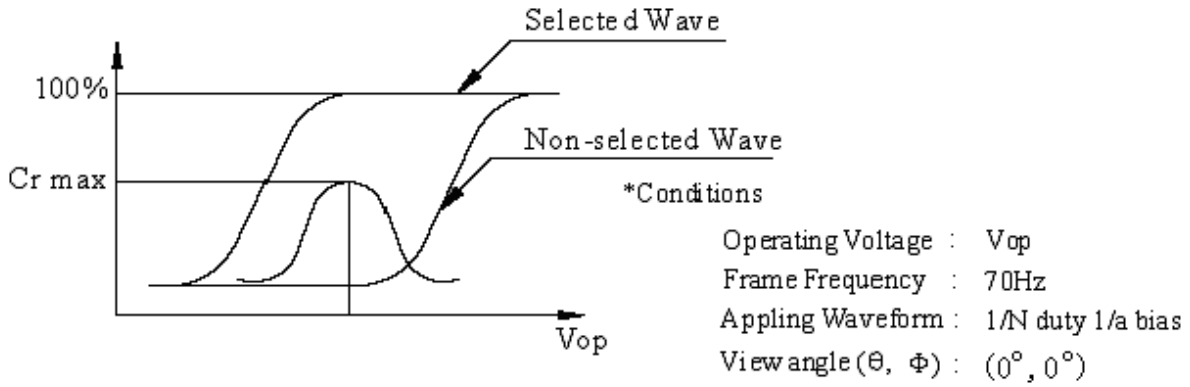
Operating Voltage: Vop

Frame Frequency: 70Hz

Appling Waveform: 1/N duty 1/a bias

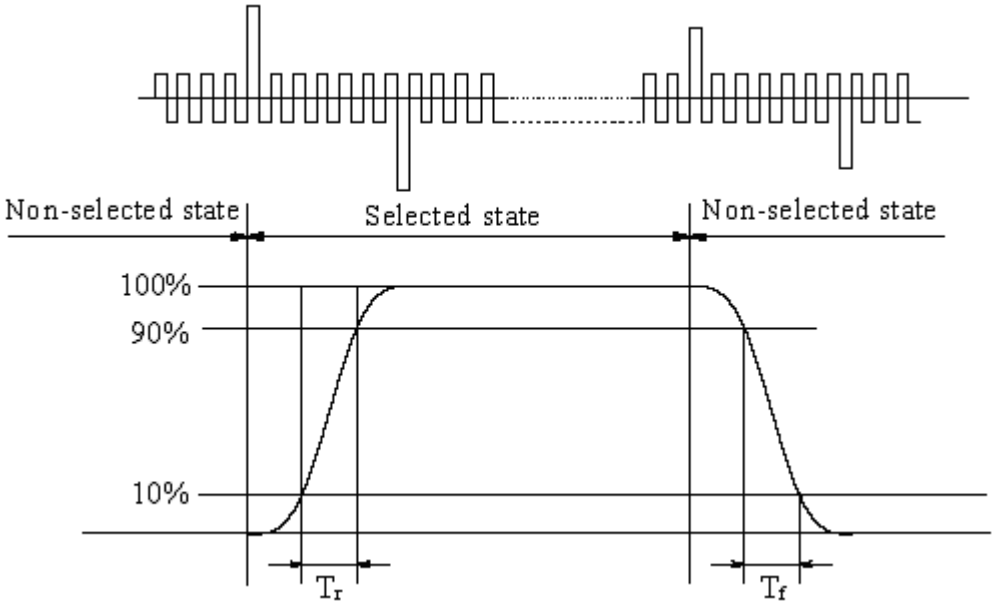
Contrast ratio: ≥2

Note 4: Definition of contrast ratio.(Test LCD using DMS501)



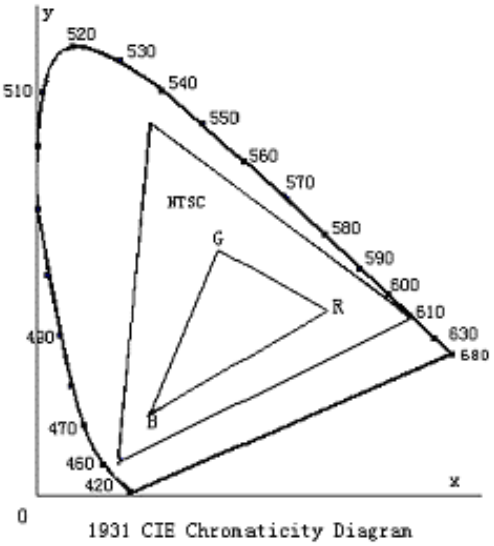
$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

Note 5: Definition of Response time(Test LCD using DMS501)



Operating Voltage: Vop
Frame Frequency: 70Hz
Appling Waveform: 1/N duty 1/a bias
View angle (θ, Φ): (0^0, 0^0)

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.



1931 CIE Chromaticity Diagran

Color gamut:

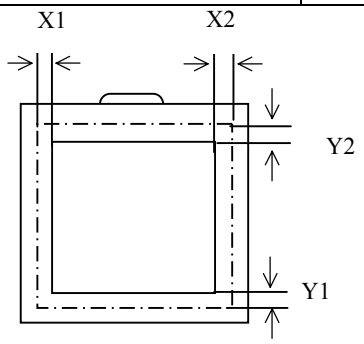
$$S = \frac{area\ \ of\ \ RGB\ \ triangle}{area\ \ of\ \ NTSC\ \ triangle} \times 100\%$$

7. Reliability

No.	Test Item	Test condition	Criterion
1	High Temperature Storage	80℃±2℃96H Restore 4H at 25℃	1. After testing, cosmetic defects should not happen. 2.Total current consumption should not be over 10% of initial value.
2	Low Temperature Storage	-30℃±2℃ 96H Restore 4H at 25℃	
3	High Temperature Operation	70℃±2℃ 48H Restore 4H at 25℃	
4	Low Temperature Operation	-20℃±2℃ 48H Restore 4H at 25℃	
5	High Temperature /Humidity Storage	40℃±2℃ 90%RH 48H	
6	Temperature Cycle	-30℃←→25℃←→80℃ 5min 30min ←→25℃ , 5min after 10cycle, Restore 4H at 25℃	
7	Vibration Test (package state)	10Hz~150Hz, 100m/s2, 120min	Not allowed cosmetic and electrical defects.
8	Shock Test (package state)	Half- sine wave, 300m/s2, 18ms	
9	Atmospheric Pressure Test	25kPa 16H Restore 2H	
10	Cable Bending Test	Bending area and angle follow design document requirement	More than 50000 times

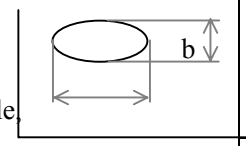
8 Quality level

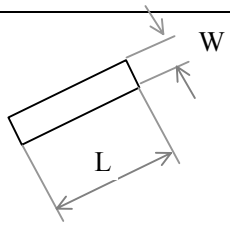
8.1 Notes for quality standard

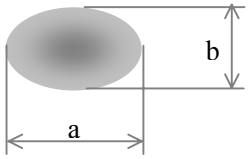
<table>
<tr><th></th><th colspan="2">Note</th></tr>
<tr><td>General</td><td colspan="2">1. Should any defects which are not specified in this standard happen, additional standard shall be determined by mutual agreement between customer and Tianma.
2. Viewing Area should be the area which Tianma guarantees.
3. Limited sample should be prior to this Inspection standard.
4. Viewing Judgement should be under static pattern.
5. Inspection conditions
Inspection distance : 250 mm (from the sample)
Temperature : 25±5℃
Inspection angle : 45degrees in LCD view direction</td></tr>
<tr><td rowspan="4">Definitions of Inspection items</td><td>Pinhole, Bright spot, Black spot, White spot, Black line, White Line, Foreign particle, Bubble</td><td>The color of a small area is different from the remainder.
The phenomenon dose not change with voltage.</td></tr>
<tr><td>Contrast variation</td><td>The color of a small area is different from the remainder.
The phenomenon changes with voltage.</td></tr>
<tr><td>Polarizer defect</td><td>Scratch, Dirt, Particle, Bubble on polarizer or between polarizer and glass.</td></tr>
<tr><td>Glass defect</td><td>Glass crack, Shaved corner of glass, Surplus glass</td></tr>
<tr><td>Definitions of Inspection ranges</td><td colspan="2"> 

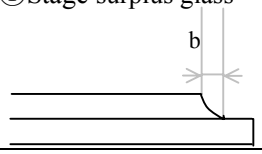
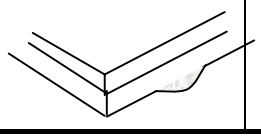
Dividing A zone and B zone proceed to make a judgment.
A zone : Inside Viewing area
B zone : Outside Viewing area
X1(A.A~V.A): mm
X2(A.A~V.A): mm
Y1(A.A~V.A): mm
Y2(A.A~V.A): mm</td></tr>
<tr><td>Outgoing Inspection standard</td><td colspan="2">Inspection level Ⅱ Normal Inspection. Sampling standard conforms to GB2828
<table>
<tr><th>Rank</th><th>Inspection Item</th><th>AQL(Number of defective LCMs counted)</th></tr>
<tr><td>Major defect</td><td>All Functional defects(Such as No display, Display abnormally, Open or missing segment, Short circuit，Missing component, No sound, Blight abnormally),Outline dimension beyond the drawing</td><td>0.65</td></tr>
<tr><td>Minor defect</td><td>Appearance defects, such as Black/White spot, Bright spot, Pinhole, Black/White line, Contrast variation, Bubble Glass defect, Polarizer defect, and so on. Details of the standard as follows.</td><td>1.50</td></tr>
</table></td></tr>
</table>

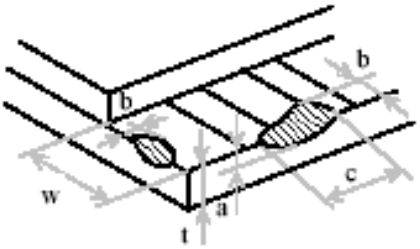
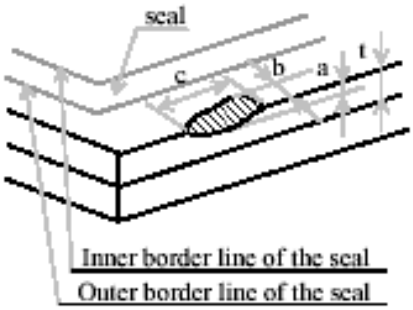
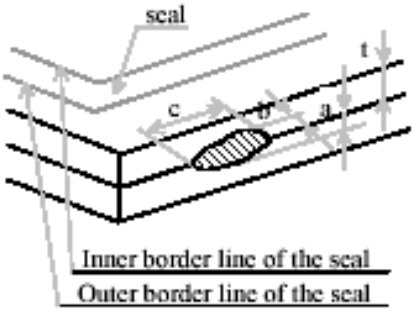
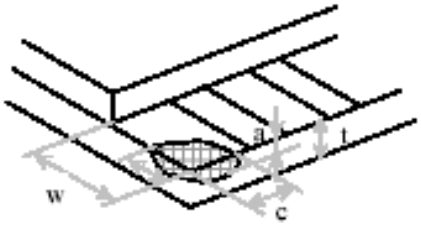
8.2Standards of inspection items

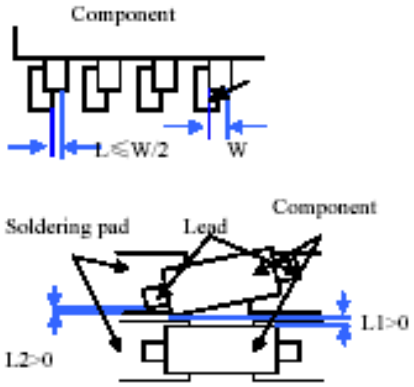
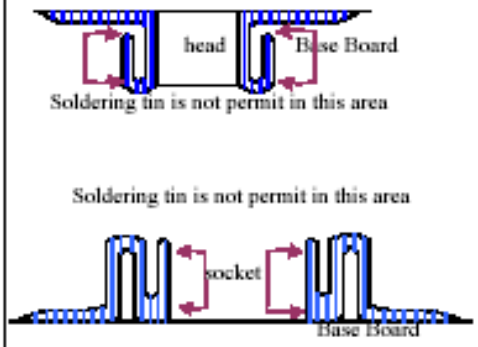
<table>
<tr><th colspan="3" rowspan="3">Inspection item</th><th colspan="3">Judgement standard</th></tr>
<tr><th colspan="2" rowspan="2">Category</th><th colspan="2">Acceptable number</th></tr>
<tr><th>A zone</th><th>B zone</th></tr>
<tr><td>1</td><td>Black spot, White spot Bright Spot, Pinhole Foreign Particle, Bubble and Particle Between polarizer and glass, Scratch on polarizer</td><td> 

Φ=(a+b)/2(mm)</td><td>A
B
C
D
Total defective point(B,C)</td><td>Φ≦0.15
0.15<Φ≦0.20
0.20<Φ≦0.30
0.30<Φ</td><td>Neglecte
2
1
0
3</td><td>Neglected</td></tr>
<tr><td>2</td><td>Black line, White line, Bubble and Particle Between Polarizer and glass, Scratch on polarizer</td><td> 

W:Width,
L:Length(mm)</td><td>A
B
C
D
Total defective point(B,C)</td><td>W≦0.10
0.01<W≦0.03 L≦3.0
0.03<W≦0.05 L≦3.0
0.05<W</td><td>Neglected
2
1
0
2</td><td>Neglected</td></tr>
<tr><td>3</td><td>Contrast variation</td><td> 

Φ=(a+b)/2(mm)</td><td>A
B
C
D
Total defective point(B,C)</td><td>Φ≦0.2
0.2<Φ≦0.3
0.3<Φ≦0.4
0.4<Φ</td><td>Neglected
2
1
0
3</td><td>Neglected</td></tr>
<tr><td>4</td><td>Bubble inside cell</td><td></td><td colspan="2">any size</td><td>none</td><td>none</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">Polarizer defect (if Polarizer is used)</td><td>Scratch and damage on polarizer, Particle on polarizer or between polarizer and glass.</td><td colspan="4">Refer to item 1 and item 2.</td></tr>
<tr><td>Bubble, dent and convex</td><td>A
B
C
Total defective point(B,C)</td><td>Φ≦0.3
0.3<Φ≦0.7
0.7<Φ</td><td>Neglected
2
0
2</td><td>Neglected</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">Surplus glass</td><td>①Stage surplus glass
 
</td><td colspan="4">b≦0.3mm</td></tr>
<tr><td>②Surrounding surplus glass
  </td><td colspan="4">Should not influence outline dimension and assembling.</td></tr>
</table>

Inspection item			Judgment standard	
			Category(application: B zone)	
7	Glass defect crack	①The front of lead terminals 	A	If a ≤ t and b ≤ 1.0, c is not limited
			B	a ≤ t, 1≤b≤2mm, c≤3mm
			C	If glass crack cover alignment mark, b≤0.5mm.
			D	Crack at two sids of lead terminals should not cover patterns and alignment mark
		②Surrounding crack—non-contact side 	b < Inner borderline of the seal	
		③ Surrounding crack— contact side 	b < Outer borderline of the seal	
		④Corner 	A	a ≤ t, b ≤ 3.0, c ≤ 3.0
			*Glass crack should not cover patterns used for	

Inspection item			Judgement standard
8	PCB defect	Component soldering: No cold soldering、short、open circuit、burr、tin ball The flat encapsulation component position deviation must be less than 1/2 width of the pin (Pic.1); the sheet component deviation: Pin deviates from the pad and contact with the near components is not permitted（Pic.2）	
		lead defect: The lead lack must be less than 1/2 of its width; The lead burr must be less than 1/2 of the seam; Impurities connect with the near leads is not permitted	
		Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted	

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol

— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water

— Ketone

— Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤80%

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.