

- **Organization:**
 - TM2SN64EPU . . . 2 097 152 x 64 Bits
 - TM4SN64EPU . . . 4 194 304 x 64 Bits
- **Single 3.3-V Power Supply ($\pm 10\%$ Tolerance)**
- **Designed for 66-MHz 4-Clock Systems**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **TM2SN64EPU — Uses Eight 16M-Bit Synchronous Dynamic RAMs (SDRAMs) ($2M \times 8$ -Bit) in Plastic Thin Small-Outline Packages (TSOPs)**
- **TM4SN64EPU — Uses Sixteen 16M-Bit SDRAMs ($2M \times 8$ -Bit) in Plastic TSOPs**
- **Byte-Read/Write Capability**
- **Performance Ranges:**
 - **High-Speed, Low-Noise Low-Voltage TTL (LVTTTL) Interface**
 - **Read Latencies 2 and 3 Supported**
 - **Support Burst-Interleave and Burst-Interrupt Operations**
 - **Burst Length Programmable to 1, 2, 4, and 8**
 - **Two Banks for On-Chip Interleaving (Gapless Access)**
 - **Ambient Temperature Range 0°C to 70°C**
 - **Gold-Plated Contacts**
 - **Pipeline Architecture**
 - **Serial Presence-Detect (SPD) Using EEPROM**

	SYNCHRONOUS CLOCK CYCLE TIME		ACCESS TIME CLOCK TO OUTPUT		REFRESH INTERVAL
	t_{CK3} (CL = 3) [†]	t_{CK2} (CL = 2)	t_{CK3} (CL = 3)	t_{CK2} (CL = 2)	
'xSN64EPU-12A [‡]	12 ns	15 ns	9 ns	9 ns	64 ms
'xSN64EPU-12	12 ns	18 ns	9 ns	10 ns	64 ms

[†] CL = CAS latency

[‡] -12A speed device is supported only at -5 to $+10\%$ V_{DD}

description

The TM2SN64EPU is a 16M-byte, 168-pin dual-in-line memory module (DIMM). The DIMM is composed of eight TMS626812DGE, 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic thin small-outline package (TSOP) mounted on a substrate with decoupling capacitors. See the TMS626812 data sheet (literature number SMOS687).

The TM4SN64EPU is a 32M-byte, 168-pin DIMM. The DIMM is composed of sixteen TMS626812DGE, 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS626812 data sheet (literature number SMOS687).

operation

The TM2SN64EPU operates as eight TMS626812DGE devices that are connected as shown in the TM2SN64EPU functional block diagram. The TM4SN64EPU operates as 16 TMS626812DGE devices connected as shown in the TM4SN64EPU functional block diagram.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

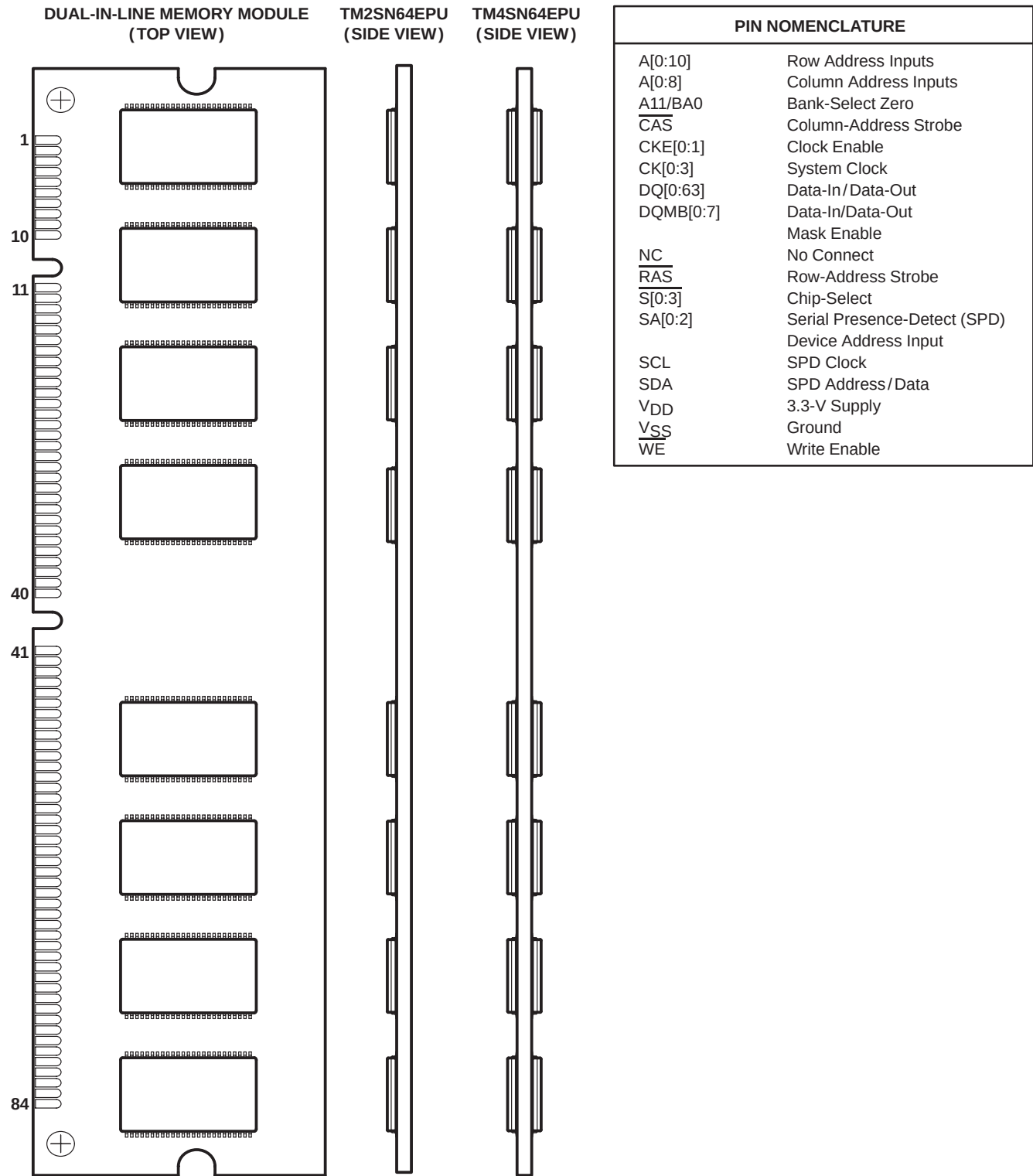
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SYNCHRONOUS DYNAMIC RAM MODULES

SMMS681 – AUGUST 1997



Pin Assignments

NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	$\overline{S2}$	87	DQ33	129	$\overline{S3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V _{DD}	48	NC	90	V _{DD}	132	NC
7	DQ4	49	V _{DD}	91	DQ36	133	V _{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{DD}	101	DQ45	143	V _{DD}
18	V _{DD}	60	DQ20	102	V _{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1	105	NC	147	NC
22	NC	64	V _{SS}	106	NC	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V _{DD}	68	V _{SS}	110	V _{DD}	152	V _{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{S0}$	72	DQ27	114	$\overline{S1}$	156	DQ59
31	NC	73	V _{DD}	115	$\overline{RAS}$	157	V _{DD}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	A11/BA0	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V _{DD}	82	SDA	124	V _{DD}	166	SA1
41	V _{DD}	83	SCL	125	CK1	167	SA2
42	CK0	84	V _{DD}	126	NC	168	V _{DD}

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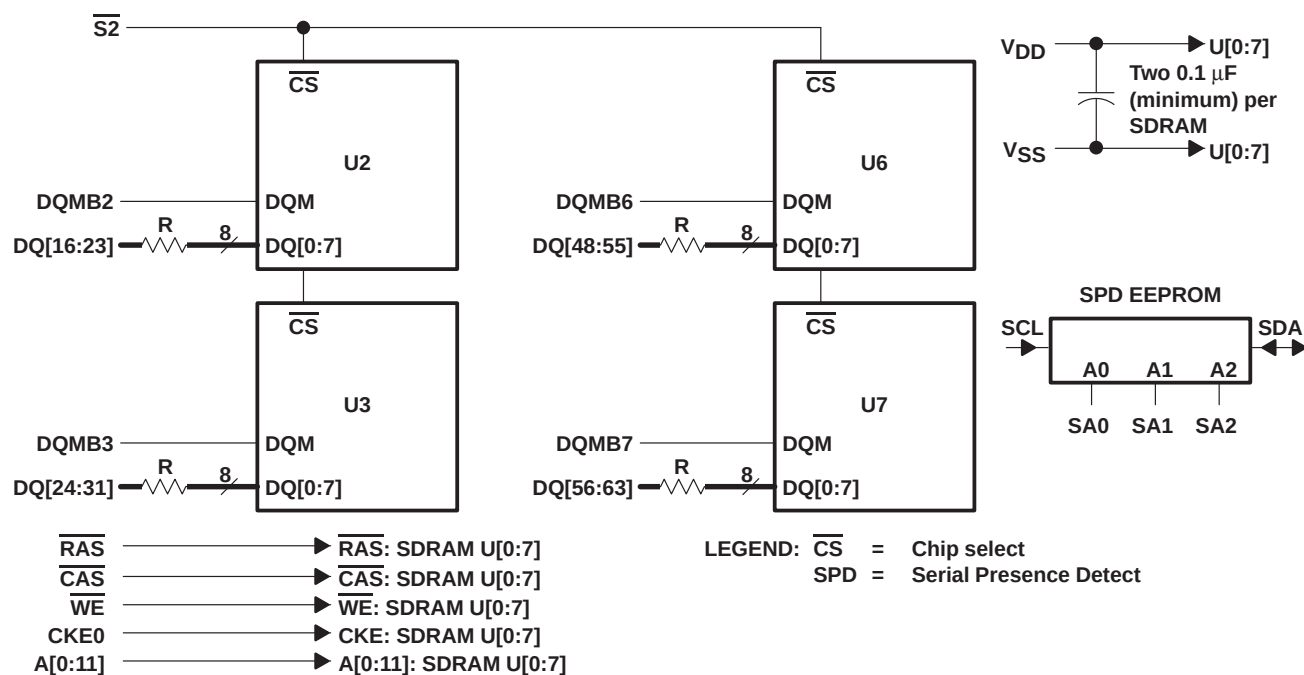
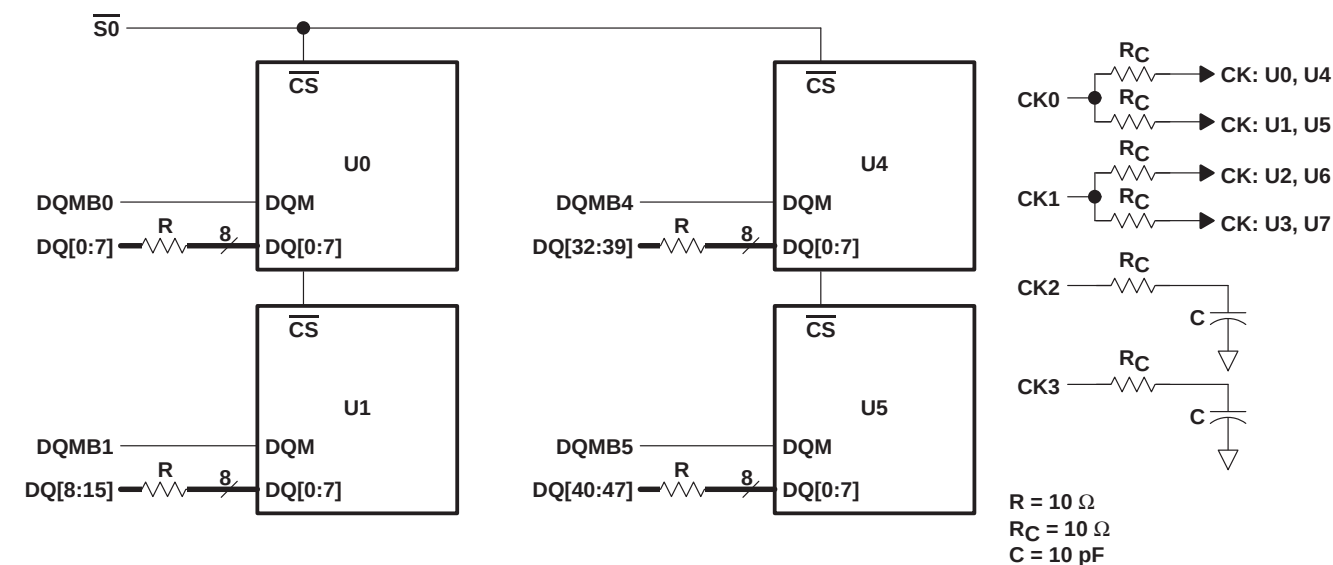
SMMS681 – AUGUST 1997

dual-in-line memory module and components

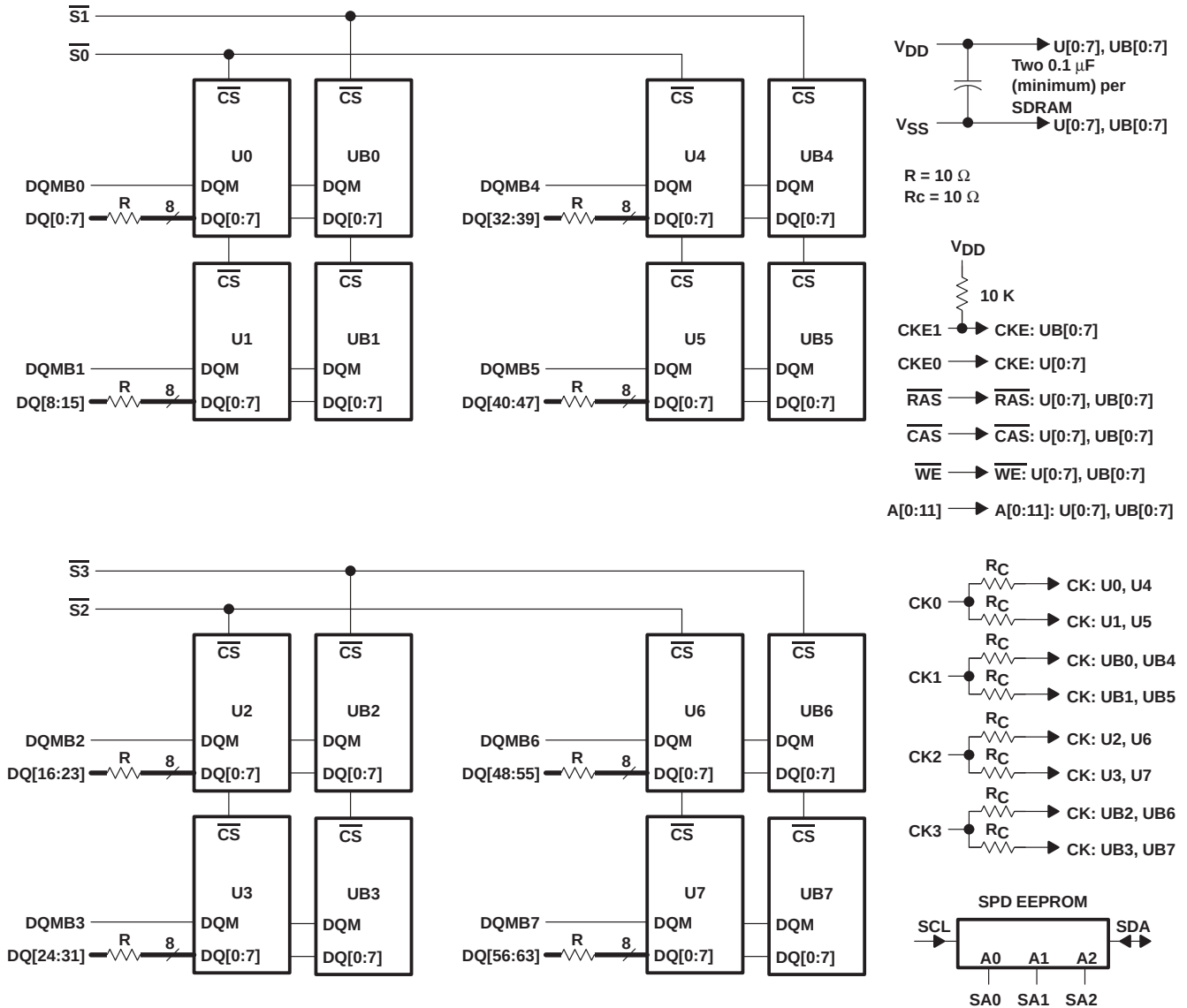
The dual-in-line memory module and components include:

- PC substrate: $1,27 \pm 0,1$ mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram for the TM2SN64EPU



functional block diagram for the TM4SN64EPU



TM2SN64EPU 2097152 BY 64-BIT
TM4SN64EPU 4194304 BY 64-BIT
SYNCHRONOUS DYNAMIC RAM MODULES

SMMS681 – AUGUST 1997

absolute maximum ratings over ambient temperature range (unless otherwise noted)[†]

Supply voltage range, V_{DD}	–0.5 V to 4.6 V
Voltage range on any pin (see Note 1)	– 0.5 V to 4.6 V
Short-circuit output current	50 mA
Power dissipation: TM2SN64EPU	8 W
TM4SN64EPU	16 W
Ambient temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 125°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{DD} Supply voltage	3	3.3	3.6	V
V_{SS} Supply voltage		0		V
V_{IH} High-level input voltage	2		$V_{DD} + 0.3$	V
V_{IH-SPD} High-level input voltage for the SPD device	2		5.5	V
V_{IL} Low-level input voltage [‡]	–0.3		0.8	V
T_A Ambient temperature	0		70	°C

[‡] V_{IL} MIN = –1.5 V ac (pulse width $\leq$ 5 ns)

capacitance over recommended ranges of supply voltage and ambient temperature, $f = 1$ MHz (see Note 2)

PARAMETER	TM2SN64EPU		TM4SN64EPU		UNIT
	MIN	MAX	MIN	MAX	
$C_i(CK)$ Input capacitance, CK input		22		22	pF
$C_i(AC)$ Input capacitance, address and control inputs: A0–A11, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		42		82	pF
$C_i(CKE)$ Input capacitance, CKE input		42		42	pF
C_o Output capacitance		10		18	pF
$C_i(DQMBx)$ Input capacitance, DQMBx input		12		12	pF
$C_i(Sx)$ Input capacitance, $\overline{Sx}$ input		22		22	pF
$C_{i/o}(SDA)$ Input/output capacitor, SDA input		9		9	pF
$C_i(SPD)$ Input capacitor, SA0, SA1, SA2, SCL inputs		7		7	pF

NOTE 2: $V_{DD} = 3.3$ V $\pm$ 0.3 V. Bias on pins under test is 0 V.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

TM2SN64EPU

PARAMETER		TEST CONDITIONS	'2SN64EPU-12A		'2SN64EPU-12		UNIT
			MIN	MAX	MIN	MAX	
V _{OH}	High-level output voltage	I _{OH} = – 2 mA	2.4		2.4		V
V _{OL}	Low-level output voltage	I _{OL} = 2 mA		0.4		0.4	V
I _I	Input current (leakage)	0 V < V _I < V _{DD} + 0.3 V, All other pins = 0 V to V _{DD}		± 10		± 10	μA
I _O	Output current (leakage)	0 V < V _O < V _{DD} + 0.3 V, Output disabled		± 10		± 10	μA
I _{CC1}	Operating current	Burst length = 1, t _{RC} ≥ t _{RC} MIN I _{OH} /I _{OL} = 0 mA, one bank activated (see Note 4)	CAS latency = 2		680		mA
			CAS latency = 3		760		mA
I _{CC2P}	Precharge standby current in power-down mode	CKE ≤ V _{IL} MAX, t _{CK} = 15 ns (see Note 5)	16		16		mA
I _{CC2PS}		CKE and CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6)	16		16		mA
I _{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V _{IH} MIN, t _{CK} = 15 ns (see Note 5)	240		240		mA
I _{CC2NS}		CKE ≥ V _{IH} MIN, CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6)	16		16		mA
I _{CC3P}	Active standby current in power-down mode	CKE ≤ V _{IL} MAX, t _{CK} = 15 ns (see Note 5)	64		64		mA
I _{CC3PS}		CKE and CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6)	64		64		mA
I _{CC3N}	Active standby current in non-power-down mode	CKE ≥ V _{IH} MIN, t _{CK} = 15 ns (see Note 5)	280		280		mA
I _{CC3NS}		CKE ≥ V _{IH} MIN, CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6)	80		80		mA
I _{CC4}	Burst current	Page burst, I _{OH} /I _{OL} = 0 mA All banks activated, n _{CCD} = one cycle (see Note 7)	CAS latency = 2		1040		mA
			CAS latency = 3		1240		mA
I _{CC5}	Auto-refresh current	t _{RC} ≤ t _{RC} MIN	CAS latency = 2		600		mA
			CAS latency = 3		680		mA
I _{CC6}	Self-refresh current	CKE ≤ V _{IL} MAX	16		16		mA

- NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state twice during t_{RC}.
5. Control, DQ, and address inputs change state once every 30 ns.
6. Control, DQ, and address inputs do not change.
7. Control, DQ, and address inputs change once every cycle.

TM2SN64EPU 2097152 BY 64-BIT
TM4SN64EPU 4194304 BY 64-BIT
SYNCHRONOUS DYNAMIC RAM MODULES

SMMS681 – AUGUST 1997

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

TM4SN64EPU

PARAMETER		TEST CONDITIONS	'4SN64EPU-12A		'4SN64EPU-12		UNIT
			MIN	MAX	MIN	MAX	
V _{OH}	High-level output voltage	I _{OH} = – 2 mA	2.4		2.4		V
V _{OL}	Low-level output voltage	I _{OL} = 2 mA		0.4		0.4	V
I _I	Input current (leakage)	0 V < V _I < V _{DD} + 0.3 V, All other pins = 0 V to V _{DD}		± 20		± 20	µA
I _O	Output current (leakage)	0 V < V _O < V _{DD} + 0.3 V, Output disabled		± 20		± 20	µA
I _{CC1}	Operating current	Burst length = 1, t _{RC} ≥ t _{RC} MIN I _{OH} /I _{OL} = 0 mA, one bank activated (see Note 4)	CAS latency = 2		616		mA
			CAS latency = 3		776		mA
I _{CC2P}	Precharge standby current in power-down mode	CKE ≤ V _{IL} MAX, t _{CK} = 15 ns (see Note 5)	32		32		mA
I _{CC2PS}		CKE and CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6)	32		32		mA
I _{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V _{IH} MIN, t _{CK} = 15 ns (see Note 5)	480		480		mA
I _{CC2NS}		CKE ≥ V _{IH} MIN, CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6)	32		32		mA
I _{CC3P}	Active standby current in power-down mode	CKE ≤ V _{IL} MAX, t _{CK} = 15 ns (see Note 5)	128		128		mA
I _{CC3PS}		CKE and CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6)	128		128		mA
I _{CC3N}	Active standby current in non-power-down mode	CKE ≥ V _{IH} MIN, t _{CK} = 15 ns (see Note 5)	560		560		mA
I _{CC3NS}		CKE ≥ V _{IH} MIN, CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6)	160		160		mA
I _{CC4}	Burst current	Page burst, I _{OH} /I _{OL} = 0 mA All banks activated, n _{CCD} = one cycle (see Note 7)	CAS latency = 2		896		mA
			CAS latency = 3		1256		mA
I _{CC5}	Auto-refresh current	t _{RC} ≤ t _{RC} MIN	CAS latency = 2		570		mA
			CAS latency = 3		696		mA
I _{CC6}	Self-refresh current	CKE ≤ V _{IL} MAX	32		32		mA

- NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state twice during t_{RC}.
5. Control, DQ, and address inputs change state once every 30 ns.
6. Control, DQ, and address inputs do not change.
7. Control, DQ, and address inputs change once every cycle.

ac timing requirements[†]

	'xSN64EPU-12A [‡]		'xSN64EPU-12		UNIT
	MIN	MAX	MIN	MAX	
t _{AC2} Access time, CK high to data out, CAS latency = 2 (see Note 8)		9		10	ns
t _{AC3} Access time, CK high to data out, CAS latency = 3 (see Note 8)		9		9	ns
t _{CK2} Cycle time, CK, CAS latency = 2	15		18		ns
t _{CK3} Cycle time, CK, CAS latency = 3	12		12		ns
t _{LZ} Delay time, CK high to DQ in low-impedance state (see Note 9)	3		3		ns
t _{HZ} Delay time, CK high to DQ in high-impedance state (see Note 10)		10		10	ns
t _{RAS} Delay time, ACTV command to DEAC or DCAB command	60	100 000	72	100 000	ns
t _{RC} Delay time, ACTV, MRS, REFR, or SLFR to ACTV, MRS, REFR, or SLFR command	90		108		ns
t _{RCD} Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 11)	30		30		ns
t _{RP} Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command	30		36		ns
t _{RRD} Delay time, ACTV command in one bank to ACTV command in the other bank	24		24		ns
t _{RSA} Delay time, MRS command to ACTV, MRS, REFR, or SLFR command	24		24		ns
t _{APR} Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	t _{RP} – (CL – 1) * t _{CK}				ns
t _{OH} Hold time, CK high to data out	3		3		ns
t _{IH} Hold time, address, control, and data input	1		1.5		ns
t _{CESP} Power down/self-refresh exit time	10		10		ns
t _{CH} Pulse duration, CK high	4		4		ns
t _{CL} Pulse duration, CK low	4		4		ns
t _{IS} Setup time, address, control, and data input	3		3		ns
t _{APW} Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command	60		60		ns
t _{WR} Delay time, final data in of WRT operation to DEAC or DCAB command	15		20		ns
t _T Transition time (see Note 12)	1	5	1	5	ns
t _{REF} Refresh interval		64		64	ms
n _{CCD} Delay time, READ or WRT command to an interrupting command	1		1		cycle
n _{CDD} Delay time, CS low or high to input enabled or inhibited	0	0	0	0	cycle
n _{CLE} Delay time, CKE high or low to CK enabled or disabled	1	1	1	1	cycle
n _{CWL} Delay time, final data in of WRT operation to READ, READ-P, WRT, WRT-P	1		1		cycle
n _{DID} Delay time, ENBL or MASK command to enabled or masked data in	0	0	0	0	cycle
n _{DOD} Delay time, ENBL or MASK command to enabled or masked data out	2	2	2	2	cycle
n _{HZP2} Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 2		2		2	cycle
n _{HZP3} Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 3		3		3	cycle
n _{WCD} Delay time, WRT command to first data in	0	0	0	0	cycle

[†] All references are made to the rising transition of CK unless otherwise noted.

[‡] -12A speed device is supported only at – 5% to +10% V_{DD}

- NOTES:
8. t_{AC} is referenced from the rising transition of CK that is previous to the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CK that is CAS latency – one cycle after the READ command. Access time is measured at output reference level 1.4 V.
 9. t_{LZ} is measured from the rising transition of CK that is CAS latency – one cycle after the READ command.
 10. t_{HZ} MAX defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
 11. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.
 12. Transition time, t_T, is measured between V_{IH} and V_{IL}.

TM2SN64EPU 2097152 BY 64-BIT
TM4SN64EPU 4194304 BY 64-BIT
SYNCHRONOUS DYNAMIC RAM MODULES

SMMS681 – AUGUST 1997

serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through a IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 1—TM2SN64EPU Table 2—TM4SN64EPU

Table 1. Serial Presence-Detect Data for the TM2SN64EPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM2SN64EPU-12A		TM2SN64EPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	$t_{CK} = 12 \text{ ns}$	C0h	$t_{CK} = 12 \text{ ns}$	C0h
10	SDRAM access from clock at CL = X	$t_{AC} = 9 \text{ ns}$	90h	$t_{AC} = 9 \text{ ns}$	90h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-Parity	00h	Non-Parity	00h
12	Refresh rate / type	15.6 μs / self-refresh	80h	15.6 μs / self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	2 banks	02h	2 banks	02h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered / Non-registered	00h	Non-buffered / Non-registered	00h

serial presence detect (continued)

Table 1. Serial Presence-Detect Data for the TM2SN64EPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM2SN64EPU-12A		TM2SN64EPU-12	
		ITEM	DATA	ITEM	DATA
22	SDRAM device attributes: general	V _{DD} tolerance = (+10%)/(–5%). Burst read/write, precharge all, auto precharge	1Eh	V _{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X – 1	t _{CK} = 15 ns	F0h	t _{CK} = 18 ns	30h
24	Maximum data-access time from clock at CL = X – 1	t _{AC} = 9 ns	90h	t _{AC} = 10 ns	A0h
25	Minimum clock cycle time at CL = X – 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X – 2	N/A	00h	N/A	00h
27	Minimum row precharge time	t _{RP} = 30 ns	1Eh	t _{RP} = 36 ns	24h
28	Minimum row-active to row-active delay	t _{RRD} = 24 ns	18h	t _{RRD} = 24 ns	18h
29	Minimum $\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ delay	t _{RCD} = 30 ns	1Eh	t _{RCD} = 30 ns	1Eh
30	Minimum $\overline{\text{RAS}}$ pulse width	t _{RAS} = 60 ns	3Ch	t _{RAS} = 72 ns	48h
31	Density of each bank on module	16M Bytes	04h	16M Bytes	04h
32–61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0–62	7	07h	89	59h
64–71	Manufacturer's JEDEC ID code per JEP–106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD	
91	Die revision code [†]	TBD		TBD	
92	PCB revision code [†]	TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD	
167–255	Open				

[†] TBD indicates values are determined at manufacturing time and are module dependent.

[‡] These TBD values are determined and programmed by the customer (optional).

TM2SN64EPU 2097152 BY 64-BIT
TM4SN64EPU 4194304 BY 64-BIT
SYNCHRONOUS DYNAMIC RAM MODULES

SMMS681 – AUGUST 1997

serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM4SN64EPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SN64EPU-12A		TM4SN64EPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTTL	01h	LVTTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	$t_{CK} = 12 \text{ ns}$	C0h	$t_{CK} = 12 \text{ ns}$	C0h
10	SDRAM access from clock at CL = X	$t_{AC} = 9 \text{ ns}$	90h	$t_{AC} = 9 \text{ ns}$	90h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-Parity	00h	Non-Parity	00h
12	Refresh rate/type	15.6 μs /self-refresh	80h	15.6 μs /self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	2 banks	02h	2 banks	02h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%)/(–5%). Burst read/write, precharge all, auto precharge	1Eh	V_{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X – 1	$t_{CK} = 15 \text{ ns}$	F0h	$t_{CK} = 18 \text{ ns}$	30h
24	Maximum data-access time from clock at CL = X – 1	$t_{AC} = 9 \text{ ns}$	90h	$t_{AC} = 10 \text{ ns}$	A0h
25	Minimum clock cycle time at CL = X – 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X – 2	N/A	00h	N/A	00h

serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM4SN64EPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SN64EPU-12A		TM4SN64EPU-12	
		ITEM	DATA	ITEM	DATA
27	Minimum row precharge time	t _{RP} = 30 ns	1Eh	t _{RP} = 36 ns	24h
28	Minimum row-active to row-active delay	t _{RRD} = 24 ns	18h	t _{RRD} = 24 ns	18h
29	Minimum $\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ delay	t _{RCD} = 30 ns	1Eh	t _{RCD} = 30 ns	1Eh
30	Minimum $\overline{\text{RAS}}$ pulse width	t _{RAS} = 60 ns	3Ch	t _{RAS} = 72 ns	48h
31	Density of each bank on module	16M Bytes	04h	16M Bytes	04h
32–61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0–62	8	08h	90	5Ah
64–71	Manufacturer's JEDEC ID code per JEP–106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD	
91	Die revision code [†]	TBD		TBD	
92	PCB revision code [†]	TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD	
167–255	Open				

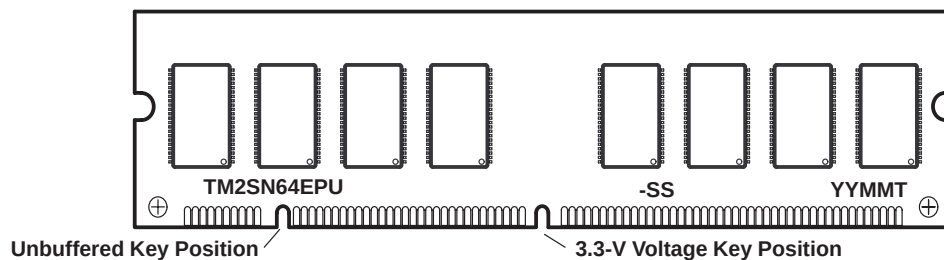
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TM2SN64EPU 2097152 BY 64-BIT
TM4SN64EPU 4194304 BY 64-BIT
SYNCHRONOUS DYNAMIC RAM MODULES

SMMS681 – AUGUST 1997

device symbolization (TM2SN64EPU)



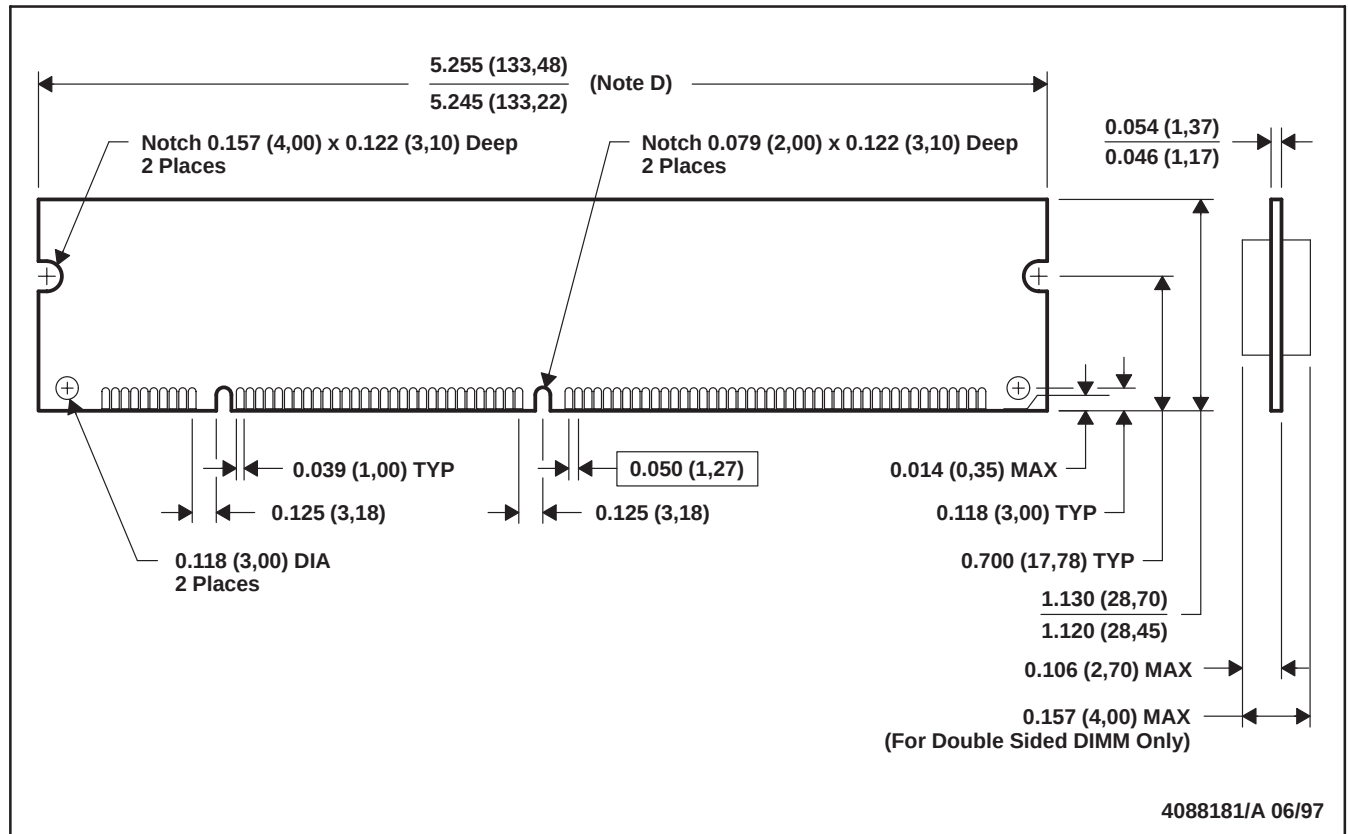
YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

MECHANICAL DATA

BS (R-PDIM-N168)

DUAL IN-LINE MEMORY MODULE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MO-161
 D. Dimension includes De-panelization variations; applies between notch and tab edge.
 E. Outline may vary above notches to allow router/panelization irregularities.

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