- **Organization**
  - **TM2SR72EPU . . . 2097152 x 72 Bits**
  - **TM4SR72EPU . . . 4194304 x 72 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **Designed for 66-MHz 4-Clock Systems**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **TM2SR72EPU — Uses Nine 16M-Bit Synchronous Dynamic RAMs (SDRAMs) (2M × 8-Bit) in Plastic Thin Small-Outline Packages (TSOPs)**
- **TM4SR72EPU — Uses 18 16M-Bit SDRAMs (2M × 8-Bit) in Plastic TSOPs**
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME		ACCESS TIME (CLOCK TO OUTPUT)		REFRESH INTERVAL
	t_{CK3} (CL = 3)†	t_{CK2} (CL = 2)	t_{CK3} (CL = 3)	t_{CK2} (CL = 2)	
'xSR72EPU-12A‡	12 ns	15 ns	9 ns	9 ns	64 ms
'xSR72EPU-12	12 ns	18 ns	9 ns	10 ns	64 ms

† CL = CAS latency
‡ -12A speed device is supported only at −5% to +10% V_{DD}

- **High-Speed, Low-Noise Low-Voltage TTL (LVTTL) Interface**
- **Byte-Read/Write Capability**
- **Read Latencies 2 and 3 Supported**
- **Support Burst-Interleave and Burst-Interrupt Operations**
- **Burst Length Programmable to 1, 2, 4, and 8**
- **Two Banks for On-Chip Interleaving (Gapless Access)**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**
- **Pipeline Architecture**
- **Serial Presence-Detect (SPD) Using EEPROM**

description

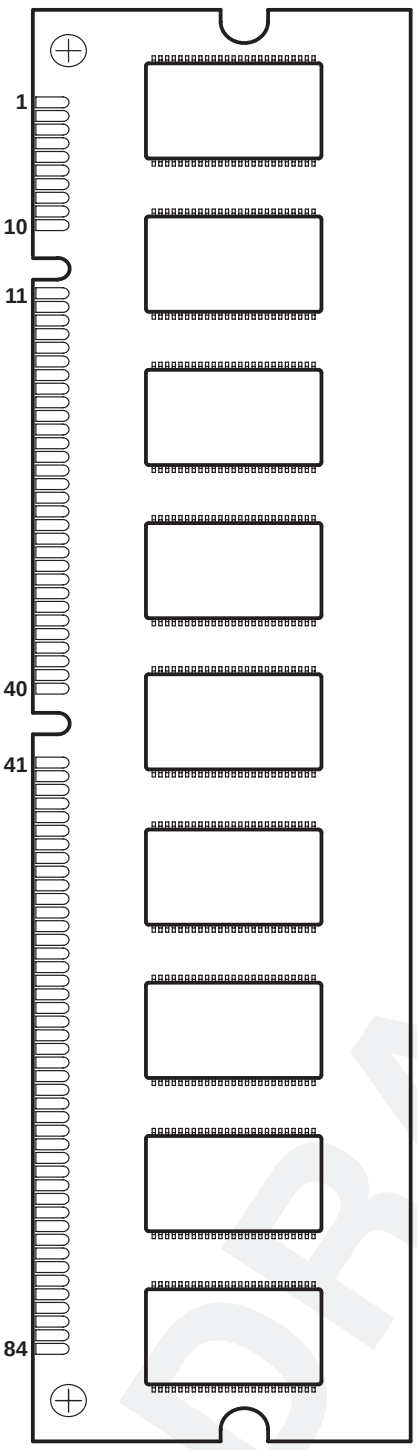
The TM2SR72EPU is a 16M-byte, 168-pin dual-in-line memory module (DIMM). The DIMM is composed of nine TMS626812DGE, 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic thin small-outline package (TSOP) mounted on a substrate with decoupling capacitors. See the TMS626812 data sheet (literature number SMOS687).

The TM4SR72EPU is a 32M-byte, 168-pin DIMM. The DIMM is composed of eighteen TMS626812DGE, 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS626812 data sheet (literature number SMOS687).

operation

The TM2SR72EPU operates as nine TMS626812DGE devices that are connected as shown in the TM2SR72EPU functional block diagram. The TM4SR72EPU operates as eighteen TMS626812DGE devices connected as shown in the TM4SR72EPU functional block diagram.

DUAL-IN-LINE MEMORY MODULE (TOP VIEW)



TM2SR72EPU (SIDE VIEW)

TM4SR72EPU (SIDE VIEW)

PIN NOMENCLATURE

A[0:10]	Row-Address Inputs
A[0:8]	Column-Address Inputs
A11/BA0	Bank-Select Zero
$\overline{CAS}$	Column-Address Strobe
CB[0:7]	Data In/Data Out
CKE[0:1]	Clock Enable
CK[0:3]	System Clock
DQ[0:63]	Data In/Data Out
DQMB[0:7]	Data-In/Data-Out Mask Enable
NC	No Connect
$\overline{RAS}$	Row-Address Strobe
$\overline{S}$[0:3]	Chip-Select
SA[0:2]	Serial Presence-Detect (SPD) Device Address Input
SCL	SPD Clock
SDA	SPD Address/Data
V_{DD}	3.3-V Supply
V_{SS}	Ground
$\overline{WE}$	Write Enable

Pin Assignments

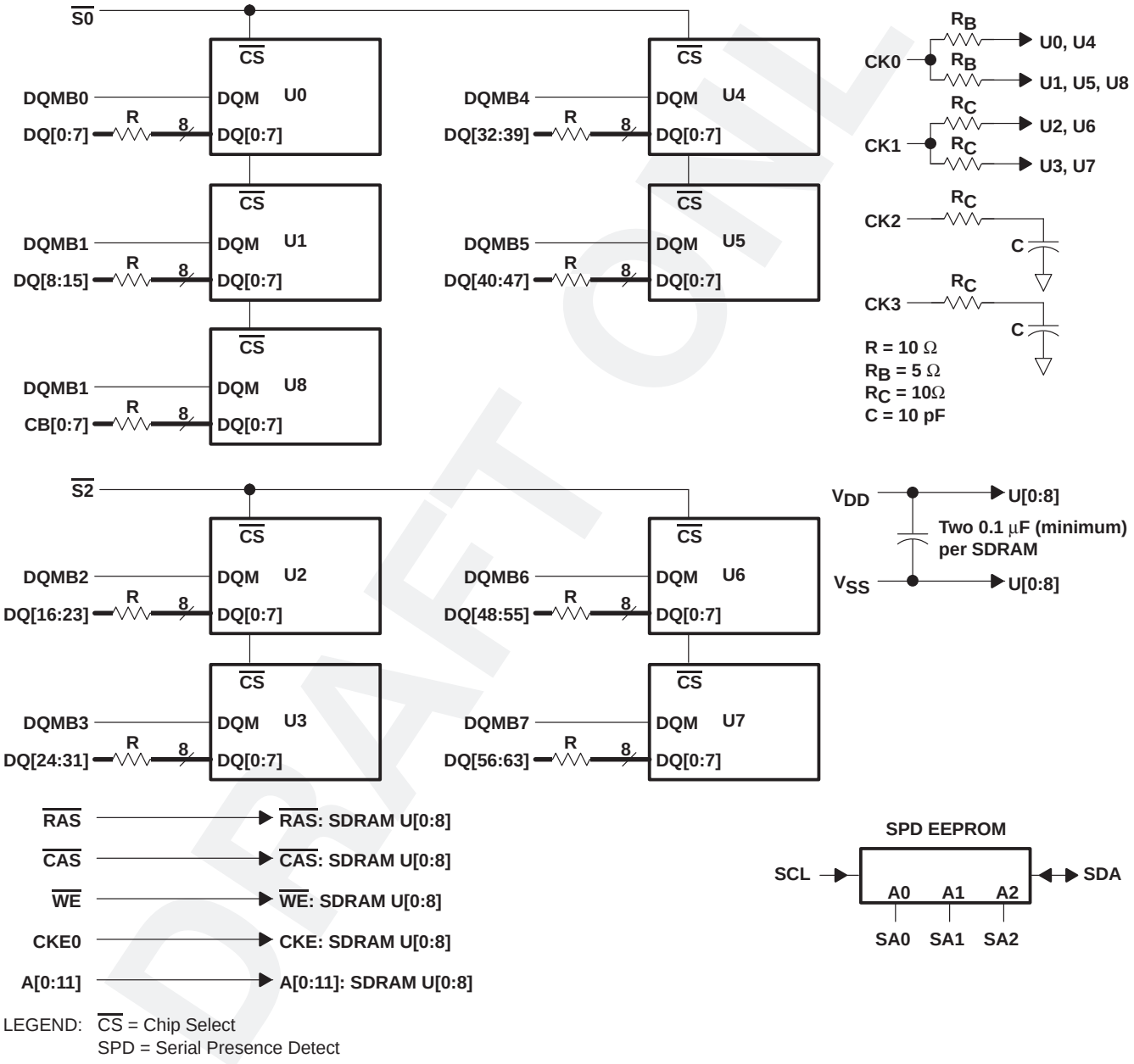
PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	$\overline{S2}$	87	DQ33	129	$\overline{S3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	NC	90	V_{DD}	132	NC
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{S0}$	72	DQ27	114	$\overline{S1}$	156	DQ59
31	NC	73	V_{DD}	115	$\overline{RAS}$	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	A11/BA0	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CK1	167	SA2
42	CK0	84	V_{DD}	126	NC	168	V_{DD}

dual-in-line memory module and components

The dual-in-line memory module and components include:

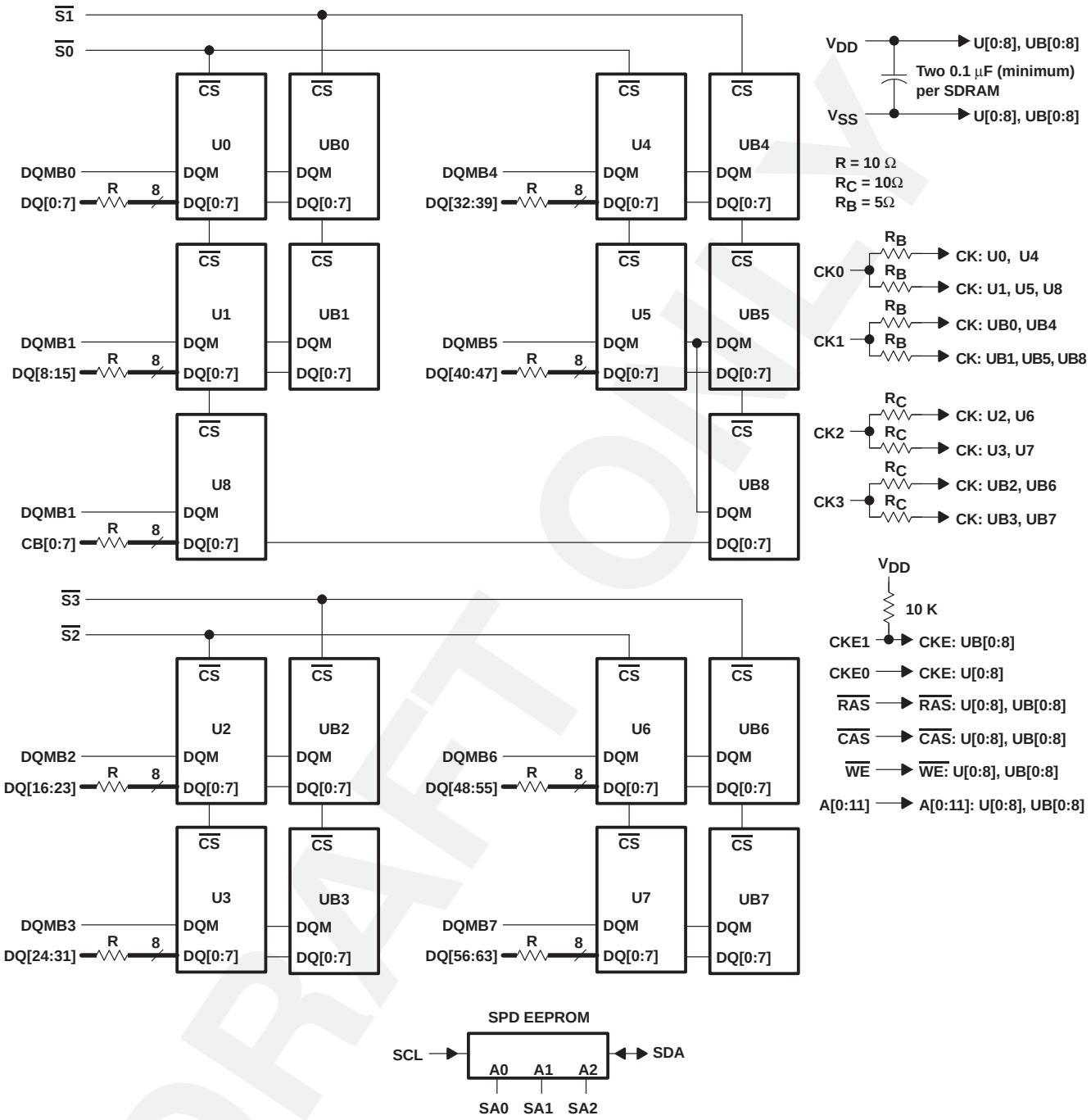
- PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram for the TM2SR72EPU



LEGEND: $\overline{CS}$ = Chip Select
SPD = Serial Presence Detect

functional block diagram for the TM4SR72EPU



absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . −0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . − 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM2SR72EPU . . . . . 9 W
TM4SR72EPU . . . . . 18 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . − 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
V_{IH-SPD}	High-level input voltage for SPD device	2		5.5	V
V_{IL}	Low-level input voltage ‡	−0.3		0.8	V
T_A	Ambient temperature	0		70	°C

‡ V_{IL} MIN = −1.5 V ac (pulse width ≤ 5 ns)

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETERS		TM2SR72EPU		TM4SR72EPU		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(CK)}$	Input capacitance, CK input		27		27	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0−A11, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		47		92	pF
$C_{i(CKE)}$	Input capacitance, CKE input		47		47	pF
C_o	Output capacitance		10		18	pF
$C_{i(DQMBx)}$	Input capacitance, DQMBx input		12		17	pF
$C_{i(Sx)}$	Input capacitance, $\overline{Sx}$ input		27		27	pF
$C_{i/o(SDA)}$	Input/output capacitor, SDA input		9		9	pF
$C_{i(SPD)}$	Input capacitor, SA0, SA1, SA2, SCL inputs		7		7	pF

NOTE 2: V_{DD} = 3.3 V ± 0.3 V. Bias on pins under test is 0 V.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

TM2SR72EPU

PARAMETER		TEST CONDITIONS		'2SR72EPU-12A		'2SR72EPU-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	0 V < V_I < V_{DD} + 0.3 V, All other pins = 0 V to V_{DD}			±10		±10	μA
I_O	Output current (leakage)	0 V < V_O < V_{DD} +0.3 V, Output disabled			±10		±10	μA
I_{CC1}	Operating current	Burst length = 1, $t_{RC} \geq t_{RC}$ MIN I_{OH}/I_{OL} = 0 mA, one bank activated (see Note 4)	CAS latency = 2		765		675	mA
			CAS latency = 3		855		855	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			18		18	mA
I_{CC2PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			18		18	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			270		270	mA
I_{CC2NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			18		18	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			72		72	mA
I_{CC3PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			72		72	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			315		315	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			90		90	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = one cycle (see Note 7)	CAS latency = 2		1170		990	mA
			CAS latency = 3		1395		1395	mA
I_{CC5}	Auto-refresh current	$t_{RC} \leq t_{RC}$ MIN	CAS latency = 2		675		630	mA
			CAS latency = 3		765		765	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			18		18	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state only twice during t_{RC}.
5. Control, DQ, and address inputs change state only once every 30 ns.
6. Control, DQ, and address inputs do not change (stable).
7. Control, DQ, and address inputs change only once every cycle.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

TM4SR72EPU

PARAMETER		TEST CONDITIONS		'4SR72EPU-12A		'4SR72EPU-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	0 V < V_I < V_{DD} + 0.3 V, All other pins = 0 V to V_{DD}			±20		±20	μA
I_O	Output current (leakage)	0 V < V_O < V_{DD} + 0.3 V, Output disabled			±20		±20	μA
I_{CC1}	Operating current	Burst length = 1, $t_{RC} \geq t_{RC}$ MIN I_{OH}/I_{OL} = 0 mA, one bank activated (see Note 4)	CAS latency = 2		783		683	mA
			CAS latency = 3		875		873	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			36		36	mA
I_{CC2PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			36		36	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			540		540	mA
I_{CC2NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			36		36	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			144		144	mA
I_{CC3PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			144		144	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			630		630	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			180		180	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = one cycle (see Note 7)	CAS latency = 2		1188		1008	mA
			CAS latency = 3		1413		1413	mA
I_{CC5}	Auto-refresh current	$t_{RC} \leq t_{RC}$ MIN	CAS latency = 2		693		648	mA
			CAS latency = 3		783		783	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			36		36	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state only twice during t_{RC}.
5. Control, DQ, and address inputs change state only once every 30 ns.
6. Control, DQ, and address inputs do not change (stable).
7. Control, DQ, and address inputs change only once every cycle.

ac timing requirements†

		'xSR72EPU-12A‡		'xSR72EPU-12		UNIT
		MIN	MAX	MIN	MAX	
t_{AC2}	Access time, CK high to data out, CAS latency = 2 (see Note 8)		9		10	ns
t_{AC3}	Access time, CK high to data out, CAS latency = 3 (see Note 8)		9		9	ns
t_{CK2}	Cycle time, CK, CAS latency = 2	15		18		ns
t_{CK3}	Cycle time, CK, CAS latency = 3	12		12		ns
t_{LZ}	Delay time, CK high to DQ in low-impedance state (see Note 9)	3		3		ns
t_{HZ}	Delay time, CK high to DQ in high-impedance state (see Note 10)		10		10	ns
t_{RC}	Delay time, ACTV, MRS, REFR, or SLFR to ACTV, MRS, REFR, or SLFR command	90		108		ns
t_{RCD}	Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 11)	30		30		ns
t_{RP}	Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command	30		36		ns
t_{RRD}	Delay time, ACTV command in one bank to ACTV command in the other bank	24		24		ns
t_{RSA}	Delay time, MRS command to ACTV, MRS, REFR, or SLFR command	24		24		ns
t_{RAS}	Delay time, ACTV command to DEAC or DCAB command	60	100000	72	100000	ns
t_{WR}	Delay time, final data in of WRT operation to DEAC or DCAB command	15		20		ns
n_{CCD}	Delay time, READ or WRT command to an interrupting command	1		1		cycle
n_{CDD}	Delay time, CS low or high to input enabled or inhibited	0	0	0	0	cycle
n_{CLE}	Delay time, CKE high or low to CK enabled or disabled	1	1	1	1	cycle
n_{CWL}	Delay time, final data in of WRT operation to READ, READ-P, WRT, WRT-P	1		1		cycle
n_{DID}	Delay time, ENBL or MASK command to enabled or masked data in	0	0	0	0	cycle
n_{DOD}	Delay time, ENBL or MASK command to enabled or masked data out	2	2	2	2	cycle
n_{HZP2}	Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 2		2		2	cycle
n_{HZP3}	Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 3		3		3	cycle
n_{WCD}	Delay time, WRT command to first data in	0	0	0	0	cycle
t_{OH}	Hold time, CK high to data out	3		3		ns
t_{IH}	Hold time, address, control, and data input	1		1.5		ns
t_{CESP}	Power-down/self-refresh exit time	10		10		ns
t_{CH}	Pulse duration, CK high	4		4		ns
t_{CL}	Pulse duration, CK low	4		4		ns
t_{IS}	Setup time, address, control, and data input	3		3		ns
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	$t_{RP} - (CL - 1) * t_{CK}$				ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command	60		60		ns
t_{REF}	Refresh interval		64		64	ms
t_T	Transition time (see Note 12)	1	5	1	5	ns

† All references are made to the rising transition of CKx, unless otherwise noted.
‡ -12A speed device is supported only at − 5% to + 10% V_{DD}

NOTES: 8. t_{AC} is referenced from the rising transition of CK that is previous to the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CKx that is CAS latency − one cycle after the READ command. Access time is measured at output reference level 1.4 V.
9. t_{LZ} is measured from the rising transition of CKx that is CAS latency − one cycle after the READ command.
10. t_{HZ} MAX defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
11. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.
12. Transition time, t_T, is measured between V_{IH} and V_{IL}.

serial presence detect

The serial-presence-detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through a IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.Tables in this section list the SPD contents as follows:

Tables in this section list the SPD contents as follows:

Table 1−TM2SR72EPU Table 2−TM4SR72EPU

Table 1. Serial Presence-Detect Data for the TM2SR72EPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM2SR72EPU-12A		TM2SR72EPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h
6	Data width of this assembly	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	t_{CK} = 12 ns	C0h	t_{CK} = 12 ns	C0h
10	SDRAM access from clock at CL = X	t_{AC} = 9 ns	90h	t_{AC} = 9 ns	90h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 µs/ self-refresh	80h	15.6 µs/ self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	2 banks	02h	2 banks	02h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h

serial presence detect (continued)

Table 1. Serial Presence-Detect Data for the TM2SR72EPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM2SR72EPU-12A		TM2SR72EPU-12	
		ITEM	DATA	ITEM	DATA
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%)/(−5%). Burst read/write, precharge all, auto precharge	1Eh	V_{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X − 1	t_{CK} = 15 ns	F0h	t_{CK} = 18 ns	30h
24	Maximum data-access time from clock at CL = X − 1	t_{AC} = 9.0 ns	90h	t_{AC} = 10 ns	A0h
25	Minimum clock cycle time at CL = X − 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X − 2	N/A	00h	N/A	00h
27	Minimum row precharge time	t_{RP} = 30 ns	1Eh	t_{RP} = 36 ns	24h
28	Minimum row-active to row-active delay	t_{RRD} = 24 ns	18h	t_{RRD} = 24 ns	18h
29	Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay	t_{RCD} = 30 ns	1Eh	t_{RCD} = 30 ns	1Eh
30	Minimum $\overline{RAS}$ pulse width	t_{RAS} = 60 ns	3Ch	t_{RAS} = 72 ns	48h
31	Density of each bank on module	16M Bytes	04h	16M Bytes	04h
32−61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0−62	25	19h	107	6Bh
64−71	Manufacturer's JEDEC ID code per JEP−106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD	
73−90	Manufacturer's part number†	TBD		TBD	
91	Die revision code†	TBD		TBD	
92	PCB revision code†	TBD		TBD	
93−94	Manufacturing date†	TBD		TBD	
95−98	Assembly serial number†	TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD	
126−127	Vendor specific data†	TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD	
167−255	Open				

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM4SR72EPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SR72EPU-12A		TM4SR72EPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h
6	Data width of this assembly	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	t_{CK} = 12 ns	C0h	t_{CK} = 12 ns	C0h
10	SDRAM access from clock at CL = X	t_{AC} = 9 ns	90h	t_{AC} = 9 ns	90h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 µs/ self-refresh	80h	15.6 µs/ self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	2 banks	02h	2 banks	02h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%)/(−5%). Burst read/write, precharge all, auto precharge	1Eh	V_{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X − 1	t_{CK} = 15 ns	F0h	t_{CK} = 18 ns	30h
24	Maximum data-access time from clock at CL = X − 1	t_{AC} = 9.0 ns	90h	t_{AC} = 10 ns	A0h
25	Minimum clock cycle time at CL = X − 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X − 2	N/A	00h	N/A	00h
27	Minimum row precharge time	t_{RP} = 30 ns	1Eh	t_{RP} = 36 ns	24h
28	Minimum row-active to row-active delay	t_{RRD} = 24 ns	18h	t_{RRD} = 24 ns	18h
29	Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay	t_{RCD} = 30 ns	1Eh	t_{RCD} = 30 ns	1Eh
30	Minimum $\overline{RAS}$ pulse width	t_{RAS} = 60 ns	3Ch	t_{RAS} = 72 ns	48h
31	Density of each bank on module	16M Bytes	04h	16M Bytes	04h

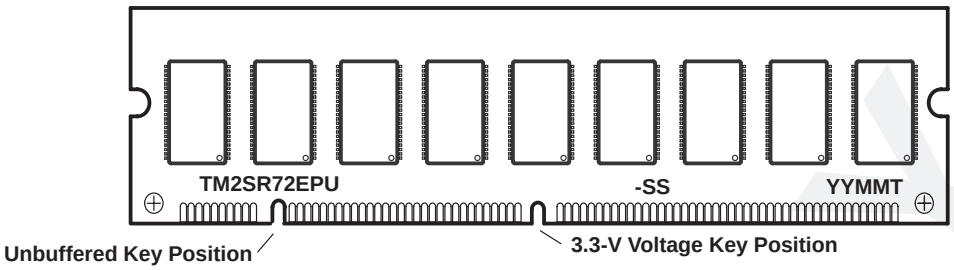
serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM4SR72EPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SR72EPU-12A		TM4SR72EPU-12	
		ITEM	DATA	ITEM	DATA
32−61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0−62	26	1Ah	108	6Ch
64−71	Manufacturer's JEDEC ID code per JEP−106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD	
73−90	Manufacturer's part number†	TBD		TBD	
91	Die revision code†	TBD		TBD	
92	PCB revision code†	TBD		TBD	
93−94	Manufacturing date†	TBD		TBD	
95−98	Assembly serial number†	TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD	
126−127	Vendor specific data†	TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD	
167−255	Open				

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

device symbolization (TM2SR72EPU)

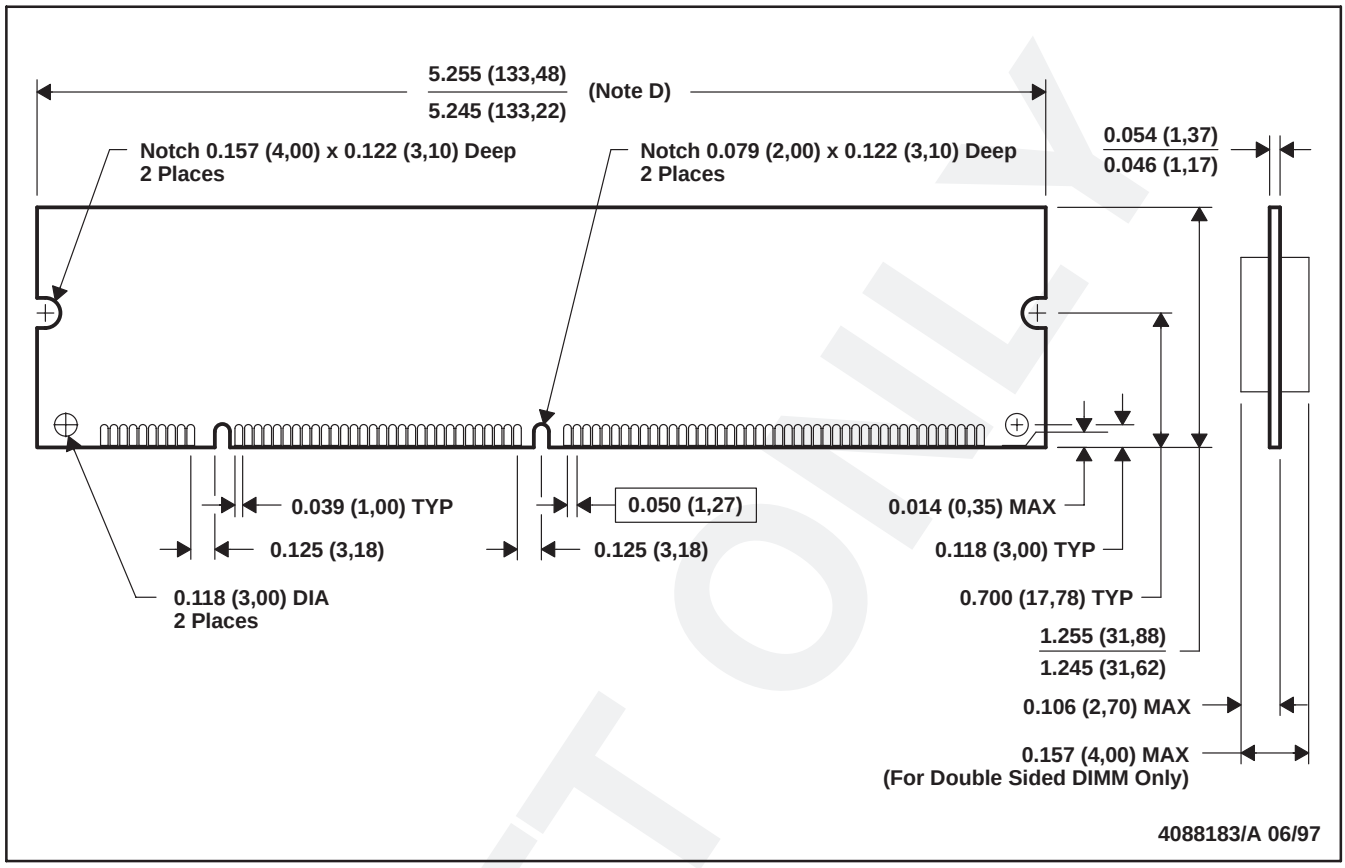


YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

MECHANICAL DATA

BU (R-PDIM-N168) **DUAL IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-161
D. Dimension includes de-panelization variations; applies between notch and tab edge.
E. Outline may vary above notches to allow router/panelization irregularities.

- **Organization**
  - **TM2SR72EPU . . . 2097152 x 72 Bits**
  - **TM4SR72EPU . . . 4194304 x 72 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **Designed for 66-MHz 4-Clock Systems**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **TM2SR72EPU — Uses Nine 16M-Bit Synchronous Dynamic RAMs (SDRAMs) (2M × 8-Bit) in Plastic Thin Small-Outline Packages (TSOPs)**
- **TM4SR72EPU — Uses 18 16M-Bit SDRAMs (2M × 8-Bit) in Plastic TSOPs**
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME		ACCESS TIME (CLOCK TO OUTPUT)		REFRESH INTERVAL
	t_{CK3} (CL = 3)†	t_{CK2} (CL = 2)	t_{CK3} (CL = 3)	t_{CK2} (CL = 2)	
'xSR72EPU-12A‡	12 ns	15 ns	9 ns	9 ns	64 ms
'xSR72EPU-12	12 ns	18 ns	9 ns	10 ns	64 ms

† CL = CAS latency
‡ -12A speed device is supported only at −5% to +10% V_{DD}

- **High-Speed, Low-Noise Low-Voltage TTL (LVTTL) Interface**
- **Byte-Read/Write Capability**
- **Read Latencies 2 and 3 Supported**
- **Support Burst-Interleave and Burst-Interrupt Operations**
- **Burst Length Programmable to 1, 2, 4, and 8**
- **Two Banks for On-Chip Interleaving (Gapless Access)**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**
- **Pipeline Architecture**
- **Serial Presence-Detect (SPD) Using EEPROM**

description

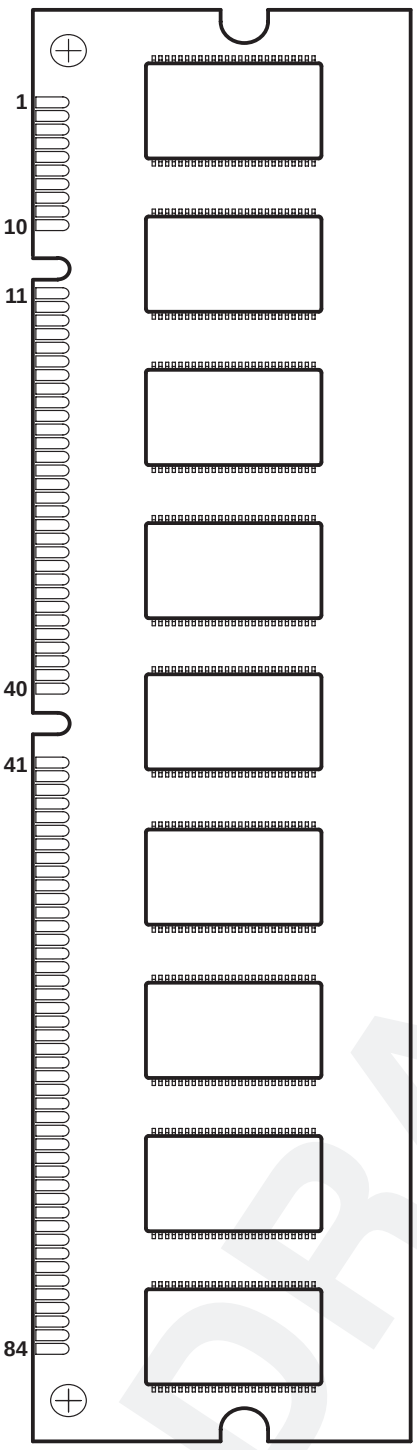
The TM2SR72EPU is a 16M-byte, 168-pin dual-in-line memory module (DIMM). The DIMM is composed of nine TMS626812DGE, 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic thin small-outline package (TSOP) mounted on a substrate with decoupling capacitors. See the TMS626812 data sheet (literature number SMOS687).

The TM4SR72EPU is a 32M-byte, 168-pin DIMM. The DIMM is composed of eighteen TMS626812DGE, 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS626812 data sheet (literature number SMOS687).

operation

The TM2SR72EPU operates as nine TMS626812DGE devices that are connected as shown in the TM2SR72EPU functional block diagram. The TM4SR72EPU operates as eighteen TMS626812DGE devices connected as shown in the TM4SR72EPU functional block diagram.

DUAL-IN-LINE MEMORY MODULE (TOP VIEW)



TM2SR72EPU (SIDE VIEW)

TM4SR72EPU (SIDE VIEW)

PIN NOMENCLATURE

A[0:10]	Row-Address Inputs
A[0:8]	Column-Address Inputs
A11/BA0	Bank-Select Zero
$\overline{\text{CAS}}$	Column-Address Strobe
CB[0:7]	Data In/Data Out
CKE[0:1]	Clock Enable
CK[0:3]	System Clock
DQ[0:63]	Data In/Data Out
DQMB[0:7]	Data-In/Data-Out Mask Enable
NC	No Connect
$\overline{\text{RAS}}$	Row-Address Strobe
$\overline{\text{S}}$[0:3]	Chip-Select
SA[0:2]	Serial Presence-Detect (SPD) Device Address Input
SCL	SPD Clock
SDA	SPD Address/Data
V_{DD}	3.3-V Supply
V_{SS}	Ground
$\overline{\text{WE}}$	Write Enable

Pin Assignments

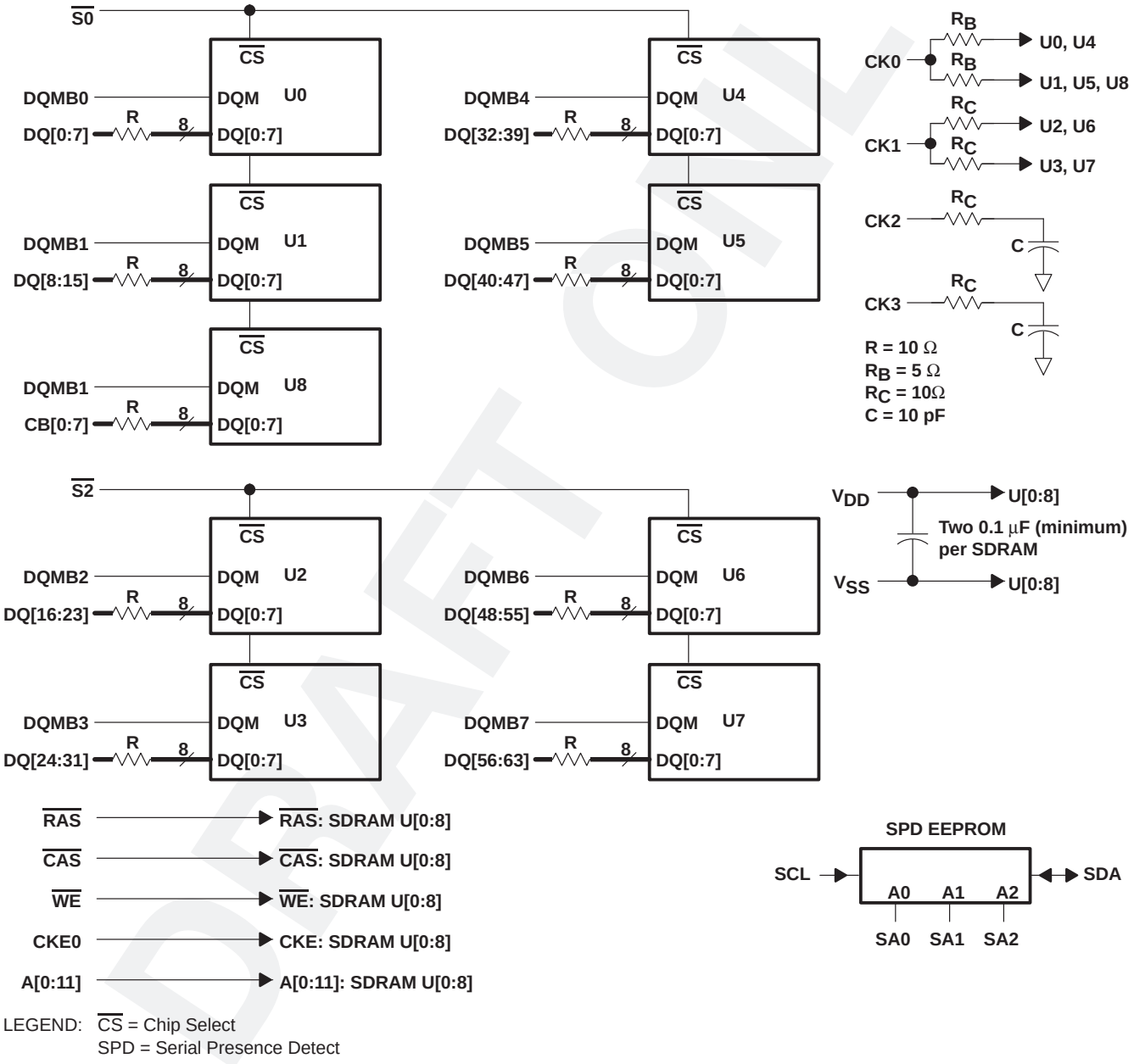
PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	$\overline{S2}$	87	DQ33	129	$\overline{S3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	NC	90	V_{DD}	132	NC
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{S0}$	72	DQ27	114	$\overline{S1}$	156	DQ59
31	NC	73	V_{DD}	115	$\overline{RAS}$	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	A11/BA0	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CK1	167	SA2
42	CK0	84	V_{DD}	126	NC	168	V_{DD}

dual-in-line memory module and components

The dual-in-line memory module and components include:

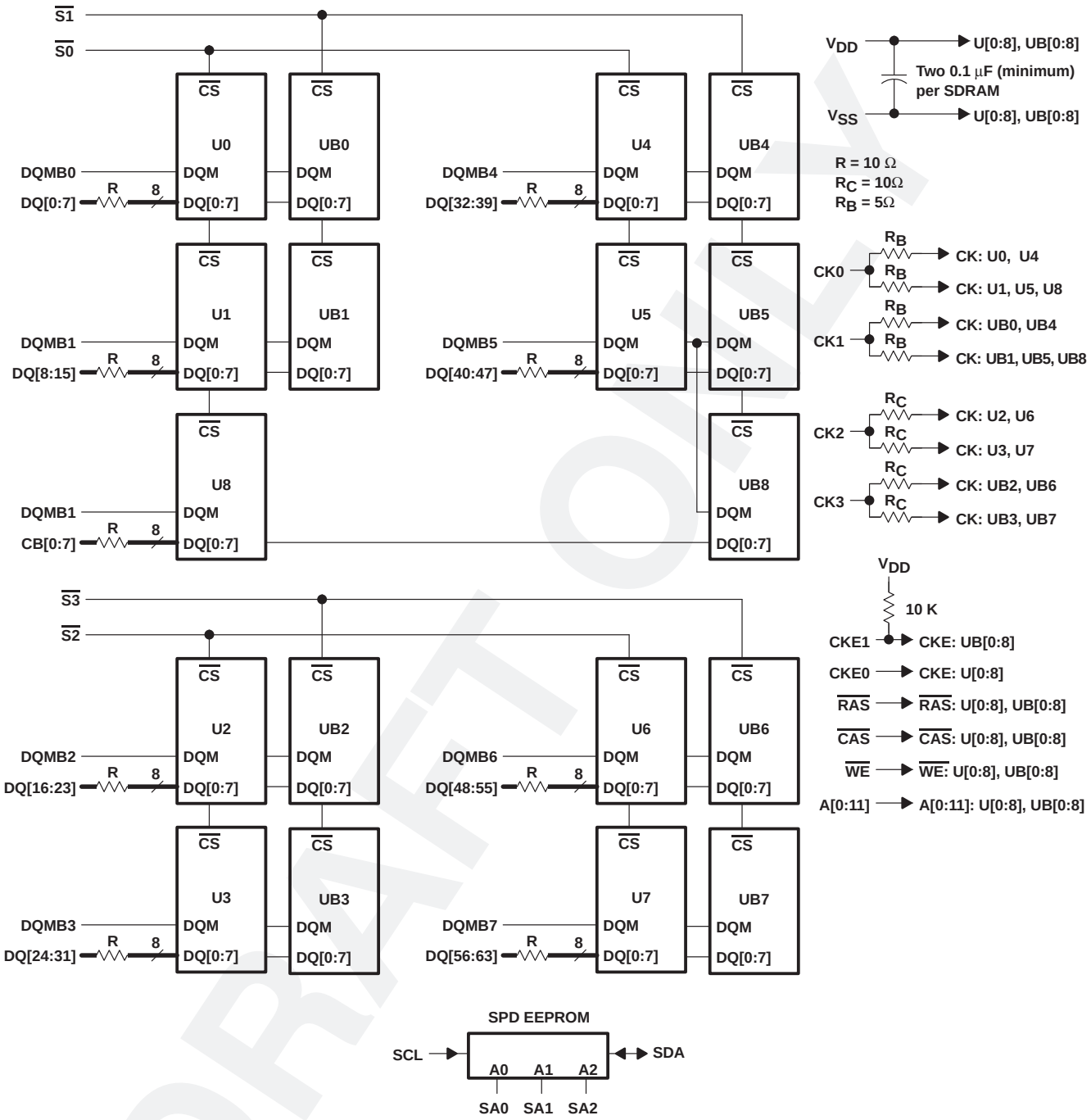
- PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram for the TM2SR72EPU



LEGEND: $\overline{CS}$ = Chip Select
SPD = Serial Presence Detect

functional block diagram for the TM4SR72EPU



absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . −0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . − 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM2SR72EPU . . . . . 9 W
TM4SR72EPU . . . . . 18 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . − 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
V_{IH-SPD}	High-level input voltage for SPD device	2		5.5	V
V_{IL}	Low-level input voltage ‡	−0.3		0.8	V
T_A	Ambient temperature	0		70	°C

‡ V_{IL} MIN = −1.5 V ac (pulse width ≤ 5 ns)

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETERS		TM2SR72EPU		TM4SR72EPU		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(CK)}$	Input capacitance, CK input		27		27	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0−A11, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		47		92	pF
$C_{i(CKE)}$	Input capacitance, CKE input		47		47	pF
C_o	Output capacitance		10		18	pF
$C_{i(DQMBx)}$	Input capacitance, DQMBx input		12		17	pF
$C_{i(Sx)}$	Input capacitance, $\overline{Sx}$ input		27		27	pF
$C_{i/o(SDA)}$	Input/output capacitor, SDA input		9		9	pF
$C_{i(SPD)}$	Input capacitor, SA0, SA1, SA2, SCL inputs		7		7	pF

NOTE 2: V_{DD} = 3.3 V ± 0.3 V. Bias on pins under test is 0 V.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

TM2SR72EPU

PARAMETER		TEST CONDITIONS		’2SR72EPU-12A		’2SR72EPU-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	0 V < V_I < V_{DD} + 0.3 V, All other pins = 0 V to V_{DD}			±10		±10	µA
I_O	Output current (leakage)	0 V < V_O < V_{DD} +0.3 V, Output disabled			±10		±10	µA
I_{CC1}	Operating current	Burst length = 1, $t_{RC} \geq t_{RC}$ MIN I_{OH}/I_{OL} = 0 mA, one bank activated (see Note 4)	CAS latency = 2		765		675	mA
			CAS latency = 3		855		855	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			18		18	mA
I_{CC2PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			18		18	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			270		270	mA
I_{CC2NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			18		18	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			72		72	mA
I_{CC3PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			72		72	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			315		315	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			90		90	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = one cycle (see Note 7)	CAS latency = 2		1170		990	mA
			CAS latency = 3		1395		1395	mA
I_{CC5}	Auto-refresh current	$t_{RC} \leq t_{RC}$ MIN	CAS latency = 2		675		630	mA
			CAS latency = 3		765		765	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			18		18	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state only twice during t_{RC}.
5. Control, DQ, and address inputs change state only once every 30 ns.
6. Control, DQ, and address inputs do not change (stable).
7. Control, DQ, and address inputs change only once every cycle.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

TM4SR72EPU

PARAMETER		TEST CONDITIONS		'4SR72EPU-12A		'4SR72EPU-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	0 V < V_I < V_{DD} + 0.3 V, All other pins = 0 V to V_{DD}			±20		±20	μA
I_O	Output current (leakage)	0 V < V_O < V_{DD} + 0.3 V, Output disabled			±20		±20	μA
I_{CC1}	Operating current	Burst length = 1, $t_{RC} \geq t_{RC}$ MIN I_{OH}/I_{OL} = 0 mA, one bank activated (see Note 4)	CAS latency = 2		783		683	mA
			CAS latency = 3		875		873	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			36		36	mA
I_{CC2PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			36		36	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			540		540	mA
I_{CC2NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			36		36	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			144		144	mA
I_{CC3PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			144		144	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			630		630	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			180		180	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = one cycle (see Note 7)	CAS latency = 2		1188		1008	mA
			CAS latency = 3		1413		1413	mA
I_{CC5}	Auto-refresh current	$t_{RC} \leq t_{RC}$ MIN	CAS latency = 2		693		648	mA
			CAS latency = 3		783		783	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			36		36	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state only twice during t_{RC}.
5. Control, DQ, and address inputs change state only once every 30 ns.
6. Control, DQ, and address inputs do not change (stable).
7. Control, DQ, and address inputs change only once every cycle.

ac timing requirements†

		'xSR72EPU-12A‡		'xSR72EPU-12		UNIT
		MIN	MAX	MIN	MAX	
t_{AC2}	Access time, CK high to data out, CAS latency = 2 (see Note 8)		9		10	ns
t_{AC3}	Access time, CK high to data out, CAS latency = 3 (see Note 8)		9		9	ns
t_{CK2}	Cycle time, CK, CAS latency = 2	15		18		ns
t_{CK3}	Cycle time, CK, CAS latency = 3	12		12		ns
t_{LZ}	Delay time, CK high to DQ in low-impedance state (see Note 9)	3		3		ns
t_{HZ}	Delay time, CK high to DQ in high-impedance state (see Note 10)		10		10	ns
t_{RC}	Delay time, ACTV, MRS, REFR, or SLFR to ACTV, MRS, REFR, or SLFR command	90		108		ns
t_{RCD}	Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 11)	30		30		ns
t_{RP}	Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command	30		36		ns
t_{RRD}	Delay time, ACTV command in one bank to ACTV command in the other bank	24		24		ns
t_{RSA}	Delay time, MRS command to ACTV, MRS, REFR, or SLFR command	24		24		ns
t_{RAS}	Delay time, ACTV command to DEAC or DCAB command	60	100000	72	100000	ns
t_{WR}	Delay time, final data in of WRT operation to DEAC or DCAB command	15		20		ns
n_{CCD}	Delay time, READ or WRT command to an interrupting command	1		1		cycle
n_{CDD}	Delay time, CS low or high to input enabled or inhibited	0	0	0	0	cycle
n_{CLE}	Delay time, CKE high or low to CK enabled or disabled	1	1	1	1	cycle
n_{CWL}	Delay time, final data in of WRT operation to READ, READ-P, WRT, WRT-P	1		1		cycle
n_{DID}	Delay time, ENBL or MASK command to enabled or masked data in	0	0	0	0	cycle
n_{DOD}	Delay time, ENBL or MASK command to enabled or masked data out	2	2	2	2	cycle
n_{HZP2}	Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 2		2		2	cycle
n_{HZP3}	Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 3		3		3	cycle
n_{WCD}	Delay time, WRT command to first data in	0	0	0	0	cycle
t_{OH}	Hold time, CK high to data out	3		3		ns
t_{IH}	Hold time, address, control, and data input	1		1.5		ns
t_{CESP}	Power-down/self-refresh exit time	10		10		ns
t_{CH}	Pulse duration, CK high	4		4		ns
t_{CL}	Pulse duration, CK low	4		4		ns
t_{IS}	Setup time, address, control, and data input	3		3		ns
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	$t_{RP} - (CL - 1) * t_{CK}$				ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command	60		60		ns
t_{REF}	Refresh interval		64		64	ms
t_T	Transition time (see Note 12)	1	5	1	5	ns

† All references are made to the rising transition of CKx, unless otherwise noted.
‡ -12A speed device is supported only at − 5% to + 10% V_{DD}

NOTES: 8. t_{AC} is referenced from the rising transition of CK that is previous to the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CKx that is CAS latency − one cycle after the READ command. Access time is measured at output reference level 1.4 V.
9. t_{LZ} is measured from the rising transition of CKx that is CAS latency − one cycle after the READ command.
10. t_{HZ} MAX defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
11. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.
12. Transition time, t_T, is measured between V_{IH} and V_{IL}.

serial presence detect

The serial-presence-detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through a IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.Tables in this section list the SPD contents as follows:

Tables in this section list the SPD contents as follows:

Table 1−TM2SR72EPU Table 2−TM4SR72EPU

Table 1. Serial Presence-Detect Data for the TM2SR72EPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM2SR72EPU-12A		TM2SR72EPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h
6	Data width of this assembly	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	t_{CK} = 12 ns	C0h	t_{CK} = 12 ns	C0h
10	SDRAM access from clock at CL = X	t_{AC} = 9 ns	90h	t_{AC} = 9 ns	90h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 µs/ self-refresh	80h	15.6 µs/ self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	2 banks	02h	2 banks	02h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h

serial presence detect (continued)

Table 1. Serial Presence-Detect Data for the TM2SR72EPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM2SR72EPU-12A		TM2SR72EPU-12	
		ITEM	DATA	ITEM	DATA
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%)/(−5%). Burst read/write, precharge all, auto precharge	1Eh	V_{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X − 1	t_{CK} = 15 ns	F0h	t_{CK} = 18 ns	30h
24	Maximum data-access time from clock at CL = X − 1	t_{AC} = 9.0 ns	90h	t_{AC} = 10 ns	A0h
25	Minimum clock cycle time at CL = X − 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X − 2	N/A	00h	N/A	00h
27	Minimum row precharge time	t_{RP} = 30 ns	1Eh	t_{RP} = 36 ns	24h
28	Minimum row-active to row-active delay	t_{RRD} = 24 ns	18h	t_{RRD} = 24 ns	18h
29	Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay	t_{RCD} = 30 ns	1Eh	t_{RCD} = 30 ns	1Eh
30	Minimum $\overline{RAS}$ pulse width	t_{RAS} = 60 ns	3Ch	t_{RAS} = 72 ns	48h
31	Density of each bank on module	16M Bytes	04h	16M Bytes	04h
32−61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0−62	25	19h	107	6Bh
64−71	Manufacturer's JEDEC ID code per JEP−106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD	
73−90	Manufacturer's part number†	TBD		TBD	
91	Die revision code†	TBD		TBD	
92	PCB revision code†	TBD		TBD	
93−94	Manufacturing date†	TBD		TBD	
95−98	Assembly serial number†	TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD	
126−127	Vendor specific data†	TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD	
167−255	Open				

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM4SR72EPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SR72EPU-12A		TM4SR72EPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h
6	Data width of this assembly	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	t_{CK} = 12 ns	C0h	t_{CK} = 12 ns	C0h
10	SDRAM access from clock at CL = X	t_{AC} = 9 ns	90h	t_{AC} = 9 ns	90h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 µs/ self-refresh	80h	15.6 µs/ self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	2 banks	02h	2 banks	02h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%)/(−5%). Burst read/write, precharge all, auto precharge	1Eh	V_{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X − 1	t_{CK} = 15 ns	F0h	t_{CK} = 18 ns	30h
24	Maximum data-access time from clock at CL = X − 1	t_{AC} = 9.0 ns	90h	t_{AC} = 10 ns	A0h
25	Minimum clock cycle time at CL = X − 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X − 2	N/A	00h	N/A	00h
27	Minimum row precharge time	t_{RP} = 30 ns	1Eh	t_{RP} = 36 ns	24h
28	Minimum row-active to row-active delay	t_{RRD} = 24 ns	18h	t_{RRD} = 24 ns	18h
29	Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay	t_{RCD} = 30 ns	1Eh	t_{RCD} = 30 ns	1Eh
30	Minimum $\overline{RAS}$ pulse width	t_{RAS} = 60 ns	3Ch	t_{RAS} = 72 ns	48h
31	Density of each bank on module	16M Bytes	04h	16M Bytes	04h

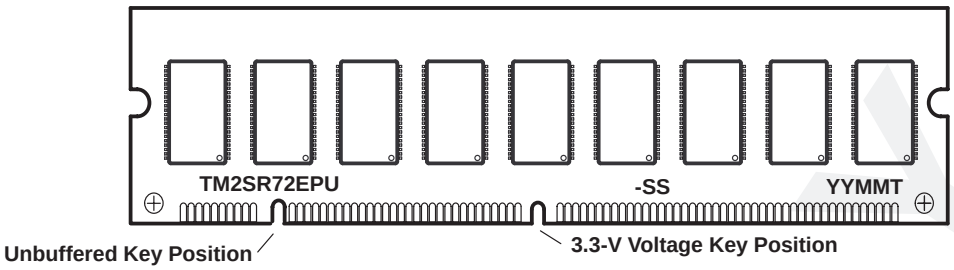
serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM4SR72EPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SR72EPU-12A		TM4SR72EPU-12	
		ITEM	DATA	ITEM	DATA
32−61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0−62	26	1Ah	108	6Ch
64−71	Manufacturer's JEDEC ID code per JEP−106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD	
73−90	Manufacturer's part number†	TBD		TBD	
91	Die revision code†	TBD		TBD	
92	PCB revision code†	TBD		TBD	
93−94	Manufacturing date†	TBD		TBD	
95−98	Assembly serial number†	TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD	
126−127	Vendor specific data†	TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD	
167−255	Open				

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

device symbolization (TM2SR72EPU)

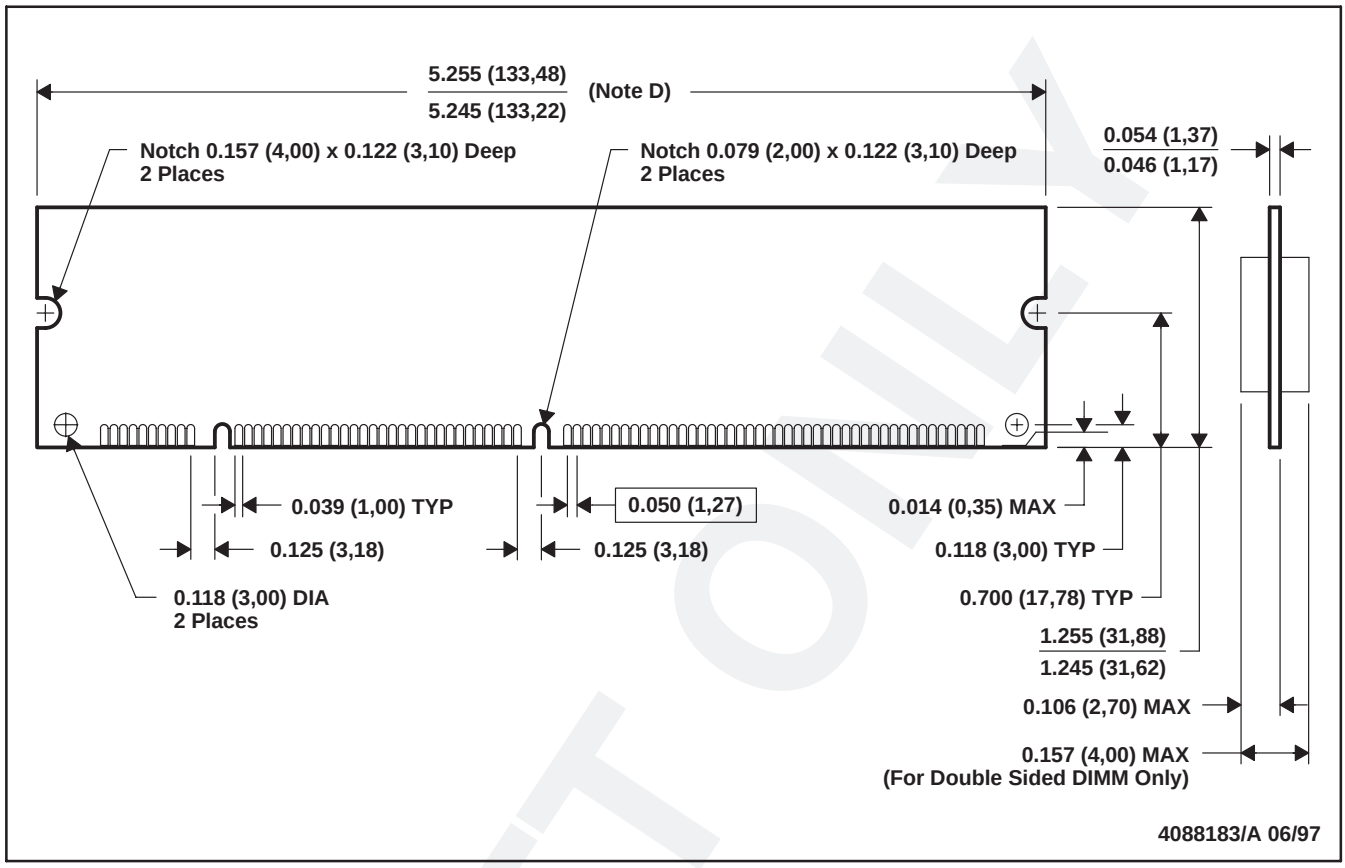


YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

MECHANICAL DATA

BU (R-PDIM-N168) **DUAL IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-161
D. Dimension includes de-panelization variations; applies between notch and tab edge.
E. Outline may vary above notches to allow router/panelization irregularities.

- **Organization**
  - **TM2SR72EPU . . . 2097152 x 72 Bits**
  - **TM4SR72EPU . . . 4194304 x 72 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **Designed for 66-MHz 4-Clock Systems**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **TM2SR72EPU — Uses Nine 16M-Bit Synchronous Dynamic RAMs (SDRAMs) (2M × 8-Bit) in Plastic Thin Small-Outline Packages (TSOPs)**
- **TM4SR72EPU — Uses 18 16M-Bit SDRAMs (2M × 8-Bit) in Plastic TSOPs**
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME		ACCESS TIME (CLOCK TO OUTPUT)		REFRESH INTERVAL
	t_{CK3} (CL = 3)†	t_{CK2} (CL = 2)	t_{CK3} (CL = 3)	t_{CK2} (CL = 2)	
'xSR72EPU-12A‡	12 ns	15 ns	9 ns	9 ns	64 ms
'xSR72EPU-12	12 ns	18 ns	9 ns	10 ns	64 ms

† CL = CAS latency
‡ -12A speed device is supported only at −5% to +10% V_{DD}

- **High-Speed, Low-Noise Low-Voltage TTL (LVTTL) Interface**
- **Byte-Read/Write Capability**
- **Read Latencies 2 and 3 Supported**
- **Support Burst-Interleave and Burst-Interrupt Operations**
- **Burst Length Programmable to 1, 2, 4, and 8**
- **Two Banks for On-Chip Interleaving (Gapless Access)**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**
- **Pipeline Architecture**
- **Serial Presence-Detect (SPD) Using EEPROM**

description

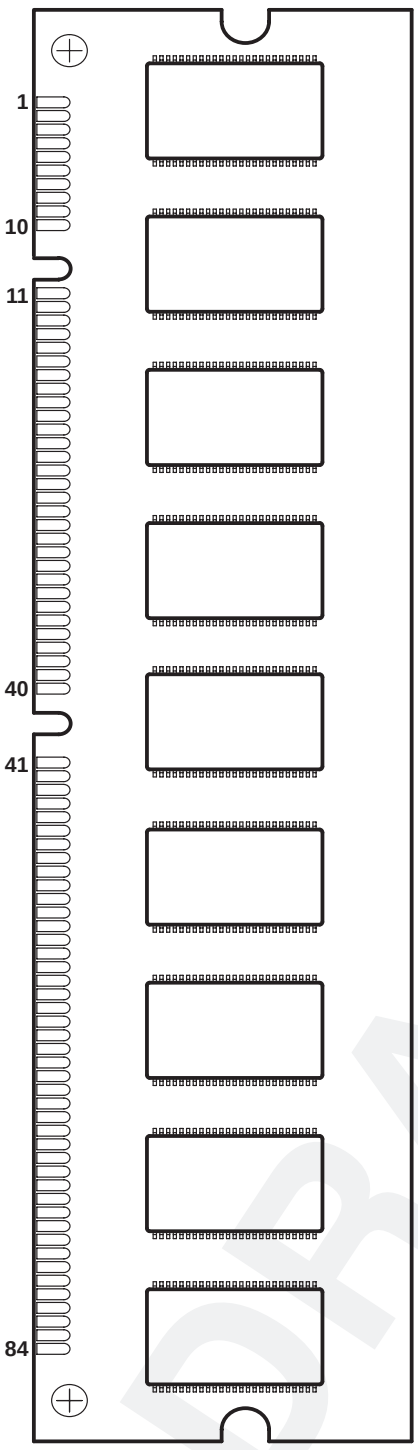
The TM2SR72EPU is a 16M-byte, 168-pin dual-in-line memory module (DIMM). The DIMM is composed of nine TMS626812DGE, 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic thin small-outline package (TSOP) mounted on a substrate with decoupling capacitors. See the TMS626812 data sheet (literature number SMOS687).

The TM4SR72EPU is a 32M-byte, 168-pin DIMM. The DIMM is composed of eighteen TMS626812DGE, 2097152 x 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS626812 data sheet (literature number SMOS687).

operation

The TM2SR72EPU operates as nine TMS626812DGE devices that are connected as shown in the TM2SR72EPU functional block diagram. The TM4SR72EPU operates as eighteen TMS626812DGE devices connected as shown in the TM4SR72EPU functional block diagram.

DUAL-IN-LINE MEMORY MODULE (TOP VIEW)



TM2SR72EPU (SIDE VIEW)

TM4SR72EPU (SIDE VIEW)

PIN NOMENCLATURE

A[0:10]	Row-Address Inputs
A[0:8]	Column-Address Inputs
A11/BA0	Bank-Select Zero
$\overline{CAS}$	Column-Address Strobe
CB[0:7]	Data In/Data Out
CKE[0:1]	Clock Enable
CK[0:3]	System Clock
DQ[0:63]	Data In/Data Out
DQMB[0:7]	Data-In/Data-Out Mask Enable
NC	No Connect
$\overline{RAS}$	Row-Address Strobe
$\overline{S}$[0:3]	Chip-Select
SA[0:2]	Serial Presence-Detect (SPD) Device Address Input
SCL	SPD Clock
SDA	SPD Address/Data
V_{DD}	3.3-V Supply
V_{SS}	Ground
$\overline{WE}$	Write Enable

Pin Assignments

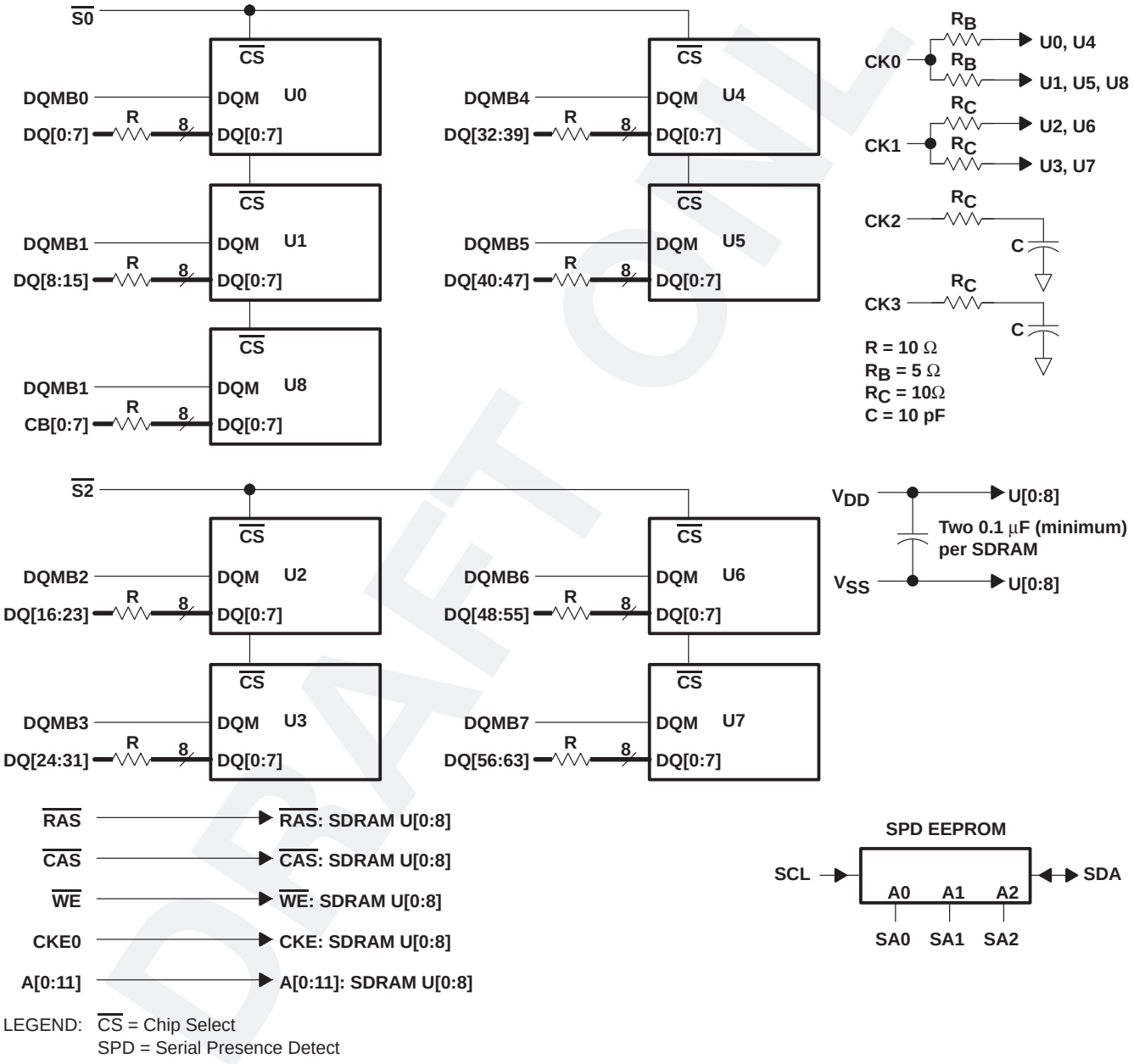
PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	$\overline{S2}$	87	DQ33	129	$\overline{S3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	NC	90	V_{DD}	132	NC
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{S0}$	72	DQ27	114	$\overline{S1}$	156	DQ59
31	NC	73	V_{DD}	115	$\overline{RAS}$	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	A11/BA0	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CK1	167	SA2
42	CK0	84	V_{DD}	126	NC	168	V_{DD}

dual-in-line memory module and components

The dual-in-line memory module and components include:

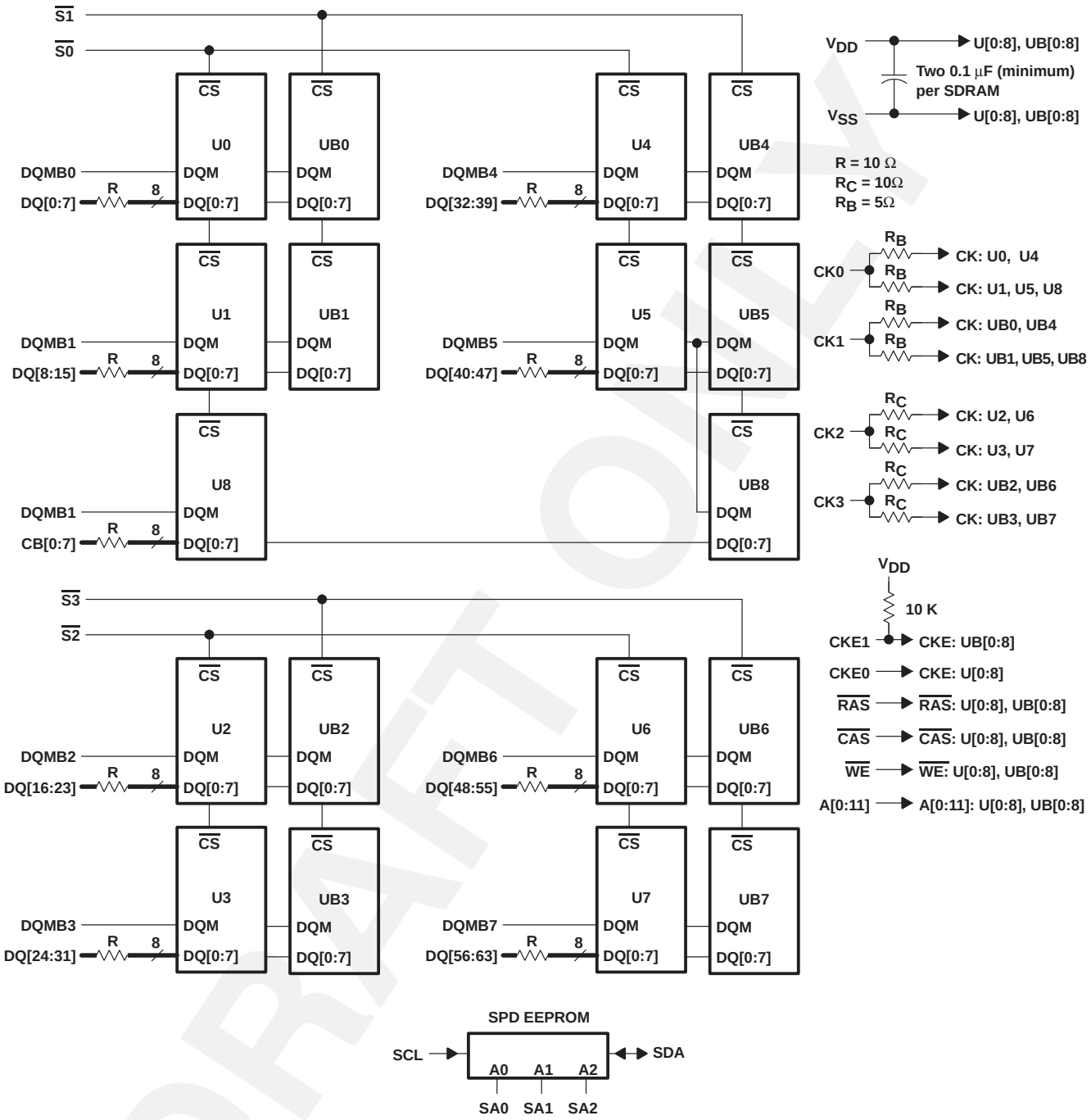
- PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram for the TM2SR72EPU



LEGEND: $\overline{CS}$ = Chip Select
SPD = Serial Presence Detect

functional block diagram for the TM4SR72EPU



absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . −0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . − 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM2SR72EPU . . . . . 9 W
TM4SR72EPU . . . . . 18 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . − 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
V_{IH-SPD}	High-level input voltage for SPD device	2		5.5	V
V_{IL}	Low-level input voltage ‡	−0.3		0.8	V
T_A	Ambient temperature	0		70	°C

‡ V_{IL} MIN = −1.5 V ac (pulse width ≤ 5 ns)

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETERS		TM2SR72EPU		TM4SR72EPU		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(CK)}$	Input capacitance, CK input		27		27	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0−A11, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		47		92	pF
$C_{i(CKE)}$	Input capacitance, CKE input		47		47	pF
C_o	Output capacitance		10		18	pF
$C_{i(DQMBx)}$	Input capacitance, DQMBx input		12		17	pF
$C_{i(Sx)}$	Input capacitance, $\overline{Sx}$ input		27		27	pF
$C_{i/o(SDA)}$	Input/output capacitor, SDA input		9		9	pF
$C_{i(SPD)}$	Input capacitor, SA0, SA1, SA2, SCL inputs		7		7	pF

NOTE 2: V_{DD} = 3.3 V ± 0.3 V. Bias on pins under test is 0 V.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

TM2SR72EPU

PARAMETER		TEST CONDITIONS		’2SR72EPU-12A		’2SR72EPU-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	0 V < V_I < V_{DD} + 0.3 V, All other pins = 0 V to V_{DD}			±10		±10	µA
I_O	Output current (leakage)	0 V < V_O < V_{DD} +0.3 V, Output disabled			±10		±10	µA
I_{CC1}	Operating current	Burst length = 1, $t_{RC} \geq t_{RC}$ MIN I_{OH}/I_{OL} = 0 mA, one bank activated (see Note 4)	CAS latency = 2		765		675	mA
			CAS latency = 3		855		855	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			18		18	mA
I_{CC2PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			18		18	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			270		270	mA
I_{CC2NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			18		18	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			72		72	mA
I_{CC3PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			72		72	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			315		315	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			90		90	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = one cycle (see Note 7)	CAS latency = 2		1170		990	mA
			CAS latency = 3		1395		1395	mA
I_{CC5}	Auto-refresh current	$t_{RC} \leq t_{RC}$ MIN	CAS latency = 2		675		630	mA
			CAS latency = 3		765		765	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			18		18	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state only twice during t_{RC}.
5. Control, DQ, and address inputs change state only once every 30 ns.
6. Control, DQ, and address inputs do not change (stable).
7. Control, DQ, and address inputs change only once every cycle.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

TM4SR72EPU

PARAMETER		TEST CONDITIONS		'4SR72EPU-12A		'4SR72EPU-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	0 V < V_I < V_{DD} + 0.3 V, All other pins = 0 V to V_{DD}			±20		±20	μA
I_O	Output current (leakage)	0 V < V_O < V_{DD} + 0.3 V, Output disabled			±20		±20	μA
I_{CC1}	Operating current	Burst length = 1, $t_{RC} \geq t_{RC}$ MIN I_{OH}/I_{OL} = 0 mA, one bank activated (see Note 4)	CAS latency = 2		783		683	mA
			CAS latency = 3		875		873	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			36		36	mA
I_{CC2PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			36		36	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			540		540	mA
I_{CC2NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			36		36	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 5)			144		144	mA
I_{CC3PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			144		144	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 5)			630		630	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 6)			180		180	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = one cycle (see Note 7)	CAS latency = 2		1188		1008	mA
			CAS latency = 3		1413		1413	mA
I_{CC5}	Auto-refresh current	$t_{RC} \leq t_{RC}$ MIN	CAS latency = 2		693		648	mA
			CAS latency = 3		783		783	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			36		36	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state only twice during t_{RC}.
5. Control, DQ, and address inputs change state only once every 30 ns.
6. Control, DQ, and address inputs do not change (stable).
7. Control, DQ, and address inputs change only once every cycle.

ac timing requirements†

		'xSR72EPU-12A‡		'xSR72EPU-12		UNIT
		MIN	MAX	MIN	MAX	
t_{AC2}	Access time, CK high to data out, CAS latency = 2 (see Note 8)		9		10	ns
t_{AC3}	Access time, CK high to data out, CAS latency = 3 (see Note 8)		9		9	ns
t_{CK2}	Cycle time, CK, CAS latency = 2	15		18		ns
t_{CK3}	Cycle time, CK, CAS latency = 3	12		12		ns
t_{LZ}	Delay time, CK high to DQ in low-impedance state (see Note 9)	3		3		ns
t_{HZ}	Delay time, CK high to DQ in high-impedance state (see Note 10)		10		10	ns
t_{RC}	Delay time, ACTV, MRS, REFR, or SLFR to ACTV, MRS, REFR, or SLFR command	90		108		ns
t_{RCD}	Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 11)	30		30		ns
t_{RP}	Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command	30		36		ns
t_{RRD}	Delay time, ACTV command in one bank to ACTV command in the other bank	24		24		ns
t_{RSA}	Delay time, MRS command to ACTV, MRS, REFR, or SLFR command	24		24		ns
t_{RAS}	Delay time, ACTV command to DEAC or DCAB command	60	100000	72	100000	ns
t_{WR}	Delay time, final data in of WRT operation to DEAC or DCAB command	15		20		ns
n_{CCD}	Delay time, READ or WRT command to an interrupting command	1		1		cycle
n_{CDD}	Delay time, CS low or high to input enabled or inhibited	0	0	0	0	cycle
n_{CLE}	Delay time, CKE high or low to CK enabled or disabled	1	1	1	1	cycle
n_{CWL}	Delay time, final data in of WRT operation to READ, READ-P, WRT, WRT-P	1		1		cycle
n_{DID}	Delay time, ENBL or MASK command to enabled or masked data in	0	0	0	0	cycle
n_{DOD}	Delay time, ENBL or MASK command to enabled or masked data out	2	2	2	2	cycle
n_{HZP2}	Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 2		2		2	cycle
n_{HZP3}	Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 3		3		3	cycle
n_{WCD}	Delay time, WRT command to first data in	0	0	0	0	cycle
t_{OH}	Hold time, CK high to data out	3		3		ns
t_{IH}	Hold time, address, control, and data input	1		1.5		ns
t_{CESP}	Power-down/self-refresh exit time	10		10		ns
t_{CH}	Pulse duration, CK high	4		4		ns
t_{CL}	Pulse duration, CK low	4		4		ns
t_{IS}	Setup time, address, control, and data input	3		3		ns
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	$t_{RP} - (CL - 1) * t_{CK}$				ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command	60		60		ns
t_{REF}	Refresh interval		64		64	ms
t_T	Transition time (see Note 12)	1	5	1	5	ns

† All references are made to the rising transition of CKx, unless otherwise noted.
‡ -12A speed device is supported only at − 5% to + 10% V_{DD}

NOTES: 8. t_{AC} is referenced from the rising transition of CK that is previous to the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CKx that is CAS latency − one cycle after the READ command. Access time is measured at output reference level 1.4 V.
9. t_{LZ} is measured from the rising transition of CKx that is CAS latency − one cycle after the READ command.
10. t_{HZ} MAX defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
11. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.
12. Transition time, t_T, is measured between V_{IH} and V_{IL}.

serial presence detect

The serial-presence-detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through a IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.Tables in this section list the SPD contents as follows:

Tables in this section list the SPD contents as follows:

Table 1−TM2SR72EPU Table 2−TM4SR72EPU

Table 1. Serial Presence-Detect Data for the TM2SR72EPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM2SR72EPU-12A		TM2SR72EPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h
6	Data width of this assembly	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	t_{CK} = 12 ns	C0h	t_{CK} = 12 ns	C0h
10	SDRAM access from clock at CL = X	t_{AC} = 9 ns	90h	t_{AC} = 9 ns	90h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 µs/ self-refresh	80h	15.6 µs/ self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	2 banks	02h	2 banks	02h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h

serial presence detect (continued)

Table 1. Serial Presence-Detect Data for the TM2SR72EPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM2SR72EPU-12A		TM2SR72EPU-12	
		ITEM	DATA	ITEM	DATA
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%)/(−5%). Burst read/write, precharge all, auto precharge	1Eh	V_{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X − 1	t_{CK} = 15 ns	F0h	t_{CK} = 18 ns	30h
24	Maximum data-access time from clock at CL = X − 1	t_{AC} = 9.0 ns	90h	t_{AC} = 10 ns	A0h
25	Minimum clock cycle time at CL = X − 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X − 2	N/A	00h	N/A	00h
27	Minimum row precharge time	t_{RP} = 30 ns	1Eh	t_{RP} = 36 ns	24h
28	Minimum row-active to row-active delay	t_{RRD} = 24 ns	18h	t_{RRD} = 24 ns	18h
29	Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay	t_{RCD} = 30 ns	1Eh	t_{RCD} = 30 ns	1Eh
30	Minimum $\overline{RAS}$ pulse width	t_{RAS} = 60 ns	3Ch	t_{RAS} = 72 ns	48h
31	Density of each bank on module	16M Bytes	04h	16M Bytes	04h
32−61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0−62	25	19h	107	6Bh
64−71	Manufacturer's JEDEC ID code per JEP−106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD	
73−90	Manufacturer's part number†	TBD		TBD	
91	Die revision code†	TBD		TBD	
92	PCB revision code†	TBD		TBD	
93−94	Manufacturing date†	TBD		TBD	
95−98	Assembly serial number†	TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD	
126−127	Vendor specific data†	TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD	
167−255	Open				

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM4SR72EPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SR72EPU-12A		TM4SR72EPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	9	09h	9	09h
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h
6	Data width of this assembly	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	t_{CK} = 12 ns	C0h	t_{CK} = 12 ns	C0h
10	SDRAM access from clock at CL = X	t_{AC} = 9 ns	90h	t_{AC} = 9 ns	90h
11	DIMM configuration type (non-parity, parity, error correcting code [ECC])	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 µs/ self-refresh	80h	15.6 µs/ self-refresh	80h
13	SDRAM width, primary DRAM	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8	0Fh	1, 2, 4, 8	0Fh
17	Number of banks on each SDRAM device	2 banks	02h	2 banks	02h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (+10%)/(−5%). Burst read/write, precharge all, auto precharge	1Eh	V_{DD} tolerance = (+10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X − 1	t_{CK} = 15 ns	F0h	t_{CK} = 18 ns	30h
24	Maximum data-access time from clock at CL = X − 1	t_{AC} = 9.0 ns	90h	t_{AC} = 10 ns	A0h
25	Minimum clock cycle time at CL = X − 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X − 2	N/A	00h	N/A	00h
27	Minimum row precharge time	t_{RP} = 30 ns	1Eh	t_{RP} = 36 ns	24h
28	Minimum row-active to row-active delay	t_{RRD} = 24 ns	18h	t_{RRD} = 24 ns	18h
29	Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay	t_{RCD} = 30 ns	1Eh	t_{RCD} = 30 ns	1Eh
30	Minimum $\overline{RAS}$ pulse width	t_{RAS} = 60 ns	3Ch	t_{RAS} = 72 ns	48h
31	Density of each bank on module	16M Bytes	04h	16M Bytes	04h

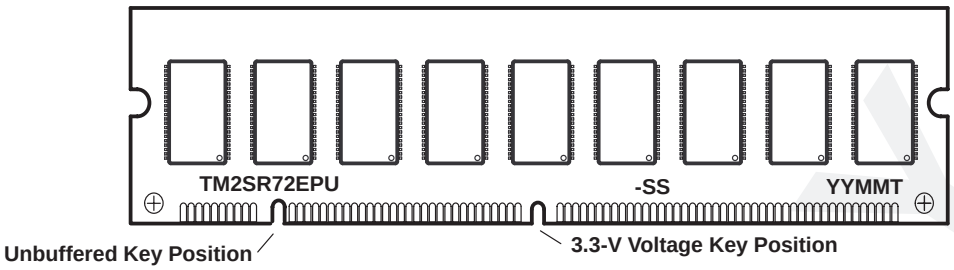
serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM4SR72EPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SR72EPU-12A		TM4SR72EPU-12	
		ITEM	DATA	ITEM	DATA
32−61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0−62	26	1Ah	108	6Ch
64−71	Manufacturer's JEDEC ID code per JEP−106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD	
73−90	Manufacturer's part number†	TBD		TBD	
91	Die revision code†	TBD		TBD	
92	PCB revision code†	TBD		TBD	
93−94	Manufacturing date†	TBD		TBD	
95−98	Assembly serial number†	TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD	
126−127	Vendor specific data†	TBD		TBD	
128−166	System integrator's specific data‡	TBD		TBD	
167−255	Open				

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

device symbolization (TM2SR72EPU)

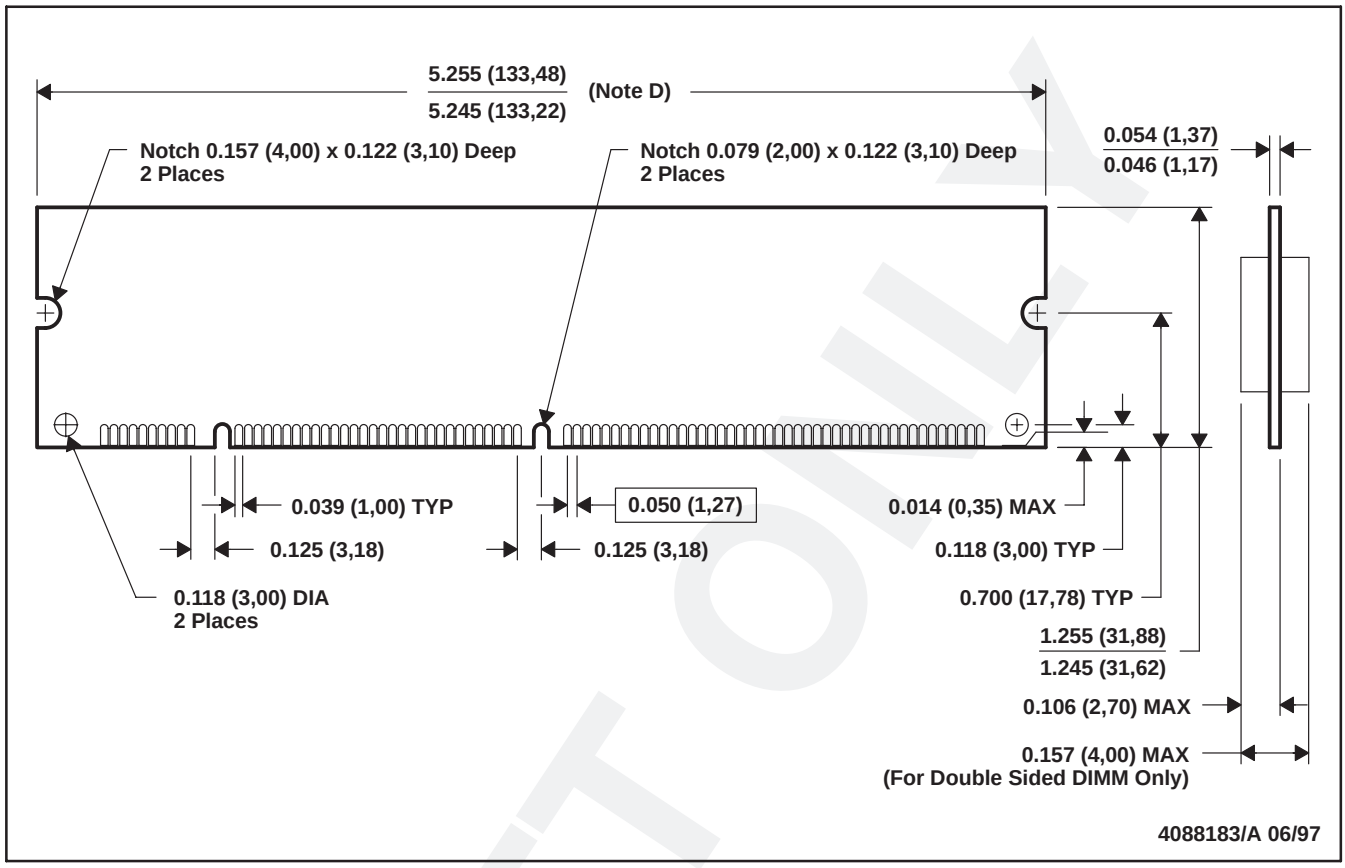


YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

MECHANICAL DATA

BU (R-PDIM-N168) **DUAL IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-161
D. Dimension includes de-panelization variations; applies between notch and tab edge.
E. Outline may vary above notches to allow router/panelization irregularities.

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