

TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN EXTENDED-DATA-OUT DYNAMIC RAM MODULES

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- **Organization**
 - TM2EP64DxN . . . 2097152 × 64 Bits
 - TM2EP72DxN . . . 2097152 × 72 Bits
 - TM4EP64DxN . . . 4194304 × 64 Bits
 - TM4EP72DxN . . . 4194304 × 72 Bits
- **Single 3.3-V Power Supply** (±10% Tolerance)
- **TM2EP64DxN** — Uses Eight 16M-Bit (2M×8-Bit) Dynamic Random Access Memories (DRAMs) in Thin Small-Outline Package (TSOP), or Small-Outline J-Lead Package (SOJ)
- **TM2EP72DxN** — Uses Nine 16M-Bit (2M×8-Bit) DRAMs in TSOP, or SOJ
- **TM4EP64DxN** — Uses 16 16M-Bit (2M×8-Bit) DRAMs in TSOP, or SOJ
- **TM4EP72DxN** — Uses 18 16M-Bit (2M×8-Bit) DRAMs in TSOP, or SOJ
- **Performance ranges**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **High-Speed, Low-Noise LVTTTL Interface**
- **Long Refresh Period: 32 ms (2 048 Cycles)**
- **3-State Output**
- **Extended-Data-Out (EDO) Operation With CAS-Before-RAS (CBR), RAS-Only, and Hidden Refresh**
- **Serial Presence Detect (SPD) Using EEPROM**
- **Ambient Air Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**

	ACCESS TIME t _{RAC} MAX	ACCESS TIME t _{CAC} MAX	ACCESS TIME t _{AA} MAX	EDO CYCLE t _{HPC} MIN
'xEPxxDxN-50	50 ns	13 ns	25 ns	20 ns
'xEPxxDxN-60	60 ns	15 ns	30 ns	25 ns
'xEPxxDxN-70	70 ns	18 ns	35 ns	30 ns

description

The TM2EP64DPN is a 16M-byte, 168-pin, dual-in-line memory module (DIMM). The DIMM is composed of eight TMS427809A, 2097152 byte × 8-bit 2K-refresh EDO DRAMs, each in a 400-mil, 28-pin plastic TSOP (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS887). The TM2EP64DJN is available with an SOJ package (DZ suffix).

The TM2EP72DPN is a 16M-byte, 168-pin DIMM. The DIMM is composed of nine TMS427809A, 2097152 byte × 8-bit 2K-refresh EDO DRAMs, mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS887). The TM2EP72DJN is available with an SOJ package (DZ suffix).

The TM4EP64DPN is a 32M-byte, 168-pin, dual-in-line memory module (DIMM). The DIMM is composed of sixteen TMS427809A, 2097152 × 8-bit 2K-refresh EDO DRAMs, mounted on a substrate with decoupling capacitors. The TM4EP64DJN is available with an SOJ package (DZ suffix).

The TM4EP72DPN is a 32M-byte, 168-pin DIMM. The DIMM is composed of 18 TMS427809A, 2097152 × 8-bit 2K-refresh EDO DRAMs, mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS887). The TM4EP72DJN is available with an SOJ package (DZ suffix).



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 **TEXAS
INSTRUMENTS**

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TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
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operation

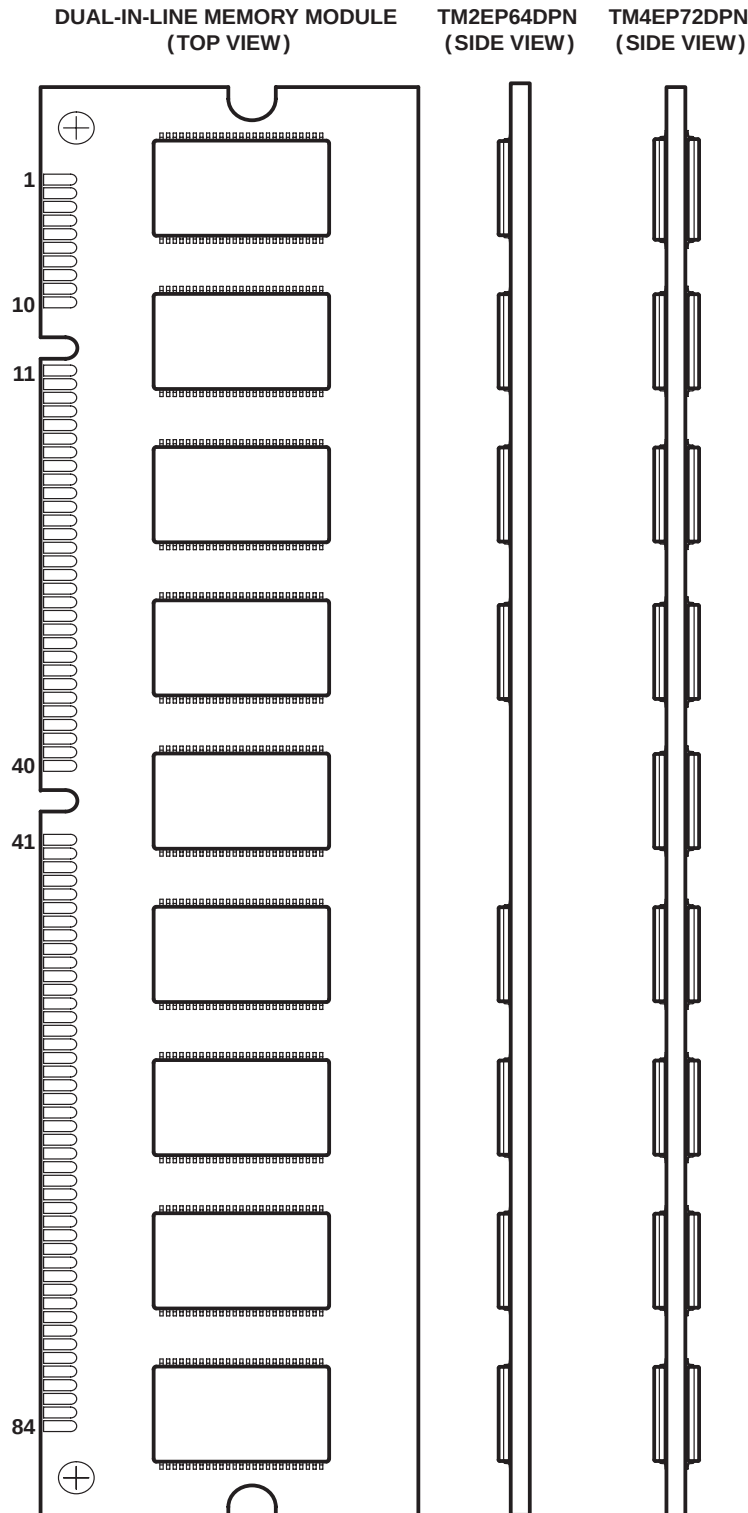
The TMxEPxxDxN DIMMs operate as displayed in Table 1.

Table 1. TMxEPxxDxN DIMM Device Table

DIMM	DEVICE AND QUANTITY ()	Connected as shown in the functional block diagram.
TM2EP64DxN	TMS427809A (8)	
TM2EP72DxN	TMS427809A (9)	
TM4EP64DxN	TMS427809A (16)	
TM4EP72DxN	TMS427809A (18)	

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PIN NOMENCLATURE	
A[0:10]	Row Address Inputs
A[0:9]	Column Address Inputs
DQ[0:63]	Data In/Data Out
CB[0:7]	Check-Bit In/Check-Bit Out
CAS[0:7]	Column-Address Strobe
RAS[0:3]	Row-Address Strobe
WE0 and WE2	Write Enable
OE0 and OE2	Output Enable
SA[0:2]	Serial Presence Detect (SPD)
	Device Add Input
SDA	SPD Address/Data
SCL	SPD Clock
NC	No-Connect Pin
V _{DD}	3.3-V Supply
V _{SS}	Ground



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Pin Assignments

NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	$\overline{\text{OE}}2$	86	DQ32	128	NC
3	DQ1	45	$\overline{\text{RAS}}2$	87	DQ33	129	$\overline{\text{RAS}}3$
4	DQ2	46	$\overline{\text{CAS}}2$	88	DQ34	130	$\overline{\text{CAS}}6$
5	DQ3	47	$\overline{\text{CAS}}3$	89	DQ35	131	$\overline{\text{CAS}}7$
6	V _{DD}	48	$\overline{\text{WE}}2$	90	V _{DD}	132	NC
7	DQ4	49	V _{DD}	91	DQ36	133	V _{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{DD}	101	DQ45	143	V _{DD}
18	V _{DD}	60	DQ20	102	V _{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	V _{SS}	106	CB5	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V _{DD}	68	V _{SS}	110	V _{DD}	152	V _{SS}
27	$\overline{\text{WE}}0$	69	DQ24	111	NC	153	DQ56
28	$\overline{\text{CAS}}0$	70	DQ25	112	$\overline{\text{CAS}}4$	154	DQ57
29	$\overline{\text{CAS}}1$	71	DQ26	113	$\overline{\text{CAS}}5$	155	DQ58
30	$\overline{\text{RAS}}0$	72	DQ27	114	$\overline{\text{RAS}}1$	156	DQ59
31	$\overline{\text{OE}}0$	73	V _{DD}	115	NC	157	V _{DD}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V _{DD}	82	SDA	124	V _{DD}	166	SA1
41	V _{DD}	83	SCL	125	NC	167	SA2
42	NC	84	V _{DD}	126	NC	168	V _{DD}



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dual-in-line memory module and components

The dual-in-line memory module and components include:

- PC substrate: $1,27 \pm 0,1$ mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper



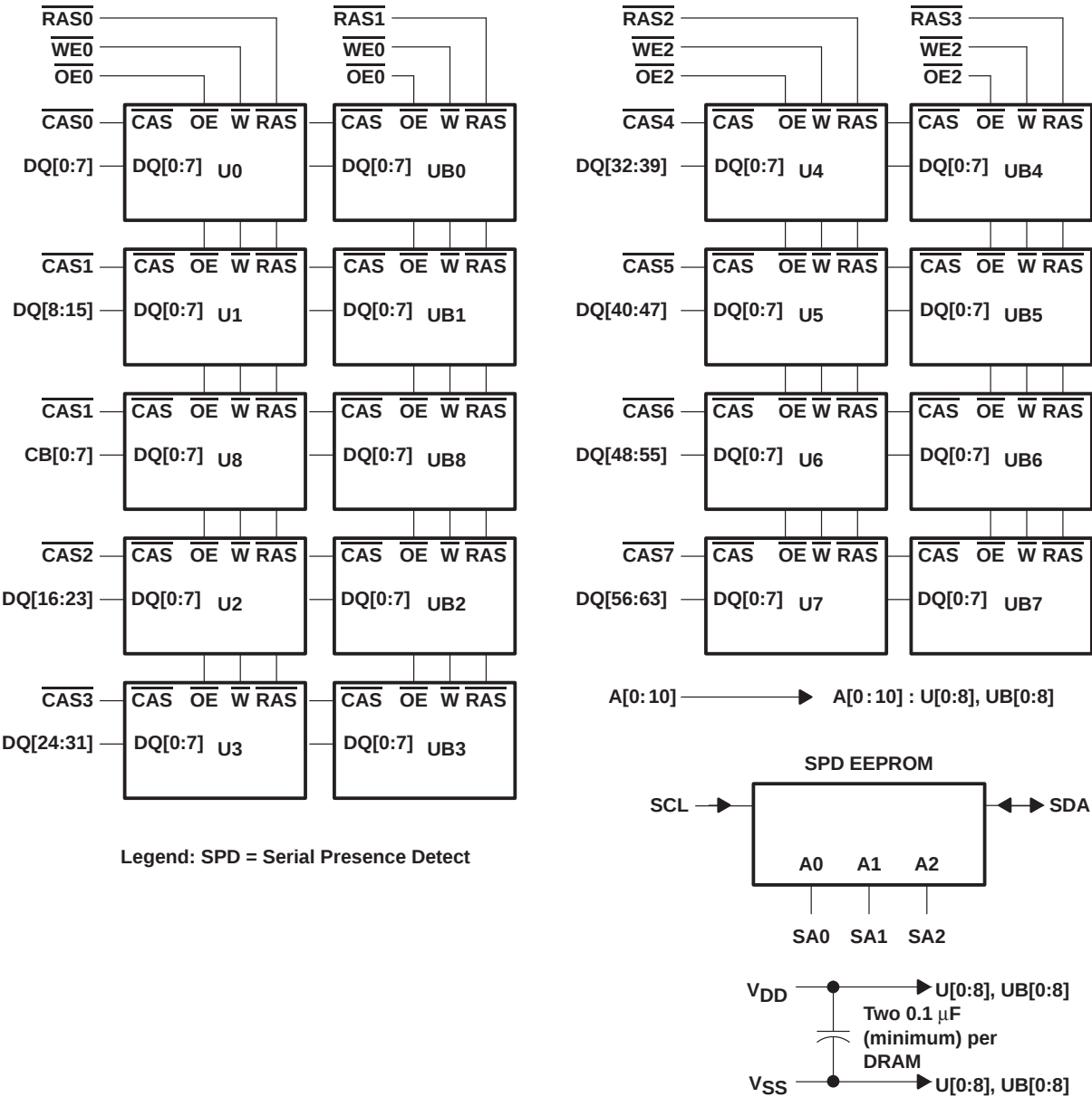
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functional block diagram

The following table shows the four DIMM modules and locations (Ux/UBx) that are used.

COMPONENT TABLE	
MODULE	LOCATIONS USED
TM2EP64DxN	U[0:7]
TM2EP72DxN	U[0:8]
TM4EP64DxN	U[0:7], UB[0:7]
TM4EP72DxN	U[0:8], UB[0:8]



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absolute maximum ratings over ambient temperature range (unless otherwise noted)[†]

Supply voltage range, V_{DD}	–0.5 V to 4.6 V
Voltage range on any pin (see Note 1)	– 0.5 V to 4.6 V
Short-circuit output current	50 mA
Power dissipation: TM2EP64DxN	8 W
TM2EP72DxN	9 W
TM4EP64DxN	16 W
TM4EP72DxN	18 W
Ambient temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 125°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		$V_{DD} + 0.3$	V
V_{IH-SPD}	High-level input voltage for the SPD device	2		5.5	V
V_{IL}	Low-level input voltage	–0.3		0.8	V
T_A	Ambient temperature	0		70	°C

capacitance over recommended ranges of supply voltage and ambient temperature, $f = 1$ MHz (see Note 2)

PARAMETER		'2EP64DxN		'2EP72DxN		'4EP64DxN		'4EP72DxN		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0–A10		42		47		82		92	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}x$		30		37		58		72	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}x$		9		16		16		30	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}x$		30		37		30		37	pF
$C_{i(W)}$	Input capacitance, $\overline{WE}x$		30		37		38		37	pF
C_o	Output capacitance		9		9		16		16	pF
$C_{i/o(SDA)}$	Input/output capacitance, SDA input		9		9		9		9	pF
$C_{i(SPD)}$	Input capacitance, SA0,SA1,SA2,SCL inputs		7		7		7		7	pF

NOTE 2: $V_{DD} = \text{NOM supply voltage} \pm 10\%$, and the bias on pins under test is 0 V.



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**electrical characteristics over recommended ranges of supply voltage and ambient temperature
(unless otherwise noted)**

TM2EP64DxN

PARAMETER		TEST CONDITIONS†		'2EP64DxN-50		'2EP64DxN-60		'2EP64DxN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	High-level output voltage	I _{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I _{OH} = – 100 µA	LVC MOS	V _{DD} – 0.2		V _{DD} – 0.2		V _{DD} – 0.2		
V _{OL}	Low-level output voltage	I _{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I _{OL} = 100 µA	LVC MOS		0.2		0.2		0.2	
I _I	Input current (leakage)	V _{DD} = 3.6 V, V _I = 0 V to 3.9 V, All others = 0 V to V _{DD}			± 10		± 10		± 10	µA
I _O	Output current (leakage)	V _{DD} = 3.6 V, V _O = 0 V to V _{DD} , CASx high			± 10		± 10		± 10	µA
I _{CC1} ‡§	Read- or write-cycle current	V _{DD} = 3.6 V, Minimum cycle			960		800		720	mA
I _{CC2}	Standby current	V _{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high			16		16		16	mA
		V _{IH} = V _{DD} – 0.2 V (LVC MOS), After one memory cycle, RASx and CASx high			8		8		8	mA
I _{CC3} ‡§	Average refresh current (RAS-only refresh or CBR)	V _{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RASx low after CASx low (CBR)			960		800		720	mA
I _{CC4} ‡¶	Average EDO current	V _{DD} = 3.6 V, t _{HPC} = MIN, RASx low, CASx cycling			880		720		640	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RASx}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
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**electrical characteristics over recommended ranges of supply voltage and ambient temperature
(unless otherwise noted) (continued)**

TM2EP72DxN

PARAMETER	TEST CONDITIONS†	'2EP72DxN-50		'2EP72DxN-60		'2EP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = – 2 mA LVTTL	2.4		2.4		2.4		V
	I _{OH} = – 100 µA LVCMOS	V _{DD} – 0.2		V _{DD} – 0.2		V _{DD} – 0.2		
V _{OL} Low-level output voltage	I _{OL} = 2 mA LVTTL		0.4		0.4		0.4	V
	I _{OL} = 100 µA LVCMOS		0.2		0.2		0.2	
I _I Input current (leakage)	V _{DD} = 3.6 V, V _I = 0 V to 3.9 V, All others = 0 V to V _{DD}		± 10		± 10		± 10	µA
I _O Output current (leakage)	V _{DD} = 3.6 V, V _O = 0 V to V _{DD} , CASx high		± 10		± 10		± 10	µA
I _{CC1} ‡§	Read- or write-cycle current V _{DD} = 3.6 V, Minimum cycle		976		816		736	mA
I _{CC2} Standby current	V _{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high		18		18		18	mA
	V _{IH} = V _{DD} – 0.2 V (LVCMOS), After one memory cycle, RASx and CASx high		9		9		9	mA
I _{CC3} ‡§	Average refresh current (RASx-only refresh or CBR) V _{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RASx low after CASx low (CBR)		976		816		736	mA
I _{CC4} ‡¶	Average EDO current V _{DD} = 3.6 V, t _{HPC} = MIN, RASx low, CASx cycling		990		810		720	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RASx}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}



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TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
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**electrical characteristics over recommended ranges of supply voltage and ambient temperature
(unless otherwise noted) (continued)**

TM4EP64DxN

PARAMETER		TEST CONDITIONS†		'4EP64DxN-50		'4EP64DxN-60		'4EP64DxN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	High-level output voltage	I _{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I _{OH} = – 100 µA	LVC MOS	V _{DD} – 0.2		V _{DD} – 0.2		V _{DD} – 0.2		
V _{OL}	Low-level output voltage	I _{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I _{OL} = 100 µA	LVC MOS		0.2		0.2		0.2	
I _I	Input current (leakage)	V _{DD} = 3.6 V, V _I = 0 V to 3.9 V, All others = 0 V to V _{DD}			± 20		± 20		± 20	µA
I _O	Output current (leakage)	V _{DD} = 3.6 V, V _O = 0 V to V _{DD} , CASx high			± 20		± 20		± 20	µA
I _{CC1} ‡§	Read- or write-cycle current	V _{DD} = 3.6 V, Minimum cycle			976		816		736	mA
I _{CC2}	Standby current	V _{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high			32		32		32	mA
		V _{IH} = V _{DD} – 0.2 V (LVC MOS), After one memory cycle, RASx and CASx high			16		16		16	mA
I _{CC3} ‡§	Average refresh current (RASx-only refresh or CBR)	V _{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RASx low after CASx low (CBR)			976		816		736	mA
I _{CC4} ‡¶	Average EDO current	V _{DD} = 3.6 V, t _{HPC} = MIN, RASx low, CASx cycling			896		736		656	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RASx}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}



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**electrical characteristics over recommended ranges of supply voltage and ambient temperature
(unless otherwise noted) (continued)**

TM4EP72DxN

PARAMETER	TEST CONDITIONS†	'4EP72DxN-50		'4EP72DxN-60		'4EP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = – 2 mA LVTTL	2.4		2.4		2.4		V
	I _{OH} = – 100 µA LVCMOS	V _{DD} – 0.2		V _{DD} – 0.2		V _{DD} – 0.2		
V _{OL} Low-level output voltage	I _{OL} = 2 mA LVTTL		0.4		0.4		0.4	V
	I _{OL} = 100 µA LVCMOS		0.2		0.2		0.2	
I _I Input current (leakage)	V _{DD} = 3.6 V, V _I = 0 V to 3.9 V, All others = 0 V to V _{DD}		± 20		± 20		± 20	µA
I _O Output current (leakage)	V _{DD} = 3.6 V, V _O = 0 V to V _{DD} , CASx high		± 20		± 20		± 20	µA
I _{CC1} ‡§	Read- or write-cycle current V _{DD} = 3.6 V, Minimum cycle		1098		918		828	mA
I _{CC2} Standby current	V _{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high		36		36		36	mA
	V _{IH} = V _{DD} – 0.2 V (LVCMOS), After one memory cycle, RASx and CASx high		18		18		18	mA
I _{CC3} ‡§	Average refresh current (RASx-only refresh or CBR) V _{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RASx low after CASx low (CBR)		1098		918		828	mA
I _{CC4} ‡¶	Average EDO current V _{DD} = 3.6 V, t _{HPC} = MIN, RASx low, CASx cycling		1008		828		738	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RASx}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}



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switching characteristics over recommended ranges of supply voltage and ambient temperature
 (see Note 3)

PARAMETER	'xEP64DxN-50 'xEP72DxN-50		'xEP64DxN-60 'xEP72DxN-60		'xEP64DxN-70 'xEP72DxN-70		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{AA} Access time from column address (see Note 4)		25		30		35	ns
t _{CAC} Access time from $\overline{\text{CASx}}$ (see Note 4)		13		15		18	ns
t _{CPA} Access time from $\overline{\text{CASx}}$ precharge (see Note 4)		28		35		40	ns
t _{RAC} Access time from $\overline{\text{RASx}}$ (see Note 4)		50		60		70	ns
t _{OEa} Access time from $\overline{\text{OEx}}$ (see Note 4)		13		15		18	ns
t _{CLZ} Delay time, $\overline{\text{CASx}}$ to output in low impedance	0		0		0		ns
t _{REZ} Output buffer turn off delay from $\overline{\text{RASx}}$ (see Note 5)	3	13	3	15	3	18	ns
t _{CEZ} Output buffer turn off delay from $\overline{\text{CASx}}$ (see Note 5)	3	13	3	15	3	18	ns
t _{OEZ} Output buffer turn off delay from $\overline{\text{OEx}}$ (see Note 5)	3	13	3	15	3	18	ns
t _{WEZ} Output buffer turn off delay from $\overline{\text{WEx}}$ (see Note 5)	3	13	3	15	3	18	ns

NOTES: 3. With ac parameters, it is assumed that $t_T = 2$ ns.

4. Access times are measured with output reference levels of $V_{OH} = 2$ V and $V_{OL} = 0.8$ V.

5. The maximum values of t_{REZ}, t_{CEZ}, t_{OEZ}, and t_{WEZ} are specified when the outputs are no longer driven. Data-in should not be driven until one of the applicable maximum values is satisfied.

EDO timing requirements (see Note 3)

	'xEP64DxN-50 'xEP72DxN-50		'xEP64DxN-60 'xEP72DxN-60		'xEP64DxN-70 'xEP72DxN-70		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{HPC} Cycle time, EDO page mode, read-write	20		25		30		ns
t _{PRWC} Cycle time, EDO read-write	57		68		78		ns
t _{CSH} Delay time, $\overline{\text{RASx}}$ active to $\overline{\text{CASx}}$ precharge	40		48		58		ns
t _{CHO} Hold time, $\overline{\text{OEx}}$ from $\overline{\text{CASx}}$	7		10		10		ns
t _{DOH} Hold time, output from $\overline{\text{CASx}}$	5		5		5		ns
t _{OEP} Precharge time, $\overline{\text{OEx}}$	5		5		5		ns
t _{CAS} Pulse duration, $\overline{\text{CASx}}$ active	8	10 000	10	10 000	12	10 000	ns
t _{WPE} Pulse duration, $\overline{\text{WEx}}$ active (output disable only)	7		7		7		ns
t _{CP} Pulse duration, $\overline{\text{CASx}}$ precharge	8		10		10		ns
t _{OCH} Setup time, $\overline{\text{OEx}}$ before $\overline{\text{CASx}}$	8		10		10		ns
t _{OEP} Precharge time, $\overline{\text{OEx}}$	5		5		5		ns

NOTE 3: With ac parameters, it is assumed that $t_T = 2$ ns.



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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ac timing requirements

		'xEP64DxN-50 'xEP72DxN-50		'xEP64DxN-60 'xEP72DxN-60		'xEP64DxN-70 'xEP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Cycle time, random read or write	84		104		124		ns
t _{RWC}	Cycle time, read-write	111		135		160		ns
t _{RASP}	Pulse duration, $\overline{\text{RASx}}$ active, fast page mode (see Note 6)	50	100 000	60	100 000	70	100 000	ns
t _{RAS}	Pulse duration, $\overline{\text{RASx}}$ active, non-page mode (see Note 6)	50	10 000	60	10 000	70	10 000	ns
t _{RP}	Pulse duration, $\overline{\text{RASx}}$ precharge	30		40		50		ns
t _{WP}	Pulse duration, write command	8		10		10		ns
t _{RASS}	Pulse duration, $\overline{\text{RASx}}$ active, self refresh (see Note 7)	100		100		100		μs
t _{RPS}	Pulse duration, $\overline{\text{RASx}}$ precharge after self refresh	90		110		130		ns
t _{ASC}	Setup time, column address	0		0		0		ns
t _{ASR}	Setup time, row address	0		0		0		ns
t _{DS}	Setup time, data in (see Note 8)	0		0		0		ns
t _{RCS}	Setup time, read command	0		0		0		ns
t _{CWL}	Setup time, write command before $\overline{\text{CASx}}$ precharge	8		10		12		ns
t _{RWL}	Setup time, write command before $\overline{\text{RASx}}$ precharge	8		10		12		ns
t _{WCS}	Setup time, write command before $\overline{\text{CASx}}$ active (early-write only)	0		0		0		ns
t _{WRP}	Setup time, $\overline{\text{WEx}}$ high before $\overline{\text{RASx}}$ low (CBR refresh only)	10		10		10		ns
t _{CSR}	Setup time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RASx}}$ (CBR refresh only)	5		5		5		ns
t _{CAH}	Hold time, column address	8		10		12		ns
t _{DH}	Hold time, data in (see Note 8)	8		10		12		ns
t _{RAH}	Hold time, row address	8		10		10		ns
t _{RCH}	Hold time, read command referenced to $\overline{\text{CASx}}$ (see Note 9)	0		0		0		ns
t _{RRH}	Hold time, read command referenced to $\overline{\text{RASx}}$ (see Note 9)	0		0		0		ns
t _{WCH}	Hold time, write command during $\overline{\text{CASx}}$ active (early-write only)	8		10		12		ns
t _{ROH}	Hold time, $\overline{\text{RASx}}$ referenced to $\overline{\text{OEx}}$	8		10		10		ns
t _{WRH}	Hold time, $\overline{\text{WEx}}$ high after $\overline{\text{RASx}}$ low (CBR refresh only)	10		10		10		ns
t _{CHR}	Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RASx}}$ (CBR refresh only)	10		10		10		ns
t _{OEH}	Hold time, $\overline{\text{OEx}}$ command	13		15		18		ns
t _{RHCP}	Hold time, $\overline{\text{RASx}}$ active from $\overline{\text{CASx}}$ precharge	28		35		40		ns
t _{CHS}	Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RASx}}$ (self refresh only)	– 50		– 50		– 50		ns
t _{AWD}	Delay time, column address to write command (read-write only)	42		49		57		ns
t _{CRP}	Delay time, $\overline{\text{CASx}}$ precharge to $\overline{\text{RASx}}$	5		5		5		ns

- NOTES: 6. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
7. During the period of $10\ \mu\text{s} \leq t_{\text{RASS}} \leq 100\ \mu\text{s}$, the device is in a transition state from normal-operation mode to self-refresh mode.
8. Referenced to the later of $\overline{\text{CASx}}$ or $\overline{\text{WEx}}$ in write operations
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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ac timing requirements (continued)

		'xEP64DxN-50 'xEP72DxN-50		'xEP64DxN-60 'xEP72DxN-60		'xEP64DxN-70 'xEP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{CWD}	Delay time, $\overline{\text{CASx}}$ to write command (read-write only)	30		34		40		ns
t _{OED}	Delay time, $\overline{\text{OEx}}$ to data in	13		15		18		ns
t _{RAD}	Delay time, $\overline{\text{RASx}}$ to column address (see Note 10)	10	25	12	30	12	35	ns
t _{RAL}	Delay time, column address to $\overline{\text{RASx}}$ precharge	25		30		35		ns
t _{CAL}	Delay time, column address to $\overline{\text{CASx}}$ precharge	18		20		25		ns
t _{RCD}	Delay time, $\overline{\text{RASx}}$ to $\overline{\text{CASx}}$ (see Note 10)	12	37	14	45	14	52	ns
t _{RPC}	Delay time, $\overline{\text{RASx}}$ precharge to $\overline{\text{CASx}}$	5		5		5		ns
t _{RSH}	Delay time, $\overline{\text{CASx}}$ active to $\overline{\text{RASx}}$ precharge	8		10		12		ns
t _{RWD}	Delay time, $\overline{\text{RASx}}$ to write command (read-write only)	67		79		92		ns
t _{CPW}	Delay time, $\overline{\text{CASx}}$ precharge to write command (read-write only)	45		54		62		ns
t _{REF}	Refresh time interval		32		32		32	ms
t _T	Transition time	2	30	2	30	2	30	ns

NOTE 10: The maximum value is specified only to ensure access time.



TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN EXTENDED-DATA-OUT DYNAMIC RAM MODULES

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serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, DRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments module comply with the current JEDEC SPD Standard. Please see the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 2 – TM2EP64DxN

Table 3 – TM2EP72DxN

Table 4 – TM4EP64DxN

Table 5 – TM4EP72DxN

Table 2. Serial Presence Detect Data for the TM2EP64DxN

BYTE NO.	FUNCTION DESCRIBED	'2EP64DxN-50		'2EP64DxN-60		'2EP64DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$ access time of module	$t_{\text{RAC}} = 50 \text{ ns}$	32h	$t_{\text{RAC}} = 60 \text{ ns}$	3Ch	$t_{\text{RAC}} = 70 \text{ ns}$	46h
10	$\overline{\text{CAS}}$ access time of module	$t_{\text{CAC}} = 13 \text{ ns}$	0Dh	$t_{\text{CAC}} = 15 \text{ ns}$	0Fh	$t_{\text{CAC}} = 18 \text{ ns}$	12h
11	DIMM configuration type (non-parity, parity, ECC)	Non-Parity	00h	Non-Parity	00h	Non-Parity	00h
12	Refresh rate/type	15.6 μs	00h	15.6 μs	00h	15.6 μs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	41	29h	53	35h	66	42h
64–71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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serial presence detect (continued)

Table 2. Serial Presence Detect Data for the TM2EP64DxN (Continued)

BYTE NO.	FUNCTION DESCRIBED	'2EP64DxN-50		'2EP64DxN-60		'2EP64DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
72	Manufacturing location [†]	TBD		TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD		TBD	
91	Die revision code [†]	TBD		TBD		TBD	
92	PCB revision code [†]	TBD		TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD		TBD	
167–255	Open						

[†] TBD indicates values are determined at manufacturing time and are module dependent.

[‡] These TBD values are determined and programmed by the customer (optional).



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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serial presence detect (continued)

Table 3. Serial Presence Detect Data for the TM2EP72DxN

BYTE NO.	FUNCTION DESCRIBED	'2EP72DxN-50		'2EP72DxN-60		'2EP72DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	72 bits	48h	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$ access time of module	$t_{\text{RAC}} = 50 \text{ ns}$	32h	$t_{\text{RAC}} = 60 \text{ ns}$	3Ch	$t_{\text{RAC}} = 70 \text{ ns}$	46h
10	$\overline{\text{CAS}}$ access time of module	$t_{\text{CAC}} = 13 \text{ ns}$	0Dh	$t_{\text{CAC}} = 15 \text{ ns}$	0Fh	$t_{\text{CAC}} = 18 \text{ ns}$	12h
11	DIMM configuration type (non-parity, parity, ECC)	ECC	02h	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 μs	00h	15.6 μs	00h	15.6 μs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h	x8	08h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	59	3Bh	71	47h	84	54h
64–71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD		TBD	
91	Die revision code [†]	TBD		TBD		TBD	
92	PCB revision code [†]	TBD		TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD		TBD	
167–255	Open						

[†] TBD indicates values are determined at manufacturing time and are module dependent.

[‡] These TBD values are determined and programmed by the customer (optional).



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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serial presence detect (continued)

Table 4. Serial Presence Detect Data for the TM4EP64DxN

BYTE NO.	FUNCTION DESCRIBED	'4EP64DxN-50		'4EP64DxN-60		'4EP64DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RASx}}$ access time of module	$t_{\text{RAC}} = 50 \text{ ns}$	32h	$t_{\text{RAC}} = 60 \text{ ns}$	3Ch	$t_{\text{RAC}} = 70 \text{ ns}$	46h
10	$\overline{\text{CASx}}$ access time of module	$t_{\text{CAC}} = 13 \text{ ns}$	0Dh	$t_{\text{CAC}} = 15 \text{ ns}$	0Fh	$t_{\text{CAC}} = 18 \text{ ns}$	12h
11	DIMM configuration type (non-parity, parity, ECC)	Non-Parity	00h	Non-Parity	00h	Non-Parity	00h
12	Refresh rate/type	15.6 μs	00h	15.6 μs	00h	15.6 μs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	42	2Ah	54	36h	67	43h
64–71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD		TBD	
91	Die revision code [†]	TBD		TBD		TBD	
92	PCB revision code [†]	TBD		TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD		TBD	
167–255	Open						

[†] TBD indicates values are determined at manufacturing time and are module dependent.

[‡] These TBD values are determined and programmed by the customer (optional).



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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serial presence detect (continued)

Table 5. Serial Presence Detect for the TM4EP72DxN

BYTE NO.	FUNCTION DESCRIBED	'4EP72DxN-50		'4EP72DxN-60		'4EP72DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	72 bits	48h	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$ access time of module	$t_{\text{RAC}} = 50 \text{ ns}$	32h	$t_{\text{RAC}} = 60 \text{ ns}$	3Ch	$t_{\text{RAC}} = 70 \text{ ns}$	46h
10	$\overline{\text{CAS}}$ access time of module	$t_{\text{CAC}} = 13 \text{ ns}$	0Dh	$t_{\text{CAC}} = 15 \text{ ns}$	0Fh	$t_{\text{CAC}} = 18 \text{ ns}$	12h
11	DIMM configuration type (non-parity, parity, ECC)	ECC	02h	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 μs	00h	15.6 μs	00h	15.6 μs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h	x8	08h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	60	3Ch	72	48h	85	55h
64–71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD		TBD	
91	Die revision code [†]	TBD		TBD		TBD	
92	PCB revision code [†]	TBD		TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD		TBD	
167–255	Open						

[†] TBD indicates values are determined at manufacturing time and are module dependent.

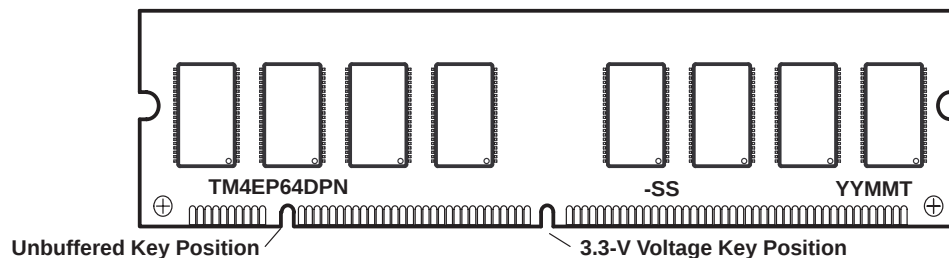
[‡] These TBD values are determined and programmed by the customer (optional).



TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN EXTENDED-DATA-OUT DYNAMIC RAM MODULES

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device symbolization (TM4EP64DPN illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

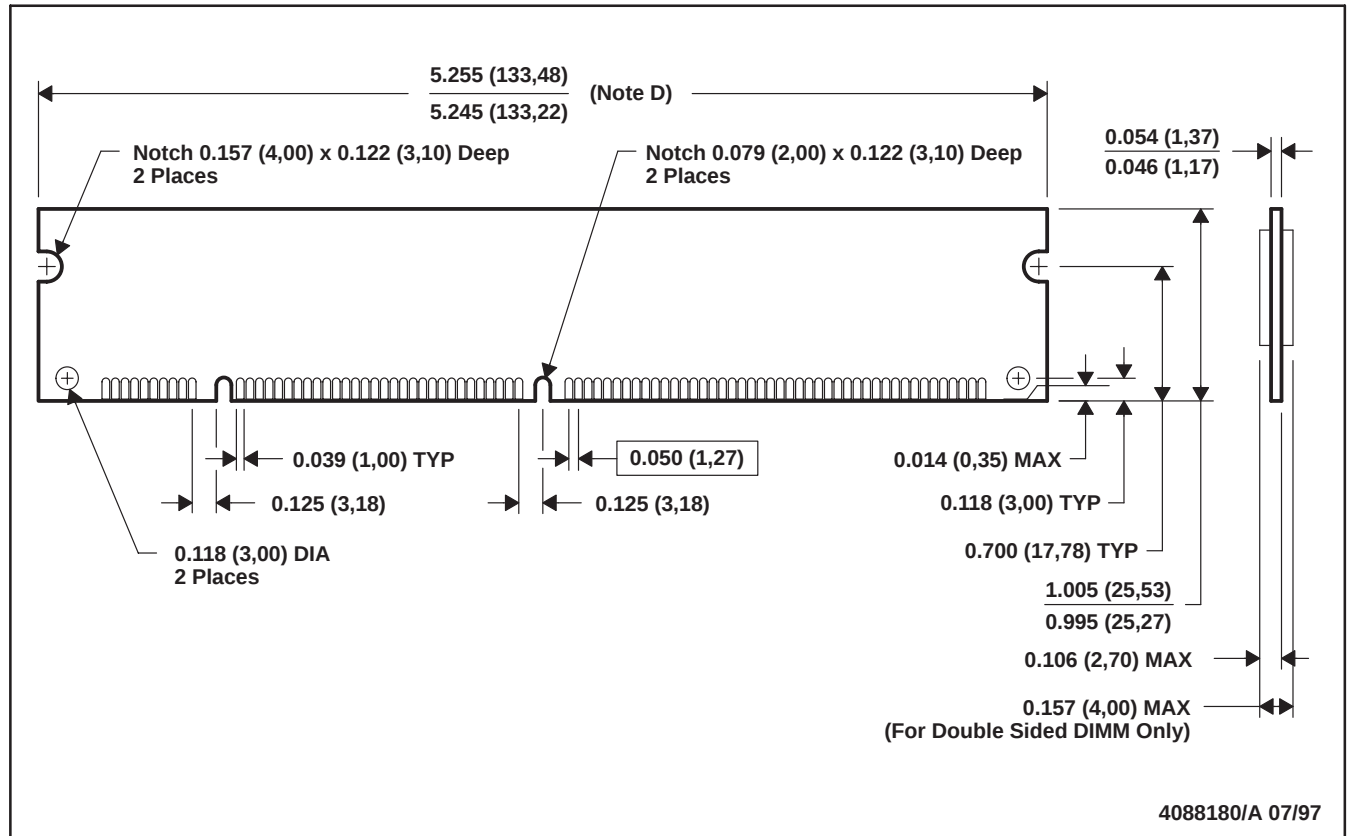
**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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MECHANICAL DATA

BR (R-PDIM-N168)

DUAL IN-LINE MEMORY MODULE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-161
 - D. Dimension includes de-panelization variations; applies between notch and tab edge.
 - E. Outline may vary above notches to allow router/panelization irregularities.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN EXTENDED-DATA-OUT DYNAMIC RAM MODULES

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- **Organization**
 - TM2EP64DxN . . . 2097152 × 64 Bits
 - TM2EP72DxN . . . 2097152 × 72 Bits
 - TM4EP64DxN . . . 4194304 × 64 Bits
 - TM4EP72DxN . . . 4194304 × 72 Bits
- **Single 3.3-V Power Supply** (±10% Tolerance)
- **TM2EP64DxN** — Uses Eight 16M-Bit (2M×8-Bit) Dynamic Random Access Memories (DRAMs) in Thin Small-Outline Package (TSOP), or Small-Outline J-Lead Package (SOJ)
- **TM2EP72DxN** — Uses Nine 16M-Bit (2M×8-Bit) DRAMs in TSOP, or SOJ
- **TM4EP64DxN** — Uses 16 16M-Bit (2M×8-Bit) DRAMs in TSOP, or SOJ
- **TM4EP72DxN** — Uses 18 16M-Bit (2M×8-Bit) DRAMs in TSOP, or SOJ
- **Performance ranges**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **High-Speed, Low-Noise LVTTTL Interface**
- **Long Refresh Period: 32 ms (2 048 Cycles)**
- **3-State Output**
- **Extended-Data-Out (EDO) Operation With CAS-Before-RAS (CBR), RAS-Only, and Hidden Refresh**
- **Serial Presence Detect (SPD) Using EEPROM**
- **Ambient Air Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**

	ACCESS TIME t _{RAC} MAX	ACCESS TIME t _{CAC} MAX	ACCESS TIME t _{AA} MAX	EDO CYCLE t _{HPC} MIN
'xEPxxDxN-50	50 ns	13 ns	25 ns	20 ns
'xEPxxDxN-60	60 ns	15 ns	30 ns	25 ns
'xEPxxDxN-70	70 ns	18 ns	35 ns	30 ns

description

The TM2EP64DPN is a 16M-byte, 168-pin, dual-in-line memory module (DIMM). The DIMM is composed of eight TMS427809A, 2097152 byte × 8-bit 2K-refresh EDO DRAMs, each in a 400-mil, 28-pin plastic TSOP (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS887). The TM2EP64DJN is available with an SOJ package (DZ suffix).

The TM2EP72DPN is a 16M-byte, 168-pin DIMM. The DIMM is composed of nine TMS427809A, 2097152 byte × 8-bit 2K-refresh EDO DRAMs, mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS887). The TM2EP72DJN is available with an SOJ package (DZ suffix).

The TM4EP64DPN is a 32M-byte, 168-pin, dual-in-line memory module (DIMM). The DIMM is composed of sixteen TMS427809A, 2097152 × 8-bit 2K-refresh EDO DRAMs, mounted on a substrate with decoupling capacitors. The TM4EP64DJN is available with an SOJ package (DZ suffix).

The TM4EP72DPN is a 32M-byte, 168-pin DIMM. The DIMM is composed of 18 TMS427809A, 2097152 × 8-bit 2K-refresh EDO DRAMs, mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS887). The TM4EP72DJN is available with an SOJ package (DZ suffix).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES

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operation

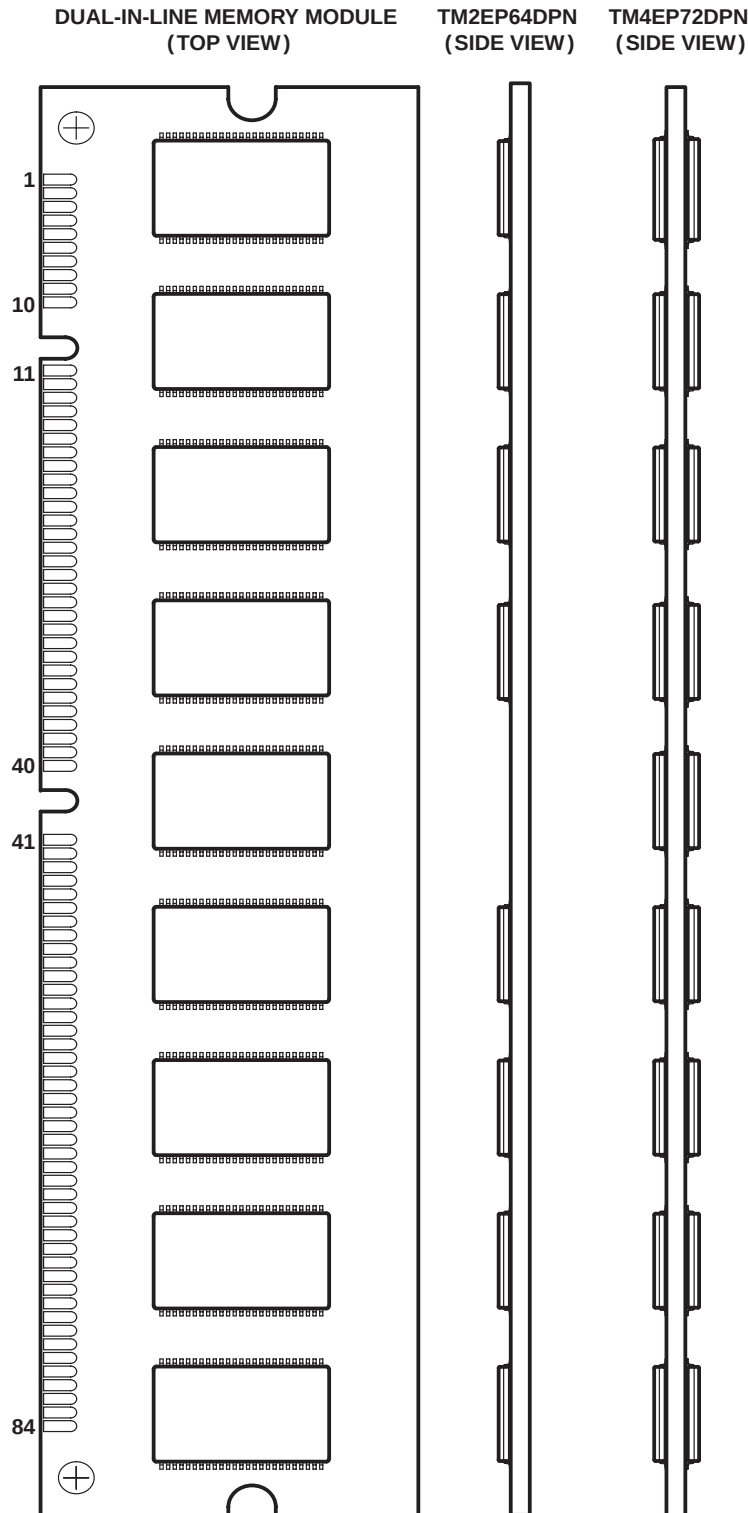
The TMxEPxxDxN DIMMs operate as displayed in Table 1.

Table 1. TMxEPxxDxN DIMM Device Table

DIMM	DEVICE AND QUANTITY ()	Connected as shown in the functional block diagram.
TM2EP64DxN	TMS427809A (8)	
TM2EP72DxN	TMS427809A (9)	
TM4EP64DxN	TMS427809A (16)	
TM4EP72DxN	TMS427809A (18)	

TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN EXTENDED-DATA-OUT DYNAMIC RAM MODULES

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PIN NOMENCLATURE

A[0:10]	Row Address Inputs
A[0:9]	Column Address Inputs
DQ[0:63]	Data In/Data Out
CB[0:7]	Check-Bit In/Check-Bit Out
CAS[0:7]	Column-Address Strobe
RAS[0:3]	Row-Address Strobe
WE0 and WE2	Write Enable
OE0 and OE2	Output Enable
SA[0:2]	Serial Presence Detect (SPD)
SDA	SPD Address/Data
SCL	SPD Clock
NC	No-Connect Pin
V _{DD}	3.3-V Supply
V _{SS}	Ground



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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Pin Assignments

NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME	NO.	PIN NAME
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	$\overline{\text{OE}}2$	86	DQ32	128	NC
3	DQ1	45	$\overline{\text{RAS}}2$	87	DQ33	129	$\overline{\text{RAS}}3$
4	DQ2	46	$\overline{\text{CAS}}2$	88	DQ34	130	$\overline{\text{CAS}}6$
5	DQ3	47	$\overline{\text{CAS}}3$	89	DQ35	131	$\overline{\text{CAS}}7$
6	V _{DD}	48	$\overline{\text{WE}}2$	90	V _{DD}	132	NC
7	DQ4	49	V _{DD}	91	DQ36	133	V _{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{DD}	101	DQ45	143	V _{DD}
18	V _{DD}	60	DQ20	102	V _{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	V _{SS}	106	CB5	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V _{DD}	68	V _{SS}	110	V _{DD}	152	V _{SS}
27	$\overline{\text{WE}}0$	69	DQ24	111	NC	153	DQ56
28	$\overline{\text{CAS}}0$	70	DQ25	112	$\overline{\text{CAS}}4$	154	DQ57
29	$\overline{\text{CAS}}1$	71	DQ26	113	$\overline{\text{CAS}}5$	155	DQ58
30	$\overline{\text{RAS}}0$	72	DQ27	114	$\overline{\text{RAS}}1$	156	DQ59
31	$\overline{\text{OE}}0$	73	V _{DD}	115	NC	157	V _{DD}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V _{DD}	82	SDA	124	V _{DD}	166	SA1
41	V _{DD}	83	SCL	125	NC	167	SA2
42	NC	84	V _{DD}	126	NC	168	V _{DD}



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dual-in-line memory module and components

The dual-in-line memory module and components include:

- PC substrate: $1,27 \pm 0,1$ mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

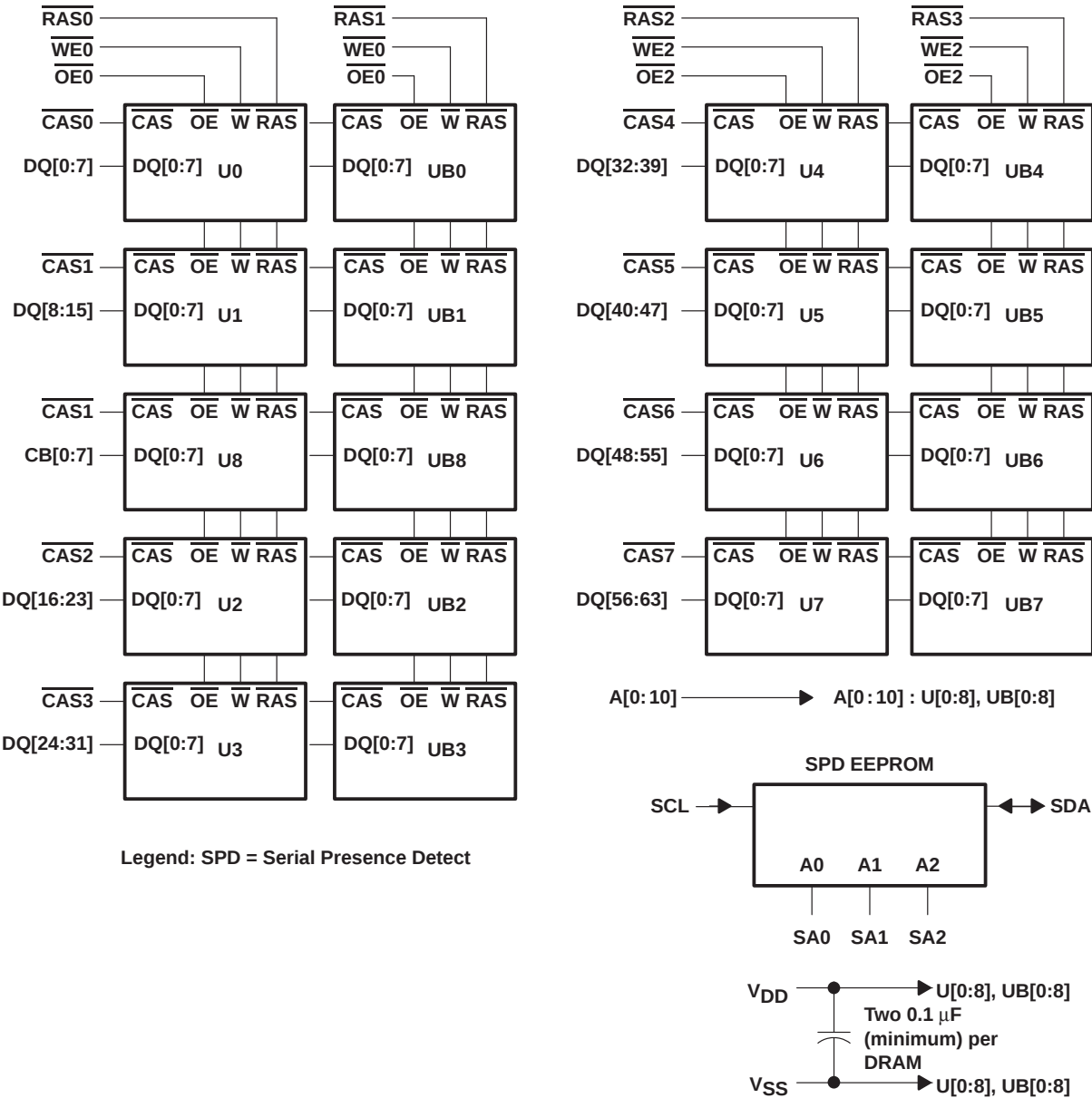
TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN EXTENDED-DATA-OUT DYNAMIC RAM MODULES

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functional block diagram

The following table shows the four DIMM modules and locations (Ux/UBx) that are used.

COMPONENT TABLE	
MODULE	LOCATIONS USED
TM2EP64DxN	U[0:7]
TM2EP72DxN	U[0:8]
TM4EP64DxN	U[0:7], UB[0:7]
TM4EP72DxN	U[0:8], UB[0:8]



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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absolute maximum ratings over ambient temperature range (unless otherwise noted)[†]

Supply voltage range, V_{DD}	–0.5 V to 4.6 V
Voltage range on any pin (see Note 1)	– 0.5 V to 4.6 V
Short-circuit output current	50 mA
Power dissipation: TM2EP64DxN	8 W
TM2EP72DxN	9 W
TM4EP64DxN	16 W
TM4EP72DxN	18 W
Ambient temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 125°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		$V_{DD} + 0.3$	V
V_{IH-SPD}	High-level input voltage for the SPD device	2		5.5	V
V_{IL}	Low-level input voltage	–0.3		0.8	V
T_A	Ambient temperature	0		70	°C

capacitance over recommended ranges of supply voltage and ambient temperature, $f = 1$ MHz (see Note 2)

PARAMETER		'2EP64DxN		'2EP72DxN		'4EP64DxN		'4EP72DxN		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0–A10		42		47		82		92	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}x$		30		37		58		72	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}x$		9		16		16		30	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}x$		30		37		30		37	pF
$C_{i(W)}$	Input capacitance, $\overline{WE}x$		30		37		38		37	pF
C_o	Output capacitance		9		9		16		16	pF
$C_{i/o(SDA)}$	Input/output capacitance, SDA input		9		9		9		9	pF
$C_{i(SPD)}$	Input capacitance, SA0,SA1,SA2,SCL inputs		7		7		7		7	pF

NOTE 2: $V_{DD} = \text{NOM supply voltage} \pm 10\%$, and the bias on pins under test is 0 V.



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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**electrical characteristics over recommended ranges of supply voltage and ambient temperature
(unless otherwise noted)**

TM2EP64DxN

PARAMETER		TEST CONDITIONS†		'2EP64DxN-50		'2EP64DxN-60		'2EP64DxN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	High-level output voltage	I _{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I _{OH} = – 100 µA	LVC MOS	V _{DD} – 0.2		V _{DD} – 0.2		V _{DD} – 0.2		
V _{OL}	Low-level output voltage	I _{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I _{OL} = 100 µA	LVC MOS		0.2		0.2		0.2	
I _I	Input current (leakage)	V _{DD} = 3.6 V, V _I = 0 V to 3.9 V, All others = 0 V to V _{DD}			± 10		± 10		± 10	µA
I _O	Output current (leakage)	V _{DD} = 3.6 V, V _O = 0 V to V _{DD} , CASx high			± 10		± 10		± 10	µA
I _{CC1} ‡§	Read- or write-cycle current	V _{DD} = 3.6 V, Minimum cycle			960		800		720	mA
I _{CC2}	Standby current	V _{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high			16		16		16	mA
		V _{IH} = V _{DD} – 0.2 V (LVC MOS), After one memory cycle, RASx and CASx high			8		8		8	mA
I _{CC3} ‡§	Average refresh current (RAS-only refresh or CBR)	V _{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RASx low after CASx low (CBR)			960		800		720	mA
I _{CC4} ‡¶	Average EDO current	V _{DD} = 3.6 V, t _{HPC} = MIN, RASx low, CASx cycling			880		720		640	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RASx}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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**electrical characteristics over recommended ranges of supply voltage and ambient temperature
(unless otherwise noted) (continued)**

TM2EP72DxN

PARAMETER	TEST CONDITIONS†	'2EP72DxN-50		'2EP72DxN-60		'2EP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = – 2 mA LVTTL	2.4		2.4		2.4		V
	I _{OH} = – 100 µA LVCMOS	V _{DD} – 0.2		V _{DD} – 0.2		V _{DD} – 0.2		
V _{OL} Low-level output voltage	I _{OL} = 2 mA LVTTL		0.4		0.4		0.4	V
	I _{OL} = 100 µA LVCMOS		0.2		0.2		0.2	
I _I Input current (leakage)	V _{DD} = 3.6 V, V _I = 0 V to 3.9 V, All others = 0 V to V _{DD}		± 10		± 10		± 10	µA
I _O Output current (leakage)	V _{DD} = 3.6 V, V _O = 0 V to V _{DD} , CASx high		± 10		± 10		± 10	µA
I _{CC1} ‡§	Read- or write-cycle current V _{DD} = 3.6 V, Minimum cycle		976		816		736	mA
I _{CC2} Standby current	V _{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high		18		18		18	mA
	V _{IH} = V _{DD} – 0.2 V (LVCMOS), After one memory cycle, RASx and CASx high		9		9		9	mA
I _{CC3} ‡§	Average refresh current (RASx-only refresh or CBR) V _{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RASx low after CASx low (CBR)		976		816		736	mA
I _{CC4} ‡¶	Average EDO current V _{DD} = 3.6 V, t _{HPC} = MIN, RASx low, CASx cycling		990		810		720	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RASx}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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**electrical characteristics over recommended ranges of supply voltage and ambient temperature
(unless otherwise noted) (continued)**

TM4EP64DxN

PARAMETER	TEST CONDITIONS†		'4EP64DxN-50		'4EP64DxN-60		'4EP64DxN-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
	I _{OH} = – 100 µA	LVC MOS	V _{DD} – 0.2		V _{DD} – 0.2		V _{DD} – 0.2		
V _{OL} Low-level output voltage	I _{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
	I _{OL} = 100 µA	LVC MOS		0.2		0.2		0.2	
I _I Input current (leakage)	V _{DD} = 3.6 V, V _I = 0 V to 3.9 V, All others = 0 V to V _{DD}			± 20		± 20		± 20	µA
I _O Output current (leakage)	V _{DD} = 3.6 V, V _O = 0 V to V _{DD} , CASx high			± 20		± 20		± 20	µA
I _{CC1} ‡§ Read- or write-cycle current	V _{DD} = 3.6 V, Minimum cycle			976		816		736	mA
I _{CC2} Standby current	V _{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high			32		32		32	mA
	V _{IH} = V _{DD} – 0.2 V (LVC MOS), After one memory cycle, RASx and CASx high			16		16		16	mA
I _{CC3} ‡§ Average refresh current (RASx-only refresh or CBR)	V _{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RASx low after CASx low (CBR)			976		816		736	mA
I _{CC4} ‡¶ Average EDO current	V _{DD} = 3.6 V, t _{HPC} = MIN, RASx low, CASx cycling			896		736		656	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RASx}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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**electrical characteristics over recommended ranges of supply voltage and ambient temperature
(unless otherwise noted) (continued)**

TM4EP72DxN

PARAMETER	TEST CONDITIONS†	'4EP72DxN-50		'4EP72DxN-60		'4EP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = – 2 mA LVTTL	2.4		2.4		2.4		V
	I _{OH} = – 100 µA LVCMOS	V _{DD} – 0.2		V _{DD} – 0.2		V _{DD} – 0.2		
V _{OL} Low-level output voltage	I _{OL} = 2 mA LVTTL		0.4		0.4		0.4	V
	I _{OL} = 100 µA LVCMOS		0.2		0.2		0.2	
I _I Input current (leakage)	V _{DD} = 3.6 V, V _I = 0 V to 3.9 V, All others = 0 V to V _{DD}		± 20		± 20		± 20	µA
I _O Output current (leakage)	V _{DD} = 3.6 V, V _O = 0 V to V _{DD} , CASx high		± 20		± 20		± 20	µA
I _{CC1} ‡§	Read- or write-cycle current V _{DD} = 3.6 V, Minimum cycle		1098		918		828	mA
I _{CC2} Standby current	V _{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high		36		36		36	mA
	V _{IH} = V _{DD} – 0.2 V (LVCMOS), After one memory cycle, RASx and CASx high		18		18		18	mA
I _{CC3} ‡§	Average refresh current (RASx-only refresh or CBR) V _{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RASx low after CASx low (CBR)		1098		918		828	mA
I _{CC4} ‡¶	Average EDO current V _{DD} = 3.6 V, t _{HPC} = MIN, RASx low, CASx cycling		1008		828		738	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RASx}} = V_{IL}$

¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}



TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN EXTENDED-DATA-OUT DYNAMIC RAM MODULES

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switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 3)

PARAMETER	'xEP64DxN-50 'xEP72DxN-50		'xEP64DxN-60 'xEP72DxN-60		'xEP64DxN-70 'xEP72DxN-70		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{AA} Access time from column address (see Note 4)		25		30		35	ns
t _{CAC} Access time from $\overline{\text{CASx}}$ (see Note 4)		13		15		18	ns
t _{CPA} Access time from $\overline{\text{CASx}}$ precharge (see Note 4)		28		35		40	ns
t _{RAC} Access time from $\overline{\text{RASx}}$ (see Note 4)		50		60		70	ns
t _{OEa} Access time from $\overline{\text{OEx}}$ (see Note 4)		13		15		18	ns
t _{CLZ} Delay time, $\overline{\text{CASx}}$ to output in low impedance	0		0		0		ns
t _{REZ} Output buffer turn off delay from $\overline{\text{RASx}}$ (see Note 5)	3	13	3	15	3	18	ns
t _{CEZ} Output buffer turn off delay from $\overline{\text{CASx}}$ (see Note 5)	3	13	3	15	3	18	ns
t _{OEZ} Output buffer turn off delay from $\overline{\text{OEx}}$ (see Note 5)	3	13	3	15	3	18	ns
t _{WEZ} Output buffer turn off delay from $\overline{\text{WEx}}$ (see Note 5)	3	13	3	15	3	18	ns

NOTES: 3. With ac parameters, it is assumed that $t_T = 2$ ns.

4. Access times are measured with output reference levels of $V_{OH} = 2$ V and $V_{OL} = 0.8$ V.

5. The maximum values of t_{REZ}, t_{CEZ}, t_{OEZ}, and t_{WEZ} are specified when the outputs are no longer driven. Data-in should not be driven until one of the applicable maximum values is satisfied.

EDO timing requirements (see Note 3)

	'xEP64DxN-50 'xEP72DxN-50		'xEP64DxN-60 'xEP72DxN-60		'xEP64DxN-70 'xEP72DxN-70		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{HPC} Cycle time, EDO page mode, read-write	20		25		30		ns
t _{PRWC} Cycle time, EDO read-write	57		68		78		ns
t _{CSH} Delay time, $\overline{\text{RASx}}$ active to $\overline{\text{CASx}}$ precharge	40		48		58		ns
t _{CHO} Hold time, $\overline{\text{OEx}}$ from $\overline{\text{CASx}}$	7		10		10		ns
t _{DOH} Hold time, output from $\overline{\text{CASx}}$	5		5		5		ns
t _{OEP} Precharge time, $\overline{\text{OEx}}$	5		5		5		ns
t _{CAS} Pulse duration, $\overline{\text{CASx}}$ active	8	10 000	10	10 000	12	10 000	ns
t _{WPE} Pulse duration, $\overline{\text{WEx}}$ active (output disable only)	7		7		7		ns
t _{CP} Pulse duration, $\overline{\text{CASx}}$ precharge	8		10		10		ns
t _{OCH} Setup time, $\overline{\text{OEx}}$ before $\overline{\text{CASx}}$	8		10		10		ns
t _{OEP} Precharge time, $\overline{\text{OEx}}$	5		5		5		ns

NOTE 3: With ac parameters, it is assumed that $t_T = 2$ ns.



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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ac timing requirements

		'xEP64DxN-50 'xEP72DxN-50		'xEP64DxN-60 'xEP72DxN-60		'xEP64DxN-70 'xEP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Cycle time, random read or write	84		104		124		ns
t _{RWC}	Cycle time, read-write	111		135		160		ns
t _{RASP}	Pulse duration, $\overline{\text{RASx}}$ active, fast page mode (see Note 6)	50	100 000	60	100 000	70	100 000	ns
t _{RAS}	Pulse duration, $\overline{\text{RASx}}$ active, non-page mode (see Note 6)	50	10 000	60	10 000	70	10 000	ns
t _{RP}	Pulse duration, $\overline{\text{RASx}}$ precharge	30		40		50		ns
t _{WP}	Pulse duration, write command	8		10		10		ns
t _{RASS}	Pulse duration, $\overline{\text{RASx}}$ active, self refresh (see Note 7)	100		100		100		μs
t _{RPS}	Pulse duration, $\overline{\text{RASx}}$ precharge after self refresh	90		110		130		ns
t _{ASC}	Setup time, column address	0		0		0		ns
t _{ASR}	Setup time, row address	0		0		0		ns
t _{DS}	Setup time, data in (see Note 8)	0		0		0		ns
t _{RCS}	Setup time, read command	0		0		0		ns
t _{CWL}	Setup time, write command before $\overline{\text{CASx}}$ precharge	8		10		12		ns
t _{RWL}	Setup time, write command before $\overline{\text{RASx}}$ precharge	8		10		12		ns
t _{WCS}	Setup time, write command before $\overline{\text{CASx}}$ active (early-write only)	0		0		0		ns
t _{WRP}	Setup time, $\overline{\text{WEx}}$ high before $\overline{\text{RASx}}$ low (CBR refresh only)	10		10		10		ns
t _{CSR}	Setup time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RASx}}$ (CBR refresh only)	5		5		5		ns
t _{CAH}	Hold time, column address	8		10		12		ns
t _{DH}	Hold time, data in (see Note 8)	8		10		12		ns
t _{RAH}	Hold time, row address	8		10		10		ns
t _{RCH}	Hold time, read command referenced to $\overline{\text{CASx}}$ (see Note 9)	0		0		0		ns
t _{RRH}	Hold time, read command referenced to $\overline{\text{RASx}}$ (see Note 9)	0		0		0		ns
t _{WCH}	Hold time, write command during $\overline{\text{CASx}}$ active (early-write only)	8		10		12		ns
t _{ROH}	Hold time, $\overline{\text{RASx}}$ referenced to $\overline{\text{OEx}}$	8		10		10		ns
t _{WRH}	Hold time, $\overline{\text{WEx}}$ high after $\overline{\text{RASx}}$ low (CBR refresh only)	10		10		10		ns
t _{CHR}	Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RASx}}$ (CBR refresh only)	10		10		10		ns
t _{OEH}	Hold time, $\overline{\text{OEx}}$ command	13		15		18		ns
t _{RHCP}	Hold time, $\overline{\text{RASx}}$ active from $\overline{\text{CASx}}$ precharge	28		35		40		ns
t _{CHS}	Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RASx}}$ (self refresh only)	– 50		– 50		– 50		ns
t _{AWD}	Delay time, column address to write command (read-write only)	42		49		57		ns
t _{CRP}	Delay time, $\overline{\text{CASx}}$ precharge to $\overline{\text{RASx}}$	5		5		5		ns

- NOTES: 6. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
7. During the period of $10\ \mu\text{s} \leq t_{\text{RASS}} \leq 100\ \mu\text{s}$, the device is in a transition state from normal-operation mode to self-refresh mode.
8. Referenced to the later of $\overline{\text{CASx}}$ or $\overline{\text{WEx}}$ in write operations
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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ac timing requirements (continued)

		'xEP64DxN-50 'xEP72DxN-50		'xEP64DxN-60 'xEP72DxN-60		'xEP64DxN-70 'xEP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{CWD}	Delay time, $\overline{\text{CASx}}$ to write command (read-write only)	30		34		40		ns
t _{OED}	Delay time, $\overline{\text{OEx}}$ to data in	13		15		18		ns
t _{RAD}	Delay time, $\overline{\text{RASx}}$ to column address (see Note 10)	10	25	12	30	12	35	ns
t _{RAL}	Delay time, column address to $\overline{\text{RASx}}$ precharge	25		30		35		ns
t _{CAL}	Delay time, column address to $\overline{\text{CASx}}$ precharge	18		20		25		ns
t _{RCD}	Delay time, $\overline{\text{RASx}}$ to $\overline{\text{CASx}}$ (see Note 10)	12	37	14	45	14	52	ns
t _{RPC}	Delay time, $\overline{\text{RASx}}$ precharge to $\overline{\text{CASx}}$	5		5		5		ns
t _{RSH}	Delay time, $\overline{\text{CASx}}$ active to $\overline{\text{RASx}}$ precharge	8		10		12		ns
t _{RWD}	Delay time, $\overline{\text{RASx}}$ to write command (read-write only)	67		79		92		ns
t _{CPW}	Delay time, $\overline{\text{CASx}}$ precharge to write command (read-write only)	45		54		62		ns
t _{REF}	Refresh time interval		32		32		32	ms
t _T	Transition time	2	30	2	30	2	30	ns

NOTE 10: The maximum value is specified only to ensure access time.



TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN EXTENDED-DATA-OUT DYNAMIC RAM MODULES

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serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, DRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments module comply with the current JEDEC SPD Standard. Please see the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 2 – TM2EP64DxN

Table 3 – TM2EP72DxN

Table 4 – TM4EP64DxN

Table 5 – TM4EP72DxN

Table 2. Serial Presence Detect Data for the TM2EP64DxN

BYTE NO.	FUNCTION DESCRIBED	'2EP64DxN-50		'2EP64DxN-60		'2EP64DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$ access time of module	$t_{\text{RAC}} = 50 \text{ ns}$	32h	$t_{\text{RAC}} = 60 \text{ ns}$	3Ch	$t_{\text{RAC}} = 70 \text{ ns}$	46h
10	$\overline{\text{CAS}}$ access time of module	$t_{\text{CAC}} = 13 \text{ ns}$	0Dh	$t_{\text{CAC}} = 15 \text{ ns}$	0Fh	$t_{\text{CAC}} = 18 \text{ ns}$	12h
11	DIMM configuration type (non-parity, parity, ECC)	Non-Parity	00h	Non-Parity	00h	Non-Parity	00h
12	Refresh rate/type	15.6 μs	00h	15.6 μs	00h	15.6 μs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	41	29h	53	35h	66	42h
64–71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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serial presence detect (continued)

Table 2. Serial Presence Detect Data for the TM2EP64DxN (Continued)

BYTE NO.	FUNCTION DESCRIBED	'2EP64DxN-50		'2EP64DxN-60		'2EP64DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
72	Manufacturing location [†]	TBD		TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD		TBD	
91	Die revision code [†]	TBD		TBD		TBD	
92	PCB revision code [†]	TBD		TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD		TBD	
167–255	Open						

[†] TBD indicates values are determined at manufacturing time and are module dependent.

[‡] These TBD values are determined and programmed by the customer (optional).



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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serial presence detect (continued)

Table 3. Serial Presence Detect Data for the TM2EP72DxN

BYTE NO.	FUNCTION DESCRIBED	'2EP72DxN-50		'2EP72DxN-60		'2EP72DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	72 bits	48h	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$ access time of module	$t_{\text{RAC}} = 50 \text{ ns}$	32h	$t_{\text{RAC}} = 60 \text{ ns}$	3Ch	$t_{\text{RAC}} = 70 \text{ ns}$	46h
10	$\overline{\text{CAS}}$ access time of module	$t_{\text{CAC}} = 13 \text{ ns}$	0Dh	$t_{\text{CAC}} = 15 \text{ ns}$	0Fh	$t_{\text{CAC}} = 18 \text{ ns}$	12h
11	DIMM configuration type (non-parity, parity, ECC)	ECC	02h	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 μs	00h	15.6 μs	00h	15.6 μs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h	x8	08h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	59	3Bh	71	47h	84	54h
64–71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD		TBD	
91	Die revision code [†]	TBD		TBD		TBD	
92	PCB revision code [†]	TBD		TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD		TBD	
167–255	Open						

[†] TBD indicates values are determined at manufacturing time and are module dependent.

[‡] These TBD values are determined and programmed by the customer (optional).



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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serial presence detect (continued)

Table 4. Serial Presence Detect Data for the TM4EP64DxN

BYTE NO.	FUNCTION DESCRIBED	'4EP64DxN-50		'4EP64DxN-60		'4EP64DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RASx}}$ access time of module	$t_{\text{RAC}} = 50 \text{ ns}$	32h	$t_{\text{RAC}} = 60 \text{ ns}$	3Ch	$t_{\text{RAC}} = 70 \text{ ns}$	46h
10	$\overline{\text{CASx}}$ access time of module	$t_{\text{CAC}} = 13 \text{ ns}$	0Dh	$t_{\text{CAC}} = 15 \text{ ns}$	0Fh	$t_{\text{CAC}} = 18 \text{ ns}$	12h
11	DIMM configuration type (non-parity, parity, ECC)	Non-Parity	00h	Non-Parity	00h	Non-Parity	00h
12	Refresh rate/type	15.6 μs	00h	15.6 μs	00h	15.6 μs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	42	2Ah	54	36h	67	43h
64–71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD		TBD	
91	Die revision code [†]	TBD		TBD		TBD	
92	PCB revision code [†]	TBD		TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD		TBD	
167–255	Open						

[†] TBD indicates values are determined at manufacturing time and are module dependent.

[‡] These TBD values are determined and programmed by the customer (optional).



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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serial presence detect (continued)

Table 5. Serial Presence Detect for the TM4EP72DxN

BYTE NO.	FUNCTION DESCRIBED	'4EP72DxN-50		'4EP72DxN-60		'4EP72DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	72 bits	48h	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$ access time of module	$t_{\text{RAC}} = 50 \text{ ns}$	32h	$t_{\text{RAC}} = 60 \text{ ns}$	3Ch	$t_{\text{RAC}} = 70 \text{ ns}$	46h
10	$\overline{\text{CAS}}$ access time of module	$t_{\text{CAC}} = 13 \text{ ns}$	0Dh	$t_{\text{CAC}} = 15 \text{ ns}$	0Fh	$t_{\text{CAC}} = 18 \text{ ns}$	12h
11	DIMM configuration type (non-parity, parity, ECC)	ECC	02h	ECC	02h	ECC	02h
12	Refresh rate/type	15.6 μs	00h	15.6 μs	00h	15.6 μs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h	x8	08h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	60	3Ch	72	48h	85	55h
64–71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location [†]	TBD		TBD		TBD	
73–90	Manufacturer's part number [†]	TBD		TBD		TBD	
91	Die revision code [†]	TBD		TBD		TBD	
92	PCB revision code [†]	TBD		TBD		TBD	
93–94	Manufacturing date [†]	TBD		TBD		TBD	
95–98	Assembly serial number [†]	TBD		TBD		TBD	
99–125	Manufacturer specific data [†]	TBD		TBD		TBD	
126–127	Vendor specific data [†]	TBD		TBD		TBD	
128–166	System integrator's specific data [‡]	TBD		TBD		TBD	
167–255	Open						

[†] TBD indicates values are determined at manufacturing time and are module dependent.

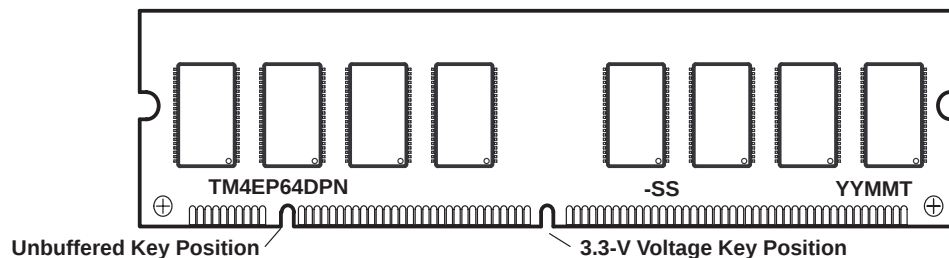
[‡] These TBD values are determined and programmed by the customer (optional).



**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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device symbolization (TM4EP64DPN illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

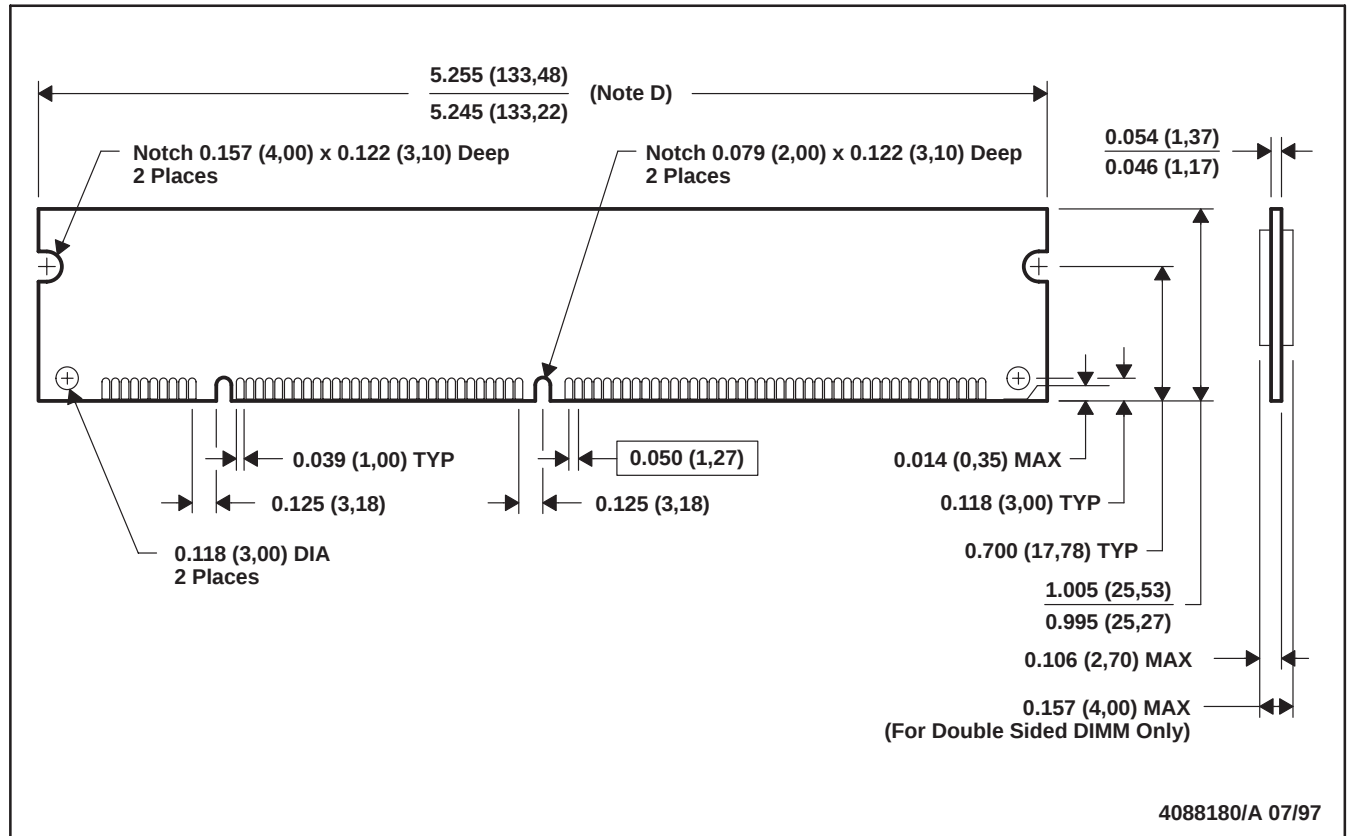
**TM2EP64DPN, TM2EP64DJN, TM4EP64DPN, TM4EP64DJN
TM2EP72DPN, TM2EP72DJN, TM4EP72DPN, TM4EP72DJN
EXTENDED-DATA-OUT DYNAMIC RAM MODULES**

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MECHANICAL DATA

BR (R-PDIM-N168)

DUAL IN-LINE MEMORY MODULE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-161
 - D. Dimension includes de-panelization variations; applies between notch and tab edge.
 - E. Outline may vary above notches to allow router/panelization irregularities.



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