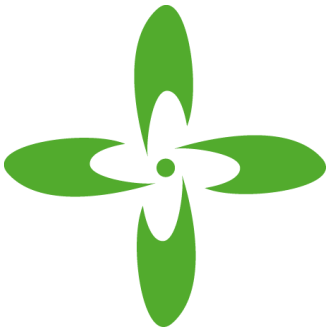

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TM52F0C63

DATA SHEET

Rev 0.93

(Please read the precautions on the second page before use)

PRECAUTIONS

1. The chip cannot enter Halt/Stop mode if the INTn pin is low and the INTn wake-up function is enabled. (INTn=0 and EXn=1, n=0~2)

AMENDMENT HISTORY

Version	Date	Description
V0.90	May, 2022	New Release
V0.91	May, 2022	Added MSOP-10 package
V0.92	Jul, 2022	1. Program Memory 10K erase times at least (p.8) 2. Removed system clock frequency requirement before entering Halt/Stop mode (p.36) 3. Added the description of pin wake-up mechanism (p.44~45) 4. Corrected current value and corresponding conditions (p.10, p.115) 5. Added the description about Halt mode. 6. Mass production writer does not support P2.0/P2.1
V0.93	Nov, 2022	1. IAP programming voltage must be greater than 4V (p.23) 2. EE programming voltage must be greater than 3V (p.118) 3. Modify VBG2.5V to VBG2.54V

CONTENTS

TM52 F8xxx FAMILY

Common Feature

CPU	Flash Program memory	RAM	Timer0~2	UART
Fast 8051 (2T)	4K~32K with IAP, ISP, ICP	256~2048 bytes	8051 Standard	8051 Standard

Family Members Features

P/N	Program Memory	Data Memory	RAM	IO Pin	PWM	SAR ADC	Touch Key	LCD	LED	Interface
TM52-F0C63	Flash 8KB	IAP share with main rom / EEPROM 128B	512B	26	16-bit x7	12-bit 19-ch	–	4com	–	UART*1 MIIC*1
TM52-F8368	Flash 8KB	IAP share with main rom	512B	26	16-bit x7	12-bit 12-ch	–	4com	–	UART*1 MIIC*1
TM52-F8274	Flash 8KB	IAP share with main rom / EEPROM 128B	1024B	26	(8+2)-bit x3	12-bit 14-ch	–	8com	4Cx6S	SPI*1 UART*1 UART2*1
TM52-F8278							16-ch			
TM52-F8273	Flash 16KB	IAP share with main rom / EEPROM 128B	1024B	26	(8+2)-bit x3	12-bit 14-ch	–	8com	4Cx6S	SPI*1 UART*1 UART2*1
TM52-F8276							16-ch			

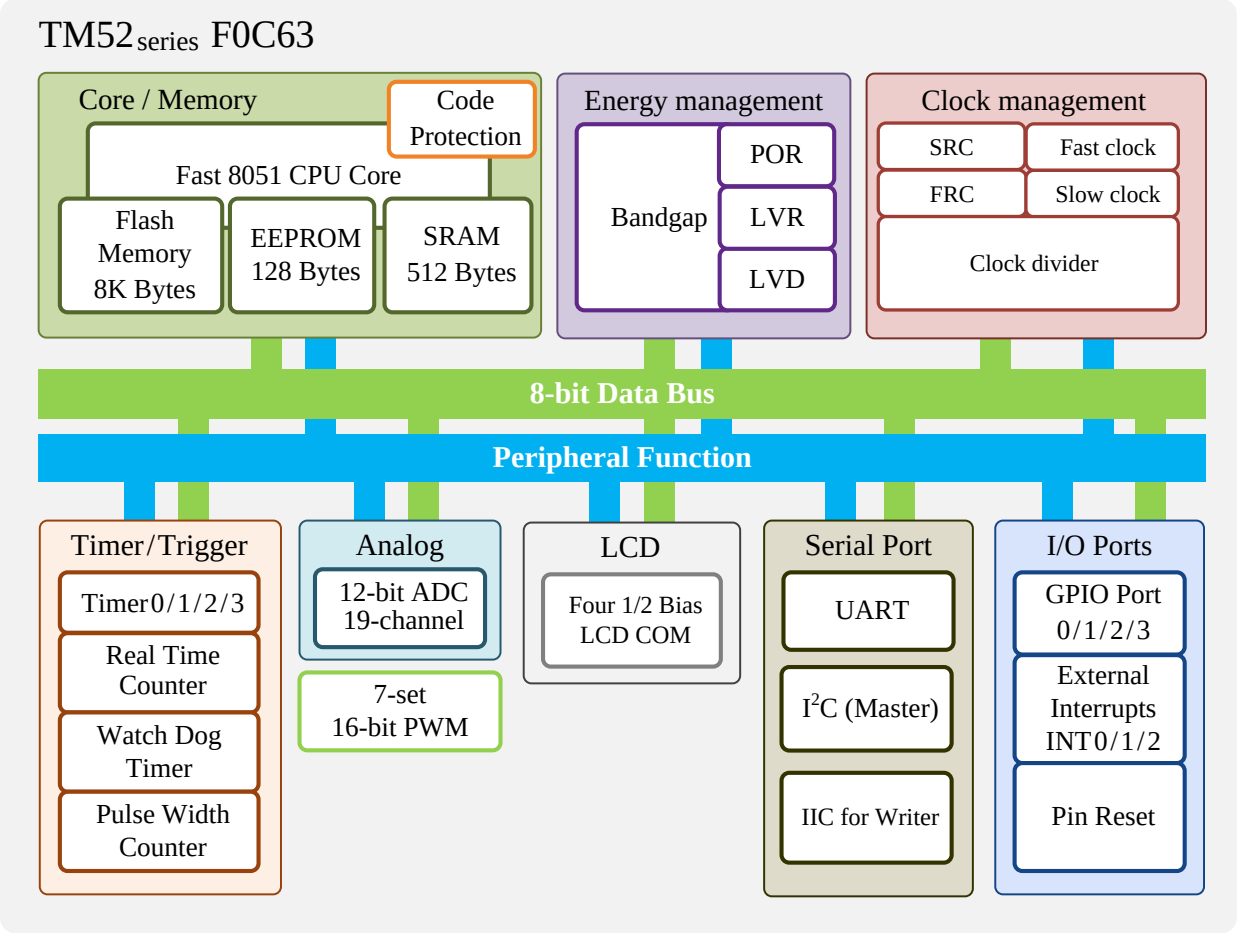
P/N	Operation Voltage	Operation Current @5V					Max. System Clock (Hz)			
		Fast FRC	Slow SRC	Idle SRC	Halt	Stop	Fast FRC	Slow SRC	FXT	FRC
TM52-F0C63	2.2~5.5V	8.3mA	2.6mA	40uA	21uA	0.1uA	–	80K	–	16.588M
TM52-F8368	2.3~5.5V	9.7mA	2.8mA	24uA	–	0.1uA	–	80K	–	16.588M
TM52-F8274	2.3~5.5V	5.3mA	1.3mA	20μA	–	0.1μA	32K	68K	12M	12.902M
TM52-F8278										
TM52-F8273	2.3~5.5V	5.3mA	1.3mA	20μA	–	0.1μA	32K	68K	12M	12.902M
TM52-F8276										

GENERAL DESCRIPTION

TM52 series F0C63 are versions of a new, fast 8051 architecture for an 8-bit microcontroller single chip with an instruction set fully compatible with industry standard 8051, and retains most 8051 peripheral's functional block. Typically, the **TM52** executes instructions six times faster than the standard 8051 architecture.

The **TM52-F0C63** provides improved performance, lower cost and fast time-to-market by integrating features on the chip, including 8K Bytes Flash program memory, 128 Bytes EEPROM, 512 Bytes SRAM, Low Voltage Reset (LVR), Low Voltage Detector (LVD), dual clock power saving operation mode, 8051 standard UART and Timer0/1/2, real time clock Timer3, 7 set 16-bit PWMs, 19 channels 12-bit A/D Convertor, master I^2C interface and Watch Dog Timer. It's a high reliability and low power consumption feature can be widely applied in consumer and home appliance products.

SYSTEM BLOCK DIAGRAM



FEATURES

1. **Standard 8051 Instruction set, fast machine cycle**
   - Executes instructions six times faster than the standard 8051.
2. **Flash Program Memory**
   - 8K Bytes
   - Support “In Circuit Programming” (ICP) or “In System Programming” (ISP) for the Flash code
   - Byte Write “In Application Programming” (IAP) mode is convenient as Data EEPROM access
   - Code Protection Capability
   - 10K erase times at least
   - 10 years data retention at least

*Each IAP address can be programmed more than 10000 times (typical value) .If the customer needs more programming times, a ROM area can be planned to disperse the address written by IAP data. Our company can provide the source code of this usage method.

3. **128 Bytes EEPROM Memory**
   - 30K~50K erase times at least
   - 10 years data retention at least
4. **Total 512 Bytes SRAM (IRAM + XRAM)**
   - 256 Bytes IRAM in the 8051 internal data memory area
   - 256 Bytes XRAM in the 8051 external data memory area (accessed by MOVX Instruction)
5. **Two System Clock type selections**
   - Fast clock from Internal RC (FRC, 16.588 MHz)
   - Slow clock from Internal RC (SRC, 80 KHz)
   - System Clock can be divided by 1/2/4/16 option
6. **8051 Standard Timer – Timer0/1/2**
   - 16-bit Timer0, also supports T0O clock output for Buzzer application
   - 16-bit Timer1, also supports T1O clock output for Buzzer application
   - 16-bit Timer2, also supports T2O clock output for Buzzer application
7. **15-bit Timer3**
   - Clock source is Slow clock
   - Interrupt period can be clock divided by 32768/16384/8192/65536 option
8. **One UART**
   - 8051 standard UART, One Wire UART option can be used for ISP or other application

*Support one UART, pin select to P30/P31 or P02/P16 by TXRXSEL (SFR 93h.7)

9. **Seven "16" bits PWMs with prescaler/ period-adjustment**
10. **One Master I^2C interface (MIIC)**

*Support one MIIC, pin select to P35/P16 by MSDASEL (SFR B7h.7) , pin select to P13/P02 by MSCLSEL (SFR B7h.6)

11. **12-bit ADC with 19 channels External Pin Input and 3 channels Internal Reference Voltage**
    - Internal Reference Voltage (VBG): 1.22V±1.5% @V_{CC}=2.5V~5.5V, 25℃
    - Internal Reference Voltage: V_{SS} (0V)
    - Internal Reference Voltage: V_{CC}/4
    - ADC reference voltage selection option: V_{CC} / 2.54V
12. **LCD Driver**
    - Software controlled COM0~3
    - 1/2 LCD Bias
13. **13 Sources, 4-level priority Interrupt**
    - Timer0/Timer1/Timer2/Timer3 Interrupt
    - INT0/INT1 pin Falling-Edge/Low-Level Interrupt
    - INT2 pin Falling-Edge Interrupt
    - Port0/1/2/3 Pin Change Interrupt
    - UART TX/RX Interrupt
    - ADC Interrupt
    - Master I^2C (MIIC) interrupt
    - LVD Interrupt
    - PWM0/PWM1 interrupt
14. **Pin Interrupt can Wake up CPU from Power-Down (Halt/Stop) mode**
    - INT0~INT2 Interrupt & Wake-up
    - Each Port0/1/2/3 pin can be defined as Interrupt & Wake-up pin (by pin change)
15. **Max. 26 Programmable I/O pins**
    - CMOS Output
    - Pseudo-Open-Drain, or Open-Drain Output
    - Schmitt Trigger Input
    - Pin Pull-up can be Enabled or Disabled
16. **Independent RC Oscillating Watch Dog Timer**
    - 400ms/200ms/100ms/50ms selectable WDT timeout options

17. Five types Reset

- Power on Reset
- Selectable External Pin Reset
- Selectable Watch Dog Reset
- Software Command Reset
- Selectable Low Voltage Reset

18. 16-level Low Voltage Reset

- 2.25V / 2.40V / 2.55V / 2.70V / 2.80V / 2.95V / 3.10V / 3.25V / 3.40V / 3.55V / 3.70V / 3.85V / 4.0V / 4.15V / 4.30V / 4.45V

19. 15-level Low Voltage Detect

- 2.40V / 2.55V / 2.70V / 2.80V / 2.95V / 3.10V / 3.25V / 3.40V / 3.55V / 3.70V / 3.85V / 4.0V / 4.15V / 4.30V / 4.45V

20. Five Power Operation Modes

- Fast/Slow/Idle/Halt/Stop mode

21. Integrated 16-bit Cyclic Redundancy Check function

22. Multiplication and division

- 8 bits Multiplier & Divider (standard 8051)
- 16 bits Multiplier & Divider
- 32 bits ÷ 16 bits Divider

23. On-chip Debug/ICE interface

- Use P3.0/P3.1 pin or P2.0/P2.1 pin
- Share with ICP programming pin
- Mass production writer only supports P3.0/P3.1

24. Operating Voltage and Current

- V_{CC} =2.2V ~ 5.5V @F_{SYS}=16.588 MHz
- I_{CC} =0.1μA @Stop mode, PWRSAV=1, V_{CC}=3V
- I_{CC} =6μA @Halt mode, PWRSAV=1, V_{CC}=3V
- I_{CC} =9μA @Idle mode, PWRSAV=1, LVRPD=0x37, V_{CC}=3V

25. Operating Temperature Range

- –40℃ ~ +105℃

26. Package Types

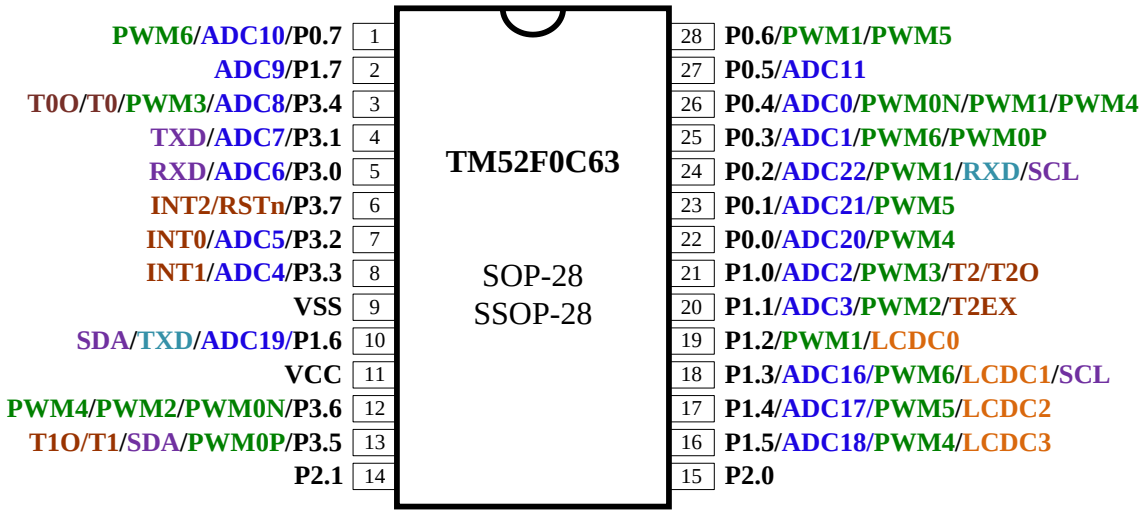
- 10-pin MSOP (118 mil)
- 16-pin SOP (150 mil)
- 20-pin TSSOP (173 mil)
- 20-pin SOP (300 mil)
- 20-pin QFN (3x3x0.75-0.4mm) (L=0.25mm)

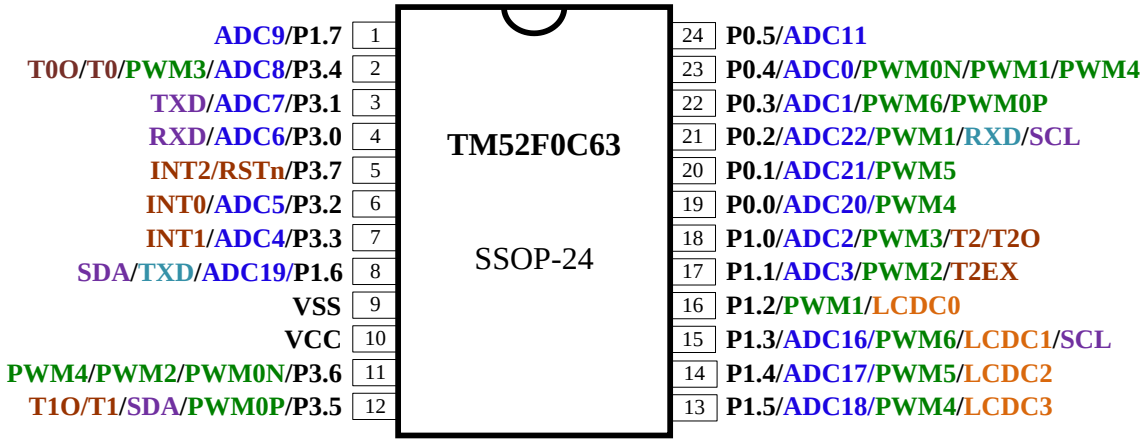
- 24-pin SSOP (150 mil)
- 28-pin SOP (300 mil)
- 28-pin SSOP (150 mil)
- 28-pin QFN (4x4x0.75-0.4mm)

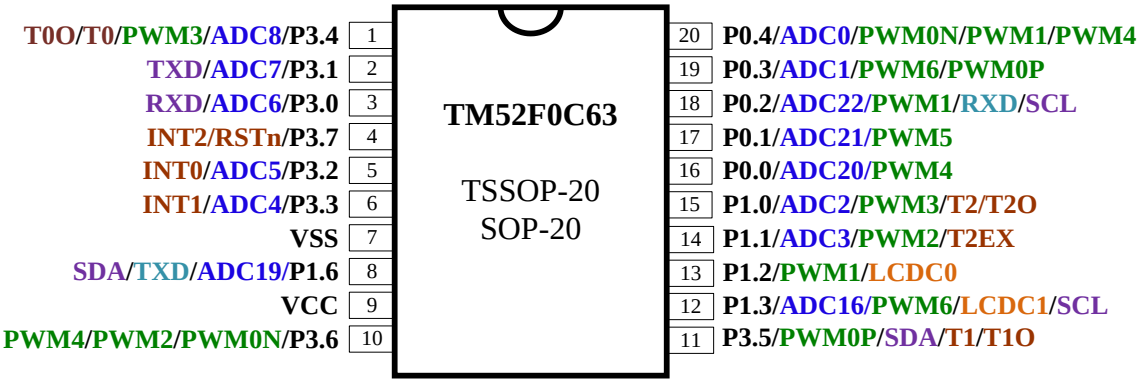
PIN ASSIGNMENT

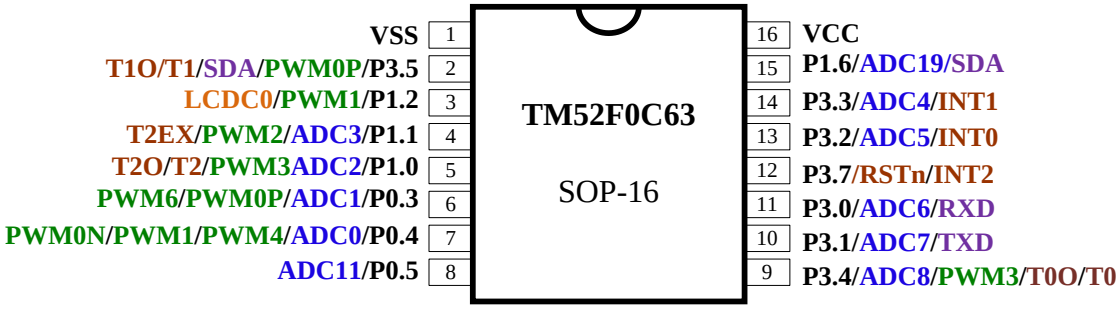
***UART default pin is P30, P31, user can set P02, P16 instead by TXRXSEL (SFR 93h.7)**
***Master I²C SDA default pin is P35, user can set P16 instead by MSDASEL (SFR B7h.7)**
***Master I²C SCL default pin is P13, user can set P02 instead by MSCLSEL (SFR B7h.6)**

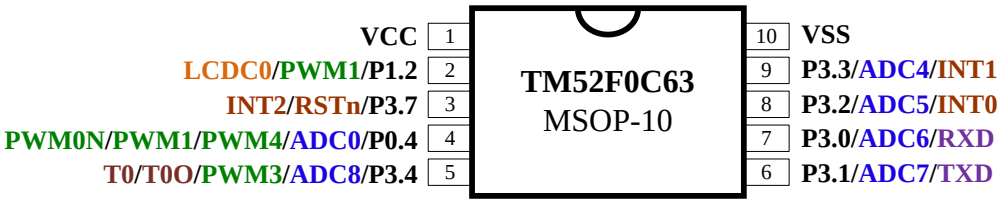
For low power applications, all digital I/Os (including unbonding or unused) should avoid high-impedance settings.

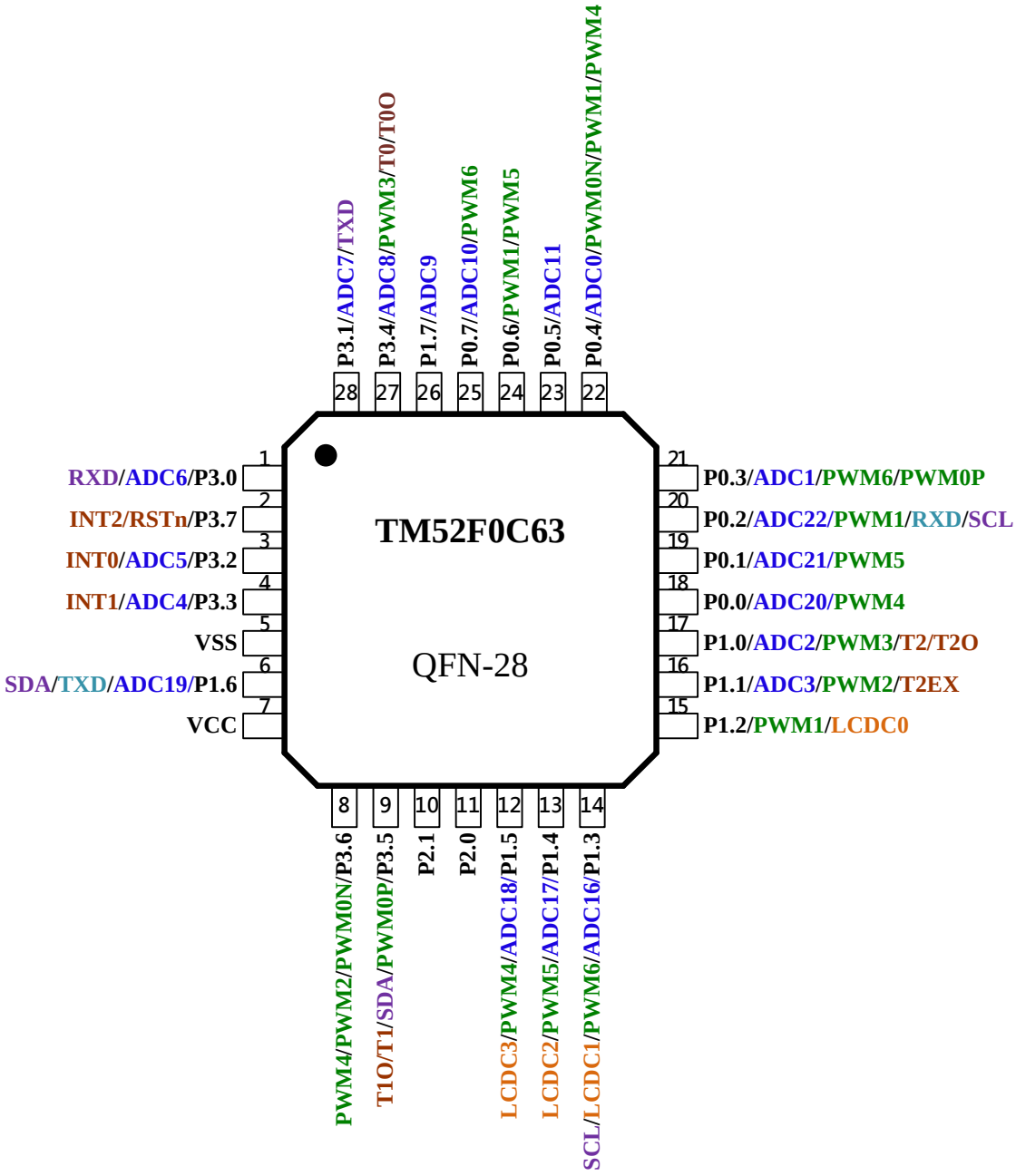


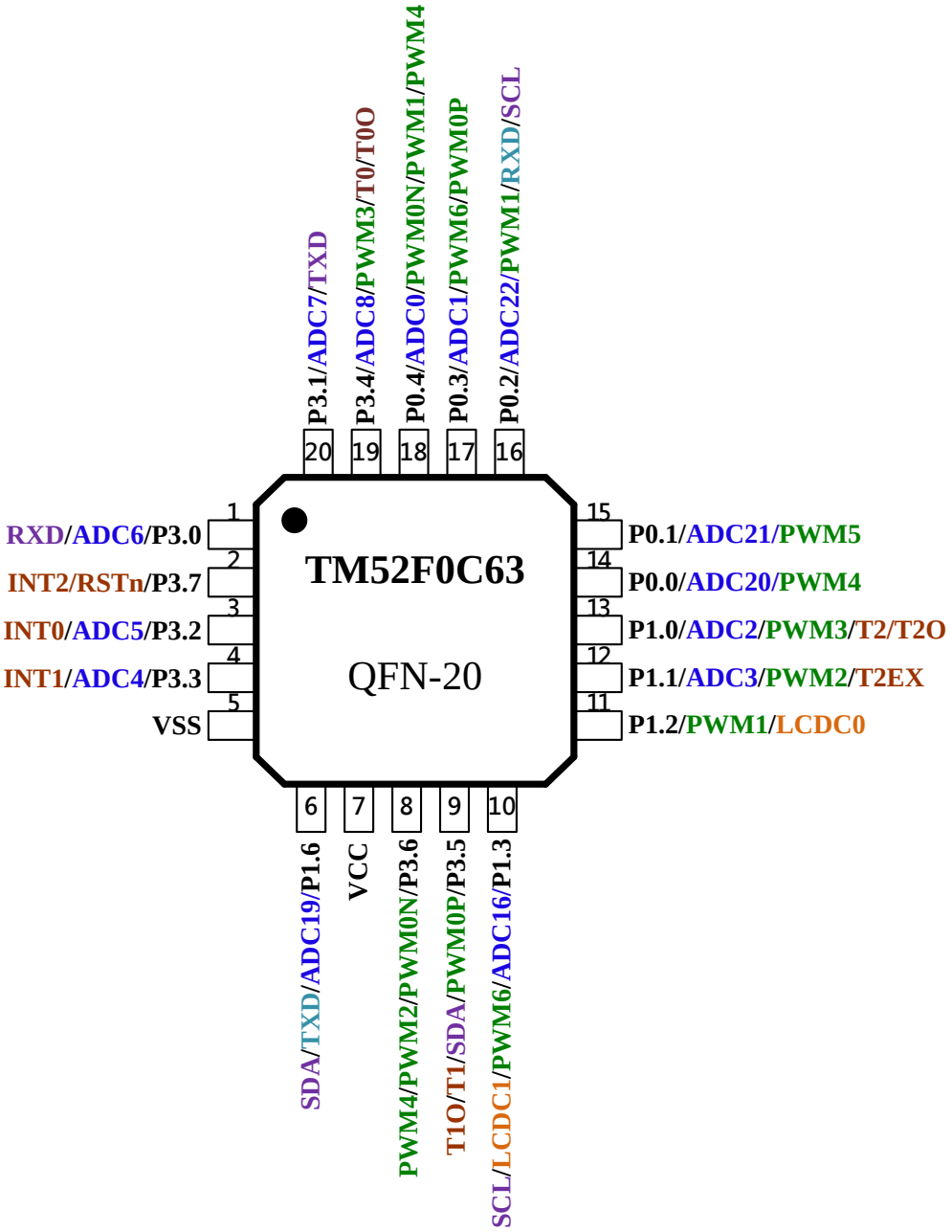



T0O/T0/PWM3/ADC8/P3.4 1
TXD/ADC7/P3.1 2
RXD/ADC6/P3.0 3
INT2/RSTn/P3.7 4
INT0/ADC5/P3.2 5
INT1/ADC4/P3.3 6
VSS 7
SDA/TXD/ADC19/P1.6 8
VCC 9
PWM4/PWM2/PWM0N/P3.6 10
TM52F0C63
TSSOP-20
SOP-20
20 P0.4/ADC0/PWM0N/PWM1/PWM4
19 P0.3/ADC1/PWM6/PWM0P
18 P0.2/ADC22/PWM1/RXD/SCL
17 P0.1/ADC21/PWM5
16 P0.0/ADC20/PWM4
15 P1.0/ADC2/PWM3/T2/T2O
14 P1.1/ADC3/PWM2/T2EX
13 P1.2/PWM1/LCDC0
12 P1.3/ADC16/PWM6/LCDC1/SCL
11 P3.5/PWM0P/SDA/T1/T1O


VSS 1
T1O/T1/SDA/PWM0P/P3.5 2
LCDC0/PWM1/P1.2 3
T2EX/PWM2/ADC3/P1.1 4
T2O/T2/PWM3ADC2/P1.0 5
PWM6/PWM0P/ADC1/P0.3 6
PWM0N/PWM1/PWM4/ADC0/P0.4 7
ADC11/P0.5 8
TM52F0C63
SOP-16
16 VCC
15 P1.6/ADC19/SDA
14 P3.3/ADC4/INT1
13 P3.2/ADC5/INT0
12 P3.7/RSTn/INT2
11 P3.0/ADC6/RXD
10 P3.1/ADC7/TXD
9 P3.4/ADC8/PWM3/T0O/T0


VCC 1
LCDC0/PWM1/P1.2 2
INT2/RSTn/P3.7 3
PWM0N/PWM1/PWM4/ADC0/P0.4 4
T0/T0O/PWM3/ADC8/P3.4 5
TM52F0C63
MSOP-10
10 VSS
9 P3.3/ADC4/INT1
8 P3.2/ADC5/INT0
7 P3.0/ADC6/RXD
6 P3.1/ADC7/TXD


TM52F0C63
QFN-28
1 RXD/ADC6/P3.0
2 INT2/RSTn/P3.7
3 INT0/ADC5/P3.2
4 INT1/ADC4/P3.3
5 VSS
6 SDA/TXD/ADC19/P1.6
7 VCC
8 PWM4/PWM2/PWM0N/P3.6
9 T1O/T1/SDA/PWM0P/P3.5
10 P2.1
11 P2.0
12 LCDC3/PWM4/ADC18/P1.5
13 LCDC2/PWM5/ADC17/P1.4
14 SCL/LCDC1/PWM6/ADC16/P1.3
15 P1.2/PWM1/LCDC0
16 P1.1/ADC3/PWM2/T2EX
17 P1.0/ADC2/PWM3/T2/T2O
18 P0.0/ADC20/PWM4
19 P0.1/ADC21/PWM5
20 P0.2/ADC22/PWM1/RXD/SCL
21 P0.3/ADC1/PWM6/PWM0P
22 P0.4/ADC0/PWM0N/PWM1/PWM4
23 P0.5/ADC11
24 P0.6/PWM1/PWM5
25 P0.7/ADC10/PWM6
26 P1.7/ADC9
27 P3.4/ADC8/PWM3/T0/T0O
28 P3.1/ADC7/TXD


TM52F0C63
QFN-20
1 RXD/ADC6/P3.0
2 INT2/RSTn/P3.7
3 INT0/ADC5/P3.2
4 INT1/ADC4/P3.3
5 VSS
6 SDA/TXD/ADC19/P1.6
7 VCC
8 PWM4/PWM2/PWM0N/P3.6
9 T1O/T1/SDA/PWM0P/P3.5
10 SCL/LCDC1/PWM6/ADC16/P1.3
11 P1.2/PWM1/LCDC0
12 P1.1/ADC3/PWM2/T2EX
13 P1.0/ADC2/PWM3/T2/T2O
14 P0.0/ADC20/PWM4
15 P0.1/ADC21/PWM5
16 P0.2/ADC22/PWM1/RXD/SCL
17 P0.3/ADC1/PWM6/PWM0P
18 P0.4/ADC0/PWM0N/PWM1/PWM4
19 P3.4/ADC8/PWM3/T0/T0O
20 P3.1/ADC7/TXD

PIN DESCRIPTION

Name	In/Out	Pin Description
P0.0~P0.7 P1.0~P1.7 P2.0~P2.1 P3.3~P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software. These pin's level change can interrupt/wake up CPU from Idle/Halt/Stop mode.
P3.0~P3.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "**pseudo open drain**" output. Pull-up resistors are assignable by software. These pin's level change can interrupt/wake up CPU from Idle/Halt/Stop mode.
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Halt/Stop mode wake up input.
INT2	I	External falling edge Interrupt input, Idle/Halt /Stop mode wake up input.
RXD	I/O	UART Mode0 transmit & receive data, Mode1/2/3 receive data
TXD	I/O	UART Mode0 transmit clock, Mode1/2/3 transmit data. In One Wire UART mode, this pin transmits and receives serial data.
T0, T1, T2	I	Timer0, Timer1, Timer2 event count pin input.
T2EX	I	Timer2 external trigger input.
T0O	O	Timer0 overflow divided by 64 output
T1O	O	Timer1 overflow divided by 2 output
T2O	O	Timer2 overflow divided by 2 output
PWM1~PWM6 PWM0P/PWM0N	O	16 bit PWM output
ADC0~ADC11, ADC16~ADC22	I	ADC input
LCDC0~LCDC3	O	LCD 1/2 bias output
SCL	I/O	Master I^2C (MIIC) SCL
SDA	I/O	Master I^2C (MIIC) SDA
RSTn	I	External active low reset input, Pull-up resistor is fixed enable.
VCC, VSS	P	Power input pin and ground

PIN SUMMERY

Pin Number	Pin Name	Type	Input			Output			Alternative Function						MISC
QFN-28			Pull-up Control	Wake up	Ext. Interrupt	CMOS Push-Pull	Pseudo Open Drain	Open Drain	LCD	ADC	UART	PWM	Timer	MIIC	
1	RXD/ADC6/P3.0	I/O	⭘	●		●	●	●		●	●				
2	INT2/RSTn/P3.7	I/O	⭘	●	●	●		●							Reset
3	INT0/ADC5/P3.2	I/O	⭘	●	●	●	●	●		●					
4	INT1/ADC4/P3.3	I/O	⭘	●	●	●		●		●					
5	VSS	P													
6	SDA/TXD/ADC19/P1.6	I/O	⭘	●		●		●		●	●			●	
7	VCC	P													
8	PWM4/PWM2/PWM0N/P3.6	I/O	⭘	●		●		●				●			
9	T1O/T1/SDA/PWM0P/P3.5	I/O	⭘	●		●		●				●	●	●	T1O
10	P2.1	I/O	⭘	●		●		●							
11	P2.0	I/O	⭘	●		●		●							
12	LCDC3/PWM4/ADC18/P1.5	I/O	⭘	●		●		●	●	●		●			
13	LCDC2/PWM5/ADC17/P1.4	I/O	⭘	●		●		●	●	●		●			
14	SCL/LCDC1/PWM6/ADC16/P1.3	I/O	⭘	●		●		●	●	●		●		●	
15	LCDC0/PWM1/P1.2	I/O	⭘	●		●		●	●			●			
16	T2EX/PWM2/ADC3/P1.1	I/O	⭘	●		●		●		●		●	●		
17	T2O/T2/PWM3/ADC2/P1.0	I/O	⭘	●		●		●		●		●	●		T2O
18	PWM4/ADC20/P0.0	I/O	⦿	●		●				●		●			
19	PWM5/ADC21/P0.1	I/O	⦿	●		●				●		●			
20	SCL/RXD/PWM1/ADC22/P0.2	I/O	⦿	●		●				●	●	●		●	
21	PWM0P/PWM6/ADC1/P0.3	I/O	⦿	●		●				●		●			
22	PWM4/PWM1/PWM0N/ADC0/P0.4	I/O	⦿	●		●				●		●			
23	ADC11/P0.5	I/O	⦿	●		●				●					
24	PWM5/PWM1/P0.6	I/O	⦿	●		●						●			
25	PWM6/ADC10/P0.7	I/O	⦿	●		●				●		●			
26	ADC9/P1.7	I/O	⭘	●		●		●		●					
27	/T0O /T0/PWM3/ADC8/P3.4	I/O	⭘	●		●		●		●		●	●		T0O
28	TXD /ADC7/P3.1	I/O	⭘	●		●	●	●		●	●				

PS:

⭘ Port1, P2.0, P2.1, Port3 these pins control Pull up resistor by operation modes

⦿ Port0 control Pull up resistor while P0OE.n=0 and P0.n=1

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The TM52 device features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a program counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as “A” or “ACC” including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR **E0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC:** Accumulator

1.2 B Register (B)

The “B” register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands are in A and B.

ex: DIV AB

When this instruction is executed, data inside A and B are divided, and the answer is stored in A.

SFR **F0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B:** B register

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer.

SFR **81h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP:** Stack Point

1.4 Dual Data Pointer (DPTRs)

TM52 device has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs.

SFR **82h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL:** Data Point low byte

SFR **83h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH:** Data Point high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	VBGEN	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.0 **DPSEL:** Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The instructions that affect the PSW are listed below.

Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR **D0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY:** ALU carry flag

D0h.6 **AC:** ALU auxiliary carry flag

D0h.5 **F0:** General purpose user-definable flag

D0h.4~3 **RS1, RS0:** The contents of (RS1, RS0) enable the working register banks as:

00: Bank 0 (00h~07h)

01: Bank 1 (08h~0Fh)

10: Bank 2 (10h~17h)

11: Bank 3 (18h~1Fh)

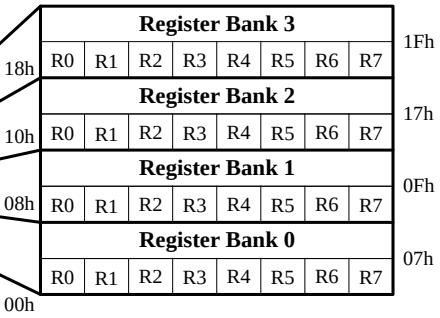
D0h.2 **OV:** ALU overflow flag

D0h.1 **F1:** General purpose user-definable flag

D0h.0 **P:** Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.

PSW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CY	**AC**	**FO**	**RS1**	**RS0**	**OV**	**F1**	**P**

RS1	RS0	Bank
1	1	3
1	0	2
0	1	1
0	0	0



2. Memory

2.1 Program Memory (Support IAP)

The Chip has an 8K Bytes Flash program memory which can support In Circuit Programming (ICP), In Application Programming (IAP) and In System Programming (ISP) function modes. The program memory address continuous space (0000h~1FFFh) is partitioned to several sectors for device operation.

2.1.1 Functional Partition

The last 16 bytes (1FF0h~1FFFh) of program memory is defined as chip Configuration Word (CFGW), which is loaded into the device control registers upon power on reset (POR). The 0000h~007Fh is occupied by Reset/Interrupt vectors as standard 8051 definition. The address space 1F00h~1FEFh is defined as the IAP area. In the in-circuit emulation (ICE) mode, user also needs to reserve the address space 0D00h~0FFFh for ICE System communication.CRC16H/L is the reserved area of the checksum. Tenx can provide a CRC verification subroutine. The user can calculate the checksum by the CRC verification subroutine to compare with CRC16H/L and check the validity of the ROM code.

8K Bytes Program Memory

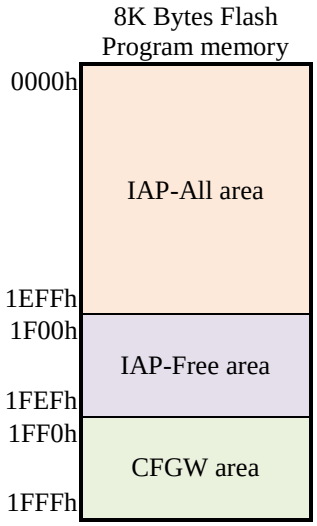
0000h 007Fh	Reset/Interrupt Vector
0080h 0CFFh	User Code area
0D00h 0FFFh	ICE mode reserve area
1000h 1EFFh	User Code area
1F00h 1FEFh	IAP-Free area
1FF0h	CRC16L
1FF1h	CRC16H
1FF2h 1FFAh	tenx reserve area
1FFBh	CFGBG
1FFDh	CFGWL (FRC)
1FFFh	CFGWH

2.1.2 Flash ICP Mode

The Flash memory can be programmed by the tenx proprietary writer **(TWR98/TWR99)**, which needs at least four wires (VCC, VSS, P3.0 and P3.1) to connect to this chip. If user wants to program the Flash memory on the target circuit board (In Circuit Program, ICP), these pins must be reserved sufficient freedom to be connected to the Writer.

2.1.3 Flash IAP Mode

The chip has "In Application Program" (IAP) capability, which allows software to read/write data from/to the Flash memory during CPU run time as conveniently as data EEPROM access. The IAP function is byte writable, meaning that the chip does not need to erase one Flash page before write. The available IAP data space is 240 Bytes after chip reset, and can be re-defined by the "IAPALL" control register as shown below.



Flash memory	IAPALL	MOVC Accessible	MOVX (IAP) Accessible
0000h~1EFFh	0	Yes	No
	1	Yes	Yes
1F00h~1FEFh	X	Yes	Yes
1FF0h~1FFEh	0	Yes	No
	1	Yes	Yes
1FFFh	X	Yes	No

In IAP mode, the program Flash memory is separated into three sectors: IAP-All area, IAP-Free area, and CFGW area. These four sectors are regulated differently.

The **IAP-All area** is protected by the IAPALL register to prevent IAP mode from writing application data to the program area, resulting in a program code error that cannot be repaired. The size of this area is 7936 Bytes. Enabling IAPALL requires writing 65h to SFR SWCMD 97h to set the IAPALL control flag. Then, software can use MOVX instructions to write application data to flash memory from 0000h to 1EFFh. If user wants to disable IAPALL function, user can write other values to SFR SWCMD 97h to clear the IAPALL control flag. User must be careful not to overwrite program code which is already resided on the same Flash memory area.

The **IAP-Free area** has no control bit to protect. It can be used to reliably store system application data that needs to be programmed once or periodically during system operation. Other areas of Flash memory can be used to store data, but this area is usually better. The size of this area is 240 Bytes, equivalent to an EEPROM, and Flash memory can provide byte access to read and write commands.

The **CFGW area** has 16 data bytes, which is located at the last 16 addresses of Flash memory. The CFGWH is not accessible to IAP, while the CFGWL and CFGBG can be read or written by IAP in case the IAPALL flag is set. CFGWL is copied to the SFR F6h and CFGBG is copied to the SFR F5h after power on reset, software then take over CFGWL's and CFGBG's control capability by modifying the SFR F6h and F5h.

2.1.4 IAP Mode Access Routines

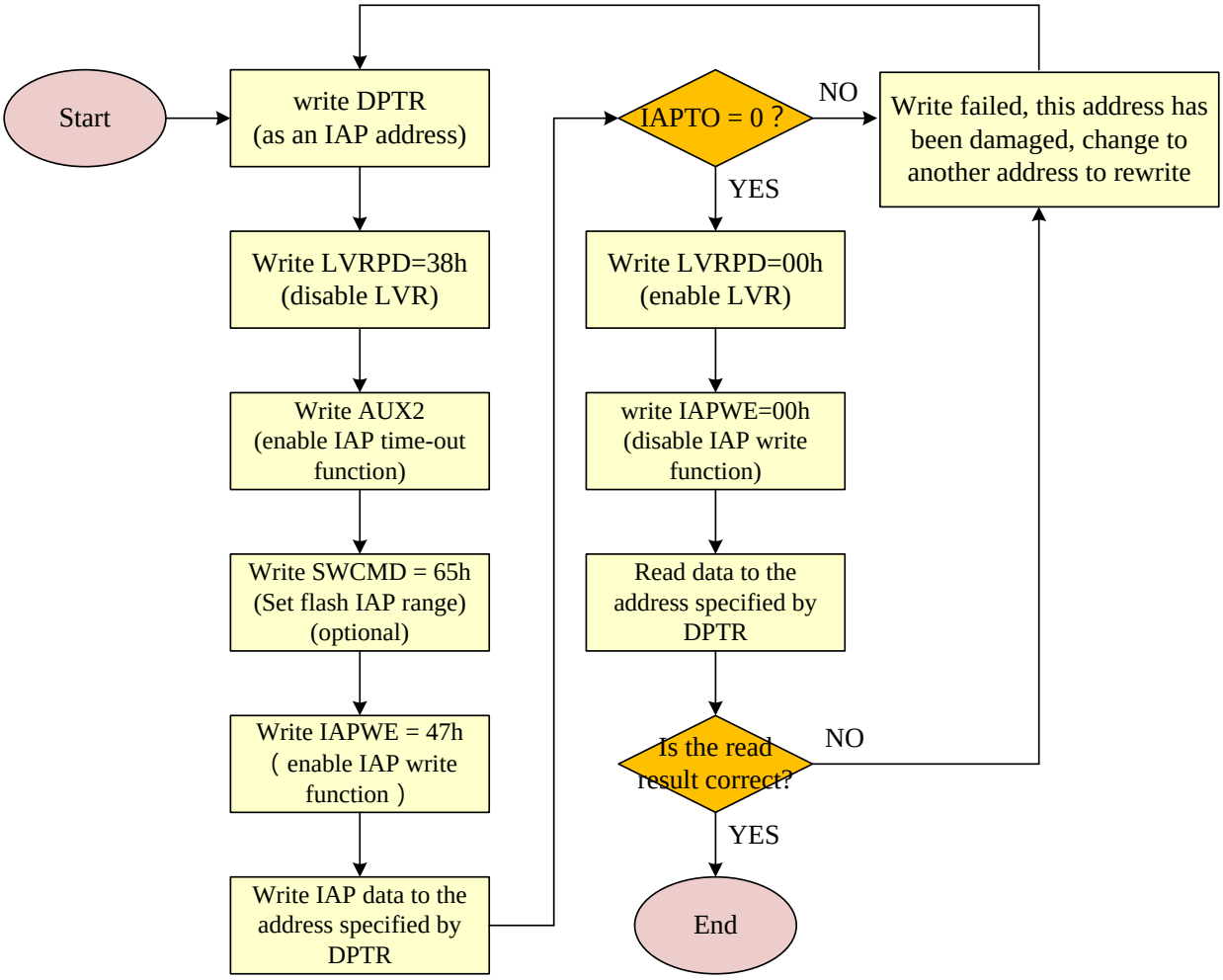
Flash IAP Write is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target Flash address (0000h~1FFEh), and the ACC contains the data being written. The chip accepts IAP write command only when IAPWE=1. Flash IAP writing one byte requires approximately 0.5 ms. Meanwhile the CPU stays in a waiting state, but all peripheral modules continue running during the writing time. The software must handle the pending interrupts after an IAP write. The chip has a build-in IAP Time-out function for escaping write fail state.

Flash IAP writing needs higher V_{CC} voltage, V_{CC}>4V, VCC capacitance greater than 220uF.

Because the Program memory and the IAP data space share the same entity, **Flash IAP Read** can be performed by the "MOVC" instruction as long as the target address points to the 0000h~1FFEh area. A Flash IAP read does not require extra CPU wait time.

IAP example:

```
 ; need 4.0V < VCC < 5.5V
MOV     DPTR, #1F00h      ; DPTR=1F00h=target IAP address
MOV     A, #5Ah           ; A=5Ah=target IAP write data
MOV     AUX2,  #04h       ; IAP Time-Out function enable
MOV     SWCMD, #65h       ; Set flash IAP range (optional)
MOV     IAPWE, #47h       ; IAP write enable
MOVX    @DPTR, A          ; Flash[1F00h] =5Ah, after IAP write
                          ; 1ms~2ms H/W writing time, CPU wait
MOV     IAPWE, #00h       ; IAP write disable, immediately after IAP write
CLR     A                 ; A=0
MOVC    A, @A+DPTR        ; Read.  A=5Ah
```



IAP Flow chart

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL/SWRST							
	–						WDTO	IAPALL
R/W	W						R	R
Reset	–						0	0

97h.7~0 **IAPALL (W):**
Write 65h, the available range of flash memory IAP is 0000h~1FEFh (IAPALL read back value is 1)
Write 00h, the available range of flash memory IAP is 1F00h~1EFFh (IAPALL read back value is 0)

97h.0 **IAPALL (R):**
0: Flash memory 0000h~1EFFh cannot use IAP, only 1F00h~1EFFh can use IAP
1: Flash memory 0000h~1EFFh and 1F00h~1EFFh can use IAP.

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPWE	IAPWE/EEPWE							
	IAPWE	IAPTO	EEPWE	–				
R/W	R	R	R	W				
Reset	0	0	0	–				

C9h.7~0 **IAPWE (W):** Write 47h to set IAPWE control flag; Write E2h to set EEPWE control flag; Write other value to clear IAPWE and EEPWE flag. It is recommended to clear it immediately after IAP or EEPROM write.

C9h.7 **IAPWE (R):** Flag indicates Flash memory can be written by IAP or not, 1=IAP Write enable.

C9h.6 **IAPTO (R):** IAP (or EEPROM write) Time-Out flag, Set by H/W when IAP (or EEPROM write) Time-out occurs. Cleared by H/W when IAPWE=0 (or EEPWE=0).

SFR **E5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRPD	LVRPD							
W	W							
Reset	0							

E5h.7~0 **LVRPD:** LVR and POR power down option
Write 0x37 to force LVR disable, POR disable
Write 0x38 to force LVR disable, POR enable

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

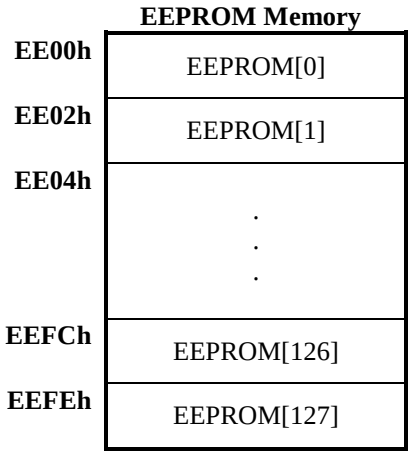
F7h.2~1 **IAPTE:** IAP (or EEPROM) write watchdog timer enable
00: Disable
01: wait1.6mS trigger watchdog time-out flag, and escape the write fail state
10: wait 3.2mS trigger watchdog time-out flag, and escape the write fail state
11: wait 12.8mS trigger watchdog time-out flag, and escape the write fail state

2.1.5 Flash ISP Mode

The “In System Programming” (ISP) usage is similar to IAP, except the purpose is to refresh the Program code. User can use UART or other method to get new Program code from external host, then writes code as the same way as IAP. ISP operation is complicated; basically it needs to assign a Boot code area to the Flash which does not change during the ISP process.

2.2 EEPROM Memory

The chip contains 128 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 50K write/erase cycles.



(Only even addresses can be used, odd addresses are invalid)

The EEPROM Write usage is similar to Flash IAP mode. It is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target EEPROM address (EE00h~EEFEh, ADDR=ADDR+2), and the ACC contains the data being written. EEPROM writing requires approximately 2 ms @V_{CC}=3V, 1 ms @V_{CC}=5V. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers, LED, and others) continue running during the writing time. The software must handle the pending interrupts after an EEPROM write. The chip has a build-in EEPROM Time-out function shared with Flash IAP for escaping write fail state. EEPROM writing needs V_{CC}>3.0V.

The EEPROM Read can be performed by the "MOVX A, @DPTR" instruction as long as the target address points to the EE00h~EEFEh area. The EEPROM read does require approximately 300ns.

```
; EEPROM example code
; need 3.0V < VCC < 5.5V
MOV     DPTR, #0EE00h       ; DPTR=EE00h=target EEPROM[0] address
MOV     A, #0A5h            ; A=A5h=target EEPROM[0] write data
MOV     EEPWE, #0E2h        ; EEPROM write enable
MOV     AUX2, #004h         ; EEPROM Time-Out function enable
MOVX    @DPTR, A            ; EEPROM[0]=A5h, after EEPROM write
                            ; 1ms~2ms H/W writing time, CPU wait
MOV     EEPWE, #000h        ; EEPROM write disable, immediately after EEPROM write
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=A5h
```

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPWE	IAPWE/EEPWE							
	IAPWE	IAPTO	EEPWE	–				
R/W	R	R	R	W				
Reset	0	0	0	–				

C9h.7~0 **EEPWE (W):** Write 47h to set IAPWE control flag; Write E2h to set EEPWE control flag; Write other value to clear IAPWE and EEPWE flag. It is recommended to clear it immediately after IAP or EEPROM write.

C9h.6 **IAPTO (R):** IAP (or EEPROM write) Time-Out flag, Set by H/W when IAP (or EEPROM write) Time-out occurs. Cleared by H/W when IAPWE=0 (or EEPWE=0).

C9h.5 **EEPWE (R):** Flag indicates EEPROM memory can be written or not, 1=EEPROM Write enable.

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.2~1 **IAPTE:** IAP (or EEPROM) write watchdog timer enable

00: Disable

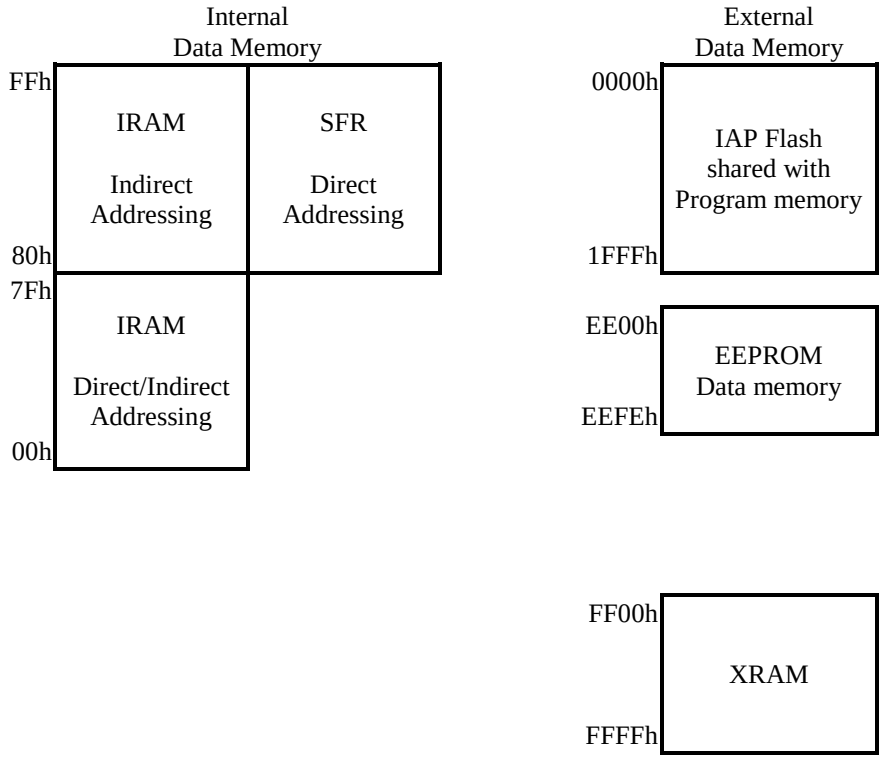
01: wait1.6mS trigger watchdog time-out flag, and escape the write fail state

10: wait 3.2mS trigger watchdog time-out flag, and escape the write fail state

11: wait 12.8mS trigger watchdog time-out flag, and escape the write fail state

2.3 Data Memory

As the standard 8051, the Chip has both Internal and External Data Memory space. The Internal Data Memory space consists of 256 Bytes IRAM and SFRs, which are accessible through a rich instruction set. The External Data Memory space consists of 256 Bytes XRAM, 128 Bytes EEPROM and IAP Flash, which can be only accessed by MOVX instruction.



IRAM

IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

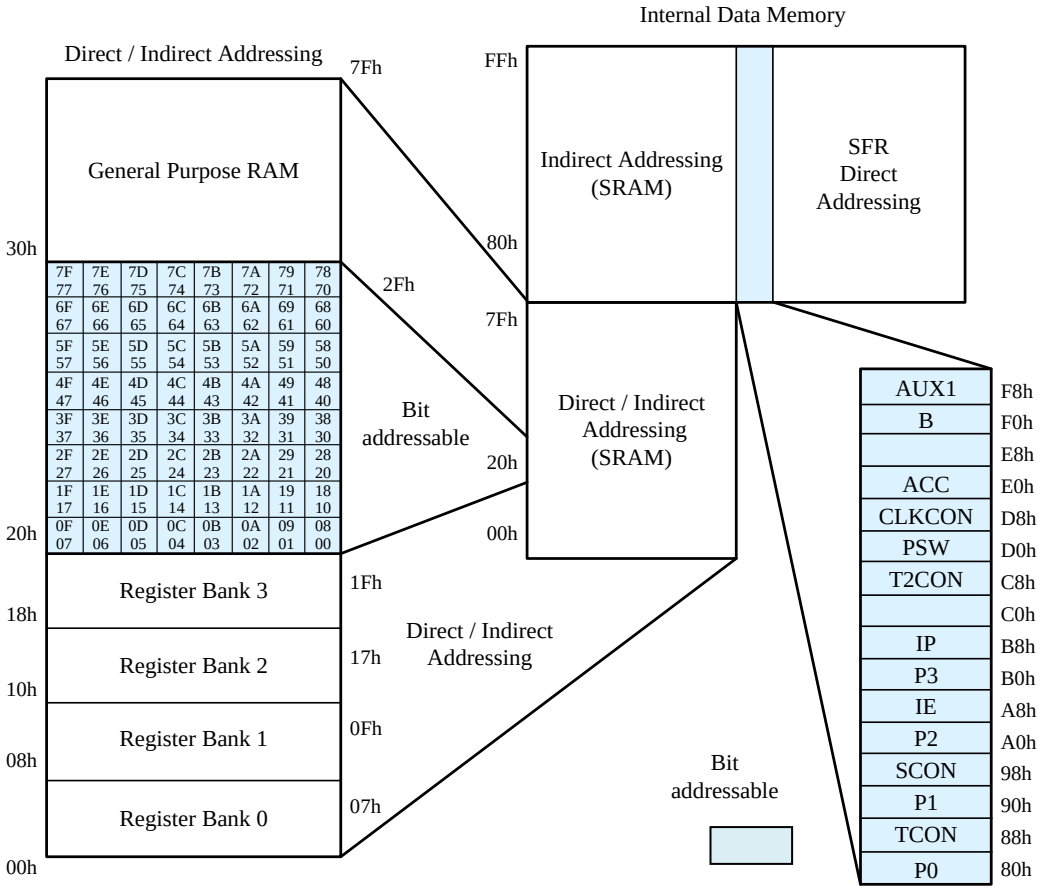
XRAM

XRAM is located in the 8051 external data memory space (address from FF00h to FFFFh). The 256Bytes XRAM can be only accessed by “MOVX” instruction.

2.4 Special Function Register (SFR)

All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit-addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with

the resources and peripherals of the Chip. The TM52 series of microcontrollers provides complete binary code with standard 8051 instruction set compatibility. Beside the standard 8051 SFRs, the Chip implements additional SFRs used to configure and access subsystems such as the ADC/LCD, which are unique to the Chip.



	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B	CRCDL	CRCDH	CRCIN		CFGBG	CFGWL	AUX2
E8h		PWM4DH	PWM4DL	PWM5DH	PWM5DL	PWM6DH	PWM6DL	
E0h	ACC	MICON	MIDAT	LVRCON	LVDCON		EXA	EXB
D8h	CLKCON	PWM0PRDH	PWM0PRDL	PWM1PRDH	PWM1PRDL	PWM3DH	PWM3DL	
D0h	PSW	PWM0DH	PWM0DL	PWM1DH	PWM1DL	PWM2DH	PWM2DL	
C8h	T2CON	IAPWE	RCP2L	RCP2H	TL2	TH2	EXA2	EXA3
C0h						P0WKUP	P2WKUP	P3WKUP
B8h	IP	IPH	IP1	IP1H				
B0h	P3						PWMOE1	PWMOE2
A8h	IE	INTE1	ADCDL	ADCDH			CHSEL	P0DIE
A0h	P2	PWMCON	P1MODL	P1MODH	P3MODL	P3MODH	PWMOE0	PWMCON2
98h	SCON	SBUF						
90h	P1	P0OE	P1LOE	PINMOD	OPTION	INTFLG	P1WKUP	SWCMD
88h	TCON	TMOD	TL0	TL1	TH0	TH1		
80h	P0	SP	DPL	DPH	INTE2	INTFLG2		PCON

3. Reset

The chip has five types of reset (Reset) methods. Power-on reset (POR), external pin reset (XRST), software reset (SWRST), watchdog timer reset (WDTR) and low voltage reset (LVR), SFR returns to default values after reset.

3.1 Power on Reset (POR)

After power-on reset, the device stays in the reset state and performs chip preheating for 40mS. A power-on reset requires the voltage on the VCC pin to discharge to near the VSS level before rising above 2.2V. POR is automatically turned off when the chip enters HALT/STOP mode and can be enabled/disabled by LVRPD (SFR E5h).

3.2 External Pin Reset (XRST)

External Pin Reset is active low. It needs to keep at least 2 SRC clock cycle long to be seen by the Chip. Can be enabled/disabled by CFGWH.

3.3 Software Command Reset (SWRST)

Software reset is generated by writing data 56h to SWCMD (SFR 97h).

3.4 Watchdog Timer Reset (WDTR)

WDT overflow reset is controlled by WDTE (SFR F7h.7~6). The WDT uses SRC as the count time base, runs in FAST/SLOW clock mode, and optionally runs or stops in IDLE/HALT/STOP clock mode. The watchdog timer overflow speed can be defined by WDTPSC (SFR 94h.5~4). WDT is cleared by CLRWDT (SFR F8h.7) or reset.

3.5 Low Voltage Reset (LVR)

Low voltage reset (LVR) can select 16 different voltage thresholds through CFGWH. When PWRSAV (SFR F7h.5) =1, the LVR will automatically turn off when the chip enters IDLE/HALT/STOP mode. It can be enabled/disabled by LVRPD (SFR E5h).

Note: *refer to AP-TM52XXXXX_02S for LVR setting information*

Operation Mode	SFR		CFGWH	LVR	Function	Note
	LVRPD	PWRSAV	LVRE			
Fast Slow	0	X	0000	ON	LVR 2.25V	
	0	X	0001	ON	LVR 2.40V	
	0	X	0010	ON	LVR 2.55V	
	0	X	0011	ON	LVR 2.70V	
	0	X	0100	ON	LVR 2.80V	
	0	X	0101	ON	LVR 2.95V	
	0	X	0110	ON	LVR 3.10V	
	0	X	0111	ON	LVR 3.25V	
	0	X	1000	ON	LVR 3.40V	
	0	X	1001	ON	LVR 3.55V	
	0	X	1010	ON	LVR 3.70V	
	0	X	1011	ON	LVR 3.85V	
	0	X	1100	ON	LVR 4.00V	
	0	X	1101	ON	LVR 4.15V	
	0	X	1110	ON	LVR 4.30V	
	0	X	1111	ON	LVR 4.45V	
Idle Halt Stop	0	0	0000	ON	LVR 2.25V	Current consumption about 60uA
	0	0	0001	ON	LVR 2.40V	
	0	0	0010	ON	LVR 2.55V	
	0	0	0011	ON	LVR 2.70V	
	0	0	0100	ON	LVR 2.80V	
	0	0	0101	ON	LVR 2.95V	
	0	0	0110	ON	LVR 3.10V	
	0	0	0111	ON	LVR 3.25V	
	0	0	1000	ON	LVR 3.40V	
	0	0	1001	ON	LVR 3.55V	
	0	0	1010	ON	LVR 3.70V	
	0	0	1011	ON	LVR 3.85V	
	0	0	1100	ON	LVR 4.00V	
	0	0	1101	ON	LVR 4.15V	
	0	0	1110	ON	LVR 4.30V	
	0	0	1111	ON	LVR 4.45V	
Idle	0	1	XXXX	ON	Disable LVR Enable POR	Current consumption about 20uA
Halt Stop	0	1	XXXX	OFF	Disable	Minimum current consumption about 0.1uA
Fast Slow Idle	1	X	XXXX	ON	Disable LVR Enable POR	Current consumption about 20uA
Halt Stop	1	X	XXXX	OFF	Disable	Minimum current consumption about 0.1uA

Note: *The current consumption of Halt mode is more than STOP mode about 2 ~ 5uA, because SRC is enabled.*

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	–	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	–	R/W		R/W		R/W	
Reset	0	–	0	0	0	0	0	0

94h.5~4 **WDTPSC:** Watchdog Timer pre-scalar time select
00: 400ms WDT overflow rate
01: 200ms WDT overflow rate
10: 100ms WDT overflow rate
11: 50ms WDT overflow rate

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL/SWRST							
R/W	W						R/W	R/W
Reset	–						–	0

97h.7~0 **SWRST:** Write 56h to generate S/W Reset

SFR **E3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRCON	–	–	–	–	LVRSEL			
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

E3h.3~0 LVRSEL: Low Voltage Reset function select. (Same as CFGWH LVRE function)
0000: Set LVR at 2.25V
0001: Set LVR at 2.40V
0010: Set LVR at 2.55V
0011: Set LVR at 2.65V
0100: Set LVR at 2.80V
0101: Set LVR at 2.95V
0110: Set LVR at 3.10V
0111: Set LVR at 3.25V
1000: Set LVR at 3.40V
1001: Set LVR at 3.55V
1010: Set LVR at 3.70V
1011: Set LVR at 3.85V
1100: Set LVR at 4.00V
1101: Set LVR at 4.15V
1110: Set LVR at 4.30V
1111: Set LVR at 4.45V

SFR **E5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRPD	LVRPD							
W	W							
Reset	0							

FE5.7~0 **LVRPD:** LVR and POR power down option
Write 0x37 to force LVR disable, POR disable
Write 0x38 to force LVR disable, POR enable

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16

R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.7~6 **WDTE:** Watchdog Timer Reset control
0x: Watchdog Timer Reset disable
10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Halt/Stop mode
11: Watchdog Timer Reset always enable

F7h.5 **PWRSAV:** chip power-saving option
Set 1 to reduce the chip's power consumption at Idle/Halt/Stop Mode

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	VBGEN	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.7 **CLRWDT:** Set to clear WDT, H/W auto clear it at next clock cycle

Flash **1FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE				PREAD	FRCPSC

1FFFh.6 **XRSTE:** External Pin Reset control
0: Disable External Pin Reset
1: Enable External Pin Reset

1FFFh.5~2 **LVRE:** Low Voltage Reset function select
0000: Set LVR at 2.25V
0001: Set LVR at 2.40V
0010: Set LVR at 2.55V
0011: Set LVR at 2.65V
0100: Set LVR at 2.80V
0101: Set LVR at 2.95V
0110: Set LVR at 3.10V
0111: Set LVR at 3.25V
1000: Set LVR at 3.40V
1001: Set LVR at 3.55V
1010: Set LVR at 3.70V
1011: Set LVR at 3.85V
1100: Set LVR at 4.00V
1101: Set LVR at 4.15V
1110: Set LVR at 4.30V
1111: Set LVR at 4.45V

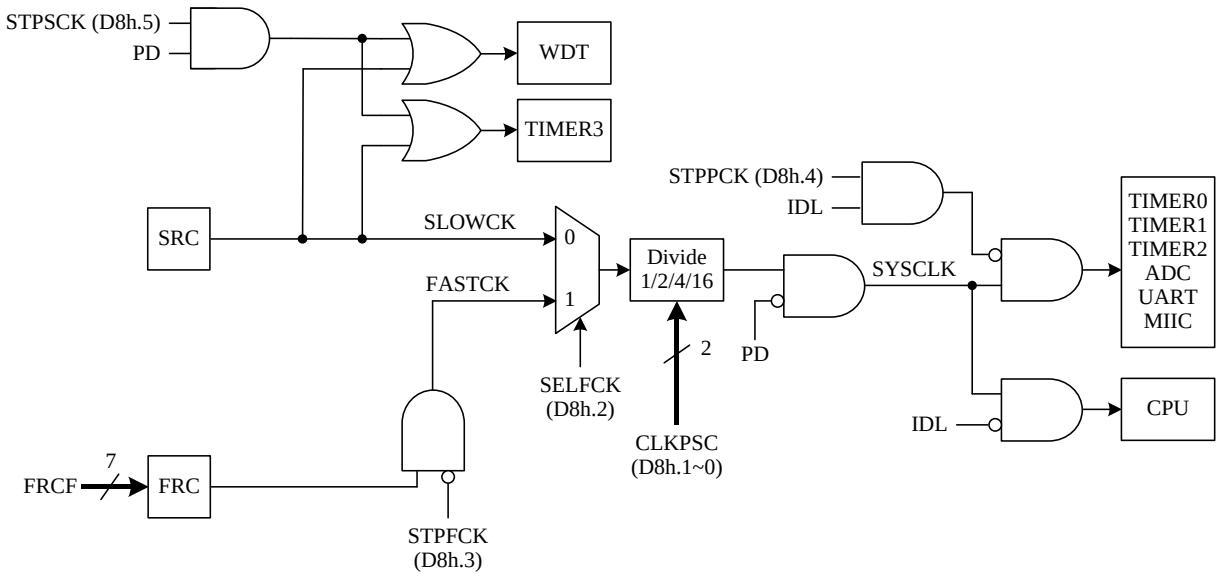
4. Clock Circuitry & Operation Mode

4.1 System Clock

The Chip is designed with dual-clock system. During runtime, user can directly switch the System clock from fast to slow or from slow to fast. It also can directly select a clock divider of 1, 2, 4 or 16. The Fast clock can be selected as FRC (Fast Internal RC, 16.588 MHz). The Slow clock can be selected as SRC (Slow Internal RC, 80 KHz). Fast mode and Slow mode are defined as the CPU running at Fast and Slow clock speeds.

After Reset, the device is running at Slow mode with 80 KHz SRC. S/W should select the proper clock rate for chip operation safety. The higher V_{CC} allows the chip to run at a higher System clock frequency. In a typical condition, a 16 MHz System clock rate requires V_{CC}> 3.1V.

The **CLKCON** SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow clock type in Fast mode and change the Fast clock type in Slow mode. Never to write both STPFCK=1 & SELFCK=1. It is recommended to write this SFR bit by bit.



Clock Structure

Note: *Because of the CLKPSC delay, it needs to wait for 16 clock cycles (max.) before switching Slow clock to Fast clock. Also refer to AP-TM52XXXXX_01S and AP-TM52XXXXX_02S about System Clock Application Note.*

SYSCLK	CLKCON (D8h)	
	bit3 STPFCK	bit2 SELFCK
Fast FRC	0	1
Slow SRC	0/1	0
Stop FRC	0 → 1	0
Switch to FRC	0	0 → 1
Switch to SRC	0	1 → 0

Flash **1FFDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	FRCF						

1FFDh.6~0 **FRCF:** FRC frequency adjustment.
FRC is trimmed to 16.588 MHz in chip manufacturing. FRCF records the adjustment data.

SFR **F6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	FRCF						
R/W	–	R/W						
Reset	–	–	–	–	–	–	–	–

F6h.6~0 **FRCF:** FRC frequency adjustment
00h= lowest frequency, 7Fh=highest frequency.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	–	–	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	–	–	R/W	R/W	R/W	R/W	R/W	
Reset	–	–	0	0	0	0	1	1

D8h.5 **STPSCK:** Set 1 to stop slow clock in Stop mode.

D8h.4 **STPPCK:** Set 1 to stop UARTs/Timer0/Timer1/Timer2/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle Mode.

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

4.2 Operation Modes

There are 5 operation modes for this device. The power consumption is lower when the system clock speed is lower.

Fast Mode:

Fast Mode is defined as the CPU running at Fast clock speed.

Slow Mode:

Slow Mode is defined as the CPU running at Slow clock speed.

Idle Mode:

Idle Mode is entered by setting the **IDL** bit in PCON SFR.

Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The "STPPCK" bit in CLKCON SFR can be set to furthermore reduce Idle mode current. If STPPCK is set, only Timer3 and pin interrupts are alive in Idle Mode, others peripherals such as Timer0/1/2, UARTs and ADC are stop. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Halt Mode:

Halt Mode is entered by setting the **PD** bit in PCON SFR and clearing the **STPSCK** bit in CLKCON SFR.

In Halt mode, all clocks are stopped, but Timer3 and WDT may be on if they are enabled. Halt mode can be terminated by reset, pin wakeup or Timer3 interrupt.

Stop Mode:

Stop Mode is entered by setting the **PD** bit in PCON SFR.

This mode is the so-called "Power Down" mode in standard 8051. In Stop mode, all clocks stop except the WDT could be alive if it is enabled. Stop Mode is terminated by Reset or pin wake up.

Note: *The chip cannot enter Halt/Stop Mode if the INTn pin is low and the INTn wake-up function is enabled. (INTn=0 and EXn=1, n=0,1,2)*

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter HALT/STOP mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter IDLE mode.

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.4 **VBGOUT:** VBG voltage output to P3.2
0: Disable 1: Enable

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	–	–	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	–	–	R/W	R/W	R/W	R/W	R/W	
Reset	–	–	1	0	0	0	1	1

D8h.5 **STPSCK:** Set 1 to stop Slow clock in Stop mode.

D8h.4 **STPPCK:** Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle Mode.

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock 1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

5. Interrupt & Wake-up

This Chip has a 13-source four-level priority interrupt structure. All enabled Interrupts can wake up CPU from Idle mode, but only the Pin Interrupts can wake up CPU from Halt/Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter whether its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	Flag	Description
0003	IE0	INT0 external pin Interrupt (can wake up Halt/Stop mode)
000B	TF0	Timer0 Interrupt
0013	IE1	INT1 external pin Interrupt (can wake up Halt/Stop mode)
001B	TF1	Timer1 Interrupt
0023	RI+TI	Serial Port (UART) Interrupt
002B	TF2+EXF2	Timer2 Interrupt
0033	–	Reserved for ICE mode use
003B	TF3	Timer3 Interrupt
0043	PXIF	Port0~Port3 external pin change Interrupt (can wake up Halt/Stop mode)
004B	IE2	INT2 external pin Interrupt (can wake up Halt/Stop mode)
0053	ADIF	ADC Interrupt
005B	MIIF	Master I^2C (MIIC) Interrupt
0063	LVDIF	LVD Interrupt
006B	–	Reserved
0073	PWM0IF+PWM1IF	PWM0~1 Interrupt

Interrupt Vector & Flag

5.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

FR **84h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE2	–	PWM1IE	PWM0IE	–	–	–	–	–
R/W	–	R/W	R/W	–	–	–	–	–
Reset	–	0	0	–	–	–	–	–

84h.6 **PWM1IE:** PWM1~PWM6 interrupt enable
0: Disable PWM1~PWM6 interrupt
1: Enable PWM1~PWM6 interrupt

84h.5 **PWM0IE:** PWM0 interrupt enable
0: Disable PWM0 interrupt
1: Enable PWM0 interrupt

SFR **96h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1WKUP	P1WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

96h.7~0 **P1WKUP:** P1.7~P1.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **C5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0WKUP	P0WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

C5h.7~0 **P0WKUP:** P0.7~P0.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **C6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2WKUP	P2WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

C6h.7~0 **P2WKUP:** P2.7~P2.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **C7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3WKUP	P3WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

C7h.7~0 **P3WKUP:** P3.7~P3.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable control.
0: Disable all Interrupts.
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.5 **ET2:** Timer2 interrupt enable
0: Disable Timer2 interrupt
1: Enable Timer2 interrupt

A8h.4 **ES:** Serial Port (UART) interrupt enable
0: Disable Serial Port (UART) interrupt
1: Enable Serial Port (UART) interrupt

A8h.3 **ET1:** Timer1 interrupt enable
0: Disable Timer1 interrupt
1: Enable Timer1 interrupt

A8h.2 **EX1:** External INT1 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT1 pin Interrupt and Halt/Stop mode wake up
1: Enable INT1 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

A8h.1 **ET0:** Timer0 interrupt enable
0: Disable Timer0 interrupt
1: Enable Timer0 interrupt

A8h.0 **EX0:** External INT0 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT0 pin Interrupt and Halt/Stop mode wake up
1: Enable INT0 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	–	LVDIE	I2CE	ADIE	EX2	PXIE	TM3IE
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A9h.7 **PWMIE:** PWM0/PWM1~PWM6 interrupt enable
0: Disable PWM0/PWM1~PWM6 interrupt 1: Enable PWM0/PWM1~PWM6 interrupt

A9h.5 **LVDIE:** LVD interrupt enable
0: Disable LVD interrupt 1: Enable LVD interrupt

A9h.4 **I2CE:** I²C interrupt enable
0: Disable I²C interrupt 1: Enable I²C interrupt

A9h.3 **ADIE:** ADC interrupt enable
0: Disable ADC interrupt 1: Enable ADC interrupt

A9h.2 **EX2:** External INT2 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT2 pin Interrupt and Halt/Stop mode wake up
1: Enable INT2 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

A9h.1 **PXIE:** Port0~Port3 pin change interrupt enable. This bit does not affect the Port0~Port3 pin's Halt/Stop mode wake up capability.
0: Disable Port0~Port3 pin change interrupt
1: Enable Port0~Port3 pin change interrupt

A9h.0 **TM3IE:** Timer3 interrupt enable
0: Disable Timer3 interrupt
1: Enable Timer3 interrupt

SFR **B9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

SFR **B8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

B9h.5, B8h.5 **PT2H, PT2 :** Timer2 Interrupt Priority control. (PT2H, PT2) =
11: Level 3 (highest priority)
10: Level 2
01: Level 1
00: Level 0 (lowest priority)

B9h.4, B8h.4 **PSH, PS :** Serial Port (UART) Interrupt Priority control. Definition as above.

B9h.3, B8h.3 **PT1H, PT1 :** Timer1 Interrupt Priority control. Definition as above.

B9h.2, B8h.2 **PX1H, PX1 :** External INT1 pin Interrupt Priority control. Definition as above.

B9h.1, B8h.1 **PT0H, PT0 :** Timer0 Interrupt Priority control. Definition as above.

B9h.0, B8h.0 **PX0H, PX0 :** External INT0 pin Interrupt Priority control. Definition as above.

SFR **BBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	PPWMH	–	PLVDH	PI2CH	PADIH	PX2H	PPXH	PT3H
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

SFR **BAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	PPWM	–	PLVD	PI2C	PADI	PX2	PPX	PT3
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

BBh.7, BAh.7 **PPWMH, PPWM :** PWM0/PWM1 Interrupt Priority control. Definition as above.

BBh.5, BAh.5 **PLVDH, PLVD :** LVD Interrupt Priority control. Definition as above.

BBh.4, BAh.4 **PI2CH, PI2C :** I^2C Interrupt Priority control. Definition as above.

BBh.3, BAh.3 **PADIH, PADI :** ADC Interrupt Priority control. Definition as above.

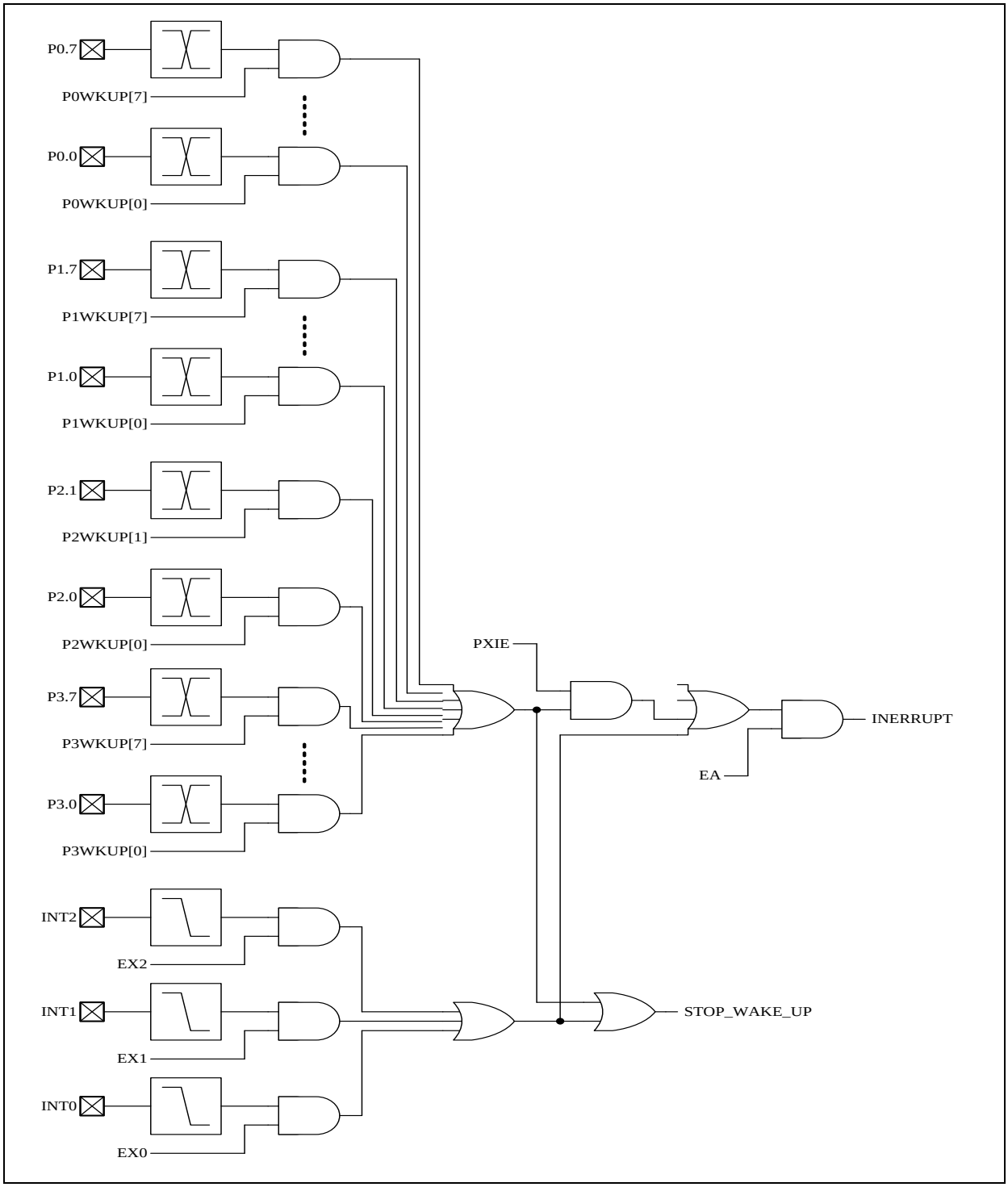
BBh.2, BAh.2 **PX2H, PX2 :** External INT2 pin Interrupt Priority control. Definition as above.

BBh.1, BAh.1 **PPXH, PPX :** Port0~Port3 Pin Change Interrupt Priority control. Definition as above.

BBh.0, BAh.0 **PT3H, PT3 :** Timer3 Interrupt Priority control. Definition as above.

5.2 Pin Interrupt

Pin Interrupts include Change Interrupt. These pins also have the Idle/Halt/Stop mode wake up capability. INT0 and INT1 are falling edge or low level triggered as the 8051 standard. INT2 is falling edge triggered and Port1 Change Interrupt is triggered by any Port1 pin state change.



Pin Interrupt & Wake up

Note: *The chip cannot enter Halt/Stop Mode if the INTn pin is low and the INTn wake-up function is enabled. (INTn=0 and EXn=1, n=0~2)*

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag.
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin

88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	ADIF	–	IE2	PXIF	TF3
R/W	–	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

95h.2 **IE2:** External Interrupt 2 (INT2 pin) edge flag
Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FBh to INTFLG to clear this bit. (***Note1***)

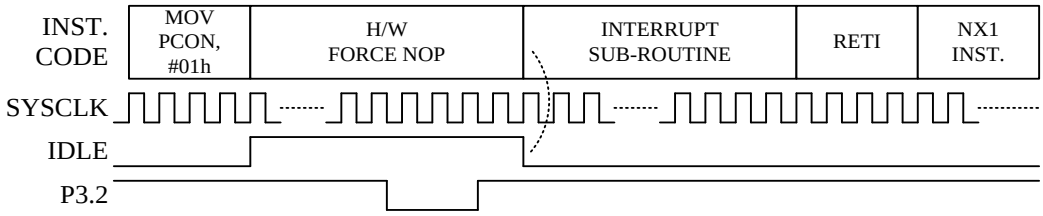
95h.1 **PXIF:** Port0~Port3 pin change interrupt flag
Set by H/W when Port0~Port3 pin state change is detected and its interrupt enable bit is set (P0WKUP/P1WKUP/P2WKUP/P3WKUP). PXIE does not affect this flag's setting.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FDh to INTFLG to clear this bit. (***Note1***)

Note1: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.*

5.3 Idle mode Wake up and Interrupt

Each interrupt enable bit (e.g. ET0, EX0) and the EA bit must be set to establish the wake-up function from Idle mode. All enabled interrupts (pins, timers, ADC, touch buttons, SPI and UART) can wake up the CPU from idle mode. When the idle is woken up, immediately enter the interrupt subroutine. When the interrupt subroutine returns, "the first instruction after IDL(PCON.0) is set" will be executed.

For all pin interrupts to be triggered, each interrupt enable bit (e.g. EX0) and the EA bit must be set to 1 and the pin trigger state must stay long enough (greater than 1 system clock) to be sampled by the system clock. When the EA is not set to 1 or the pin trigger state does not stay long enough, it will not wake up and will not generate an interrupt subroutine.



EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter HALT/STOP mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter IDLE mode.

5.4 Halt/Stop mode Wake up and Interrupt

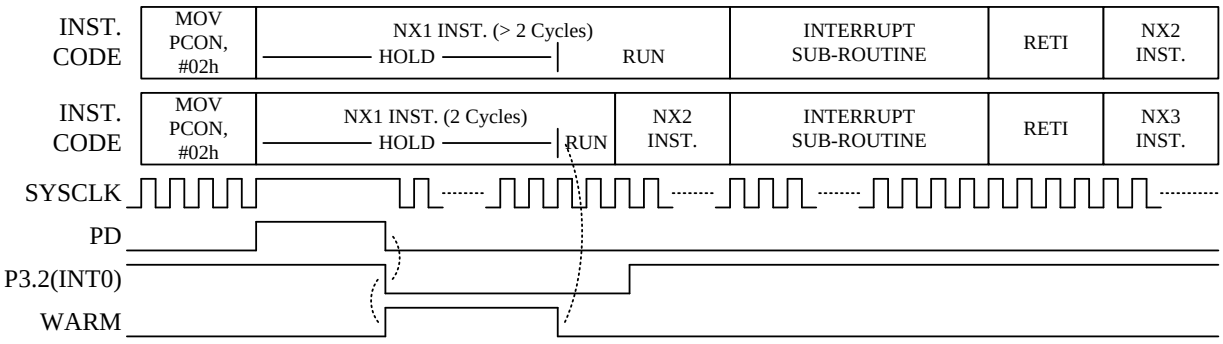
Each interrupt enable bit (e.g. ET3, EX0) and the EA bit must be set to 1 to establish the Halt/Stop mode interrupt function. All enabled interrupts (pins, Timer3) can wake up the CPU from Halt/Stop mode. Once Halt/Stop is woken up, "the first instruction after PD(PCON.1) is set" is executed immediately before the interrupt is serviced.

In addition to setting EX0/EX1/EX2, the INT0~2 pin interrupt needs to set EA=1 and the pin trigger state stays long enough (greater than 64 system clocks) to be sampled by the system clock, that is to say, when EA is not set to 1 or if the pin trigger state does not stay long enough, the CPU will only wake up without entering the interrupt subroutine.

In addition to setting P0WKUP/P1WKUP/P2WKUP/P3WKUP, Port0~3 WKUP pin interrupt needs to set EA=1, that is to say, when EA is not set to 1, the CPU will only be woken up and will not enter the interrupt subroutine.

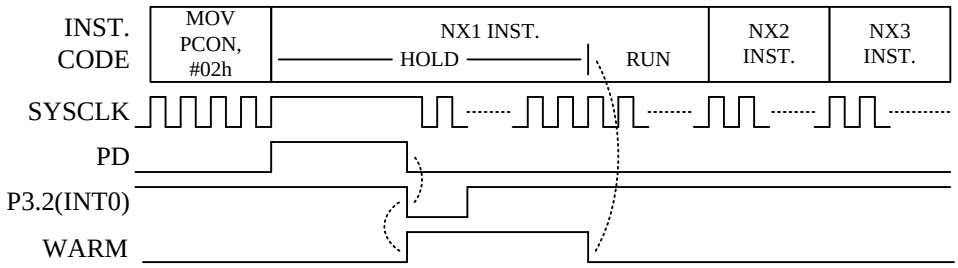
Note: *It is recommended to place the NX1/NX2 with NOP Instruction in figures below.*
Note: *The chip cannot enter Halt/Stop mode if the INTn pin is low and the INTn wake-up function is enabled. (INTn=0 and EXn=1, n=0~2)*

INT0~2 Pin Interrupt:



EA=EX0=1

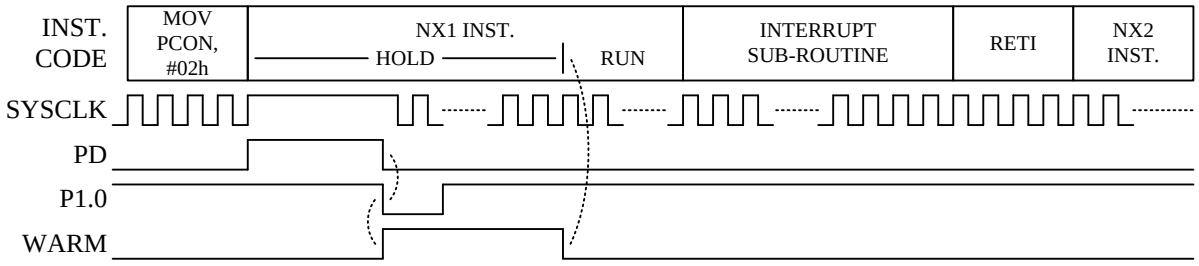
Input the interrupt pulse whose width is greater than 64 system clocks, then the Idle/Stop mode will wake up and enter the interrupt subroutine



EA=EX0= 1

Input the interrupt pulse whose width is less than 64 system clocks, then the Idle/Stop mode will wake up but will not enter the interrupt subroutine

Port0~3 WKUP Pin Interrupt:



EA=PXIE=1, P1WKUP[0]=1

Input any width WKUP pin interrupt, the Idle/Stop mode will wake up and enter the interrupt subroutine

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter HALT/STOP mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter IDLE mode.

6. I/O Ports

The Chip has total 26 multi-function I/O pins. All I/O pins follow the standard 8051 "Read-Modify-Write" feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR (ex: ANL P1, A; INC P2; CPL P3.0).

Port1 & P2.1~P2.0 & Port 3

These pins can operate in four different modes as below.

Mode	Port1, P2.1~P2.0, Port3 pin function		Px.n SFR data	Pin State	Resistor Pull-up	Digital Input
	P3.0~P3.2	Others				
Mode 0	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Pull-up	Y	Y
Mode 1	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Hi-Z	N	Y
Mode 2	CMOS Output		0	Drive Low	N	N
			1	Drive High	N	N
Mode 3	Analog input for ADC, digital input buffer is disabled		X (don't care)	–	N	N

I/O Pin Function Table

If a Port1, P2.1~P2.0 or Port3 pin is used for Schmitt-trigger input, S/W must set the I/O pin to Mode0 or Mode1 and set the corresponding Port Data SFR to 1 to disable the pin's output driving circuitry.

Beside I/O port function, each Port1, P2.1~P2.0 and Port3 pin has one or more alternative functions, such as ADC. Most of the functions are activated by setting the individual pin mode control SFR to Mode3. Port1/Port3 pins have standard 8051 auxiliary definition such as INT0/1, T0/1/2, or RXD/TXD. These pin functions need to set the pin mode SFR to Mode0 or Mode1 and keep the P1.n/P3.n SFR at 1.

Pin Name	8051	Wake-up	CKO	ADC	PWM	LCD	others	Mode3
P1.0	T2	Y	T2O	AD2	PWM3			AD2
P1.1	T2EX	Y		AD3	PWM2			AD3
P1.2		Y			PWM1	LCDC0		
P1.3		Y		AD16	PWM6	LCDC1	SCL	AD16
P1.4		Y		AD17	PWM5	LCDC2		AD17
P1.5		Y		AD18	PWM4	LCDC3		AD18
P1.6		Y		AD19			SDA/TXD	AD19
P1.7		Y		AD9				AD9
P3.0	RXD	Y		AD6				AD6
P3.1	TXD	Y		AD7				AD7
P3.2	INT0	Y		AD5			VBGO	AD5
P3.3	INT1	Y		AD4				AD4
P3.4	T0	Y	T0O	AD8	PWM3			AD8
P3.5	T1	Y	T1O		PWM0P		SDA	
P3.6		Y			PWM0N PWM2 PWM4			
P3.7	INT2	Y					RSTn	
P2.0		Y						
P2.1		Y						

Port1, P2.1~P2.0, Port3 multi-function Table

The necessary SFR setting for Port1/P2.1~P2.0/Port3 pin's alternative function is list below.

Alternative Function	Mode	Px.n SFR data	Pin State	Other necessary SFR setting
T0, T1, T2, T2EX, INT0, INT1, INT2	**0**	1	Input with Pull-up	
	1	1	Input	
RXD, TXD	**0**	1	Input with Pull-up / Pseudo Open Drain Output	TXRXSEL
	1	1	Input / Pseudo Open Drain Output	
SCL (I^2C Master)	**0**	X	I^2C Clock Output (Open Drain Output, Pull-up)	MSCLSEL
	2	X	I^2C Clock Output (CMOS Push-Pull)	
SDA (I^2C Master)	**0**	1	I^2C DATA (Pull-up)	MSDASEL
T0O, T1O, T2O	**0**	X	Clock Open Drain Output with Pull-up	T0OE T1OE T2OE
	1	X	Clock Open Drain Output	
	2	X	Clock Output (CMOS Push-Pull)	
VBGO	**X**	X	Bandgap Voltage output	VBGOUT
LCDC0~ LCDC3	**X**	X	1/2 Bias Output	P1LOE
ADx	**3**	X	ADC Channel	
PWM0~PWM6	**0**	X	PWM Open Drain Output with Pull-up	PWMOE0 PWMOE1 PWMOE2
	1	X	PWM Open Drain Output	
	2	X	PWM Output (CMOS Push-Pull)	

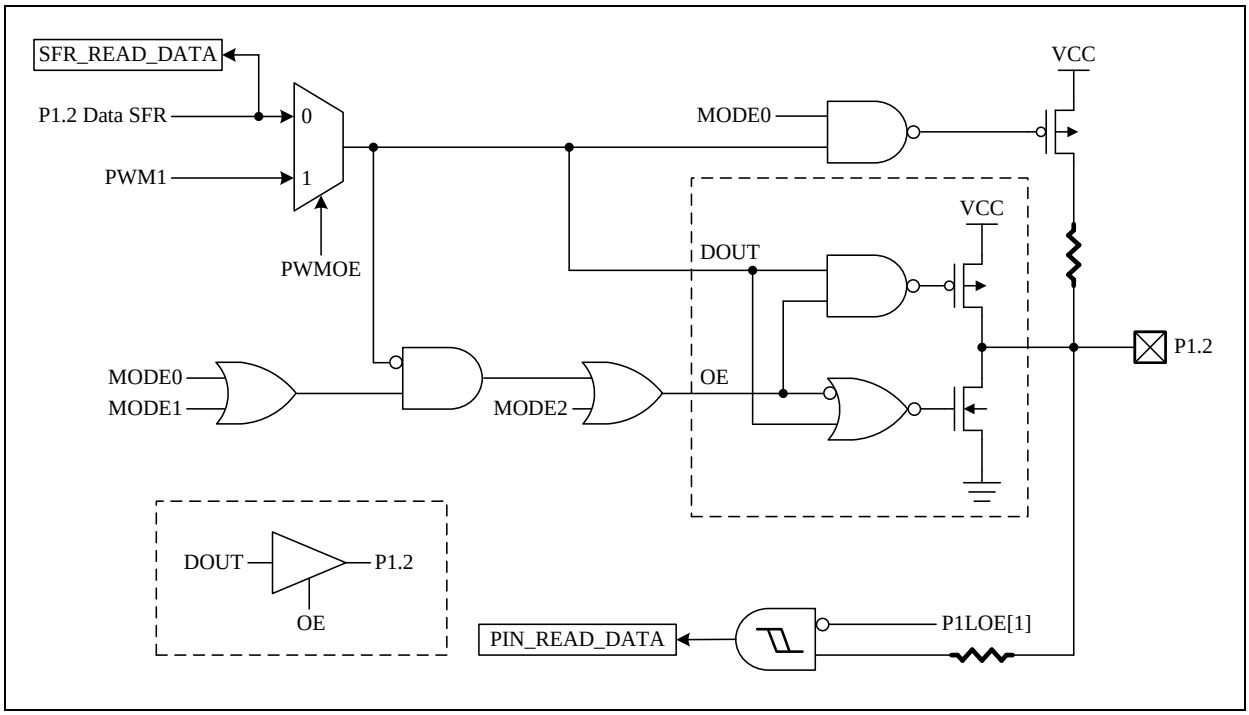
Mode Setting for Port1, P2.1~P2.0, Port3 Alternative Function

For tables above, a "**CMOS Output**" pin means it can sink and drive at least 4 mA current. It is not recommended to use such pin as input function.

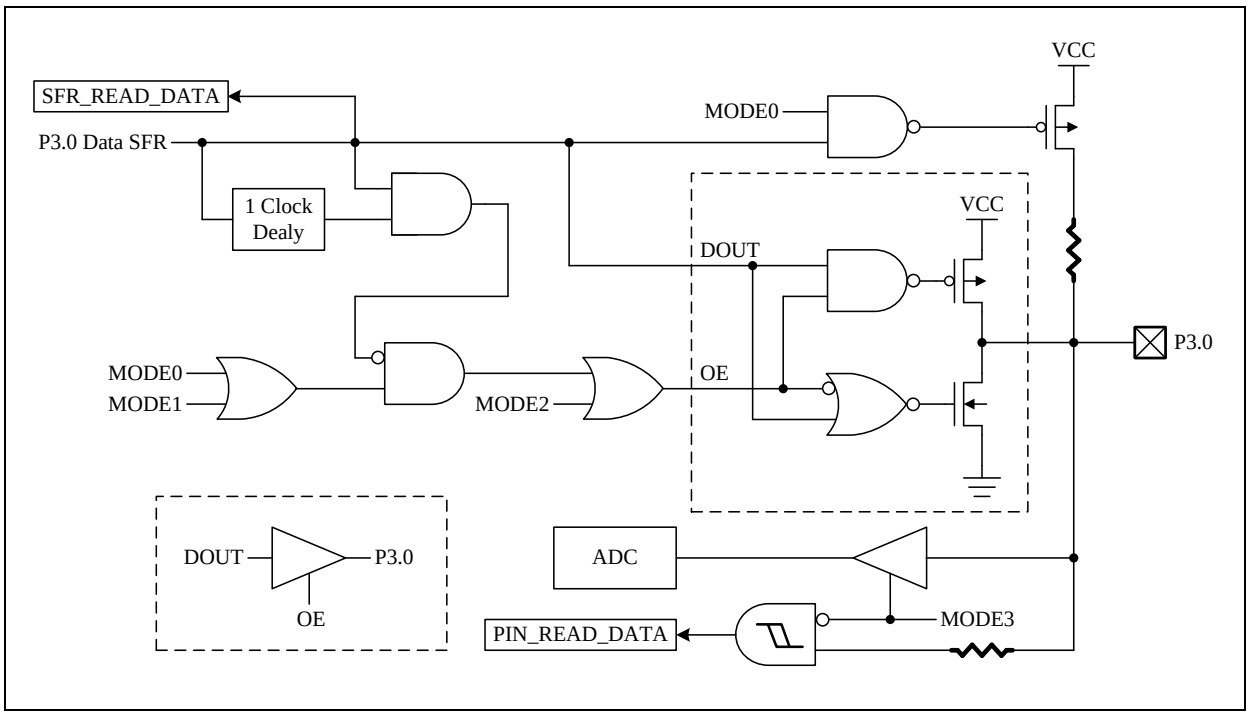
An "**Open Drain**" pin means it can sink at least 4 mA current but only drive a small current (<20 μA). It can be used as input or output function and typically needs an external pull up resistor.

An 8051 standard pin is a "**Pseudo Open Drain**" pin. It can sink at least 4 mA current when output is at low level, and drives at least 4 mA current for 1~2 clock cycle when output transits from low to high, then keeps driving a small current (<20 μA) to maintain the pin at high level. It can be used as input or output function.

Note2: *for the necessary SFR setting above, LCD/LED pin has the highest priority. Therefore, if a pin is not used for Segment (ex: pin is I/O, ADC, TK, and SPI…), S/W must disable the LCD/LED function.*



P1.2 Pin Structure



P3.0 Pin Structure

SFR **90h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

90h.7~0 **P1:** Port1 data

SFR **A0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.1~0 **P2.1~P2.0:** P2.1~P2.0 data

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.7~0 **P3:** Port1 data

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.4 **VBGOUT:** Bandgap voltage output control
0: Disable
1: Bandgap voltage output to P3.2 pin

SFR **92h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1LOE	–	–	–	–	P1LOE3	P1LOE2	P1LOE1	P1LOE0
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

92h.3 **P1LOE3:** LCD 1/2 bais Output
0: Disable
1: P15 as LCD 1/2 bais Output

92h.2 **P1LOE2:** LCD 1/2 bais Output
0: Disable
1: P14 as LCD 1/2 bais Output

92h.1 **P1LOE1:** LCD 1/2 bais Output
0: Disable
1: P13 as LCD 1/2 bais Output

92h.0 **P1LOE0:** LCD 1/2 bais Output
0: Disable
1: P12 as LCD 1/2 bais Output

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	TXRXSEL	T2OE	T1OE	T0OE	P2MOD1		P2MOD0	
R/W	R/W	R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	1	0	1

93h.7 **TXRXSEL:** UART TXD/RXD pin select
0: P31 as TXD, P30 as RXD
1: P16 as TXD, P02 as RXD

93h.6 **T2OE:** Timer2 signal output (T2O) control

0: Disable "Timer2 overflow divided by 2" output to P1.0 pin
1: Enable "Timer2 overflow divided by 2" output to P1.0 pin

93h.5 **T1OE:** Timer1 signal output (T1O) control
0: Disable "Timer1 overflow divided by 2" output to P3.5 pin
1: Enable "Timer1 overflow divided by 2" output to P3.5 pin

93h.4 **T0OE:** Timer0 signal output (T0O) control
0: Disable "Timer0 overflow divided by 64" output to P3.4 pin
1: Enable "Timer0 overflow divided by 64" output to P3.4 pin

93h.3~2 **P2MOD1:** P2.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

93h.1~0 **P2MOD0:** P2.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

SFR **A2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A2h.7~6 **P1MOD3:** P1.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.3 is ADC input

A2h.5~4 **P1MOD2:** P1.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A2h.3~2 **P1MOD1:** P1.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.1 is ADC input

A2h.1~0 **P1MOD0:** P1.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.0 is ADC input

SFR **A3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A3h.7~6 **P1MOD7:** P1.7 pin control
00: Mode0

01: Mode1
10: Mode2
11: Mode3, P1.7 is ADC input

A3h.5~4 **P1MOD6:** P1.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.6 is ADC input

A3h.3~2 **P1MOD5:** P1.5 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.5 is ADC input

A3h.1~0 **P1MOD4:** P1.4 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.4 is ADC input

SFR **A4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A4h.7~6 **P3MOD3:** P3.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.3 is ADC input

A4h.5~4 **P3MOD2:** P3.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.2 is ADC input

A4h.3~2 **P3MOD1:** P3.1 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.1 is ADC input

A4h.1~0 **P3MOD0:** P3.0 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.0 is ADC input

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A5h.7~6 **P3MOD7:** P3.7 pin control
00: Mode0
01: Mode1

10: Mode2
11: Mode3

A5h.5~4 **P3MOD6:** P3.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A5h.3~2 **P3MOD5:** P3.5 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A5h.1~0 **P3MOD4:** P3.4 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.4 is ADC input

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE0	PWM1OE3	PWM1OE2	PWM1OE1	PWM1OE0	PWM0NOE1	PWM0POE1	PWM0NOE0	PWM0POE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A6h.7 **PWM1OE3:** PWM1 output control
0: Disable 1: PWM1 enable and output to P1.2

A6h.6 **PWM1OE2:** PWM1 output control
0: Disable 1: PWM1 enable and output to P0.6

A6h.5 **PWM1OE1:** PWM1 output control
0: Disable 1: PWM1 enable and output to P0.4

A6h.4 **PWM1OE0:** PWM1 output control
0: Disable 1: PWM1 enable and output to P0.2

A6h.3 **PWM0NOE1:** PWM0N output control
0: Disable 1: PWM0N enable and output to P3.6

A6h.2 **PWM0POE1:** PWM0P output control
0: Disable 1: PWM0P enable and output to P3.5

A6h.1 **PWM0NOE0:** PWM0N output control
0: Disable 1: PWM0N enable and output to P0.4

A6h.0 **PWM0POE0:** PWM0P output control
0: Disable 1: PWM0P enable and output to P0.3

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE1	PWM4OE3	PWM4OE2	PWM4OE1	PWM4OE0	PWM3OE1	PWM3OE0	PWM2OE1	PWM2OE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B6h.7 **PWM4OE3:** PWM4 output control
0: Disable 1: PWM4 enable and output to P3.6

B6h.6 **PWM4OE2:** PWM4 output control
0: Disable 1: PWM4 enable and output to P1.5

B6h.5 **PWM4OE1:** PWM4 output control
0: Disable 1: PWM4 enable and output to P0.4

B6h.4 **PWM4OE0:** PWM4 output control
0: Disable 1: PWM4 enable and output to P0.0

B6h.3 **PWM3OE1:** PWM3 output control
0: Disable 1: PWM3 enable and output to P3.4
B6h.2 **PWM3OE0:** PWM3 output control
0: Disable 1: PWM3 enable and output to P1.0
B6h.1 **PWM2OE1:** PWM2 output control
0: Disable 1: PWM2 enable and output to P3.6
B6h.0 **PWM2OE0:** PWM2 output control
0: Disable 1: PWM2 enable and output to P1.1

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE2	MSDASEL	MSCLSEL	PWM6OE2	PWM6OE1	PWM6OE0	PWM5OE2	PWM5OE1	PWM5OE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B7h.7 **MSDASEL:** Master I^2C SDA select
0: P3.5 as Master I^2C SDA
1: P1.6 as Master I^2C SDA
B7h.6 **MSCLSEL:** Master I^2C SCL select
0: P1.3 as Master I^2C SCL
1: P0.2 as Master I^2C SCL
B7h.5 **PWM6OE2:** PWM6 output control
0: Disable 1: PWM6 enable and output to P1.3
B7h.4 **PWM6OE1:** PWM6 output control
0: Disable 1: PWM6 enable and output to P0.7
B7h.3 **PWM6OE0:** PWM6 output control
0: Disable 1: PWM6 enable and output to P0.3
B7h.2 **PWM5OE2:** PWM5 output control
0: Disable 1: PWM5 enable and output to P1.4
B7h.1 **PWM5OE1:** PWM5 output control
0: Disable 1: PWM5 enable and output to P0.6
B7h.0 **PWM5OE0:** PWM5 output control
0: Disable 1: PWM5 enable and output to P0.1

Port0

These pins are shared with ADC, LCD. If a Port0 is defined as I/O pin, it can be used as CMOS push-pull output or Schmitt-trigger input. The pin's pull up function is enable while SFR bit P0OE.n=0 and P0.n=1.

Port0 pin function	P0OE.n	P0.n SFR data	Pin State	Resistor Pull-up	Digital Input
Input	0	0	Hi-Z	N	Y
	0	1	Pull-up	Y	Y
CMOS Output	1	0	Drive Low	N	N
	1	1	Drive High	N	N

Port0 Pin Function Table

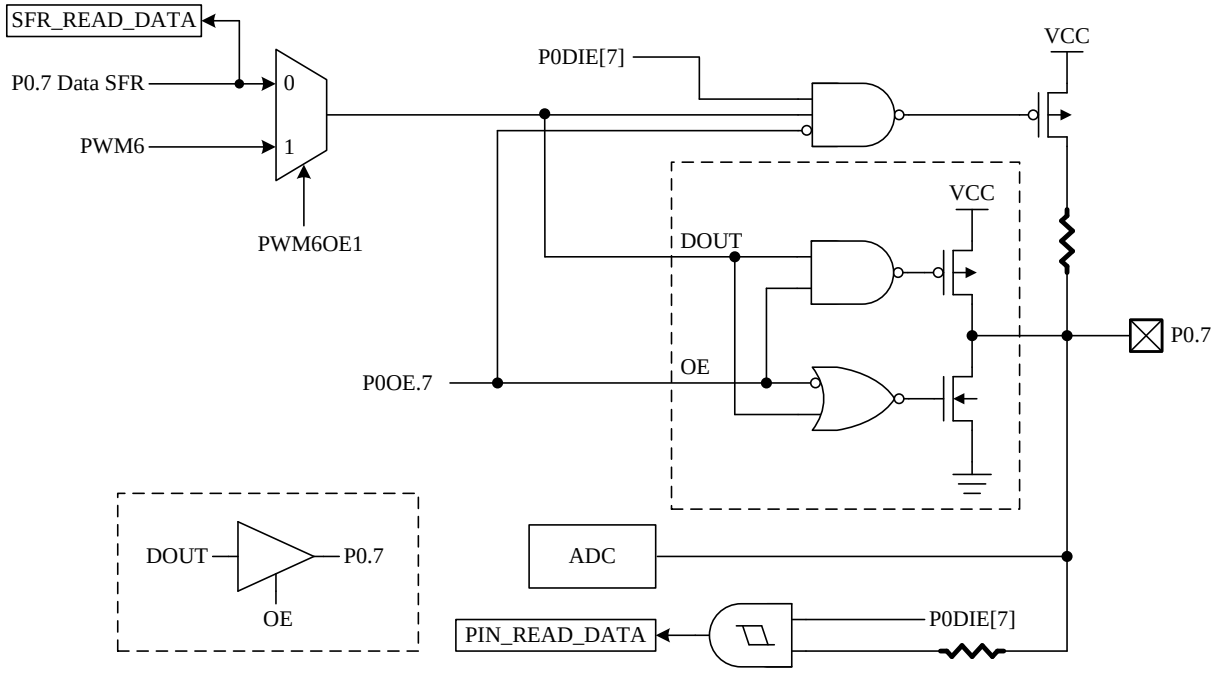
Pin Name	Wake-up	ADC	PWM	Others
P0.0	Y	AD20	PWM4	
P0.1	Y	AD21	PWM5	
P0.2	Y	AD22	PWM1	RXD/SCL
P0.3	Y	AD1	PWM0P/PWM6	
P0.4	Y	AD0	PWM0N/PWM1/PWM4	
P0.5	Y	AD11		
P0.6	Y		PWM1/PWM5	
P0.7	Y	AD10	PWM6	

Port0 multi-function Table

The necessary SFR setting for Port0 pin's alternative function is list below.

Alternative Function	PxOE.n	Px.n SFR data	Pin State	other necessary SFR setting
RXD	0	1	Input with Pull-up	TXRXSEL
SCL (I^2C Master)	0	X	I^2C Clock Output (Open Drain Output, Pull-up)	MSCLSEL
	1	X	I^2C Clock Output (CMOS Push-Pull)	
ADx	0	0	ADC Channel	P0DIE
PWM0~PWM6	**0**	X	PWM Open Drain Output	PWMOE0 PWMOE1 PWMOE2
	1	X	PWM Output (CMOS Push-Pull)	

Mode Setting for Port0 Alternative Function Table



P0.7 Pin Structure

SFR **80h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

80h.7~0 **P0:** Port0 data, also controls the P0.n pin's pull-up function. If the P0.n SFR data is "1" and the corresponding P0OE.n = 0 (input mode), the pull-up is enabled.

SFR **91h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0OE	P0OE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

91h.7~0 **P0OE:** Port0 CMOS Push-Pull output enable control
0: Disable
1: Enable

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	TXRXSEL	T2OE	T1OE	T0OE	P2MOD1		P2MOD0	
R/W	R/W	R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	1	0	1

93h.7 **TXRXSEL:** UART TXD/RXD pin select
0: P31 as TXD, P30 as RXD
1: P16 as TXD, P02 as RXD

SFR **AFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0DIE	P0DIE7	P0DIE6	P0DIE5	P0DIE4	P0DIE3	P0DIE2	P0DIE1	P0DIE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

AFh.7 **P0DIE7:** Port digital input enable
0: P0.7 is ADC input and disabledigital input
1: enable P0.7 digital input

AFh.6 **P0DIE6:** Port digital input enable
0: disable P0.6 digital input
1: enable P0.6 digital input

AFh.5 **P0DIE5:** Port digital input enable
0: P0.5 is ADC input and disable digital input
1: enable P0.5 digital input

AFh.4 **P0DIE4:** Port digital input enable
0: P0.4is ADC input and disable digital input
1: enable P0.4 digital input

AFh.3 **P0DIE3:** Port digital input enable
0: P0.3 is ADC input and disable digital input
1: enable P0.3 digital input

AFh.2 **P0DIE2:** Port digital input enable
0: disable P0.2 digital input
1: enable P0.2 digital input

AFh.1 **P0DIE1:** Port digital input enable
0: disable P0.1 digital input
1: enable P0.1 digital input

AFh.0 **P0DIE0:** Port digital input enable
0: disable P0.0 digital input
1: enable P0.0 digital input

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE0	PWM1OE3	PWM1OE2	PWM1OE1	PWM1OE0	PWM0NOE1	PWM0POE1	PWM0NOE0	PWM0POE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A6h.7 **PWM1OE3:** PWM1 output control
0: Disable 1: PWM1 enable and output to P1.2

A6h.6 **PWM1OE2:** PWM1 output control
0: Disable 1: PWM1 enable and output to P0.6

A6h.5 **PWM1OE1:** PWM1 output control
0: Disable 1: PWM1 enable and output to P0.4

A6h.4 **PWM1OE0:** PWM1 output control
0: Disable 1: PWM1 enable and output to P0.2

A6h.3 **PWM0NOE1:** PWM0N output control
0: Disable 1: PWM0N enable and output to P3.6

A6h.2 **PWM0POE1:** PWM0P output control
0: Disable 1: PWM0P enable and output to P3.5

A6h.1 **PWM0NOE0:** PWM0N output control
0: Disable 1: PWM0N enable and output to P0.4

A6h.0 **PWM0POE0:** PWM0P output control
0: Disable 1: PWM0P enable and output to P0.3

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE1	PWM4OE3	PWM4OE2	PWM4OE1	PWM4OE0	PWM3OE1	PWM3OE0	PWM2OE1	PWM2OE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B6h.7 **PWM4OE3:** PWM4 output control
0: Disable 1: PWM4 enable and output to P3.6

B6h.6 **PWM4OE2:** PWM4 output control
0: Disable 1: PWM4 enable and output to P1.5

B6h.5 **PWM4OE1:** PWM4 output control
0: Disable 1: PWM4 enable and output to P0.4

B6h.4 **PWM4OE0:** PWM4 output control
0: Disable 1: PWM4 enable and output to P0.0

B6h.3 **PWM3OE1:** PWM3 output control
0: Disable 1: PWM3 enable and output to P3.4

B6h.2 **PWM3OE0:** PWM3 output control
0: Disable 1: PWM3 enable and output to P1.0

B6h.1 **PWM2OE1:** PWM2 output control
0: Disable 1: PWM2 enable and output to P3.6

B6h.0 **PWM2OE0:** PWM2 output control
0: Disable 1: PWM2 enable and output to P1.1

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE2	MSDASEL	MSCLSEL	PWM6OE2	PWM6OE1	PWM6OE0	PWM5OE2	PWM5OE1	PWM5OE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B7h.7 **MSDASEL:** Master I^2C SDA select
0: P3.5 as Master I^2C SDA
1: P1.6 as Master I^2C SDA

B7h.6 **MSCLSEL:** Master I^2C SCL select
0: P1.3 as Master I^2C SCL
1: P0.2 as Master I^2C SCL

B7h.5 **PWM6OE2:** PWM6 output control
0: Disable 1: PWM6 enable and output to P1.3

B7h.4 **PWM6OE1:** PWM6 output control
0: Disable 1: PWM6 enable and output to P0.7

B7h.3 **PWM6OE0:** PWM6 output control
0: Disable 1: PWM6 enable and output to P0.3

B7h.2 **PWM5OE2:** PWM5 output control
0: Disable 1: PWM5 enable and output to P1.4

B7h.1 **PWM5OE1:** PWM5 output control
0: Disable 1: PWM5 enable and output to P0.6

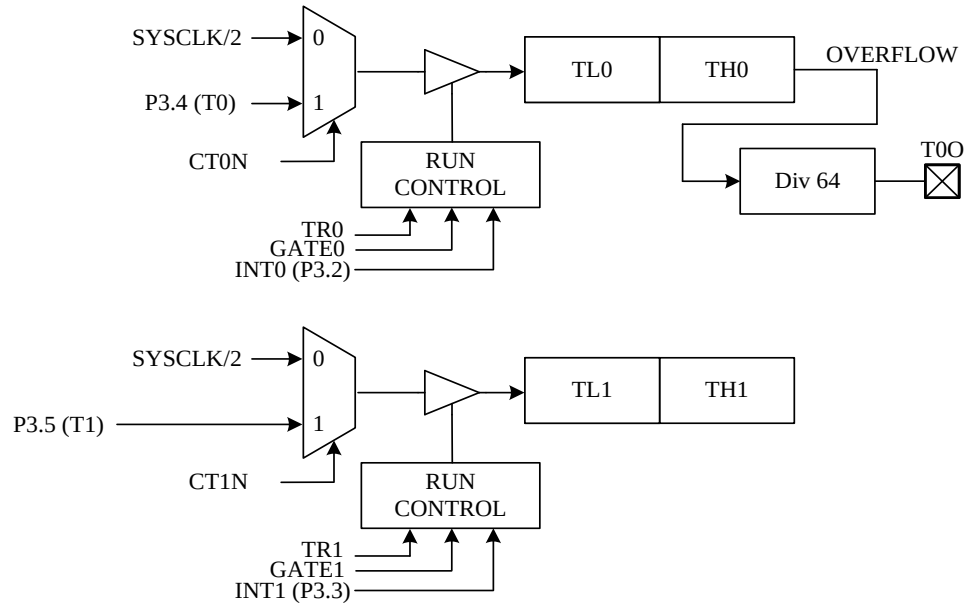
B7h.0 **PWM5OE0:** PWM5 output control
0: Disable 1: PWM5 enable and output to P0.1

7. Timers

Timer0, Timer1 and Timer2 are provided as standard 8051 compatible timer/counter. Compare to the traditional 12T 8051, the Chip's Timer0/1/2 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every "2 System clock" rate; in counter mode, T0/T1/T2 pin input pulse must be wider than 2 System clock to be seen by this device. In addition to the standard 8051 timers function. The T0O pin can output the "Timer0 overflow divided by 64" signal, and the T2O pin can output the "Timer2 overflow divided by 2" signal.

Timer0 / Timer1

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).



Timer0 and Timer1 Structure

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs

88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR **89h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set

89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin's negative edge

89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops

89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

89h.2 **CT0N:** Timer0 Counter/Timer select bit
0: Timer mode, Timer0 data increases at 2 System clock cycle rate
1: Counter mode, Timer0 data increases at T0 pin's negative edge

89h.1~0 **TMOD0:** Timer0 mode select
00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR **8Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR **8Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

SFR **8Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

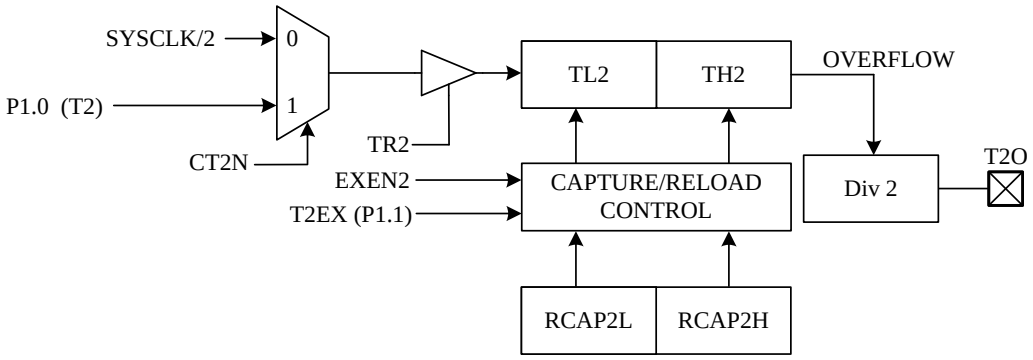
SFR **8Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

***Note**: See also Chapter 5 for more information on Timer0/1 interrupt enable and priority.*
***Note**: See also Chapter 6 for details on T0O pin output settings.*

Timer2

Timer2 is controlled through the TCON2 register with the low and high bytes of Timer/Counter2 stored in TL2 and TH2 and the low and high bytes of the Timer2 reload/capture registers stored in RCAP2L and RCAP2H.



Timer2 Structure

SFR **C8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

C8h.7 **TF2:** Timer2 overflow flag
Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.

C8h.6 **EXF2:** T2EX interrupt pin falling edge flag
Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.

C8h.5 **RCLK:** UART receive clock control bit
0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3
1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3

C8h.4 **TCLK:** UART transmit clock control bit
0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3
1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3

C8h.3 **EXEN2:** T2EX pin enable
0: T2EX pin disable
1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0

C8h.2 **TR2:** Timer2 run control
0: Timer2 stops
1: Timer2 runs

C8h.1 **CT2N:** Timer2 Counter/Timer select bit
0: Timer mode, Timer2 data increases at 2 System clock cycle rate
1: Counter mode, Timer2 data increases at T2 pin's negative edge

C8h.0 **CPRL2N:** Timer2 Capture/Reload control bit
0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1.
1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1.
If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.

SFR **CAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2L	RCP2L							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CAh.7~0 **RCP2L:** Timer2 reload/capture data low byte

SFR **CBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2H	RCP2H							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CBh.7~0 **RCP2H:** Timer2 reload/capture data high byte

SFR **CCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL2	TL2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CCh.7~0 **TL2:** Timer2 data low byte

SFR **CDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH2	TH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CDh.7~0 **TH2:** Timer2 data high byte

***Note**: See also Chapter 5 for more information on Timer2 interrupt enable and priority.*
***Note**: See also Chapter 6 for details on T2O pin output settings.*

Timer3

Timer3 works as a time-base counter, which generates interrupts periodically. It generates an interrupt flag (TF3) with the clock divided by 32768, 16384, 8192, or 65536 depending on the TM3PSC SFR.

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	TM3CKS	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.6 **TM3CKS:**Timer3 时钟源选择。
0：慢时钟源（SRC）
1：FRC/512（~32KHz）

94h.1~0 **TM3PSC:** Timer3 Interrupt rate
00: Timer3 Interrupt rate is 32768 Slow clock cycle
01: Timer3 Interrupt rate is 16384 Slow clock cycle
10: Timer3 Interrupt rate is 8192 Slow clock cycle
11: Timer3 Interrupt rate is 65536 Slow clock cycle

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	ADIF	–	IE2	PXIF	TF3
R/W	–	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

95h.0 **TF3:** Timer3 Interrupt Flag
Set by H/W when Timer3 reaches TM3PSC setting cycles. Cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit. (***Note1***)

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	VBGEN	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.6 **CLRTM3:** Set 1 to clear Timer3, H/W auto clear it at next clock cycle.

Note: *also refer to Chapter 5 for more information about Timer3 Interrupt enable and priority.*

T0O, T1O and T2O Output Control

This device can generate various frequency waveform pin output (in CMOS or Open-Drain format) for Buzzer. The T0O and T2O waveform is divided by Timer0/Timer2 overflow signal. The T0O waveform is Timer0 overflow divided by 64, and T2O waveform is Timer2 overflow divided by 2. User can control their frequency by Timers auto reload speed. Set T0OE and T2OE SFRs can output these waveforms.

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	TXRXSEL	T2OE	T1OE	T0OE	P2MOD1		P2MOD0	
R/W	R/W	R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	1	0	1

93h.6 **T2OE:** Timer2 signal output (T2O) control
0: Disable "Timer2 overflow divided by 2" output to P1.0 pin
1: Enable "Timer2 overflow divided by 2" output to P1.0 pin

93h.5 **T1OE:** Timer1 signal output (T1O) control
0: Disable "Timer1 overflow divided by 2" output to P3.5 pin
1: Enable "Timer1 overflow divided by 2" output to P3.5 pin

93h.4 **T0OE:** Timer0 signal output (T0O) control
0: Disable "Timer0 overflow divided by 64" output to P3.4 pin
1: Enable "Timer0 overflow divided by 64" output to P3.4 pin

8. UART

The UART uses SCON and SBUF SFRs. SCON is the control register, SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are completely independent. In addition to standard 8051's full duplex mode, this chip also provides one wire mode. If the UART1W bit is set, both transmit and receive data use P3.1 pin.

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.7 **SMOD:** UART double baud rate control bit
0: Disable UART double baud rate
1: Enable UART double baud rate

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	TXRXSEL	T2OE	T1OE	T0OE	P2MOD1		P2MOD0	
R/W	R/W	R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	1	0	1

93h.7 **TXRXSEL:** UART TXD/RXD pin select
0: P31 as TXD, P30 as RXD
1: P16 as TXD, P02 as RXD

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	-	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	-	R/W		R/W		R/W	
Reset	0	-	0	0	0	0	0	0

94h.7 **UART1W:** One wire UART mode enable, both TXD/RXD use P3.1 or p1.6 pin
0: Disable one wire UART mode
1: Enable one wire UART mode

SFR **98h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** Serial port mode select bit 0,1
00: Mode0: 8 bit shift register, Baud Rate=F_{SYSCLK}/2
01: Mode1: 8 bit UART, Baud Rate is variable
10: Mode2: 9 bit UART, Baud Rate=F_{SYSCLK}/32 or/64
11: Mode3: 9 bit UART, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2
SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART reception enable
0: Disable reception
1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR **99h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

99h.7~0 **SBUF:** UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

F_{SYSCLK} denotes System clock frequency, the UART baud rate is calculated as below.

- **Mode 0:**
  Baud Rate=F_{SYSCLK}/2
- **Mode 1, 3:** if using Timer1 auto reload mode
  Baud Rate= (SMOD + 1) x F_{SYSCLK}/ (32 x 2 x (256 – TH1))
- **Mode 1, 3:** if using Timer2
  Baud Rate=Timer2 overflow rate/16 = F_{SYSCLK}/ (32 x (65536 – RCP2H, RCP2L))
- **Mode 2:**
  Baud Rate= (SMOD + 1) x F_{SYSCLK}/64

Note: *also refer to Chapter 5 for more information about UART Interrupt enable and priority.*
Note: *also refer to Chapter 7 for more information about how Timer2 controls UART clock.*

9. PWMs

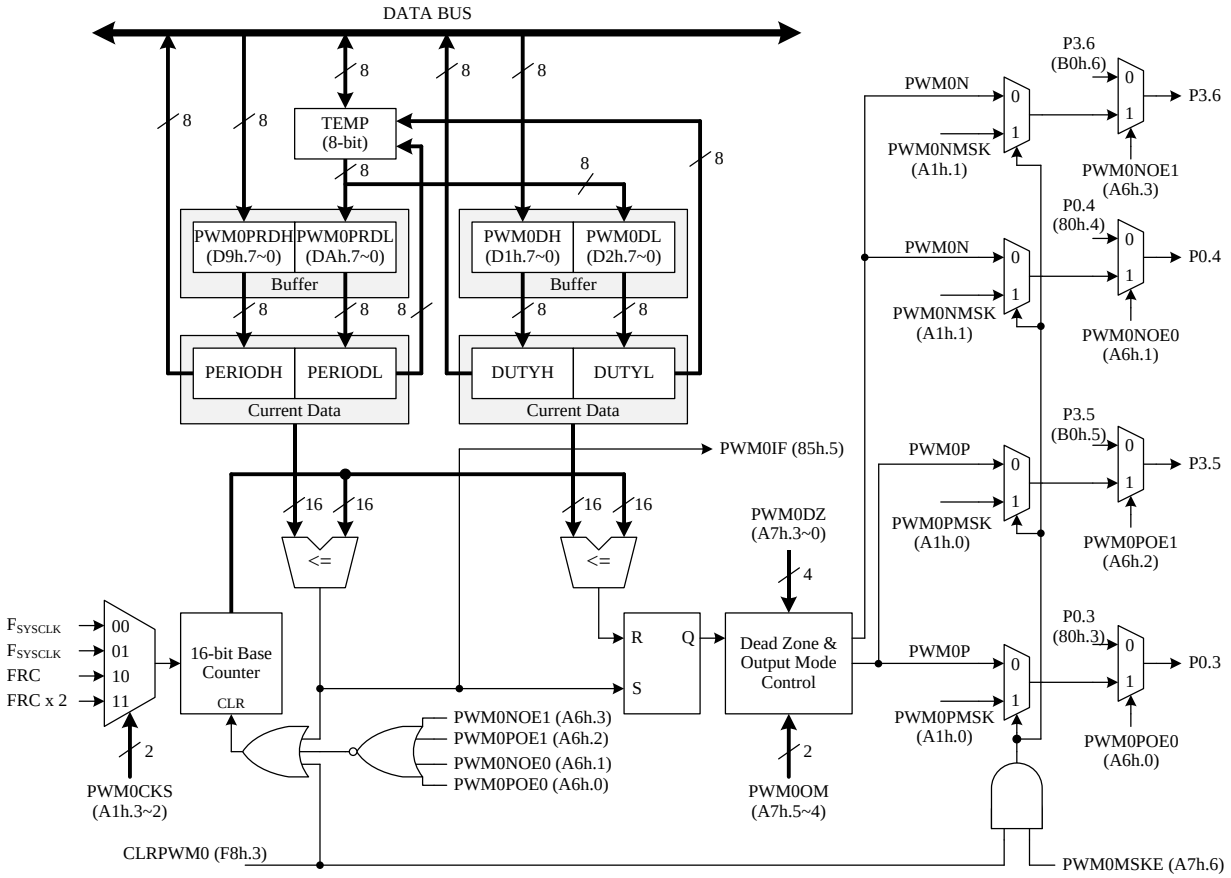
This Chip has seven 16-bit PWM modules, PWM0 to PWM6. The PWM can generate varies frequency waveform with 65536 duty resolution on the basis of the PWM clock. The PWM clock can select FRC double frequency (FRC x 2), FRC or F_{SYSCLK} as its clock source. Users should pay attention to the setting, the period of PWM must be greater than duty.

The pin mode SFR controls the PWM output waveform format. Mode1 makes the PWM open drain output and Mode2 makes the PWM CMOS push-pull output.

The 16-bit PWM0PRD, PWM1PRD and PWM0D ~ PWM6D registers all have a low and high byte structure. The high bytes can be directly accessed, but as the low bytes can only be accessed via an internal 8-bit buffer, reading or writing to these register pairs must be carried out in a specific way. The important point to notes is that data transfer to and from the 8-bit buffer and its related low byte only takes place when write or read operation to its corresponding high bytes is executed. Briefly speaking, write low byte first and then high byte; read high byte first and then low byte.

PWM0

The PWM0POE0 / PWM0POE1 are used to select the output for PWM0P, and the PWM0NOE0 / PWM0NOE1 are used to select the output for PWM0N. These four bits also can be PWM0 control bit. If those four bits are cleared, the PWM0 will be cleared and stopped, otherwise the PWM0 is running. The CLRPWM0 bit has the same function. When CLRPWM0 bit is set, the PWM0 will be cleared and held, otherwise the PWM0 is running. The PWM0 structure is shown as follow.



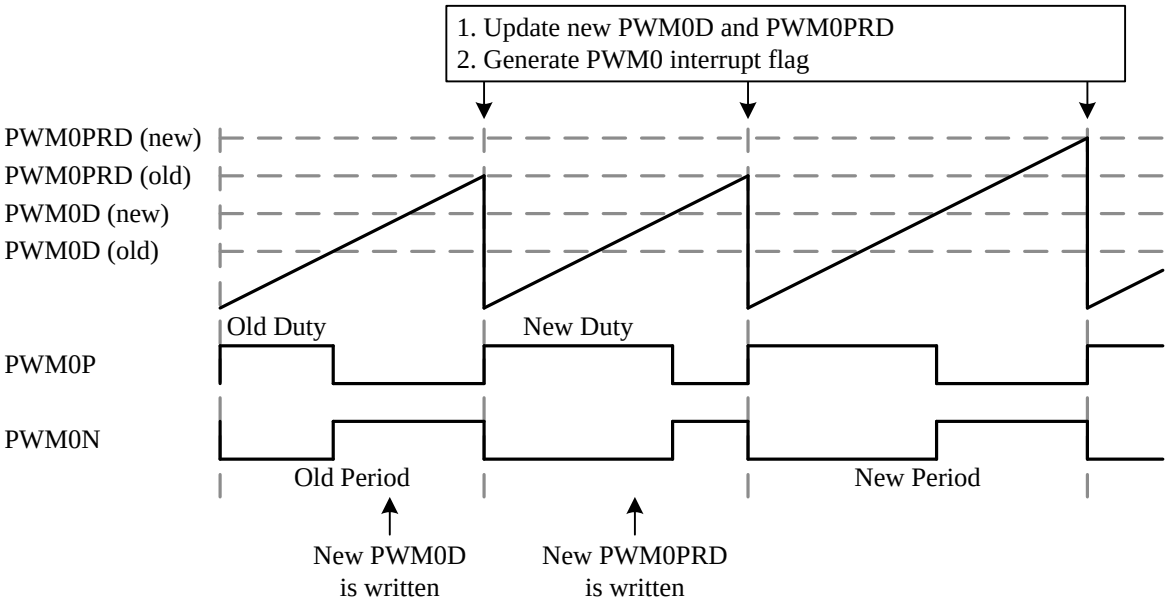
PWM0 Structure

The PWM0 duty cycle can be changed by writing to PWM0DH and PWM0DL. The PWM0 output signal resets to a low level whenever the 16-bit base counter matches the 16-bit PWM0 duty register {PWM0DH, PWM0DL}. The PWM0 period can be set by writing the period value to the PWM0PRDH and PWM0PRDL registers. After writing the PWM0D or PWM0PRD register, the new values will immediately save to their own buffer. H/W will update these values at the end of current period or while PWM0 is cleared. At the end of current period, H/W will set the PWM0IF bit and generate an interrupt if a PWM0 interrupt is enabled.

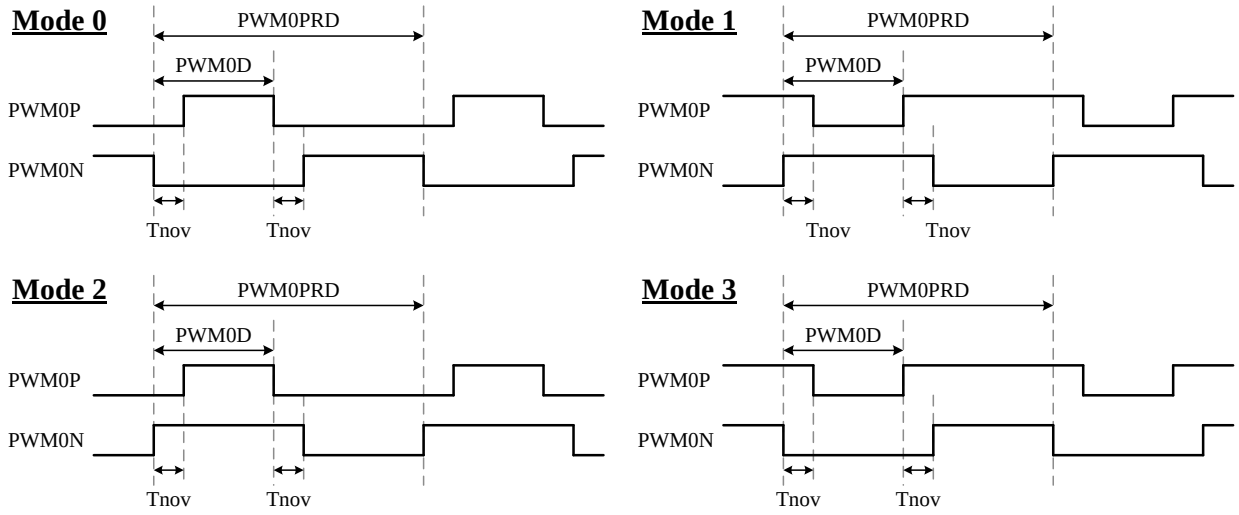
The PWM0 has two operation modes, normal mode and half-bridge mode. PWM0 output signal can be output via PWM0P and PWM0N with four differnet modes. These two outputs are non-overlapped with time interval Tnov. Non-overlapping time interval is also named as dead zone or dead band. Tnov is determined by setting PWM0DZ bits. The value 0~15 of PWM0DZ map onto 0~15, 16 PWM0CLK cycles respectively. If PWM0DZ=0, PWM0 outputs is directly passed to PWM0P and PWM0N so that waveforms of them have the same duty cycle. Note that, if high pulse width or low pulse width of PWM0 output is shorter than Tnov, the real waveforms of these two outputs will different from the expected waveforms. If the PWM0MSKE bit is set, the outputs can be masked to force output fix signal while S/W set the CLRPWM0 bit is set by H/W.

Normal Mode

The normal mode PWM is a simple structure, which switches its output high and low at uniform repeatable intervals. The PWM0D is the output duty cycle, and the output period is PWM0PRD+1. The output waveform of PWM0 is shown below.



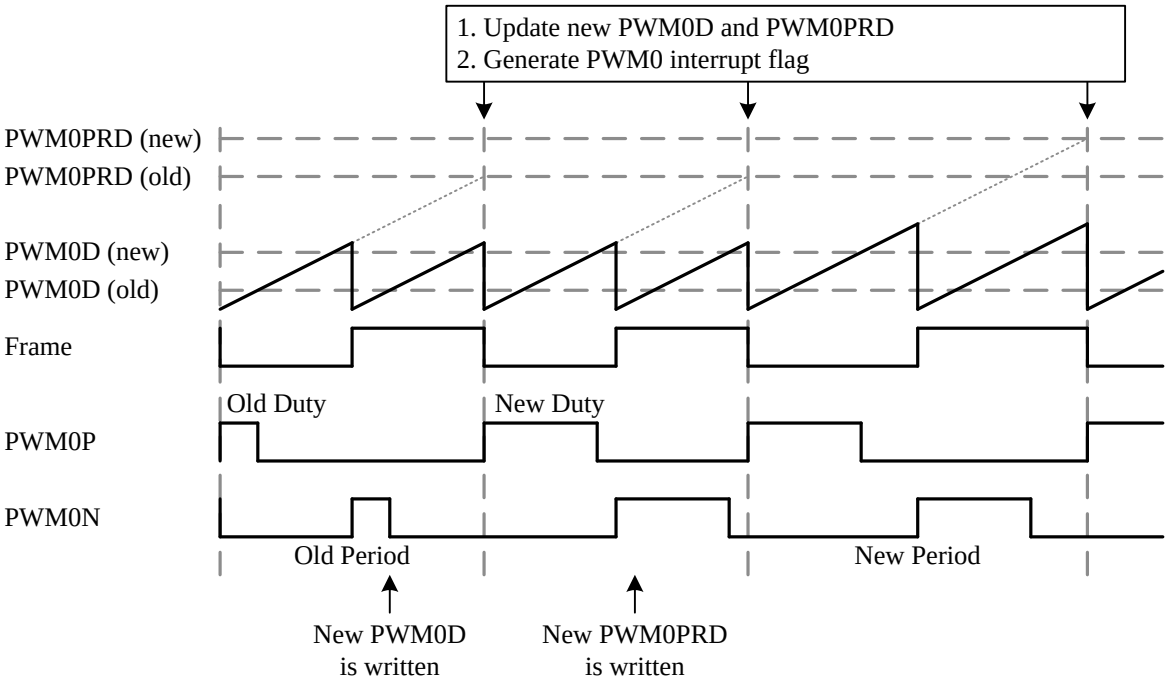
PWM0 normal mode output waveform (PWM0OM=0, PWM0DZ=0)



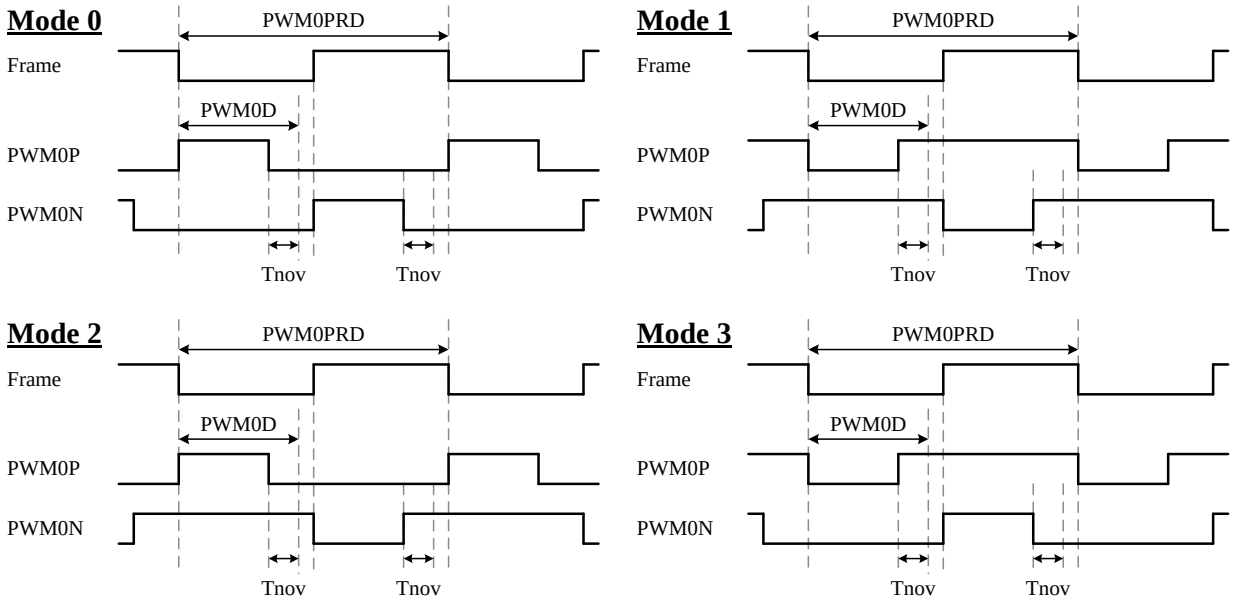
PWM0 normal mode output modes

Half-Bridge Mode

The half-bridge mode PWM is similar to the normal mode but Dead zone is prohibited in half-bridge mode (SFR PWM0DZ must be 0). It has two frames in a period, PWM0P only output in the first frame, PWM0N only output in the second frame. The width of these two frames must be same, so their width is the integer part of PWM0PRD/2. Because each output channel only output in one frame, the maximum duty cycle is same as the width of a frame. If the PWM0D is larger than PWM0PRD/2, H/W will force set the duty cycle to PWM0PRD/2. Following figure shows the output waveform and the output modes.



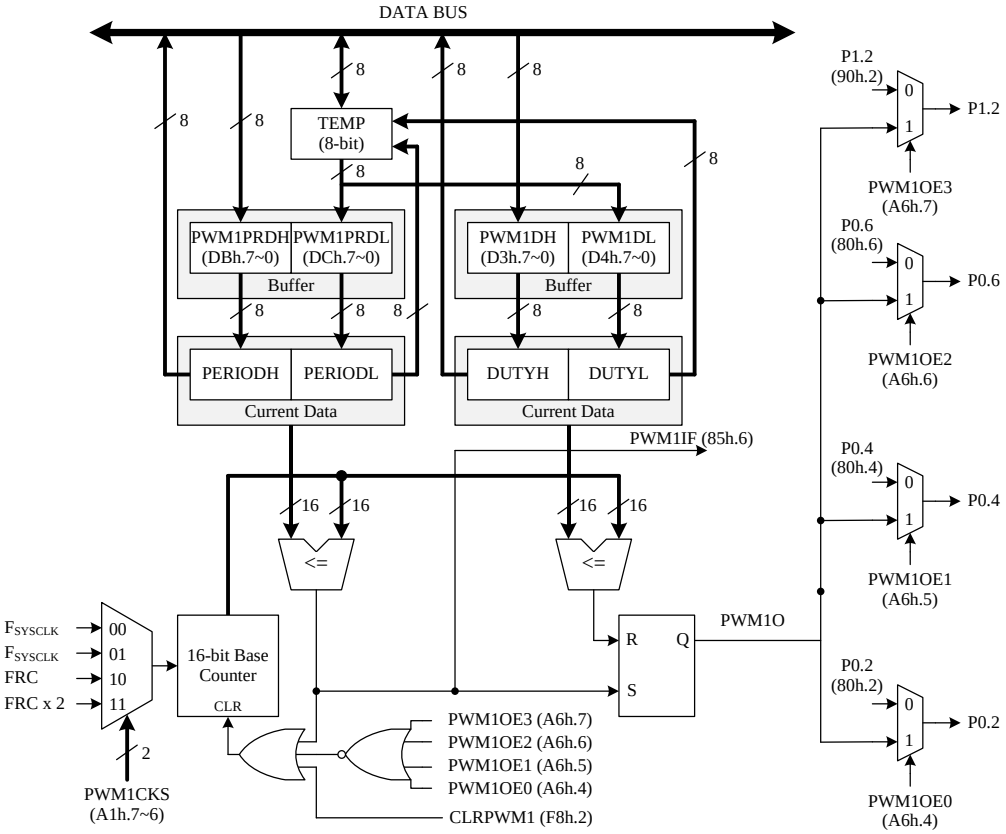
PWM0 half-bridge mode output waveform (PWM0OM=0, PWM0DZ=0)



PWM0 half-bridge mode output modes

PWM1~PWM6

The Chip has six 16-bit PWM modules PWM1~PWM6. PWM1~6 are sharing period, clock source and interrupt (PWM1IF). The following takes PWM1 as an example for description. The PWM can generate varies frequency waveform with 65536 duty resolution on the basis of the PWM clock. The PWM clock can select double frequency (FRC x 2), FRC or F_{SYSCLK} as its clock source.



PWM0 Structure

SFR **84h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE2	–	PWM1IE	PWM0IE	–	–	–	–	–
R/W	–	R/W	R/W	–	–	–	–	–
Reset	–	0	0	–	–	–	–	–

84h.6 **PWM1IE:** PWM1~PWM6 interrupt enable
0: Disable PWM1~PWM6 interrupt
1: Enable PWM1~PWM6 interrupt

84h.5 **PWM0IE:** PWM0 interrupt enable
0: Disable PWM0 interrupt
1: Enable PWM0 interrupt

SFR **85h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG2	–	PWM1IF	PWM0IF	–	–	–	–	–
R/W	–	R/W	R/W	–	–	–	–	–
Reset	–	0	0	–	–	–	–	–

85h.6 **PWM1IF:** PWM1~PWM6 interrupt flag
Set by H/W at the end of PWM1 period, S/W writes BFh to INTFLG2 to clear this flag.

85h.5 **PWM0IF:** PWM0 interrupt enable
Set by H/W at the end of PWM0 period, S/W writes DFh to INTFLG2 to clear this flag.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	–	LVDIE	I2CE	ADIE	EX2	PXIE	TM3IE
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A9h.7 **PWMIE:** PWM0/PWM1~PWM6 interrupt enable
0: Disable PWM0/PWM1~PWM6 interrupt
1: Enable PWM0/PWM1~PWM6 interrupt

SFR **A1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON	PWM1CKS		–	–	PWM0CKS		PWM0NMSK	PWM0PMSK
R/W	R/W		–	–	R/W		R/W	R/W
Reset	0	0	–	–	0	0	0	0

A1h.7~6 **PWM1CKS:** PWM1~PWM6 clock source
00: F_{SYSCLK}
01: F_{SYSCLK}
10: FRC
11: FRCx2 (Vcc>2.7V)

A1h.3~2 **PWM0CKS:** PWM0 clock source
00: F_{SYSCLK}
01: F_{SYSCLK}
10: FRC
11: FRCx2 (Vcc>2.7V)

A1h.1 **PWM0NMSK:** PWM0N mask data while CLRPWM0=1

A1h.0 **PWM0PMSK:** PWM0P mask data while CLRPWM0=1

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE0	PWM1OE3	PWM1OE2	PWM1OE1	PWM1OE0	PWM0NOE1	PWM0POE1	PWM0NOE0	PWM0POE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A6h.7 **PWM1OE3:** PWM1 output control
0: Disable 1: PWM1 enable and output to P1.2

A6h.6 **PWM1OE2:** PWM1 output control
0: Disable 1: PWM1 enable and output to P0.6

A6h.5 **PWM1OE1:** PWM1 output control
0: Disable 1: PWM1 enable and output to P0.4

A6h.4 **PWM1OE0:** PWM1 output control
0: Disable 1: PWM1 enable and output to P0.2

A6h.3 **PWM0NOE1:** PWM0N output control
0: Disable 1: PWM0N enable and output to P3.6

A6h.2 **PWM0POE1:** PWM0P output control
0: Disable 1: PWM0P enable and output to P3.5

A6h.1 **PWM0NOE0:** PWM0N output control
0: Disable 1: PWM0N enable and output to P0.4

A6h.0 **PWM0POE0:** PWM0P output control
0: Disable 1: PWM0P enable and output to P0.3

SFR **A7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON2	PWM0MOD	PWM0MSKE	PWM0OM		PWM0DZ			
R/W	R/W	R/W	R/W		R/W			
Reset	0	0	0	0	0	0	0	0

A7h.7 **PWM0MOD:** PWM0 mode select
0: Normal mode
1: Half-bridge mode

A7h.6 **PWM0MSKE:** PWM0 mask output enable
0: Disable
1: Enable, PWM0P/PWM0N output data by PWM0PMSK/PWM0NMSK while CLRPWM0=1

A7h.5~4 **PWM0OM:** PWM0 output mode select
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A7h.3~0 **PWM0DZ:** PWM0 dead zone (Dead zone is prohibited in half-bridge mode)
0000: 0 x T_{PWMCLK}
0001: 1 x T_{PWMCLK}
...
1111: 15 x T_{PWMCLK}

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE1	PWM4OE3	PWM4OE2	PWM4OE1	PWM4OE0	PWM3OE1	PWM3OE0	PWM2OE1	PWM2OE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B6h.7 **PWM4OE3:** PWM4 output control
0: Disable 1: PWM4 enable and output to P3.6

B6h.6 **PWM4OE2:** PWM4 output control
0: Disable 1: PWM4 enable and output to P1.5

B6h.5 **PWM4OE1:** PWM4 output control
0: Disable 1: PWM4 enable and output to P0.4

B6h.4 **PWM4OE0:** PWM4 output control
0: Disable 1: PWM4 enable and output to P0.0

B6h.3 **PWM3OE1:** PWM3 output control
0: Disable 1: PWM3 enable and output to P3.4

B6h.2 **PWM3OE0:** PWM3 output control
0: Disable 1: PWM3 enable and output to P1.0

B6h.1 **PWM2OE1:** PWM2 output control
0: Disable 1: PWM2 enable and output to P3.6

B6h.0 **PWM2OE0:** PWM2 output control
0: Disable 1: PWM2 enable and output to P1.1

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE2	MSDASEL	MSCLSEL	PWM6OE2	PWM6OE1	PWM6OE0	PWM5OE2	PWM5OE1	PWM5OE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B7h.5 **PWM6OE2:** PWM6 output control
0: Disable 1: PWM6 enable and output to P1.3

B7h.4 **PWM6OE1:** PWM6 output control
0: Disable 1: PWM6 enable and output to P0.7

B7h.3 **PWM6OE0:** PWM6 output control
0: Disable 1: PWM6 enable and output to P0.3

B7h.2 **PWM5OE2:** PWM5 output control
0: Disable 1: PWM5 enable and output to P1.4

B7h.1 **PWM5OE1:** PWM5 output control
0: Disable 1: PWM5 enable and output to P0.6

B7h.0 **PWM5OE0:** PWM5 output control
0: Disable 1: PWM5 enable and output to P0.1

SFR **D1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DH	PWM0DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D1h.7~0 **PWM0DH:** PWM0 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DL	PWM0DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D2h.7~0 **PWM0DL:** PWM0 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DH	PWM1DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D3h.7~0 **PWM1DH:** PWM1 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DL	PWM1DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D4h.7~0 **PWM1DL:** PWM1 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2DH	PWM2DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D5h.7~0 **PWM2DH:** PWM2 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2DL	PWM2DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D6h.7~0 **PWM2DL:** PWM2 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **D9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRDH	PWM0PRDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

D9h.7~0 **PWM0PRDH:** PWM0 period high byte
write sequence: PWMxPRDL then PWMxPRDH
read sequence: PWMxPRDH then PWMxPRDL

SFR **DAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRDL	PWM0PRDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DAh.7~0 **PWM0PRDL:** PWM0 period low byte
write sequence: PWMxPRDL then PWMxPRDH
read sequence: PWMxPRDH then PWMxPRDL

SFR **DBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRDH	PWM1PRDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DBh.7~0 **PWM1PRDH:** PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 period high byte
write sequence: PWMxPRDL then PWMxPRDH
read sequence: PWMxPRDH then PWMxPRDL

SFR **DCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRDL	PWM1PRDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DCh.7~0 **PWM1PRDL:** PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 period low byte
write sequence: PWMxPRDL then PWMxPRDH
read sequence: PWMxPRDH then PWMxPRDL

SFR **DDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3DH	PWM3DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

DDh.7~0 **PWM3DH:** PWM3 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **DEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3DL	PWM3DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

DEh.7~0 **PWM3DL:** PWM3 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **E9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM4DH	PWM4DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

E9h.7~0 **PWM4DH:** PWM4 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **EAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM4DL	PWM4DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

EAh.7~0 **PWM4DL:** PWM4 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **EBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM5DH	PWM5DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

EBh.7~0 **PWM5DH:** PWM5 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **ECh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM5DL	PWM5DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

ECh.7~0 **PWM5DL:** PWM5 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **EDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM6DH	PWM6DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

EDh.7~0 **PWM6DH:** PWM6 duty high byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **EEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM6DL	PWM6DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

EEh.7~0 **PWM6DL:** PWM6 duty low byte
write sequence: PWMxDL then PWMxDH
read sequence: PWMxDH then PWMxDL

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	VBGEN	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.3 **CLRPWM0:** PWM0 clear enable
0: PWM0 is running
1: PWM0 is cleared and held

F8h.2 **CLRPWM1:** PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 clear enable
0: PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 is running
1: PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 is cleared and held

10. Low Voltage Detection (LVD)

The chip also provides a low voltage detection (LVD) function, and the SFR LVDSEL can select 15 LVDs with different voltage thresholds.

Operation Mode	PWRSAV (SFR F7.5)	LVDSEL (SFR E4h.3~0)	LVD	Function	Note
X	X	0000	OFF		
Fast/Slow	X	0001	ON	LVD 2.40V	
		0010	ON	LVD 2.55V	
		0011	ON	LVD 2.65V	
		0100	ON	LVD 2.80V	
		0101	ON	LVD 2.95V	
		0110	ON	LVD 3.10V	
		0111	ON	LVD 3.25V	
		1000	ON	LVD 3.40V	
		1001	ON	LVD 3.55V	
		1010	ON	LVD 3.70V	
		1011	ON	LVD 3.85V	
		1100	ON	LVD 4.00V	
		1101	ON	LVD 4.15V	
		1110	ON	LVD 4.30V	
		1111	ON	LVD 4.45V	
Idle/Halt/Stop	0	0001	ON	LVD 2.40V	
		0010	ON	LVD 2.55V	
		0011	ON	LVD 2.65V	
		0100	ON	LVD 2.80V	
		0101	ON	LVD 2.95V	
		0110	ON	LVD 3.10V	
		0111	ON	LVD 3.25V	
		1000	ON	LVD 3.40V	
		1001	ON	LVD 3.55V	
		1010	ON	LVD 3.70V	
		1011	ON	LVD 3.85V	
		1100	ON	LVD 4.00V	
		1101	ON	LVD 4.15V	
		1110	ON	LVD 4.30V	
		1111	ON	LVD 4.45V	
Idle/Halt/Stop	1	xxxx	OFF	LVD disable	Minimum current consumption About 0.1uA

Low voltage detect table

SFR **E4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDCON	–	–	–	LVDIF	LVDSEL			
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

E4h.4 **LVDIF :** LVD interrupt flag, write 0 to clear this bit

E4h.3~0 **LVDSEL:** Low Voltage detect select

0000: LVD disable
0001: Set LVD at 2.40V
0010: Set LVD at 2.55V
0011: Set LVD at 2.65V
0100: Set LVD at 2.80V
0101: Set LVD at 2.95V
0110: Set LVD at 3.10V
0111: Set LVD at 3.25V
1000: Set LVD at 3.40V
1001: Set LVD at 3.55V
1010: Set LVD at 3.70V
1011: Set LVD at 3.85V
1100: Set LVD at 4.00V
1101: Set LVD at 4.15V
1110: Set LVD at 4.30V
1111: Set LVD at 4.45V

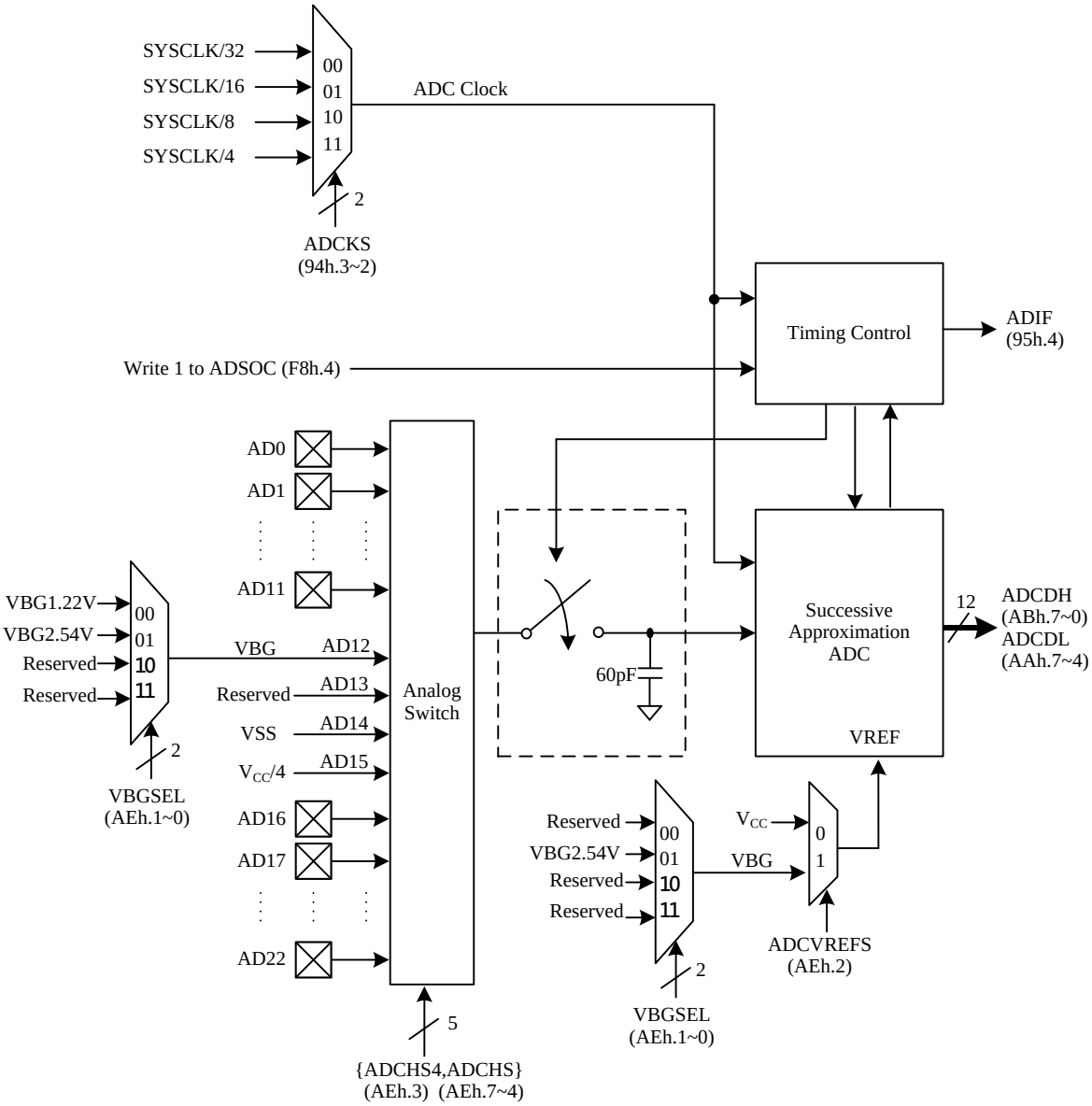
SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	1	1	0

F7h.5 Set 1 to reduce the chip's power consumption at Idle/Halt/Stop Mode

11. ADC

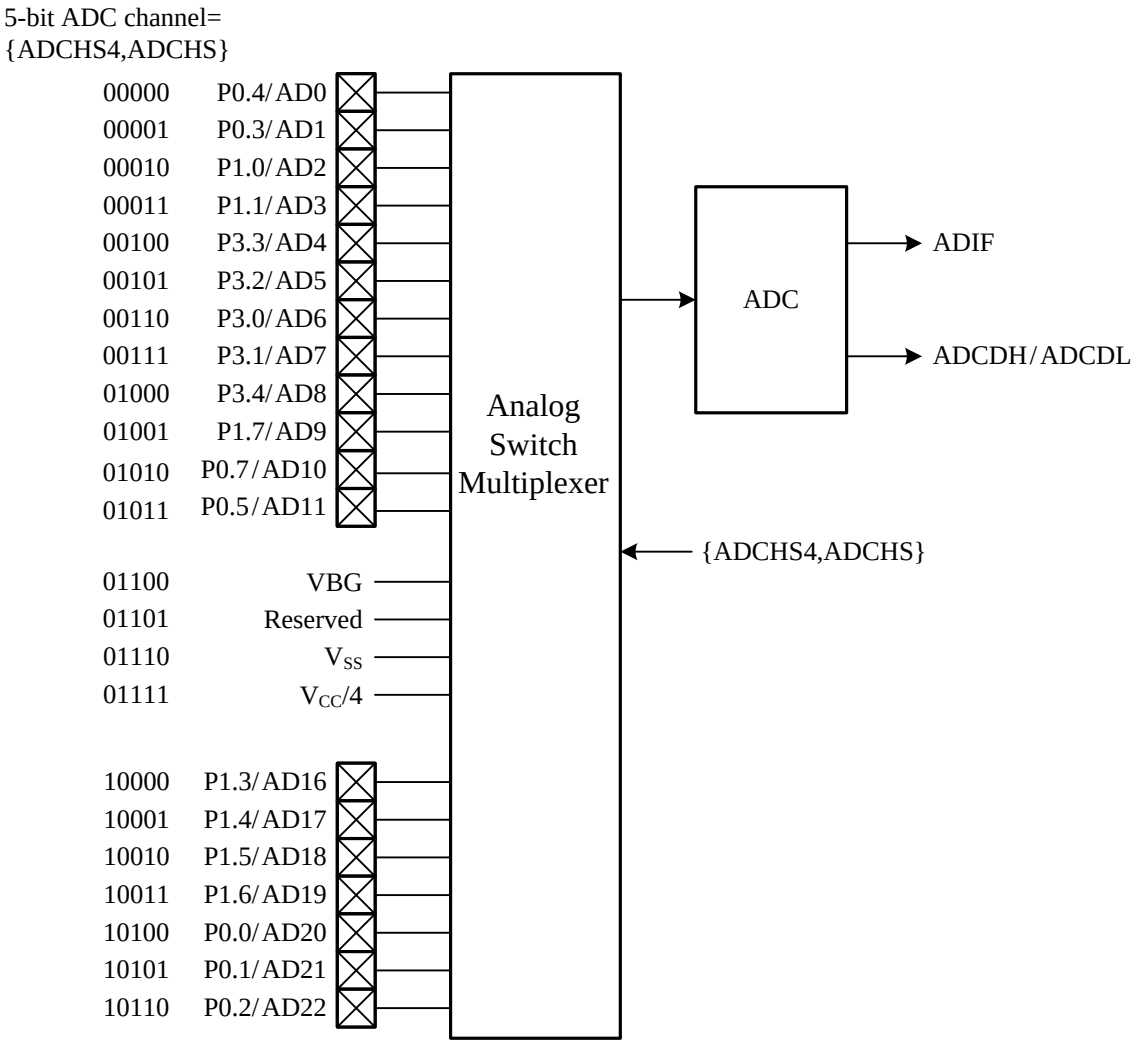
The Chip offers a 12-bit ADC consisting of a 19-channel analog input multiplexer, control register, clock generator, 12-bit successive approximation register, and output data register. To use the ADC, set the ADCKS bits first to choose a proper ADC clock frequency, which must be less than 1 MHz. Then, launch the ADC conversion by setting the ADSOC bit, and H/W will automatic clear it at the end of the conversion. After the end of the conversion, H/W will set the ADIF bit and generate an interrupt if an ADC interrupt is enabled. The ADIF bit can be cleared by writing 0 to this bit or 1 to the ADSOC bit. The analog input level must remain within the range from V_{SS} to V_{CC}.

Using the ADCVREFS option, the ADC internal reference voltage source (VREF) can be selected as V_{CC} or VBG 2.54V. When ADCVREFS=1, VBGSEL must be set to 2'b01.



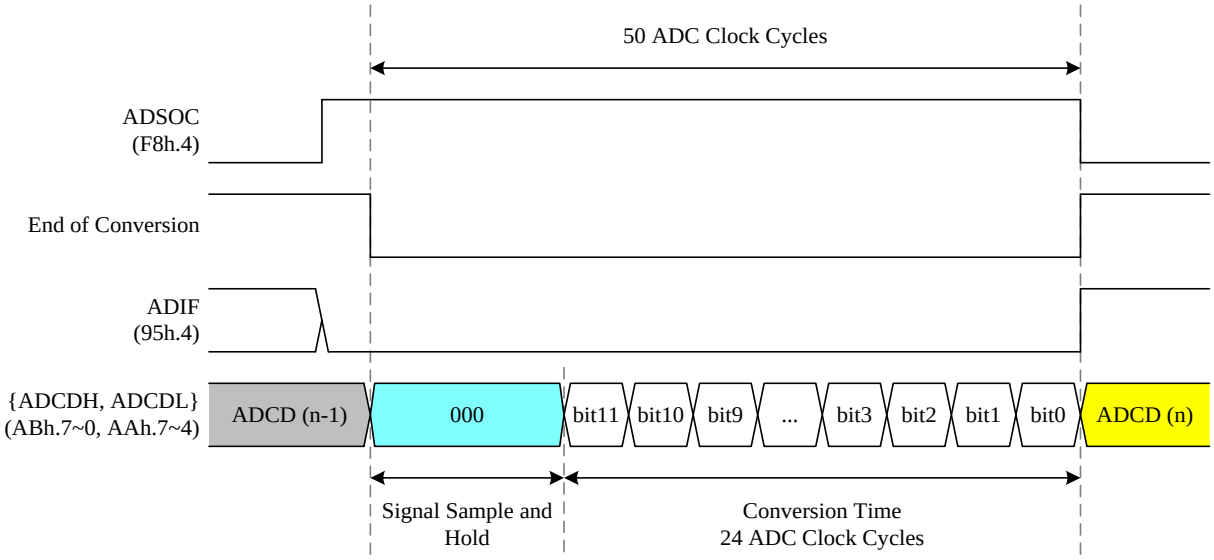
ADC Channels

The ADC channels are connected to the analog input pins via the analog switch multiplexer. The analog switch multiplexer is controlled by the ADCHS4 and ADCHS register. The Chip offers up to 19 IO input pins, designated AD0~AD11, AD16~AD22. In addition, there are 3 internal reference voltages (VBG, VSS, VCC/4). When ADCHS is set to 1110b, the analog input will connect to V_{SS}, and when ADCHS is set to 1100b, the analog input will connect to VBG.



ADC Conversion Time

The conversion time is the time required for the ADC to convert the voltage. The ADC requires two ADC clock cycles to convert each bit and several clock cycles to sample and hold the input voltage. A total of 50 ADC clock cycles are required to perform the complete conversion. When the conversion time is complete, the ADIF interrupt flag is set by H/W, and the result is loaded into the ADCDH and ADCDL registers of the 12-bit A/D result.



SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	-	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	-	R/W		R/W		R/W	
Reset	0	-	0	0	0	0	0	0

94h.3~2 **ADCKS:** ADC clock rate select

00: $F_{SYSCLK}/32$
01: $F_{SYSCLK}/16$
10: $F_{SYSCLK}/8$
11: $F_{SYSCLK}/4$

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	ADIF	–	IE2	PXIF	TF3
R/W	–	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

95h.4 **ADIF:** ADC interrupt flag

Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag. (***Note1***)

SFR **AAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDL	ADCDL				–	–	–	–
R/W	R				–	–	–	–
Reset	–	–	–	–	–	–	–	–

AAh.7~4 **ADCDL:** ADC data bit 3~0

SFR **ABh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDH	ADCDH							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ABh.7~0 **ADCDH:** ADC data bit 11~4

SFR **AEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHSEL	ADCHS				ADCH4	ADCVREFS	VBGSEL	
R/W	R/W				R/W	R/W	R/W	
Reset	1	1	1	1	0	0	0	0

AEh.7~4 **ADCHS:** 5-bit ADC channel select = {ADCHS4,ADCHS}.

00000: ADC0 (P04) 01100: VBGO
00001: ADC1 (P03) 01101: Reserved
00010: ADC2 (P10) 01110: VSS
00011: ADC3 (P11) 01111: 1/4VCC
00100: ADC4 (P33) 10000: ADC16 (P13)
00101: ADC5 (P32) 10001: ADC17 (P14)
00110: ADC6 (P30) 10010: ADC18 (P15)
00111: ADC7 (P31) 10011: ADC19 (P16)
01000: ADC8 (P34) 10100: ADC20 (P00)
01001: ADC9 (P17) 10101: ADC21 (P01)
01010: ADC10 (P07) 10110: ADC22 (P02)
01011: ADC11 (P05) 10111: Reserved

AEh. 3 **ADCHS4:** 5-bit ADC channel select = {ADCHS4,ADCHS}.

AEh.2 **ADCVREFS:** ADC reference voltage select

0: V_{CC}
1: VBG

AEh.1~0 **VBGSEL:** VBG voltage select

When ADCVREF is selected as VBG, VBGSEL is prohibited from using 1.22V.

00: 1.22V
01: 2.54V (need V_{CC}>2.8V)
10: Reserved
11: Reserved

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	VBGEN	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W
Reset	0	0	0	0	1	1	–	0

F8h.5 **VBGEN**: force VBG generator enable

0: VBG generator is automatically enable and disable
1: Force VBG generator enable except in IDLE/HALT/STOP mode.

F8h.4 **ADSOC:** Start ADC conversion

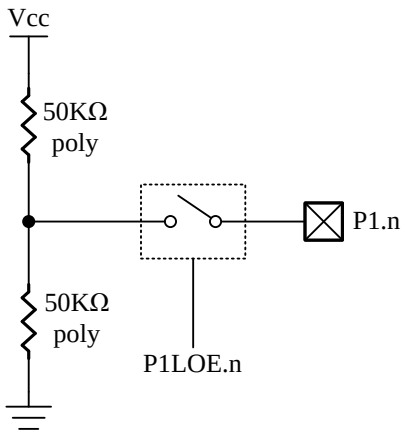
Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

Note: See also Chapter 5 for more information on ADC interrupt enable and priority.

Note: Also refer to Chapter 6 for details on ADC pin input settings.

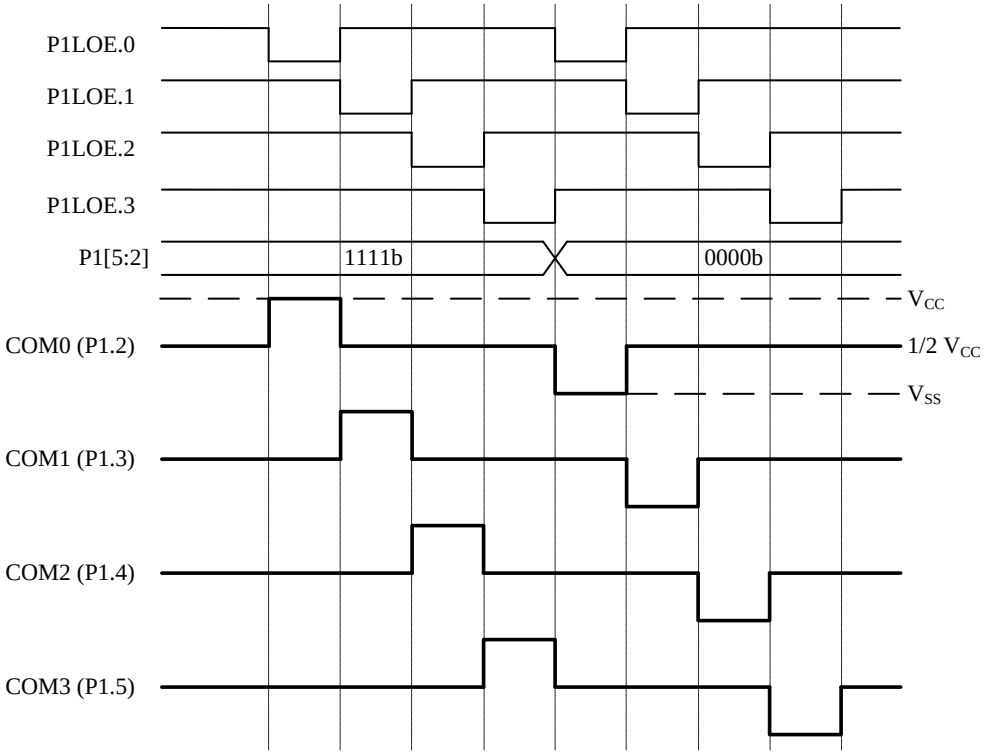
12. S/W Controller LCD Driver

The chip supports an S/W controlled method to driving LCD. It is capable of driving the LCD panel with 88 dots (Max.) by 4 Commons (COM) and 22 Segments (SEG). The P1.2~P1.5 are used for Common pins COM0~COM3 and others pins can be used for Segment pins. COM0~COM3 are capable of driving 1/2 bias when P1.2~P1.5's P1LOE=1. Refer to the following figures.



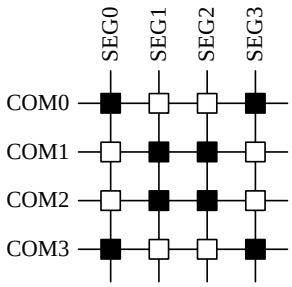
LCD COM0~3 Circuit

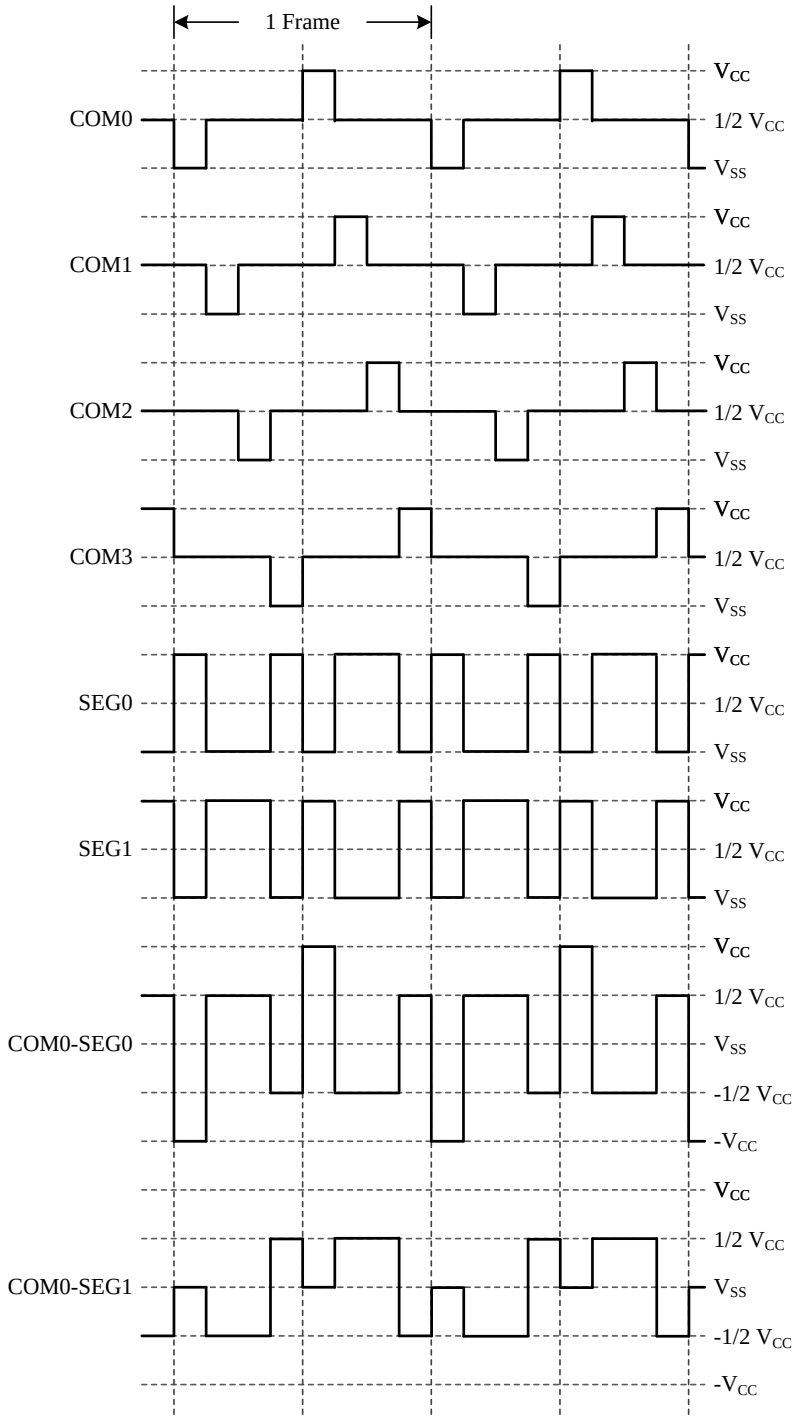
The frequency of any repeating waveform output on the COM pin can be used to represent the LCD frame rate. The figure below shows an LCD frame.



S/W Controlled LCD COM0~3 Scanning

1/4 Duty, 1/2 Bias Output Waveform





SFR **92h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1LOE	–	–	–	–	P1LOE3	P1LOE2	P1LOE1	P1LOE0
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

92h.3 **P1LOE3:** LCD 1/2 bais Output
0: Disable
1: P15 as LCD 1/2 bais Output

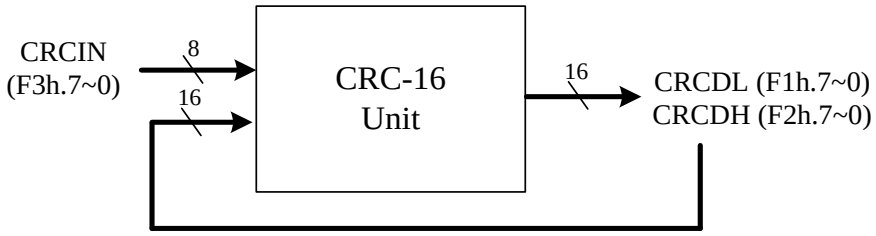
92h.2 **P1LOE2:** LCD 1/2 bais Output
0: Disable
1: P14 as LCD 1/2 bais Output

92h.1 **P1LOE1:** LCD 1/2 bais Output
0: Disable
1: P13 as LCD 1/2 bais Output

92h.0 **P1LOE0:** LCD 1/2 bais Output
0: Disable
1: P12 as LCD 1/2 bais Output

13. Cyclic Redundancy Check (CRC)

The chip supports an integrated 16-bit Cyclic Redundancy Check function. The Cyclic Redundancy Check (CRC) calculation unit is an error detection technique test algorithm and uses to verify data transmission or storage data correctness. The CRC calculation takes a 8-bit data stream or a block of data as input and generates a 16-bit output remainder. The data stream is calculated by the same generator polynomial.



CRC Block Diagram

The CRC generator provides the 16-bit CRC result calculation based on the CRC-16-IBM polynomial. In this CRC generator, there are only one polynomial available for the numeric values calculation. It can't support the 16-bit CRC calculations based on any other polynomials. Each write operation to the CRCIN register creates a combination of the previous CRC value stored in the CRCDH and CRCDL registers. It will take one MCU instruction cycle to calculate.

CRC-16-IBM (Modbus) Polynomial representation: $X^{16} + X^{15} + X^2 + 1$

SFR **F1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDL	CRCDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

F1h.7~0 **CRCDL:** 16-bit CRC checksum data bit 7~0

SFR **F2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDH	CRCDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

F2h.7~0 **CRCDL:** 16-bit CRC checksum data bit 15~8

SFR **F3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCIN	CRCIN							
W	W							
Reset	–	–	–	–	–	–	–	–

F3h.7~0 **CRCIN:** CRC input data register

14. Multiplier and Divider

The chip provide multiplier and divider have the following functions. The 8 bit operation is fully compatible with industry standard 8051.

- 8 bits × 8 bits = 16 bit (standard 8051)
- 8 bits ÷ 8 bits = 8 bits, 8 bits remainder (standard 8051)
- 16 bits × 16 bits = 32 bit
- 16 bits ÷ 16 bits = 16 bits, 16 bits remainder
- 32 bits ÷ 16 bits = 32 bits, 16 bits remainder

No matter 8bit / 16bit / 32bit operation, it's easy to execute by MUL AB and DIV AB instruction. There is extra SFR EXA/EXA2/EXA3/EXB for 16bit / 32bit multiply and divide operation.

For 8 bit multiplier/divider operation, be sure SFR bit muldiv16=0 and div32=0.

For 16 bit multiplier operation, multiplicand, multiplier and product as follows. 16 bit multiplier takes 16 System clock cycles to execute.

Condition	**SFR bit muldiv16=1 and div32=0**			
Multiplication	**Byte3**	**Byte2**	**Byte1**	**Byte0**
Multiplicand	-	-	EXA	A
Multiplier	-	-	EXB	B
Product	EXB	B	A	EXA
OV	Product (EXB or B) !=0		-	-

For 16 bit divider operation, dividend, divisor, quotient, remainder read as follows. 16 bit divider takes 16 System clock cycles to execute.

Condition	**SFR bit muldiv16=1 and div32=0**			
Division	**Byte3**	**Byte2**	**Byte1**	**Byte0**
Dividend	-	-	EXA	A
Divisor	-	-	EXB	B
Quotient	-	-	A	EXA
Remainder	-	-	B	EXB
OV	Divisor EXB = B =0			

For 32 bits ÷ 16 bits operation, dividend, divisor, quotient, remainder read as follows. 32 bit divider takes 32 System clock cycles to execute.

Condition	**SFR bit muldiv16=1 and div32=1**			
Division	**Byte3**	**Byte2**	**Byte1**	**Byte0**
Dividend	EXA3	EXA2	EXA	A
Divisor	-	-	EXB	B
Quotient	A	EXA	EXA2	EXA3
Remainder	-	-	B	EXB
OV	Divisor EXB=B =0			

SFR **CEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA2	EXA2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CEh.7~0 **EXA2:** Expansion accumulator 2

SFR **CFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA3	EXA3							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CFh.7~0 **EXA3:** Expansion accumulator 3

SFR **E6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXA	EXA							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E6h.7~0 **EXA:** Expansion accumulator

SFR **E7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXB	EXB							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E7h.7~0 **EXB:** Expansion B register

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0	0	0

F7h.3 **DIV32:**
only active when MULDVI16 =1
0: instruction DIV as 16/16 bit division operation
1: instruction DIV as 32/16 bit division operation

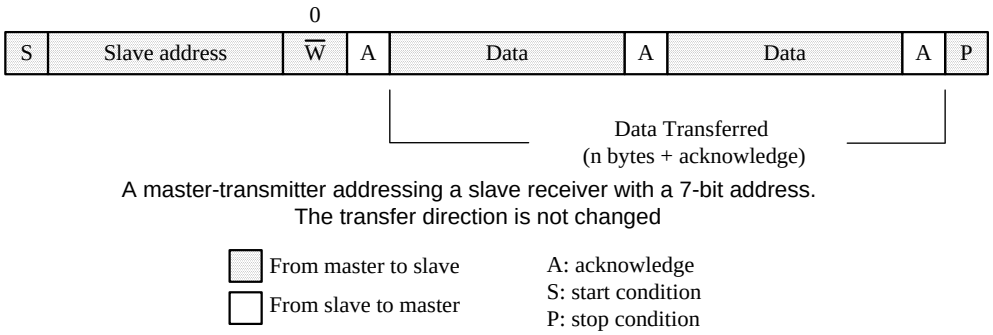
F7h.0 **MULDIV16:**
0: instruction MUL/DIV as 8*8, 8/8 operation
1: instruction MUL/DIV as 16*16, 16/16 or 32/16 operation

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MUL AB	Multiply A by B	1	8/16	A4
DIV AB	Divide A by B	1	8/16/32	84

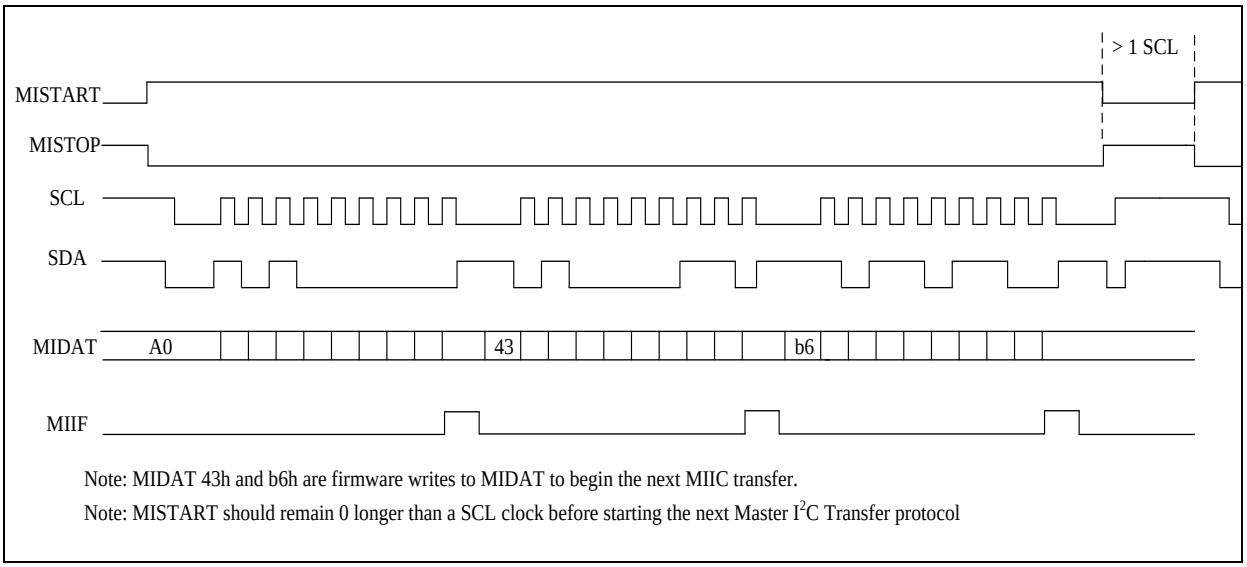
15. Master I²C Interface

Master I²C interface Transmitter mode:
At the beginning write slave address and direction bit to MIDAT and set MISTART. After the START condition (MISTART), the 7 bits slave address and one bit direction bit are sent. When MIIF convert to 1, address and direction bit transmission was complete. After sending the address and direction bit, user should clear MIIF and write MIDAT to start first data transmission. When MIIF convert to 1, data transfer to slave was complete. User can write MIDAT again to transfer next data to slave. Set MISTOP to finish transmitter mode.

MISTART must remain at 1 for the next transfer. After final data transmit/receive, set MISTOP to finish transmit/receive protocol. MISTART should remain 0 longer than a SCL clock before starting the next Master I²C protocol. SCL clock can be adjusted via MICR.



Master I²C Transmit flow:
(1) Write slave address and direction bit to MIDAT
(2) Clear MISTOP and set MISTART to start I²C transmission
(3) Wait until MIIF converter to 1 (interrupt will be issued according to the user's request) and Clear MIIF
(4) Write data to MIDAT to start next transfer (MISTART must remain at 1)
(5) Wait until MIIF converter to 1 (interrupt will be issued according to the user's request) and Clear MIIF, Loop (3) ~(4) for next transfer.
(6) Clear MISTART and set MISTOP to stop the I²C transfer



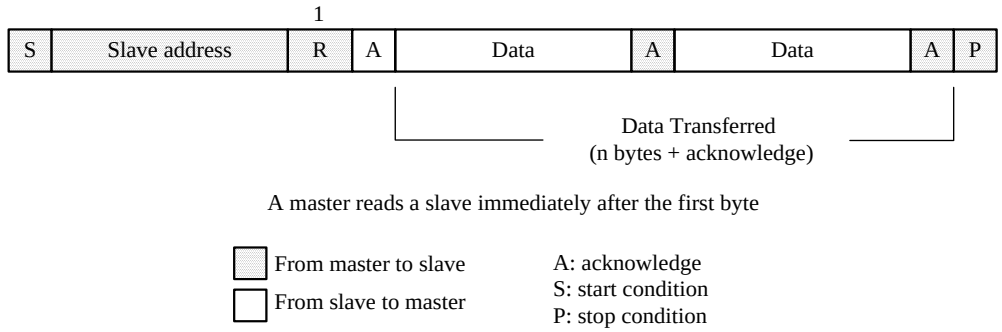
Master Transmit Timing

Note: MISTART should remain 0 longer than a SCL period before starting the next Master I²C protocol.

Master I²C interface Receive mode:

At the beginning write slave address and direction bit to MIDAT and set MISTART. After the START condition (MISTART), the 7 bits slave address and one bit direction bit are sent. When MIIF convert to 1, address and direction bit transmission was complete. After sending the address and direction bit, user should clear MIIF and read MIDAT to start first receive data (The first reading of MIDAT does not represent the data returned by the slave). When MIIF convert to 1, data receive from slave was complete. User can read MIDAT to get data from slave, and start next receive. Set MISTOP to finish receive mode.

MISTART must remain at 1 for the next transfer. After final data transmit/receive, set MISTOP to finish transmit/receive protocol. MISTART should remain 0 longer than a SCL clock before starting the next Master I²C protocol. SCL clock can be adjusted via MICR.



Master I²C Receive flow:

(1) Write slave address and direction bit to MIDAT

(2) Clear MISTOP and set MISTART to start I²C transmission

(3) Wait until MIIF converter to 1 (interrupt will be issued according to the user's request)

(4) Clear MIIF

(5) Read data from MIDAT to start first receive data

(The first reading of MIDAT does not represent the data returned by the slave)

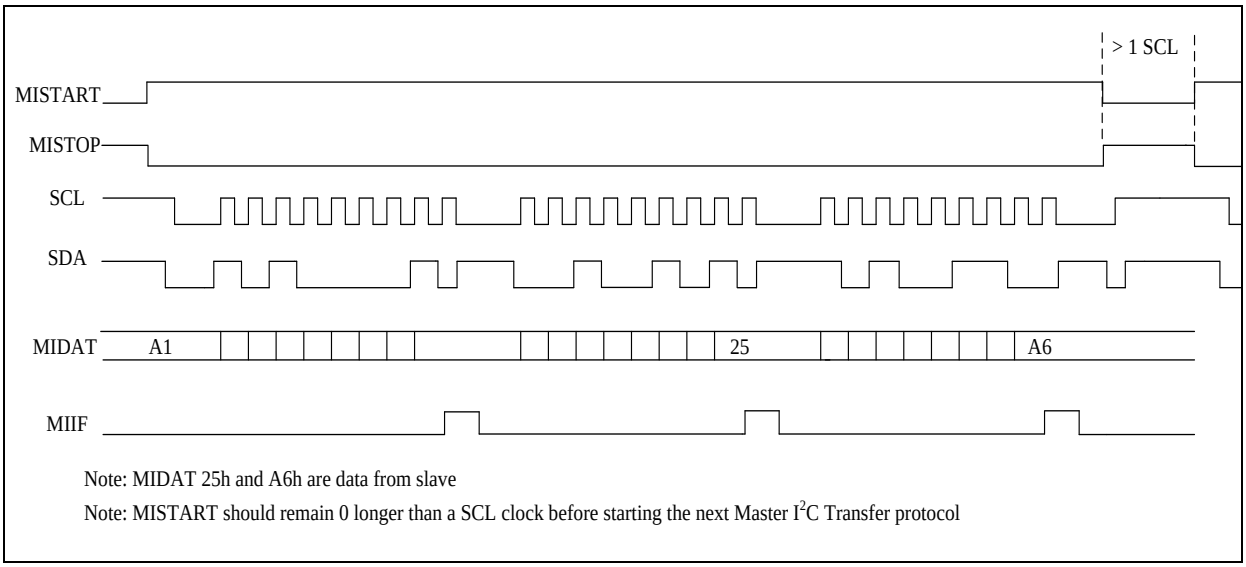
(6) Wait until MIIF converter to 1

(7) Clear MIIF

(8) Read slave data from MIDAT and receive next data

(9) Loop (6) ~(8)

(10) Set MISTOP to stop the I²C transfer



Note: MIDAT 25h and A6h are data from slave

Note: MISTART should remain 0 longer than a SCL clock before starting the next Master I^2C Transfer protocol

Master Receive Timing

Alternative Function	**Mode**	P1/P3 SFR data	Pin State	Other necessary SFR setting
SCL (I^2C Master)	**0**	X	I^2C Clock Output (Open Drain Output, Pull-up)	MSCLSEL
	2	X	I^2C Clock Output (CMOS Push-Pull)	
SDA (I^2C Master)	**0**	1	I^2C DATA (Pull-up)	MSDASEL

Alternative Function	P0OE.n	P0 SFR data	Pin State	other necessary SFR setting
SCL (I^2C Master)	0	X	I^2C Clock Output (Open Drain Output, Pull-up)	MSCLSEL
	1	X	I^2C Clock Output (CMOS Push-Pull)	

Pin Mode Setting for Master I^2C

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	–	LVDIE	I2CE	ADIE	EX2	PXIE	TM3IE
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A9h.4 **I2CE:** I²C interrupt enable
0: Disable I²C interrupt 1: Enable I²C interrupt

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE2	MSDASEL	MSCLSEL	PWM6OE2	PWM6OE1	PWM6OE0	PWM5OE2	PWM5OE1	PWM5OE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B7h.7 **MSDASEL:** Master I^2C SDA select
0: P3.5 as Master I^2C SDA
1: P1.6 as Master I^2C SDA

B7h.6 **MSCLSEL:** Master I^2C SCL select
0: P1.3 as Master I^2C SCL
1: P0.2 as Master I^2C SCL

SFR **E1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MICON	MIEN	MIACKO	MIIF	MIACKI	MISTART	MISTOP	MICR	
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

E1h.7 **MIEN**:Master I^2C enable
0: disable 1: enable

E1h.6 **MIACKO**: When Master I^2C receive data, send acknowledge to I^2C Bus
0: ACK to slave device 1: NACK to slave device

E1h.5 **MIIF**: Master I^2C Interrupt flag
0: write 0 to clear it
1: Master I^2C transfer one byte complete

E1h.4 **MIACKI**: When Master I^2C transfer, acknowledgement form I^2C bus (read only)
0: ACK received 1: NACK received

E1h.3 **MISTART**: Master I^2C Start bit
1: start I^2C bus transfer

E1h.2 **MISTOP**: Master I^2C Stop bit
1: send STOP signal to stop I^2C bus

E1h.1~0 **MICR:** Master I^2C (SCL) clock frequency selection
00: Fsys/4 (ex. If Fsys=16MHz, I^2C clock is 4M Hz)
01: Fsys/16 (ex. If Fsys=16MHz, I^2C clock is 1M Hz)
10: Fsys/64 (ex. If Fsys=16MHz, I^2C clock is 250K Hz)
11: Fsys/256 (ex. If Fsys=16MHz, I^2C clock is 62.5K Hz)

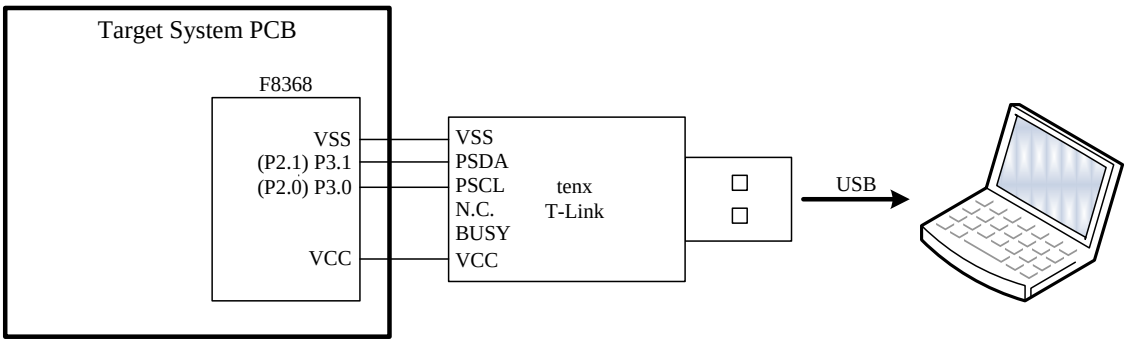
SFR **E2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIDAT	MIDAT							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

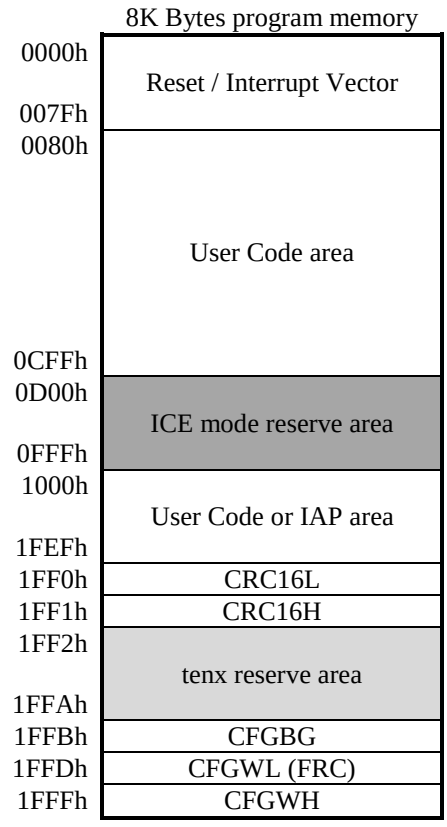
E2h.7~0 **MIDAT**: Master I^2C data shift register
(W):After Start and before Stop condition, write this register will resume transmission to I^2C bus
(R): After Start and before Stop condition, read this register will resume receiving from I^2C bus

16. In Circuit Emulation (ICE) Mode

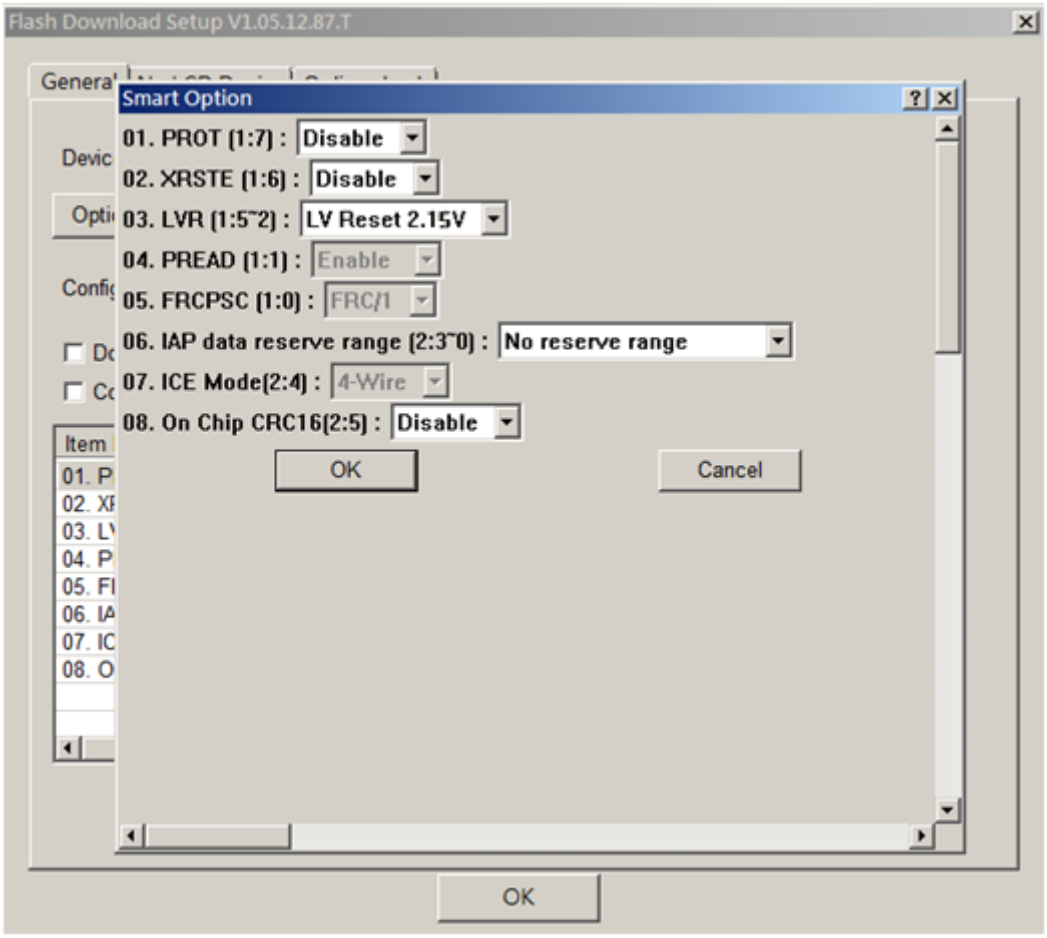
This device can support the In Circuit Emulation Mode. To use the ICE Mode, user just needs to connect P3.0 and P3.1 pin to the tenx proprietary EV Module. The benefit is that user can emulate the whole system without changing the on board target device. But there are some limits for the ICE mode as below.

1. The device must be un-protect.
2. The device's P3.0 and P3.1 pins must work in input Mode (P3MOD0 = 0/1 and P3MOD1=0/1).
3. The Program Memory's addressing space 0D00h~0FFFh and 0033h~003Ah are occupied by tenx EV module. So user Program cannot access these spaces.
4. The T-Link communication pin's function cannot be emulated.
5. The P3.0 and P3.1 pin's can be replaced by P2.0 and P2.1. (Only emulation can be replaced, mass production writer only supports P3.0/P3.1)





ICE tool settings introduction



No.	Item	Description
01	PROT	**Enable:** Flash code is protect, Writer cannot access the ROM code **Disable:** Flash code is not protect, Writer can access the ROM code (default)
02	XRSTE	**Enable:** P3.7 is external reset pin **Disable:** P3.7 is normal I/O pin (default)
03	LVRE	**16-level Low Voltage Reset select** 0000: Set LVR at 2.15V 1000: Set LVR at 3.30V 0001: Set LVR at 2.30V 1001: Set LVR at 3.45V 0010: Set LVR at 2.45V 1010: Set LVR at 3.60V 0011: Set LVR at 2.55V 1011: Set LVR at 3.75V 0100: Set LVR at 2.70V 1100: Set LVR at 3.90V 0101: Set LVR at 2.85V 1101: Set LVR at 4.05V 0110: Set LVR at 3.00V 1110: Set LVR at 4.20V 0111: Set LVR at 3.15V 1111: Set LVR at 4.35V
04	PREAD	Reserved
05	FRCPSC	Reserved
06	IAP data reserve range	IAP-allow area range select
07	ICE Mode	Reserved
08	On Chip CRC16	**Enable:** On chip CRC-16 function enable **Disable:** On chip CRC-16 function disable (default)

SFR & CFGW MAP

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	0000-0000	**P0**	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	**SP**	SP							
82h	0000-0000	**DPL**	DPL							
83h	0000-0000	**DPH**	DPH							
84h	x00x-xxxx	**INTE2**	–	PWM1IE	PWM0IE	–	–	–	–	–
85h	x00x-xxxx	**INTFLG2**	–	PWM1IF	PWM0IF	–	–	–	–	–
87h	0xxx-0000	**PCON**	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	**TMOD**	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	**TL0**	TL0							
8Bh	0000-0000	**TL1**	TL1							
8Ch	0000-0000	**TH0**	TH0							
8Dh	0000-0000	**TH1**	TH1							
90h	1111-1111	**P1**	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
91h	0000-0000	**P0OE**	P0OE							
92h	xxxx-0000	**P1LOE**	–	–	–	–	P1LOE			
93h	0000-0101	**PINMOD**	TXRXSEL	T2OE	T1OE	T0OE	P2MOD1		P2MOD0	
94h	0000-0000	**OPTION**	UART1W	–	WDTPSC		ADCKS		TM3PSC	
95h	xxx0-x000	**INTFLG**	–	–	–	ADIF	–	IE2	PXIF	TF3
96h	0000-0000	**P1WKUP**	P1WKUP							
97h	xxxx-xx00	**SWCMD**	IAPALL / SWRST / WDTO							
98h	0000-0000	**SCON**	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	**SBUF**	SBUF							
A0h	1111-1111	**P2**	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
A1h	00xx-0000	**PWMCON**	PWM1CKS		–	–	PWM0CKS		PWM0NMSK	PWM0PMSK
A2h	0101-0101	**P1MODL**	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
A3h	0101-0101	**P1MODH**	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
A4h	0101-0101	**P3MODL**	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
A5h	0101-0101	**P3MODH**	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
A6h	0000-0000	**PWMOE0**	PWM1OE3	PWM1OE2	PWM1OE1	PWM1OE0	PWM0NOE1	PWM0POE1	PWM0NOE0	PWM0POE0
A7h	0000-0000	**PWMCON2**	PWM0MOD	PWM0MSKE	PWM0OM		PWM0DZ			
A8h	0x00-0000	**IE**	EA	–	ET2	ES	ET1	EX1	ET0	EX0
A9h	xx00-0000	**INTE1**	PWMIE	–	LVDIE	I2CE	ADIE	EX2	PXIE	TM3IE
AAh	xxxx-xxxx	**ADCDL**	ADCDL				–	–	–	–
ABh	xxxx-xxxx	**ADCDH**	ADCDH							
AEh	1111-x000	**CHSEL**	ADCHS				ADCHS4	ADCVREFS	VBGSEL	
AFh	0000-0000	**P0DIE**	P0DIE							
B0h	1111-1111	**P3**	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
B6h	0000-0000	**PWMOE1**	PWM4OE3	PWM4OE2	PWM4OE1	PWM4OE0	PWM3OE1	PEM3OE0	PWM2OE1	PWM2OE0
B7h	0000-0000	**PWMOE2**	MSDASEL	MSCLSEL	PWM6OE2	PWM6OE1	PWM6OE0	PWM5OE2	PWM5OE1	PWM5OE0
B8h	xx00-0000	**IP**	–	–	PT2	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	**IPH**	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
BAh	0x00-0000	**IP1**	PPWM	–	PLVD	PI2C	PADI	PX2	PPX	PT3
BBh	0x00-0000	**IP1H**	PPWMH	–	PLVDH	PI2CH	PADIH	PX2H	PPXH	PT3H
C5h	0000-0000	**P0WKUP**	P0WKUP							
C6h	0000-0000	**P2WKUP**	P2WKUP							
C7h	0000-0000	**P3WKUP**	P3WKUP							
C8h	0000-0000	**T2CON**	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
C9h	000x-xxxx	**IAPWE**	IAPWE / IAPTO / EEPWE							
CAh	0000-0000	**RCP2L**	RCP2L							
CBh	0000-0000	**RCP2H**	RCP2H							
CCh	0000-0000	**TL2**	TL2							
CDh	0000-0000	**TH2**	TH2							
CEh	0000-0000	**EXA2**	EXA2							
CFh	0000-0000	**EXA3**	EXA3							
D0h	0000-0000	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
D1h	0000-0000	**PWM0DH**	PWM0DH							
D2h	0000-0000	**PWM0DL**	PWM0DL							

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D3h	0000-0000	**PWM1DH**	PWM1DH							
D4h	0000-0000	**PWM1DL**	PWM1DL							
D5h	0000-0000	**PWM2DH**	PWM2DH							
D6h	0000-0000	**PWM2DL**	PWM2DL							
D8h	xxx0-0011	**CLKCON**	–	–	–	STPPCK	STPFCK	SELFCK	CLKPSC	
D9h	1111-1111	**PWM0PRDH**	PWM0PRDH							
DAh	1111-1111	**PWM0PRDL**	PWM0PRDL							
DBh	1111-1111	**PWM1PRDH**	PWM1PRDH							
DCh	1111-1111	**PWM1PRDL**	PWM1PRDL							
DDh	0000-0000	**PWM3DH**	PWM3DH							
DEh	0000-0000	**PWM3DL**	PWM3DL							
E0h	0000-0000	**ACC**	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
E1h	000x-0100	**MICON**	MIEN	MIACKO	MIIF	MIACKI	MISTART	MISTOP	MICR	
E2h	0000-0000	**MIDAT**	MIDAT							
E3h	xxxx-0000	**LVRCON**					LVRSEL			
E4h	xxx0-0000	**LVDCON**	–	–	–	LVDIF	LVDSEL			
E5h	0000-0000	**LVRPD**	LVRPD							
E6h	0000-0000	**EXA**	EXA							
E7h	0000-0000	**EXB**	EXB							
E9h	0000-0000	**PWM4DH**	PWM4DH							
EAh	0000-0000	**PWM4DL**	PWM4DL							
EBh	0000-0000	**PWM5DH**	PWM5DH							
ECh	0000-0000	**PWM5DL**	PWM5DL							
EDh	0000-0000	**PWM6DH**	PWM6DH							
EEh	0000-0000	**PWM6DL**	PWM6DL							
F0h	0000-0000	**B**	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F1h	1111-1111	**CRCDL**	CRCDL							
F2h	1111-1111	**CRCDH**	CRCDH							
F3h	0000-0000	**CRCIN**	CRCIN							
F5h	xxxx-xxxx	**CFGBG**	–	–	–	BGTRIM				
F6h	xxxx-xxxx	**CFGWL**	–	FRCF						
F7h	0000-1110	**AUX2**	WDTE		PWRSAV	VBGOUT	DIV32	IAPTE		MULDIV16
F8h	0000-1100	**AUX1**	CLRWDT	CLRTM3	VBGEN	ADSOC	CLRPWM0	CLRPWM1	–	DPSEL

Flash Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1FFBh	**CFGBG**	–	–	–	BGTRIM				
1FFDh	**CFGWL**	–	FRCF						
1FFFh	**CFGWH**	PROT	XRSTE	LVRE				PREAD	FRCPSC

SFR & CFGW DESCRIPTION

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
80h	**P0**	7~0	P0	R/W	00h	Port0 has no pin out, so P0 is used as general purpose register
81h	**SP**	7~0	SP	R/W	07h	Stack Point
82h	**DPL**	7~0	DPL	R/W	00h	Data Point low byte
83h	**DPH**	7~0	DPH	R/W	00h	Data Point high byte
84h	**INTE2**	6	PWM1IE	R/W	0	PWM1~PWM6 interrupt enable 0: Disable PWM1~PWM6 interrupt 1: Enable PWM1~PWM6 interrupt
		5	PWM0IE	R/W	0	PWM0 interrupt enable 0: Disable PWM0 interrupt 1: Enable PWM0 interrupt
85h	**INTFLG2**	6	PWM1IF	R/W	0	PWM1~PWM6 interrupt flag Set by H/W at the end of PWM1 period, S/W writes BFh to INTFLG2 to clear this flag.
		5	PWM0IF	R/W	0	PWM0 interrupt enable Set by H/W at the end of PWM0 period, S/W writes DFh to INTFLG2 to clear this flag.
87h	**PCON**	7	SMOD	R/W	0	Set 1 to enable UART double baud rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit
		1	PD	R/W	0	Power down control bit, set 1 to enter HALT/STOP mode
		0	IDL	R/W	0	Idle control bit, set 1 to enter IDLE mode
88h	**TCON**	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control. 1: timer runs; 0: timer stops
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control. 1:timer runs; 0:timer stops
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
89h	**TMOD**	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin's negative edge
		5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	**TL0**	7~0	TL0	R/W	00h	Timer0 data low byte
8Bh	**TL1**	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	**TH0**	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	**TH1**	7~0	TH1	R/W	00h	Timer1 data high byte
90h	**P1**	7~0	P1	R/W	FFh	Port1 data
91h	**P0OE**	7~0	P0OE	R/W	00h	Port0 CMOS Push-Pull output enable control 0: Disable 1: Enable
92h	**P1LOE**	3	P1LOE3	R/W	0	LCD 1/2 bais Output 0: Disable 1: P15 as LCD 1/2 bais Output
		2	P1LOE2	R/W	0	LCD 1/2 bais Output 0: Disable 1: P14 as LCD 1/2 bais Output
		1	P1LOE1	R/W	0	LCD 1/2 bais Output 0: Disable 1: P13 as LCD 1/2 bais Output
		0	P1LOE0	R/W	0	LCD 1/2 bais Output 0: Disable 1: P12 as LCD 1/2 bais Output

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
93h	**PINMOD**	7	TXRXSEL	R/W	0	UART TXD/RXD pin select 0: P31 as TXD, P30 as RXD 1: P16 as TXD, P02 as RXD
		6	T2OE	R/W	0	Timer2 signal output (T2O) control 0: Disable "Timer2 overflow divided by 2" output to P1.0 pin 1: Enable "Timer2 overflow divided by 2" output to P1.0 pin
		5	T1OE	R/W	0	Timer1 signal output (T1O) control 0: Disable "Timer1 overflow divided by 2" output to P3.5 pin 1: Enable "Timer1 overflow divided by 2" output to P3.5 pin
		4	T0OE	R/W	0	Timer0 signal output (T0O) control 0: Disable "Timer0 overflow divided by 64" output to P3.4 pin 1: Enable "Timer0 overflow divided by 64" output to P3.4 pin
		3~2	P2MOD1	R/W	01	P2.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not defined
		1~0	P2MOD0	R/W	01	P2.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not defined
94h	**OPTION**	7	UART1W	R/W	0	Set 1 to enable one wire UART mode, both TXD/RXD use P3.1 pin or P1.6.
		6	TM3CKS	R/W	0	Timer3 clock source select. 0: Slow Clock (SRC) 1: FRC/512
		5~4	WDTPSC	R/W	00	Watchdog Timer pre-scalar time select 00: 400ms WDT overflow rate 01: 200ms WDT overflow rate 10: 100ms WDT overflow rate 11: 50ms WDT overflow rate
		3~2	ADCKS	R/W	00	ADC clock rate select 00: F_{SYSCLK}/32 01: F_{SYSCLK}/16 10: F_{SYSCLK}/8 11: F_{SYSCLK}/4
		1~0	TM3PSC	R/W	00	Timer3 Interrupt rate 00: Timer3 Interrupt rate is 32768 Slow clock cycle 01: Timer3 Interrupt rate is 16384 Slow clock cycle 10: Timer3 Interrupt rate is 8192 Slow clock cycle 11: Timer3 Interrupt rate is 65536 Slow clock cycle
95h	**INTFLG**	4	ADIF	R/W	0	ADC interrupt flag Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.
		2	IE2	R/W	0	External Interrupt 2 (INT2 pin) edge flag Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine. S/W can write FBh to INTFLG to clear this bit.
		1	PXIF	R/W	0	Port1 pin change Interrupt flag Set by H/W when a Port1 pin state change is detected and its interrupt enable bit is set (P0WKUP/P1WKUP/P2WKUP/P3WKUP). PXIE does not affect this flag's setting. It is cleared automatically when the program performs the interrupt service routine. S/W can write FDh to INTFLG to clear this bit.
		0	TF3	R/W	0	Timer3 Interrupt Flag Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.
96h	**P1WKUP**	7~0	P1WKUP	R/W	00h	P1.7~P1.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
97h	**SWCMD**	7~0	SWRST	W		Write 56h to generate S/W Reset
		7~0	IAPALL	W		Write 65h, the available range of flash memory IAP is 0000h~1FEFh (IAPALL read back value is 1) Write 00h, the available range of flash memory IAP is 1F00h~1EFFh (IAPALL read back value is 0)
		1	WDTO	R	0	WatchDog Time-Out flag
		0	IAPALL	R	0	0: Flash memory 0000h~1EFFh cannot use IAP, only 1F00h~1EFFh can use IAP 1: Flash memory 0000h~1EFFh and 1F00h~1EFFh can use IAP.
98h	**SCON**	7	SM0	R/W	0	UART Serial port mode select bit 0, 1 (SM0, SM1) = 00: Mode0: 8 bit shift register, Baud Rate=F_{SYSCLK}/2 01: Mode1: 8 bit UART, Baud Rate is variable 10: Mode2: 9 bit UART, Baud Rate=F_{SYSCLK}/32 or /64 11: Mode3: 9 bit UART, Baud Rate is variable
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	Set 1 to enable UART Reception
		3	TB8	R/W	0	Transmitter bit 8, ninth bit to transmit in Modes 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0
		1	TI	R/W	0	Transmit Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W
		0	RI	R/W	0	Receive Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.
99h	**SBUF**	7~0	SBUF	R/W	–	UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
A0h	**P2**	7~2	P2.7~P2.2	R/W	FFh	P2.7~P2.2 have no pin out, so these bits are used as general purpose register
		1~0	P2.1~P2.0	R/W	11	P2.1~P2.0 data
A1h	**PWMCON**	7~6	PWM1CKS	R/W	00	PWM1 clock source 00: F_{SYSCLK} 01: F_{SYSCLK} 10: FRC 11: FRCx2 (Vcc>2.7V)
		3~2	PWM0CKS	R/W	00	PWM0 clock source 00: F_{SYSCLK} 01: F_{SYSCLK} 10: FRC 11: FRCx2 (Vcc>2.7V)
		1	PWM0NMSK	R/W	0	PWM0N mask data while CLRPWM0=1
		0	PWM0PMSK	R/W	0	PWM0N mask data while CLRPWM0=1
A2h	**P1MODL**	7~6	P1MOD3	R/W	01	P1.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P1.3 is ADC input
		5~4	P1MOD2	R/W	01	P1.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3
		3~2	P1MOD1	R/W	01	P1.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P1.1 is ADC input
		1~0	P1MOD0	R/W	01	P1.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P1.0 is ADC input

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A3h	**P1MODH**	7~6	P1MOD7	R/W	01	P1.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P1.7 is ADC input
		5~4	P1MOD6	R/W	01	P1.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P1.6 is ADC input
		3~2	P1MOD5	R/W	01	P1.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P1.5 is ADC input
		1~0	P1MOD4	R/W	01	P1.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P1.4 is ADC input
A4h	**P3MODL**	7~6	P3MOD3	R/W	01	P3.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P3.3 is ADC input
		5~4	P3MOD2	R/W	01	P3.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P3.2 is ADC input
		3~2	P3MOD1	R/W	01	P3.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P3.1 is ADC input
		1~0	P3MOD0	R/W	01	P3.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P3.0 is ADC input
A5h	**P3MODH**	7~6	P3MOD7	R/W	01	P3.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3
		5~4	P3MOD6	R/W	01	P3.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3
		3~2	P3MOD5	R/W	01	P3.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3
		1~0	P3MOD4	R/W	01	P3.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P3.4 is ADC input
A6h	**PWMOE0**	7	PWM1OE3	R/W	0	PWM1 output control 0: Disable 1: PWM1 enable and output to P1.2
		6	PWM1OE2	R/W	0	PWM1 output control 0: Disable 1: PWM1 enable and output to P0.6
		5	PWM1OE1	R/W	0	PWM1 output control 0: Disable 1: PWM1 enable and output to P0.4
		4	PWM1OE0	R/W	0	PWM1 output control 0: Disable 1: PWM1 enable and output to P0.2
		3	PWM0NOE1	R/W	0	PWM0N output control 0: Disable 1: PWM0N enable and output to P3.6
		2	PWM0POE1	R/W	0	PWM0P output control 0: Disable 1: PWM0P enable and output to P3.5
		1	PWM0NOE0	R/W	0	PWM0N output control 0: Disable 1: PWM0N enable and output to P0.4
		0	PWM0POE0	R/W	0	PWM0P output control 0: Disable 1: PWM0P enable and output to P0.3
A7h	**PWMCON2**	7	PWM0MOD	R/W	0	PWM0 mode select 0: Normal mode 1: Half-bridge mode
		6	PWM0MSKE	R/W	0	PWM0 mask output enable 0: Disable 1: Enable, PWM0P/PWM0N output data by PWM0PMSK/PWM0NMSK while CLRPWM0=1
		5~4	PWM0OM	R/W	00	PWM0 output mode select 00: Mode0 01: Mode1 10: Mode2 11: Mode3
		3~0	PWM0DZ	R/W	0000	PWM0 dead zone (Dead zone is prohibited in half-bridge mode) 0000: 0 x T_{PWMCLK} 0001: 1 x T_{PWMCLK} … 1111: 15 x T_{PWMCLK}

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A8h	**IE**	7	EA	R/W	0	Global interrupt enable control. 0: Disable all Interrupts. 1: Each interrupt is enabled or disabled by its own interrupt control bit.
		5	ET2	R/W	0	Set 1 to enable Timer2 interrupt
		4	ES	R/W	0	Set 1 to enable Serial Port (UART) Interrupt
		3	ET1	R/W	0	Set 1 to enable Timer1 Interrupt
		2	EX1	R/W	0	Set 1 to enable external INT1 pin Interrupt & Halt/Stop mode wake up capability
		1	ET0	R/W	0	Set 1 to enable Timer0 Interrupt
		0	EX0	R/W	0	Set 1 to enable external INT0 pin Interrupt & Halt/Stop mode wake up capability
A9h	**INTE1**	7	PWMIE	R/W	0	Set 1 to enable PWM0/PWM1~PWM6 interrupt
		5	LVDIE	R/W	0	Set 1 to enable LVD interrupt
		4	I2CE	R/W	0	Set 1 to enable I^2C interrupt
		3	ADIE	R/W	0	Set 1 to enable ADC Interrupt
		2	EX2	R/W	0	Set 1 to enable external INT2 pin Interrupt & Halt/Stop mode wake up capability
		1	PXIE	R/W	0	Set 1 to enable Port0/Port1/Port2/Port3 Pin Change Interrupt
		0	TM3IE	R/W	0	Set 1 to enable Timer3 Interrupt
AAh	**ADCDL**	7~4	ADCDL	R	–	ADC data bit 3~0
ABh	**ADCDH**	7~0	ADCDH	R	–	ADC data bit 11~4
AEh	**CHSEL**	7~4	ADCHS	R/W	1111	5-bit ADC channel select = {ADCHS4,ADCHS}. 00000: AD0 (P0.4) 00001: AD1 (P0.3) 00010: AD2 (P1.0) 00011: AD3 (P1.1) 00100: AD4 (P3.3) 00101: AD5 (P3.2) 00110: AD6 (P3.0) 00111: AD7 (P3.1) 01000: AD8 (P3.4) 01001: AD9 (P1.7) 01010: AD10 (P0.7) 01011: AD11 (P0.5) 01100: VBG 01101: Reserved 01110: V_{SS} 01111: $V_{CC}/4$ 10000: AD16 (P1.3) 10001: AD17 (P1.4) 10010: AD18 (P1.5) 10011: AD19 (P1.6) 10100: AD20 (P0.0) 10101: AD21 (P0.1) 10110: AD22 (P0.2) 10111: Reserved
		3	ADCHS4	R/W	0	5-bit ADC channel select = {ADCHS4,ADCHS}.
		2	ADCVREFS	R/W	0	ADC reference voltage 0: V_{CC} 1: VBG
		1~0	VBGSEL	R/W	00	VBG voltage select, When ADCVREF is selected as VBG, VBGSEL is prohibited from using 1.22V. 00: 1.22V 01: 2.54V (need VCC>2.8V) 10: Reserved 11:Reserved

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
AFh	**P0DIE**	7	P0DIE7	R/W	1	Port digital input enable 0: P0.7 is ADC input and disable digital input 1: enable P0.7 digital input
		6	P0DIE6	R/W	1	Port digital input enable 0: disable P0.6 digital input 1: enable P0.6 digital input
		5	P0DIE5	R/W	1	Port digital input enable 0: P0.5 is ADC input and disable digital input 1: enable P0.5 digital input
		4	P0DIE4	R/W	1	Port digital input enable 0: P0.4is ADC input and disable digital input 1: enable P0.4 digital input
		3	P0DIE3	R/W	1	Port digital input enable 0: P0.3 is ADC input and disable digital input 1: enable P0.3 digital input
		2	P0DIE2	R/W	1	Port digital input enable 0: P0.2 is ADC input and disable digital input 1: enable P0.2 digital input
		1	P0DIE1	R/W	1	Port digital input enable 0: P0.1 is ADC input and disable digital input 1: enable P0.1 digital input
		0	P0DIE0	R/W	1	Port digital input enable 0: P0.0 is ADC input and disable digital input 1: enable P0.0 digital input
B0h	**P3**	7~0	P3	R/W	FFh	Port3 data
B6h	**PWMOE1**	7	PWM4OE3	R/W	0	PWM4 output control 0: Disable 1: PWM4 enable and output to P3.6
		6	PWM4OE2	R/W	0	PWM4 output control 0: Disable 1: PWM4 enable and output to P1.5
		5	PWM4OE1	R/W	0	PWM4 output control 0: Disable 1: PWM4 enable and output to P0.4
		4	PWM4OE0	R/W	0	PWM4 output control 0: Disable 1: PWM4 enable and output to P0.0
		3	PWM3OE1	R/W	0	PWM3 output control 0: Disable 1: PWM3 enable and output to P3.4
		2	PWM3OE0	R/W	0	PWM3 output control 0: Disable 1: PWM3 enable and output to P1.0
		1	PWM2OE1	R/W	0	PWM2 output control 0: Disable 1: PWM2 enable and output to P3.6
		0	PWM2OE0	R/W	0	PWM2 output control 0: Disable 1: PWM2 enable and output to P1.1

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
B7h	**PWMOE2**	7	MSDASEL	R/W	0	Master I²C SDA select 0: P3.5 as Master I²C SDA 1: P1.6 as Master I²C SDA
		6	MSCLSEL	R/W	0	Master I²C SCL select 0: P1.3 as Master I²C SCL 1: P0.2 as Master I²C SCL
		5	PWM6OE2	R/W	0	PWM6 output control 0: Disable 1: PWM6 enable and output to P1.3
		4	PWM6OE1	R/W	0	PWM6 output control 0: Disable 1: PWM6 enable and output to P0.7
		3	PWM6OE0	R/W	0	PWM6 output control 0: Disable 1: PWM6 enable and output to P0.3
		2	PWM5OE2	R/W	0	PWM5 output control 0: Disable 1: PWM5 enable and output to P1.4
		1	PWM5OE1	R/W	0	PWM5 output control 0: Disable 1: PWM5 enable and output to P0.6
		0	PWM5OE0	R/W	0	PWM5 output control 0: Disable 1: PWM5 enable and output to P0.1
B8h	**IP**	5	PT2	R/W	0	Timer2 Interrupt Priority Low bit
		4	PS	R/W	0	Serial Port (UART) Interrupt Priority Low bit
		3	PT1	R/W	0	Timer1 Interrupt Priority Low bit
		2	PX1	R/W	0	External INT1 Pin Interrupt Priority Low bit
		1	PT0	R/W	0	Timer0 Interrupt Priority Low bit
		0	PX0	R/W	0	External INT0 Pin Interrupt Priority Low bit
B9h	**IPH**	5	PT2H	R/W	0	Timer2 Interrupt Priority High bit
		4	PSH	R/W	0	Serial Port (UART) Interrupt Priority High bit
		3	PT1H	R/W	0	Timer1 Interrupt Priority High bit
		2	PX1H	R/W	0	External INT1 Pin Interrupt Priority High bit
		1	PT0H	R/W	0	Timer0 Interrupt Priority High bit
		0	PX0H	R/W	0	External INT0 Pin Interrupt Priority High bit
BAh	**IP1**	7	PPWM	R/W	0	PWM0/PWM1 Interrupt Priority Low bit
		5	PLVD	R/W	0	LVD Interrupt Priority Low bit
		4	PI2C	R/W	0	I²C Interrupt Priority Low bit
		3	PADI	R/W	0	ADC Interrupt Priority Low bit
		2	PX2	R/W	0	External INT2 Pin Interrupt Priority Low bit
		1	PPX	R/W	0	Port0~Port3 pin change Interrupt Priority Low bit
		0	PT3	R/W	0	Timer3 Interrupt Priority Low bit
BBh	**IP1H**	7	PPWMH	R/W	0	PWM0/PWM1 Interrupt Priority High bit
		5	PLVDH	R/W	0	LVD Interrupt Priority High bit
		4	PI2CH	R/W	0	I²C Interrupt Priority High bit
		3	PADIH	R/W	0	ADC Interrupt Priority High bit
		2	PX2H	R/W	0	External INT2 Pin Interrupt Priority High bit
		1	PPXH	R/W	0	Port0~Port3 Interrupt Priority High bit
		0	PT3H	R/W	0	Timer3 Interrupt Priority High bit
C5h	**P0WKUP**	7~0	P0WKUP	R/W	00h	P0.7~P0.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.
C6h	**P2WKUP**	7~0	P2WKUP	R/W	00h	P2.7~P2.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.
C7h	**P3WKUP**	7~0	P3WKUP	R/W	00h	P3.7~P3.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
C8h	**T2CON**	7	TF2	R/W	0	Timer2 overflow flag Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
		6	EXF2	R/W	0	T2EX interrupt pin falling edge flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
		5	RCLK	R/W	0	UART receive clock control bit 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3
		4	TCLK	R/W	0	UART transmit clock control bit 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
		3	EXEN2	R/W	0	T2EX pin enable 0: T2EX pin disable 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0
		2	TR2	R/W	0	Timer2 run control 0:timer stops 1:timer runs
		1	CT2N	R/W	0	Timer2 Counter/Timer select bit 0: Timer mode, Timer2 data increases at 2 System clock cycle rate 1: Counter mode, Timer2 data increases at T2 pin's negative edge
		0	CPRL2N	R/W	0	Timer2 Capture/Reload control bit 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1. 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1. If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.
C9h	**IAPWE**	7~0	IAPWE	W	–	Write 47h to set IAPWE control flag; Write other value to clear IAPWE and EEPWE flag. It is recommended to clear it immediately after IAP write.
		7~0	EEPWE	W	–	Write E2h to set EEPWE control flag; Write other value to clear IAPWE and EEPWE flag. It is recommended to clear it immediately after EEPROM write.
		7	IAPWE	R	0	Flag indicates Flash memory can be written by IAP or not 0: IAP Write disable 1: IAP Write enable
		6	IAPTO	R	0	IAP (or EEPROM write) Time-Out flag Set by H/W when IAP (or EEPROM write) Time-out occurs. Cleared by H/W when IAPWE=0 and EEPWE=0.
		5	EEPWE	R	0	Flag indicates EEPROM memory can be written or not 0: EEPROM Write disable 1: EEPROM Write enable
CAh	**RCP2L**	7~0	RCP2L	R/W	00h	Timer2 reload/capture data low byte
CBh	**RCP2H**	7~0	RCP2H	R/W	00h	Timer2 reload/capture data high byte
CCh	**TL2**	7~0	TL2	R/W	00h	Timer2 data low byte
CDh	**TH2**	7~0	TH2	R/W	00h	Timer2 data high byte
CEh	**EXA2**	7~0	EXA2	R/W	00h	Expansion accumulator 2
CFh	**EXA3**	7~0	EXA3	R/W	00h	Expansion accumulator 3
D0h	**PSW**	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	Register Bank Select bit 1
		3	RS0	R/W	0	Register Bank Select bit 0
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
D1h	**PWM0DH**	7~0	PWM0DH	R/W	00h	PWM0 duty high byte
D2h	**PWM0DL**	7~0	PWM0DL	R/W	00h	PWM0 duty low byte
D3h	**PWM1DH**	7~0	PWM1DH	R/W	00h	PWM1 duty high byte
D4h	**PWM1DL**	7~0	PWM1DL	R/W	00h	PWM1 duty low byte
D5h	**PWM2DH**	7~0	PWM2DH	R/W	00h	PWM2 duty high byte
D6h	**PWM2DL**	7~0	PWM2DL	R/W	00h	PWM2 duty low byte
D8h	**CLKCON**	5	STPSCK	R/W	1	Set 1 to stop Slow clock in Stop Mode.
		4	STPPCK	R/W	0	Set 1 to stop UART/Timer0/1/2 clock in Idle mode for current reducing.
		3	STPFCK	R/W	0	Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
		2	SELFCK	R/W	0	System clock select. This bit can be changed only when STPFCK=0. 0: Slow clock 1: Fast clock
		1~0	CLKPSC	R/W	11	System clock prescaler. Effective after 16 clock cycles (Max.) delay. 00: System clock is Fast/Slow clock divided by 16 01: System clock is Fast/Slow clock divided by 4 10: System clock is Fast/Slow clock divided by 2 11: System clock is Fast/Slow clock divided by 1
D9h	**PWM0PRDH**	7~0	PWM0PRDH	R/W	FFh	PWM0 period high byte
DAh	**PWM0PRDL**	7~0	PWM0PRDL	R/W	FFh	PWM0 period low byte
DBh	**PWM1PRDH**	7~0	PWM1PRDH	R/W	FFh	PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 period high byte
DCh	**PWM1PRDL**	7~0	PWM1PRDL	R/W	FFh	PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 period low byte
DDh	**PWM3DH**	7~0	PWM3DH	R/W	00h	PWM3 duty high byte
DEh	**PWM3DL**	7~0	PWM3DL	R/W	00h	PWM3 duty low byte
E0h	**ACC**	7~0	ACC	R/W	00h	Accumulator
E1h	**MICON**	7	MIEN	R/W	0	Master I^2C enable 0: disable 1: enable
		6	MIACKO	R/W	0	When Master I^2C receive data, send acknowledge to I^2C Bus 0: ACK to slave device 1: NACK to slave device
		5	MIIF	R/W	0	Master I^2C Interrupt flag 0: write 0 to clear it 1: Master I^2C transfer one byte complete
		4	MIACKI	R	–	When Master I^2C transfer, acknowledgement form I^2C bus (read only) 0: ACK received 1: NACK received
		3	MISTART	R/W	0	Master I^2C Start bit 1: start I^2C bus transfer
		2	MISTOP	R/W	1	Master I^2C Stop bit 1: send STOP signal to stop I^2C bus
		1~0	MICR	R/W	00	Master I^2C (SCL) clock frequency selection 00: Fsys/4 (ex. If Fsys=16MHz, I^2C clock is 4M Hz) 01: Fsys/16 (ex. If Fsys=16MHz, I^2C clock is 1M Hz) 10: Fsys/64 (ex. If Fsys=16MHz, I^2C clock is 250K Hz) 11: Fsys/256 (ex. If Fsys=16MHz, I^2C clock is 62.5K Hz)
E2h	**MIDAT**	7~0	MIDAT	R/W	00	Master I^2C data shift register (W): After Start and before Stop condition, write this register will resume transmission to I^2C bus (R): After Start and before Stop condition, read this register will resume receiving from I^2C bus

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
E3h	**LVRCON**	3~0	LVRSEL	R/W	0h	Low Voltage Reset(LVR) select. (Same as CFGWH LVRE function) 0000: Set LVR at 2.25V 0001: Set LVR at 2.40V 0010: Set LVR at 2.55V 0011: Set LVR at 2.65V 0100: Set LVR at 2.80V 0101: Set LVR at 2.95V 0110: Set LVR at 3.10V 0111: Set LVR at 3.25V 1000: Set LVR at 3.40V 1001: Set LVR at 3.55V 1010: Set LVR at 3.70V 1011: Set LVR at 3.85V 1100: Set LVR at 4.00V 1101: Set LVR at 4.15V 1110: Set LVR at 4.30V 1111: Set LVR at 4.45V
E4h	**LVDCON**	4	LVDIF	R/W	0	LVD interrupt flag, write 0 to clear this bit
		3~0	LVDSEL	R/W	0h	Low Voltage Detect(LVD) select 0000: LVD disable 0001: Set LVD at 2.40V 0010: Set LVD at 2.55V 0011: Set LVD at 2.65V 0100: Set LVD at 2.80V 0101: Set LVD at 2.95V 0110: Set LVD at 3.10V 0111: Set LVD at 3.25V 1000: Set LVD at 3.40V 1001: Set LVD at 3.55V 1010: Set LVD at 3.70V 1011: Set LVD at 3.85V 1100: Set LVD at 4.00V 1101: Set LVD at 4.15V 1110: Set LVD at 4.30V 1111: Set LVD at 4.45V
E5h	**LVRPD**	7~0	LVRPD	W	00h	LVRPD: LVR and POR power down option Write 0x37 to force LVR disable, POR disable Write 0x38 to force LVR disable, POR enable
E6h	**EXA**	7~0	EXA	R/W	00h	Expansion accumulator
E7h	**EXB**	7~0	EXB	R/W	00h	Expansion B register
E9h	**PWM4DH**	7~0	PWM4DH	R/W	00h	PWM4 duty high byte
EAh	**PWM4DL**	7~0	PWM4DL	R/W	00h	PWM4 duty low byte
EBh	**PWM5DH**	7~0	PWM5DH	R/W	00h	PWM5 duty high byte
ECh	**PWM5DL**	7~0	PWM5DL	R/W	00h	PWM5 duty low byte
EDh	**PWM6DH**	7~0	PWM6DH	R/W	00h	PWM6 duty high byte
EEh	**PWM6DL**	7~0	PWM6DL	R/W	00h	PWM6 duty low byte
F0h	**B**	7~0	B	R/W	00h	B register
F1h	**CRCDL**	7~0	CRCDL	R/W	FFh	16-bit CRC data bit 7~0
F2h	**CRCDH**	7~0	CRCDH	R/W	FFh	16-bit CRC data bit 15~8
F3h	**CRCIN**	7~0	CRCIN	W	–	CRC input data
F5h	**CFGBG**	4~0	BGTRIM	R/W	–	VBG trimming value
F6h	**CFGWL**	6~0	FRCF	R/W	–	FRC frequency adjustment 00h: lowest frequency 7Fh: highest frequency
F7h	**AUX2**	7~6	WDTE	R/W	–	Watchdog Timer Reset control 0x: WDT disable 10: WDT enable in Fast/Slow mode, disable in Idle/Halt/Stop mode

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
						11: WDT always enable
		5	PWRSAV	R/W	–	Set 1 to reduce the chip's power consumption at Idle/Halt/Stop Mode.
		4	VBGOUT	R/W	0	Bandgap voltage output control 0: P3.2 as normal I/O 1: Bandgap voltage output to P3.2 pin, when ADCHS = 4'b1100
		3	DIV32	R/W	0	only active when MULDVI16 =1 0: instruction DIV as 16/16 bit division operation 1: instruction DIV as 32/16 bit division operation
		2~1	IAPTE	R/W	11	IAP (or EEPROM write) watchdog timer enable 00: Disable 01: wait 1.6mS trigger watchdog time-out flag 10: wait 3.2mS trigger watchdog time-out flag 11: wait 12.8mS trigger watchdog time-out flag
		0	MULDIV16	R/W	0	0: instruction MUL/DIV as 8*8, 8/8 operation 1: instruction MUL/DIV as 16*16, 16/16 or 32/16 operation
F8h	**AUX1**	7	CLRWDT	R/W	0	Set 1 to clear WDT, H/W auto clear it at next clock cycle
		6	CLRTM3	R/W	0	Set 1 to clear Timer3, HW auto clear it at next clock cycle.
		5	VBGEN	R/W	0	force VBG generator enable 0: VBG generator is automatically enable and disable 1: Force VBG generator enable except in IDLE/HALT/STOP mode.
		4	ADSOC	R/W	0	ADC Start of Conversion Set 1 to start ADC conversion. Cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		3	CLRPWM0	R/W	1	PWM0 clear enable 0: PWM0 is running 1: PWM0 is cleared and held
		2	CLRPWM1	R/W	1	PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 clear enable 0: PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 is running 1: PWM1/PWM2/PWM3/PWM4/PWM5/PWM6 is cleared and held
		0	DPSEL	R/W	0	Active DPTR Select

Adr	Flash	Bit#	Bit Name	Description
1FFBh	**CFGBG**	4~0	BGTRIM	FRC frequency adjustment. VBG is trimmed to 1.22V in chip manufacturing. BGTRIM records the adjustment data.
1FFDh	**CFGWL**	6~0	FRCF	FRC frequency adjustment. FRC is trimmed to 16.588 MHz in chip manufacturing. FRCF records the adjustment data.
1FFFh	**CFGWH**	7	PROT	Flash Code Protect, 1=Protect
		6	XRSTE	External Pin Reset enable, 1=enable.
		5~2	LVRE	Low Voltage Reset function select 0000: Set LVR at 2.25V 0001: Set LVR at 2.40V 0010: Set LVR at 2.55V 0011: Set LVR at 2.65V 0100: Set LVR at 2.80V 0101: Set LVR at 2.95V 0110: Set LVR at 3.10V 0111: Set LVR at 3.25V 1000: Set LVR at 3.40V 1001: Set LVR at 3.55V 1010: Set LVR at 3.70V 1011: Set LVR at 3.85V 1100: Set LVR at 4.00V 1101: Set LVR at 4.15V 1110: Set LVR at 4.30V 1111: Set LVR at 4.45V
		1	PREAD	Reserved
		0	FRCPSC	Reserved

INSTRUCTION SET

Instructions are 1, 2 or 3 bytes long as listed in the 'byte' column below. Each instruction takes 2~32 System clock cycles to execute as listed in the 'cycle' column below.

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ADD A,Rn	Add register to A	1	2	28-2F
ADD A,dir	Add direct byte to A	2	2	25
ADD A,@Ri	Add indirect memory to A	1	2	26-27
ADD A,#data	Add immediate to A	2	2	24
ADDC A,Rn	Add register to A with carry	1	2	38-3F
ADDC A,dir	Add direct byte to A with carry	2	2	35
ADDC A,@Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A,#data	Add immediate to A with carry	2	2	34
SUBB A,Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	2	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8/16	A4
DIV AB	Divide A by B	1	8/16/32	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ANL A,Rn	AND register to A	1	2	58-5F
ANL A,dir	AND direct byte to A	2	2	55
ANL A,@Ri	AND indirect memory to A	1	2	56-57
ANL A,#data	AND immediate to A	2	2	54
ANL dir,A	AND A to direct byte	2	2	52
ANL dir,#data	AND immediate to direct byte	3	4	53
ORL A,Rn	OR register to A	1	2	48-4F
ORL A,dir	OR direct byte to A	2	2	45
ORL A,@Ri	OR indirect memory to A	1	2	46-47
ORL A,#data	OR immediate to A	2	2	44
ORL dir,A	OR A to direct byte	2	2	42
ORL dir,#data	OR immediate to direct byte	3	4	43
XRL A,Rn	Exclusive-OR register to A	1	2	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A,#data	Exclusive-OR immediate to A	2	2	64
XRL dir,A	Exclusive-OR A to direct byte	2	2	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4
SWAP A	Swap Nibbles of A	1	2	C4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
RL A	Rotate A left	1	2	23
RLC A	Rotate A left through carry	1	2	33
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MOV A,Rn	Move register to A	1	2	E8-EF
MOV A,dir	Move direct byte to A	2	2	E5
MOV A,@Ri	Move indirect memory to A	1	2	E6-E7
MOV A,#data	Move immediate to A	2	2	74
MOV Rn,A	Move A to register	1	2	F8-FF
MOV Rn,dir	Move direct byte to register	2	4	A8-AF
MOV Rn,#data	Move immediate to register	2	2	78-7F
MOV dir,A	Move A to direct byte	2	2	F5
MOV dir,Rn	Move register to direct byte	2	4	88-8F
MOV dir,dir	Move direct byte to direct byte	3	4	85
MOV dir,@Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir,#data	Move immediate to direct byte	3	4	75
MOV @Ri,A	Move A to indirect memory	1	2	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	2	76-77
MOV DPTR,#data	Move immediate to data pointer	3	4	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	8	93
MOVC A,@A+PC	Move code byte relative PC to A	1	8	83
MOVX A,@Ri	Move external data(A8) to A	1	8	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	8	E0
MOVX @Ri,A	Move A to external data(A8)	1	8	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	8	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A,Rn	Exchange A and register	1	2	C8-CF
XCH A,dir	Exchange A and direct byte	2	2	C5
XCH A,@Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C,bit	AND direct bit to carry	2	4	82
ANL C,/bit	AND direct bit inverse to carry	2	4	B0
ORL C,bit	OR direct bit to carry	2	4	72
ORL C,/bit	OR direct bit inverse to carry	2	4	A0
MOV C,bit	Move direct bit to carry	2	2	A2
MOV bit,C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	**Description**	**byte**	**cycle**	**Opcode**
ACALL addr 11	Absolute jump to subroutine	2	4 (+2)	11-F1
LCALL addr 16	Long jump to subroutine	3	4 (+2)	12
RET	Return from subroutine	1	4 (+2)	22
RETI	Return from interrupt	1	4 (+2)	32
AJMP addr 11	Absolute jump unconditional	2	4 (+2)	01-E1
LJMP addr 16	Long jump unconditional	3	4 (+2)	02
SJMP rel	Short jump (relative address)	2	4 (+2)	80
JC rel	Jump on carry = 1	2	4 (or 6)	40
JNC rel	Jump on carry = 0	2	4 (or 6)	50
JB bit,rel	Jump on direct bit = 1	3	4 (or 6)	20
JNB bit,rel	Jump on direct bit = 0	3	4 (or 6)	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	4 (or 6)	10
JMP @A+DPTR	Jump indirect relative DPTR	1	4 (+2)	73
JZ rel	Jump on accumulator = 0	2	4 (or 6)	60
JNZ rel	Jump on accumulator … 0	2	4 (or 6)	70
CJNE A,dir,rel	Compare A,direct, jump not equal relative	3	4 (or 6)	B5
CJNE A,#data,rel	Compare A,immediate, jump not equal relative	3	4 (or 6)	B4
CJNE Rn,#data,rel	Compare register,immediate, jump not equal relative	3	4 (or 6)	B8-BF
CJNE @Ri,#data,rel	Compare indirect,immediate, jump not equal relative	3	4 (or 6)	B6-B7
DJNZ Rn,rel	Decrement register, jump not zero relative	2	4 (or 6)	D8-DF
DJNZ dir,rel	Decrement direct byte, jump not zero relative	3	4 (or 6)	D5

MISCELLANEOUS				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A=25℃)

Parameter	Rating	Unit
Supply voltage	V_{SS} –0.3 ~ V_{SS} +5.5	V
Input voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output current high per all PIN	–80	mA
Output current low per all PIN	+150	
Maximum Operating Voltage	5.5	V
Operating temperature	–40 ~ +105	°C
Storage temperature	–65 ~ +150	

2. DC Characteristics (T_A=25 ℃, V_{CC}=2.2V ~ 5.5V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Operating Voltage	V_{CC}	F_{SYS}=16.588 MHz		2.2	–	5.5	V
Input High Voltage	V_{IH}	All Input	V_{CC}=5V	0.6V_{CC}	–	–	V
			V_{CC}=3V	0.6V_{CC}	–	–	V
Input Low Voltage	V_{IL}	All Input	V_{CC}=5V	–	–	0.2V_{CC}	V
			V_{CC}=3V	–	–	0.2V_{CC}	V
I/O Port Source Current	I_{OH}	All Output	V_{CC}=5V, V_{OH}=0.9V_{CC}	6	12	–	mA
			V_{CC}=3V, V_{OH}=0.9V_{CC}	2.5	5	–	
I/O Port Sink Current	I_{OL}	All Output,	V_{CC}=5V, V_{OL}=0.1V_{CC}	22	44	–	mA
			V_{CC}=3V, V_{OL}=0.1V_{CC}	10	20	–	
Supply Current	I_{DD}	FAST mode V_{CC}=5V	FRC=16.588 MHz		8.3		mA
			FRC=8.694 MHz	–	5.6	–	
		FAST mode V_{CC}=3V	FRC=16.588 MHz	–	4.7	–	
			FRC=8.694 MHz		3.4		
		SLOW mode	SRC, V_{CC}=5V	–	2.6	–	
			SRC, V_{CC}=3V	–	1.7	–	
		IDLE mode (PWRSAV=0)	SRC, V_{CC}=5V		95		µA
			SRC, V_{CC}=3V		55		
		IDLE mode (PWRSAV=1)	SRC, V_{CC}=5V		40		
			SRC, V_{CC}=3V		16		
		IDLE mode (PWRSAV=1,LVRPD=0x37)	SRC, V_{CC}=5V	–	26	–	
			SRC, V_{CC}=3V		9		
		HLAT mode (PWRSAV=1)	V_{CC}=5V		21		
			V_{CC}=3V	–	6	–	
		STOP mode	V_{CC}=5V		0.3		
			V_{CC}=3V		0.1		

LVR Reference Voltage	V_{LVR}	T_A=25°C		–	4.45	–	V
					4.30		
					4.15		
					3.00		
					3.85		
					3.70		
					3.55		
					3.40		
					3.25		
					3.10		
					2.95		
					2.80		
					2.65		
					2.55		
					2.40		
					2.25		
LVR Hysteresis Voltage	V_{HYST}	T_A=25°C		–	±0.1	–	V
LVD Reference Voltage	V_{LVD}	T_A=25°C		–	4.45	–	V
					4.30		
					4.15		
					3.00		
					3.85		
					3.70		
					3.55		
					3.40		
					3.25		
					3.10		
					2.95		
					2.80		
					2.65		
					2.55		
					2.40		
Low Voltage Detection time	T_{LVR}	T_A=25°C		100	–	–	μs
Pull-Up Resistor	R_P	V_{IN}=0V	V_{CC}=5V	–	33	–	KΩ
			V_{CC}=3V	–	55	–	

3. Clock Timing

Parameter	Condition	Min	Typ	Max	Unit
FRC Frequency	25℃, V_{CC}=4.5V	–1%	16.588	+1%	MHz
	0℃ ~ 105℃, V_{CC}=4.5V	–1.5%	16.588	+1.5%	
	0℃ ~ 105℃, V_{CC}=3.0 ~ 5.5V	–3.5%	16.588	+3.5%	

4. Reset Timing Characteristics (T_A= –40°C ~ +105°C)

Parameter	Conditions	Min	Typ	Max	Unit
RESET Input Low width	Input V_{CC}=5V ± 10 %	30	–	–	μs
WDT wakeup time	V_{CC}=5V, WDTPSC=11	–	49	–	ms
	V_{CC}=3V, WDTPSC=11	–	55	–	
CPU start up time	V_{CC} = 4V	–	22.4	–	ms

5. ADC Electrical Characteristics (T_A= 25°C, V_{CC}= 3.0V ~ 5.5V, V_{SS}= 0V)

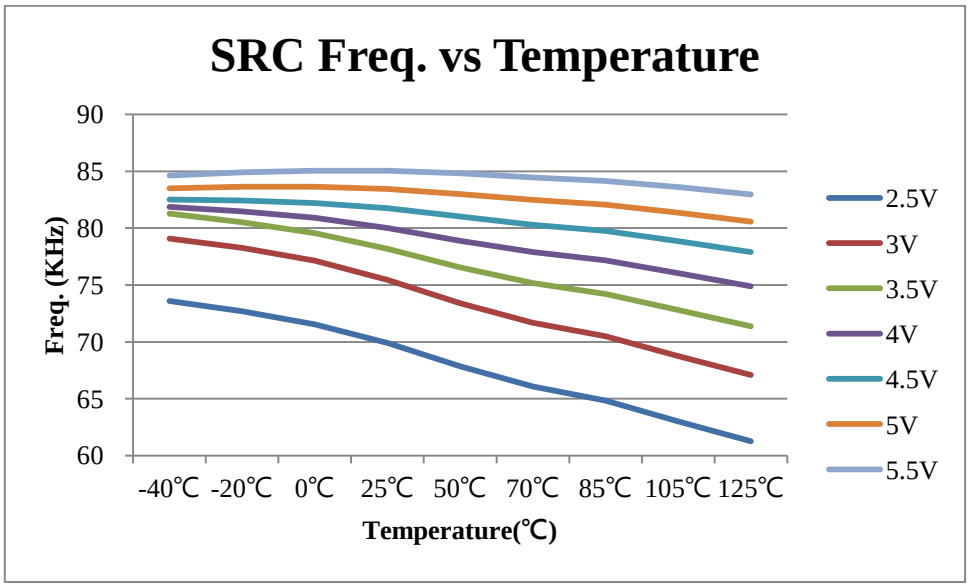
Parameter	Conditions		Min	Typ	Max	Unit
Total Accuracy	V_{CC}=5.12 V, V_{SS}=0V		–	±2.5	±4	LSB
Integral Non-Linearity			–	±3.2	±5	
Max Input Clock (f_{ADC})	Source impedance (Rs < 10KΩ)		–	–	2	MHz
	Source impedance (Rs < 20KΩ)		–	–	1	
	Source impedance (Rs < 50KΩ)		–	–	0.5	
	Source is VBG (ADCHS=1100b)		–	–	1.2	
Conversion Time	F_{ADC} = 1MHz		–	50	–	μs
Bandgap Reference Voltage (V_{BG})	–	V_{CC}=2.5V~5.5V 25℃	-1.5%	1.22	+1.5%	V
		V_{CC}=2.5V~5.5V -40℃~105℃	-1.8%	1.22	+1.8%	
ADC Reference Voltage (V_{ADC})	ADCVREFS=1	V_{CC}=3V~5.5V 25℃	-1.7%	2.54	+1.7%	
		V_{CC}=2.8V~5.5V -40℃~105℃	-2.3%	2.54	+2.3%	
V_{CC}/4 Reference Voltage ($V_{1/4}$)	–	V_{CC}=5V, 25℃	-0.8%	1.252	+0.8%	
		V_{CC}=3.6V, 25℃	-0.8%	0.902	+0.8%	
Input Voltage	–		V_{SS}	–	V_{CC}	V

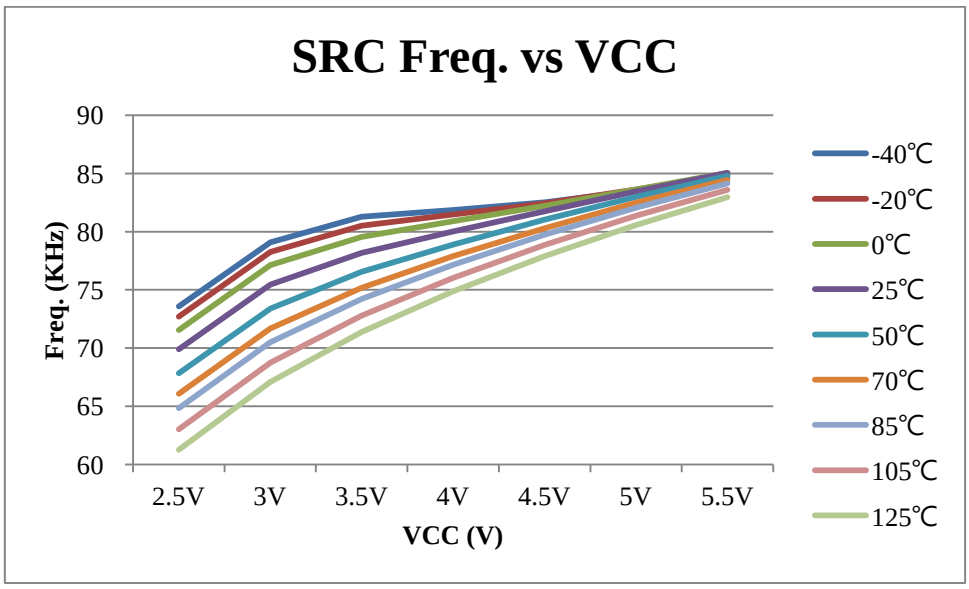
6. EEPROM Characteristics

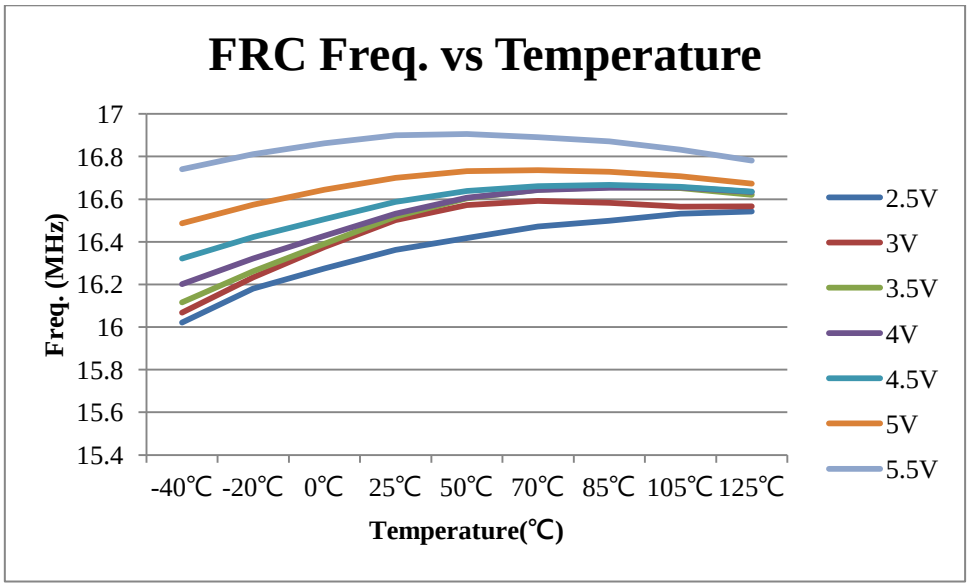
Parameter	Conditions	Min	Typ	Max	Unit
Write Voltage	–20℃ ~ 85℃	3.0	5	5.5	V
	0℃ ~105℃	4.5	5	5.5	
Write Endurance*	V_{CC}=5V, -20℃	30K	–	–	cycles
	V_{CC} =5V, -10℃	50K	–	–	
	V_{CC} =3.0V~5V, 85℃	50K	–	–	
	V_{CC} =4.5V, 0℃~105℃	50K	–	–	

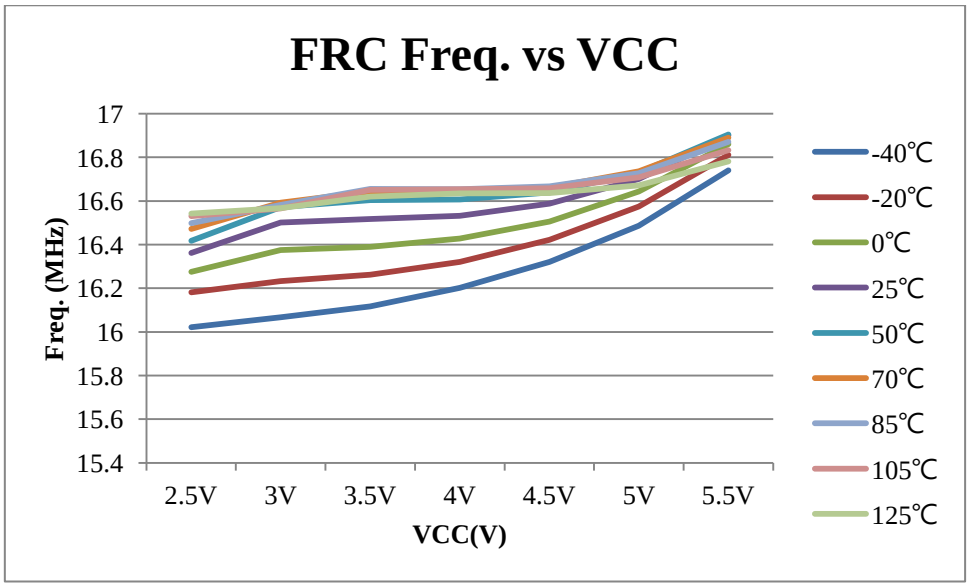
Note: The value of this parameter is based on the characteristics of tested samples.

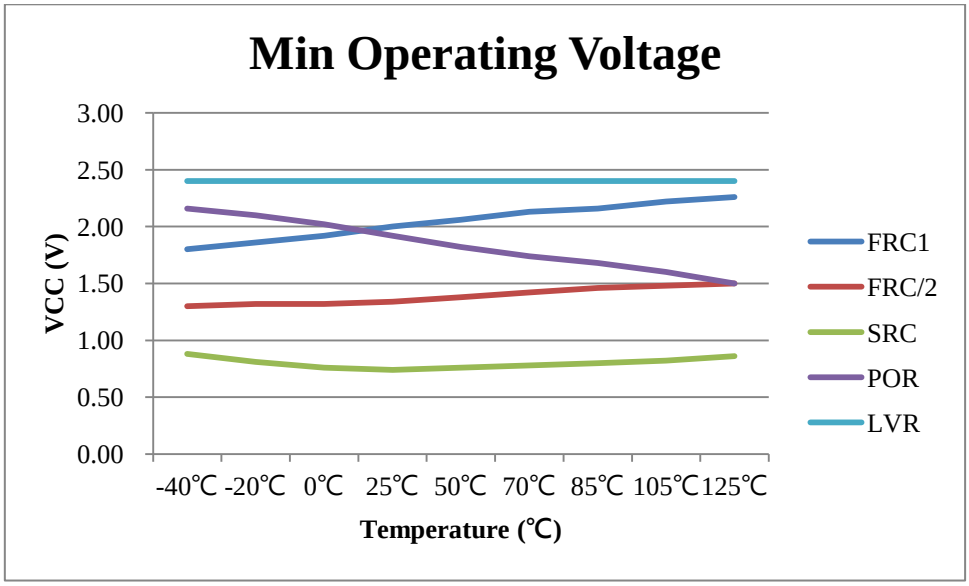
7. Characteristic Graphs



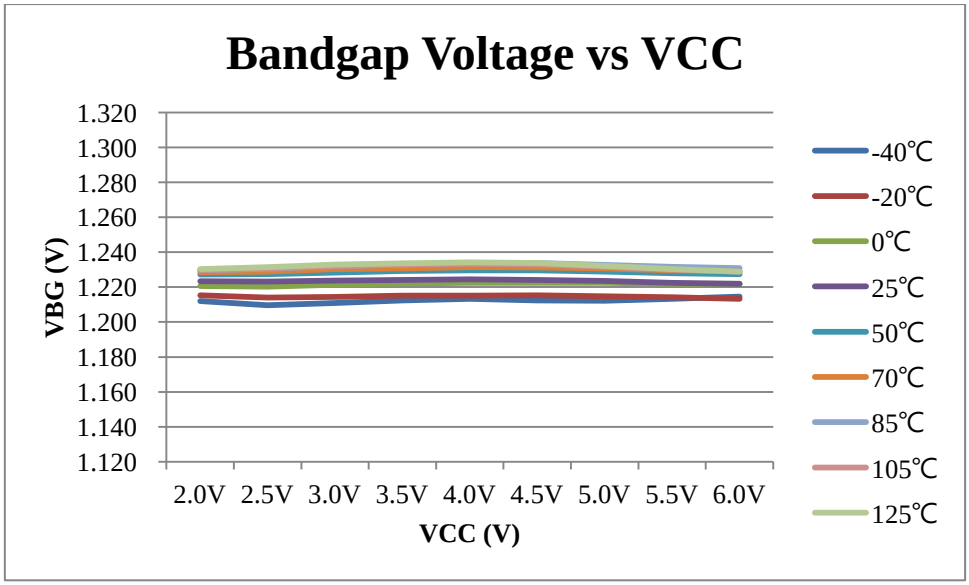



FRC Freq. vs Temperature
Freq. (MHz)
17
16.8
16.6
16.4
16.2
16
15.8
15.6
15.4
-40℃ -20℃ 0℃ 25℃ 50℃ 70℃ 85℃ 105℃ 125℃
Temperature(℃)
2.5V
3V
3.5V
4V
4.5V
5V
5.5V


FRC Freq. vs VCC
Freq. (MHz)
17
16.8
16.6
16.4
16.2
16
15.8
15.6
15.4
2.5V 3V 3.5V 4V 4.5V 5V 5.5V
VCC(V)
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃
105℃
125℃



*POR: Power on reset. VCC should greater than POR when power on. Due to the variation of the manufacturing process, the POR value will be slightly different between different chips.
*There are 16 levels of LVR to choose from by setting CFGWH



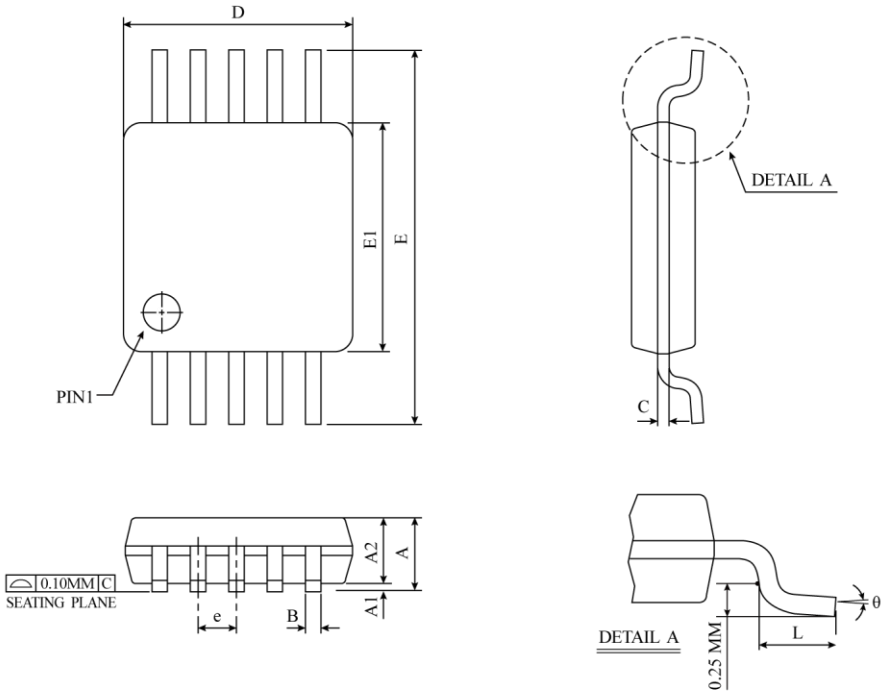
Package and Dice Information

Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

Ordering information

Ordering number	Package
TM52F0C63-MTP	Wafer/Dice blank chip
TM52F0C63-COD	Wafer/Dice with code
TM52F0C63-MTP-53	MSOP 10-pin (118mil)
TM52F0C63-MTP-16	SOP-16 (150mil)
TM52F0C63-MTP-46	TSSOP-20 (173mil)
TM52F0C63-MTP-21	SOP-20 (300mil)
TM52F0C63-MTP-28	SSOP-24 (150mil)
TM52F0C63-MTP-23	SOP-28 (300mil)
TM52F0C63-MTP-29	SSOP-28 (150mil)
TM52F0C63-MTP-D1	QFN-20 (3*3*0.75-0.4mm)(L=0.25mm)
TM52F0C63-MTP-C3	QFN-28 (4x4x0.75-0.4mm)

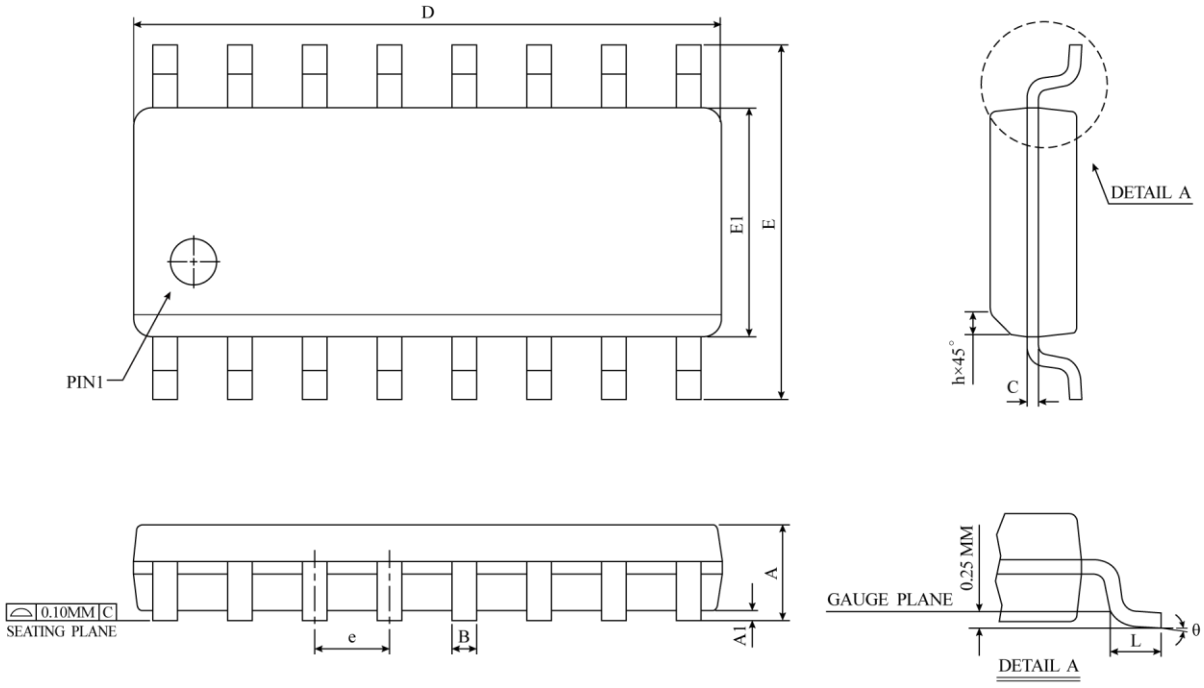
MSOP-10 (118mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.81	0.96	1.10	0.032	0.038	0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.75	0.85	0.95	0.030	0.034	0.037
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	0.50 BSC			0.020 BSC		
L	0.40	0.55	0.70	0.016	0.022	0.028
θ	0°	3°	6°	0°	3°	6°
JEDEC						

△ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.12 MM (0.005 INCH) PER SIDE.
DIMENSION " E1 " DOES NOT INCLUDE MOLD PROTRUSIONS
MOLD PROTRUSIONS SHALL NOT EXCEED 0.25 MM (0.010 INCH) PER SIDE.

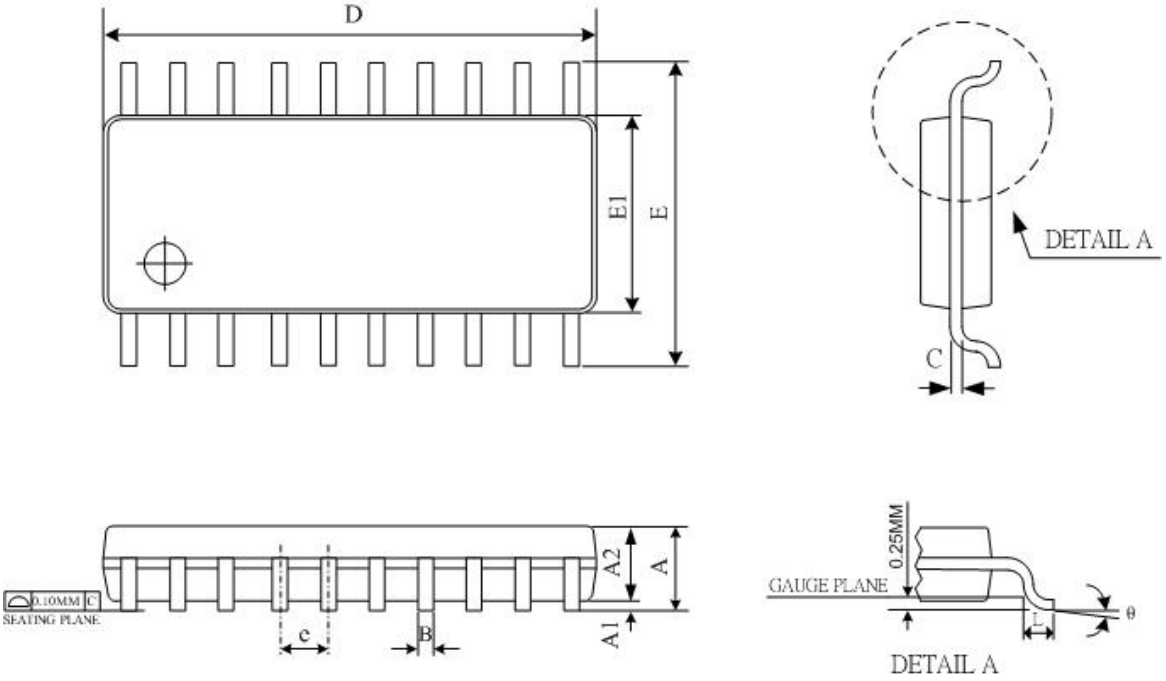
SOP-16 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	9.80	9.90	10.00	0.3859	0.3898	0.3937
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AC)					

* NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

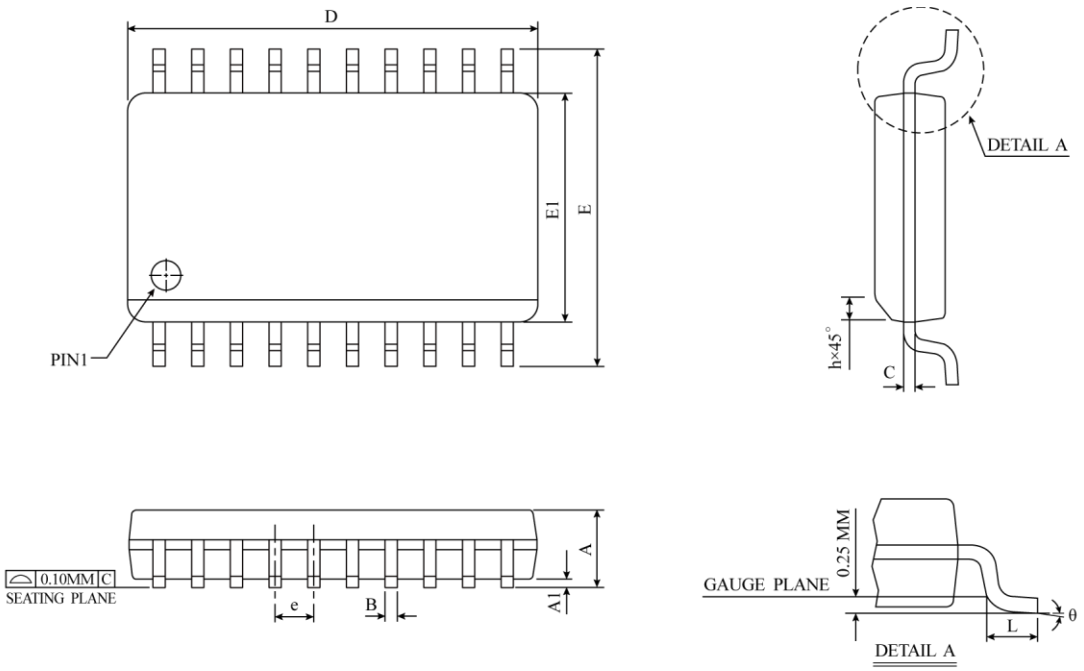
TSSOP-20 (173mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.2	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.8	0.93	1.05	0.031	0.036	0.041
B	0.19	-	0.3	0.007	-	0.012
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.55	0.246	0.252	0.258
E1	4.3	4.4	4.5	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0 °		8 °	0 °		8 °
JEDEC	MO-153 AC REV.F					

Notes：
1.DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
2.DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
3.DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08MM TOTAL IN EXCESS OF THE "B" DIMENSION AT MAXIMUM METERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07MM.

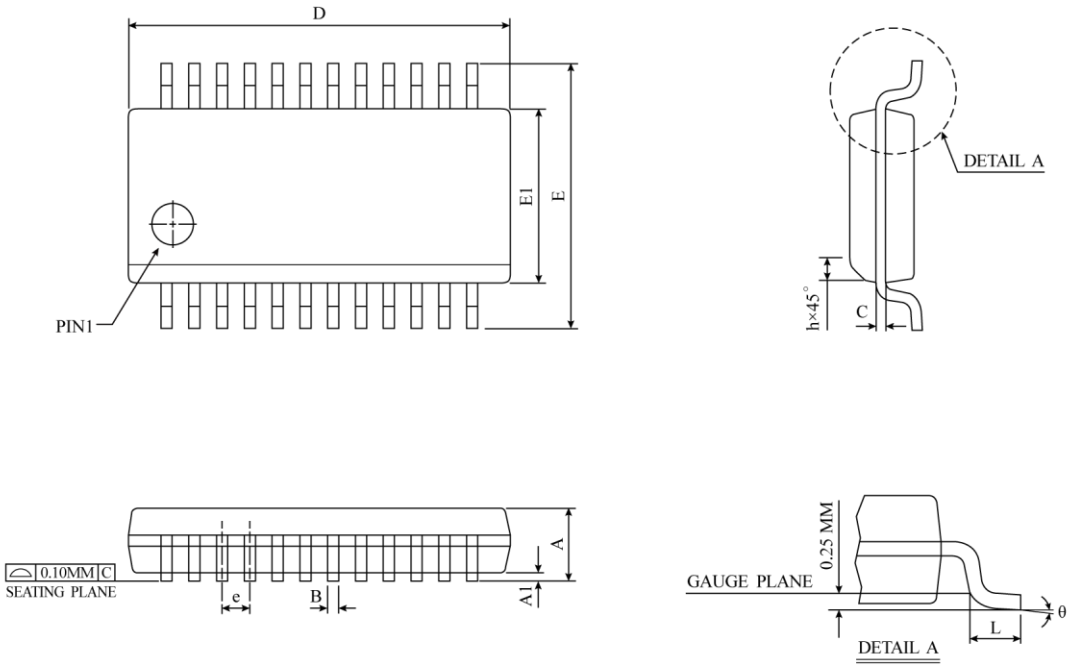
SOP-20 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	12.60	12.80	13.00	0.4961	0.5040	0.5118
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AC)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

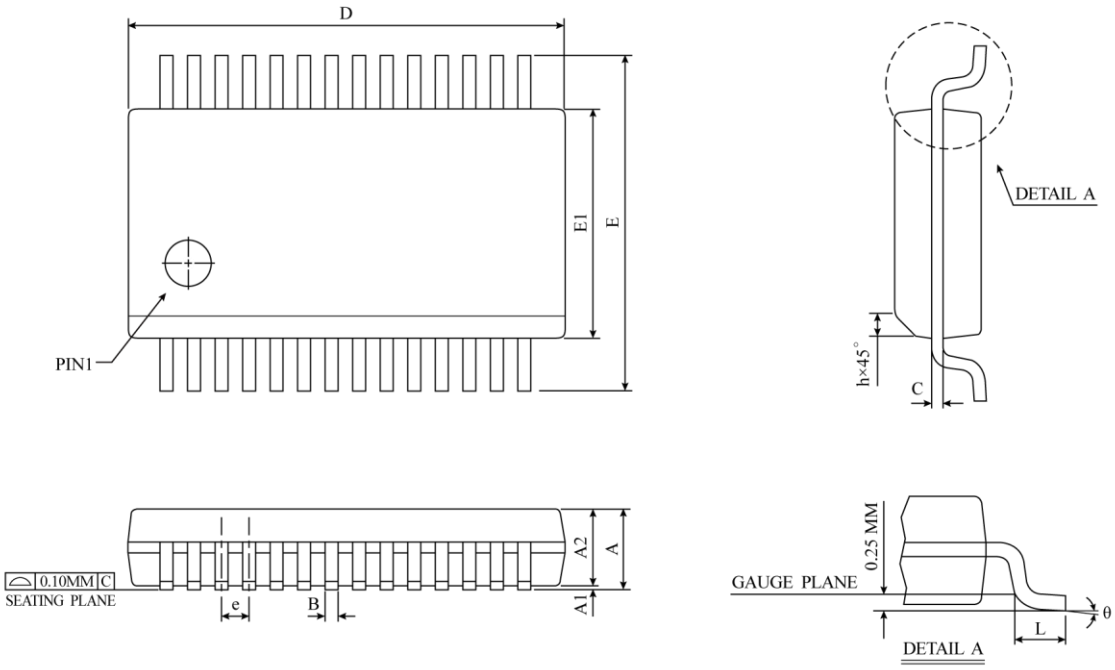
SSOP-24 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.18	0.25	0.004	0.007	0.010
A2	-	-	1.50	-	-	0.059
B	0.20	0.25	0.30	0.008	0.010	0.012
C	0.18	0.22	0.25	0.007	0.009	0.010
D	8.56	8.65	8.74	0.337	0.341	0.344
E	5.79	6.00	6.20	0.228	0.236	0.244
E1	3.81	3.90	3.99	0.150	0.154	0.157
e	0.635 BSC			0.025 BSC		
L	0.41	0.84	1.27	0.016	0.033	0.050
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-137 (AE)					

Ⓑ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD PROTRUSIONS OR GAT BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE.

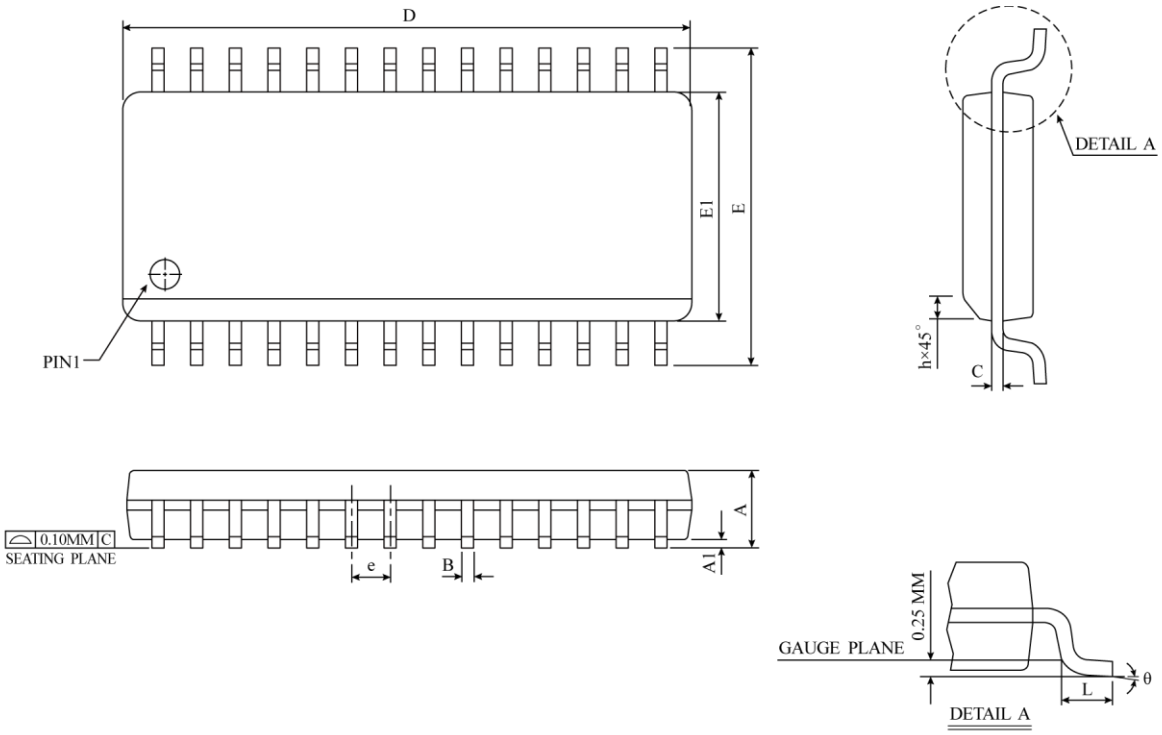
SSOP-28 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.65	1.80	0.06	0.06	0.07
A1	0.102	0.176	0.249	0.004	0.007	0.010
A2	1.40	1.475	1.55	0.06	0.06	0.06
B	0.20	0.25	0.30	0.01	0.01	0.01
C	0.2TYP			0.008TYP		
e	0.635TYP			0.025TYP		
D	9.804	9.881	9.957	0.386	0.389	0.392
E	5.842	6.020	6.198	0.230	0.237	0.244
E1	3.86	3.929	3.998	0.152	0.155	0.157
L	0.406	0.648	0.889	0.016	0.026	0.035
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-137(AF)					

△B *NOTES：DIMENSION "D" DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE.

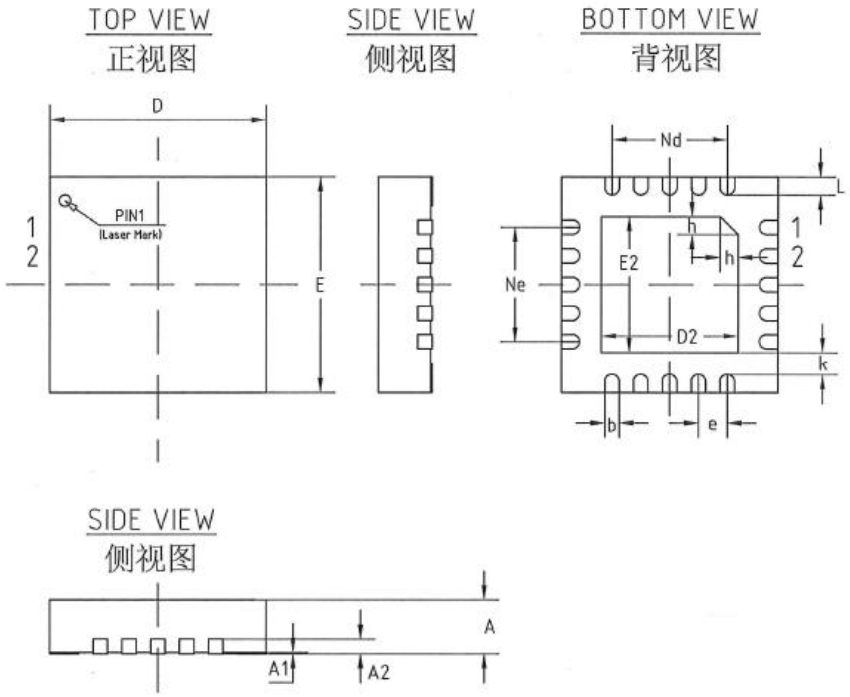
SOP-28 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	17.70	17.90	18.10	0.6969	0.7047	0.7125
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AE)					

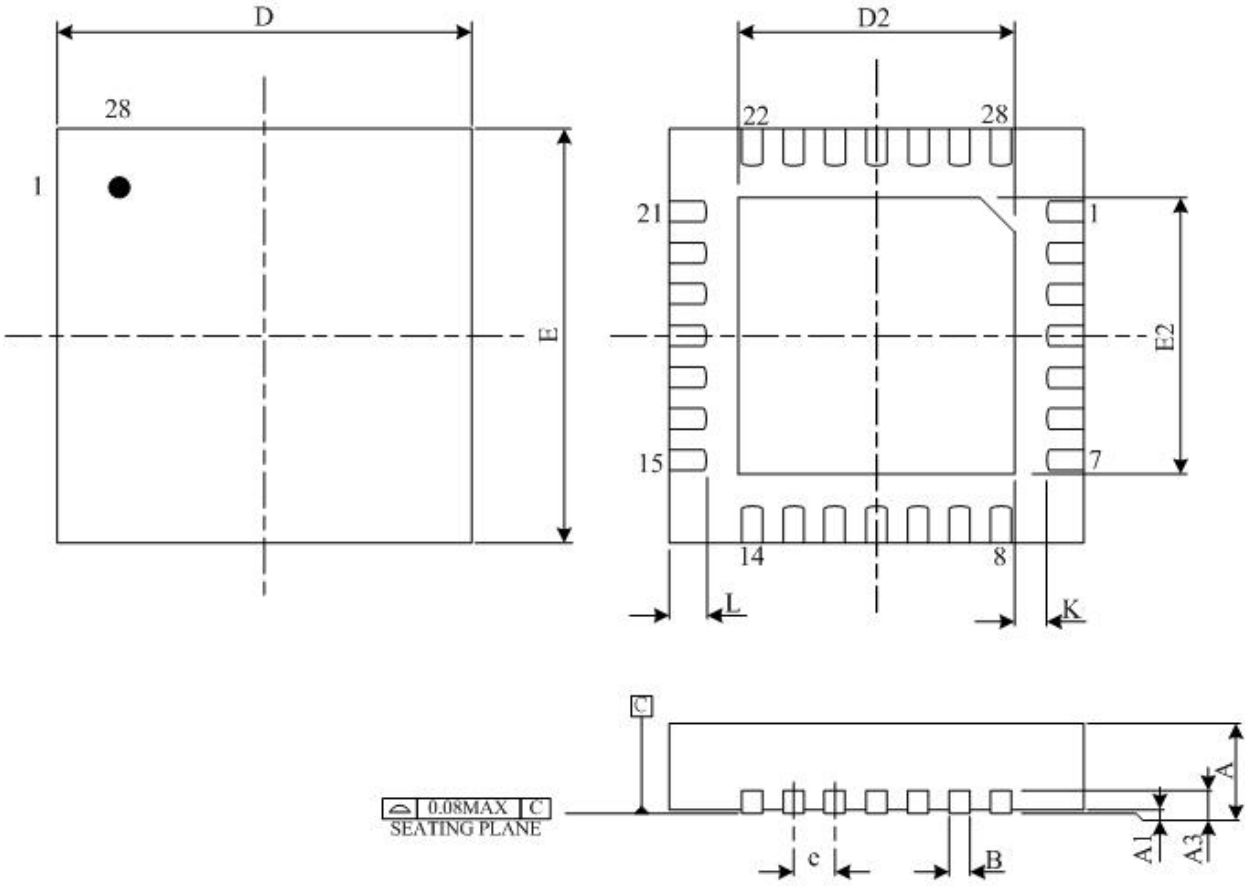
* NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

QFN 20 (3*3*0.75-0.4mm) (L=0.25mm) Package Dimension



机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2	0.203 REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
D2	1.80	1.90	2.00
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
e	0.40 BSC		
K	0.20	0.30	0.40
L	0.20	0.25	0.30
h	0.20	0.25	0.30
Ne	1.60 BSC		
Nd	1.60 BSC		

QFN-28 (4x4x0.75-0.4mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.7	0.75	0.8	0.028	0.030	0.031
A1	0	0.02	0.05	0	0.001	0.002
A3		0.203 REF			0.008 REF	
B	0.15	0.2	0.25	0.006	0.008	0.010
D		4 BSC			0.157	
E		4 BSC			0.157	
D2	2.2	2.3	2.4	0.087	0.091	0.094
E2	2.2	2.3	2.4	0.087	0.091	0.094
e		0.4 BSC			0.016	
L	0.3	0.4	0.5	0.012	0.016	0.020
K		0.45 REF			0.018	
JEDEC		MO-220				