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TM52F2230B/34B

DATA SHEET

Rev 0.95

cAMENDMENT HISTORY

Version	Date	Description
V0.90	Jan, 2015	New release
V0.91	Dec, 2015	**Remark: DS-TM52F2230_34 change Doc No. to DS-TM52F2230_30B_34_34B.** 1. Add F2230B/F2234B device 2. Working voltage (p5, p6, p21) 3. Device comparison table (p9) 4. ICE interface (p9, p70) 5. IAPWE description (p18) 6. VCON setting guide (p23) 7. LVR setting guide (p25) 8. CLKPSC description (p28) 9. Add SRC Diagram (p87) 10. Add LVR1/POR vs Temperature Diagram (p88) 11. Other details of the modifications
V0.92	Apr, 2016	1. Flash description (P16) 2. Stop mode description (P30, P35) 3. ICE mode figure (P70)
V0.93	Sep, 2016	1. Remove F2230/F2234 device 2. Other details of the modifications
V0.94	Oct, 2017	1. Operating voltage suggest modifications 2. Modify SPI Block diagram
V0.95	May, 2018	1. Add package type QFN-32 2. Other details of the modifications

CONTENTS

TM52 F22xx FAMILY

Common Feature

CPU	Flash Program memory	RAM bytes	Dual Clock	Operation Mode	Timer0 Timer1 Timer2	UART	Real-time Timer3	LBD	LVR
Fast 8051 (2T)	8K~32K with IAP, ISP, ICP	512 ~ 2304	SXT SRC FXT FRC	Fast Slow Idle Stop	8051 Standard		0.5~61ppm Adjustable	2.4V ~ 3.1V	1.6V

Family Members Features

P/N	Flash	RAM bytes	IO Pin	RFC ADC	SAR ADC	Touch Key	LCD	LED	SPI	others
TM52-F2261	16K	768	32	3-ch	–	14-ch	43 x 10 1.0~1.5V adj.-Bias	30x6 40mA hi-Sink	Yes	–
TM52-F2264						–				
TM52-F2260	16K	1280	25	3-ch	–	–	36 x 4 1.0V bias	–	–	–
TM52-F2280B	8K	512	32	3-ch	6bit 7-ch	15-ch	23 x 8 1.0~1.5V adj.-Bias	10x4 40mA hi-Sink	Yes	–
TM52-F2284B						–				
TM52-F2230B	32K	2304	32	3-ch	6bit 7-ch	15-ch	–	–	Yes	PWM
TM52-F2234B										

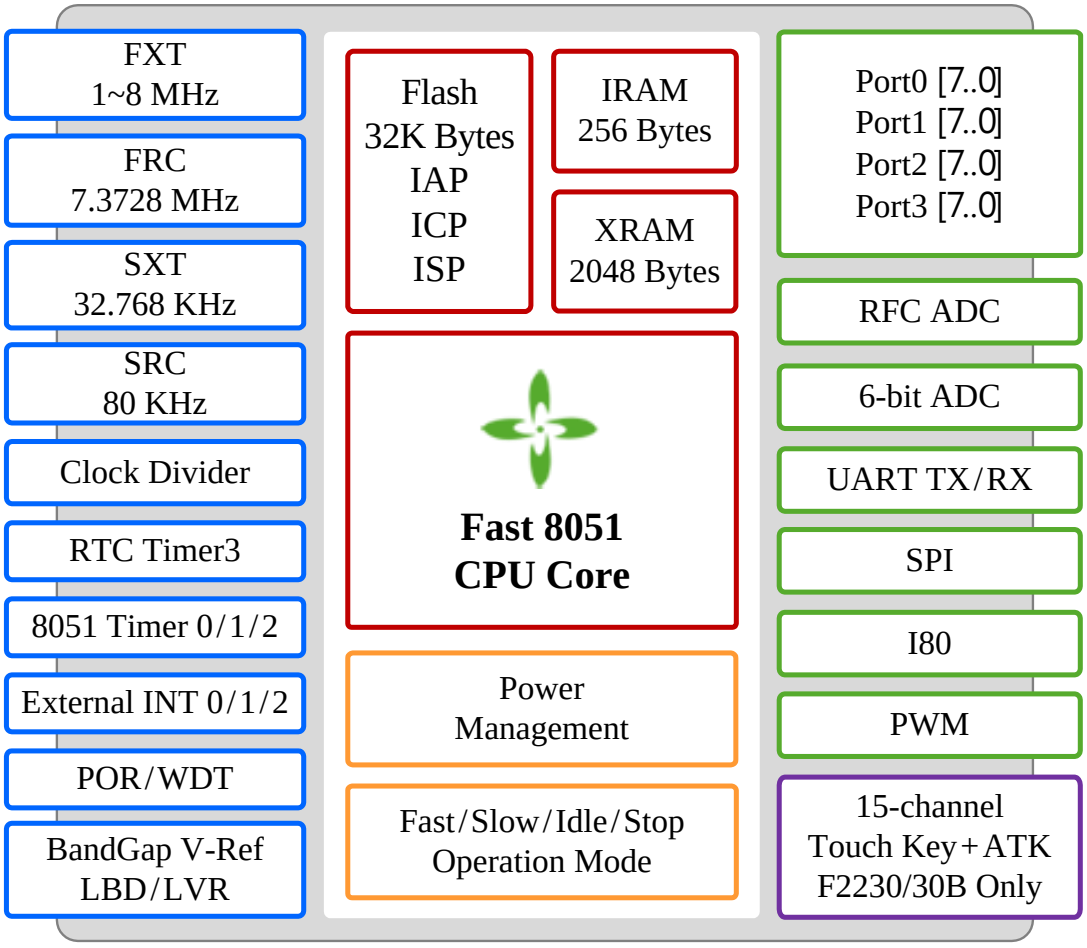
P/N	Operation Voltage	Idle Mode Current (V_{BAT}=3V) with 32KHz wake-up & LVR On				Max. System Clock (Hz)			
		TK Off LCD Off	TK Off LCD On	TK On LCD Off	TK On LCD On	SXT	SRC	FXT	FRC
TM52-F2261	2.0~4.2V	0.8uA	1.4uA	1.3uA	1.9uA	32K	–	–	4M
TM52-F2264				–	–				
TM52-F2260	2.0~4.2V	0.7uA	1.0uA	–	–	32K	–	–	4M
TM52-F2280B	2.0~5.5V	1.3uA	2.4uA	1.7uA	2.8uA	32K	80K	8M	7.37M
TM52-F2284B				–	–				
TM52-F2230B	2.0~5.5V	1.4uA	–	1.8uA	–	32K	80K	8M	7.37M
TM52-F2234B				–					

GENERAL DESCRIPTION

TM52 series F2230B/34B are versions of a new, fast 8051 architecture for an 8-bit microcontroller single chip with an instruction set fully compatible with industry standard 8051, C language development platform, and retains most 8051 peripheral's functional block. Typically, the **TM52-F2230B/34B** executes instructions six times faster than the standard 8051 architecture.

The **TM52-F2230B/34B** provides improved performance, lower cost and fast time-to-market by integrating features on the chip, including 32K Bytes Flash program memory, 2304 Bytes SRAM, Low Voltage Reset (LVR1/2), Low Battery Detector (LBD), dual clock power saving operation mode, SPI Interface, 8051 standard UART and Timer0/1/2, adjustable real time clock Timer3, 15 channels Touch Key with ATK (F2230B only), 6-bit SAR ADC, Resistance to Frequency Converter (RFC) and Watchdog Timer. Its high reliability and low power consumption feature can be widely applied in consumer and home appliance products.

BLOCK DIAGRAM



TM52 series F2230B/34B

FEATURES

1. **Standard 8051 Instruction set, fast machine cycle**
   - Executes instructions six times faster than the standard 8051.
2. **32K Bytes Flash Program Memory**
   - Support "In Circuit Programming" (ICP) or "In System Programming" (ISP) for the Flash code
   - Byte Write "In Application Programming" (IAP) mode is convenient as Data EEPROM access
   - Code Protection Capability
3. **Total 2304 Bytes SRAM (IRAM+XRAM)**
   - 256 Bytes IRAM in the 8051 internal data memory area
   - 2048 Bytes XRAM in the 8051 external data memory area (accessed by MOVX Instruction)
4. **Five System Clock type Selections**
   - Fast clock from Crystal (FXT, 1~8 MHz)
   - Fast clock from Internal RC (FRC, 7.3728 MHz @V_{BAT}=2.8V~5.5V)
   - Fast clock from External RC (RFC)
   - Slow clock from Crystal (SXT, 32768 Hz)
   - Slow clock from Internal RC (SRC, 80 KHz @V_{DD}=3V, 40 KHz @V_{DD}=1.5V)
   - System Clock can be divided by 1/2/4/8/16/32 option
   - System Clock output pin (TCO) for EL/IR application
5. **8051 Standard Timer – Timer0/1/2**
   - 16-bit Timer0, also supports RFC or SXT clock input counting
   - 16-bit Timer1, also supports T1O/T1B clock output for Buzzer/IR application
   - 16-bit Timer2, also supports T2O clock output for Buzzer/IR application
6. **23-bit Timer3 used for Real Time 32768 Hz Crystal counting**
   - ± 0.5 ppm ~ 61 ppm interrupt rate adjustable
   - MSB 8-bit overflow auto-reload
   - 0.25 sec, 0.5 sec, 1.0 sec or overflow Interrupt
7. **15-Channel Touch Key (F2230B only)**
   - 1~4 Key H/W Auto Scan Mode (ATK), Sensitivity Adjustable for each Key
   - Interrupt / Wake-up CPU while Key Pressed
8. **6-bit ADC for low pin count key scan**
   - Up to 100KHz conversion rate
9. **Resistance to Frequency Converter (RFC)**
   - RFC clock divided by 1/4/16/64 signal can be assigned as Timer0 event count input
   - RFC clock can be used as System clock source

10. **8051 Standard UART**
    - One Wire UART option can be used for ISP or other application
11. **An independent "8+2" bits PWM with prescaler/period-adjustment**
12. **SPI Interface**
    - Master or Slave mode selectable
    - Programmable transmit bit rate
    - Serial clock phase and polarity options
    - MSB-first or LSB-first selectable
13. **I80 Interface**
14. **11-Sources, 4-level priority Interrupt**
    - Timer0/Timer1/Timer2/Timer3 Interrupt
    - INT0/INT1 Falling-Edge/Low-Level Interrupt
    - Port1 Pin Change Interrupt
    - UART TX/RX Interrupt
    - P2.7 (INT2) Interrupt
    - Touch Key Interrupt
    - SPI Interrupt
15. **Pin Interrupt can Wake up CPU from Power-Down (Stop) mode**
    - P3.2/P3.3 (INT0/INT1) Interrupt & Wake-up
    - P2.7 (INT2) Interrupt & Wake-up
    - Each Port1 pin can be defined as Interrupt & Wake-up pin (by pin change)
16. **Max. 32 Programmable I/O pins**
    - CMOS Output
    - Pseudo-Open-Drain, or Open-Drain Output
    - Schmitt Trigger Input
    - Pin Pull-up can be Enabled or Disabled
17. **BandGap Voltage Reference for Low Battery Detection (LBD)**
    - Detect V_{BAT} voltage level from 2.4V to 4.5V
18. **Built-in tiny current LDO Regulator for chip internal power supply (V_{DD})**
    - V_{DD} voltage level can be set to $0.4*V_{BAT}$ ~ $0.66*V_{BAT}$ in different mode
19. **Watch Dog Timer based on System Clock**
    - Running in Fast/Slow Mode, Stop counting in Idle/Stop Mode
    - 32K or 64K counts overflow Reset

20. Six types Reset

- Power on Reset
- Selectable External Pin Reset
- Selectable Watch Dog Reset
- Software Command Reset
- Selectable Battery Low Voltage Reset #1 (LVR1, when V_{BAT}<1.6V)
- Selectable Battery Low Voltage Reset #2 (LVR2, when V_{BAT}<2.4V~4.5V)

21. 4 Power Operation Modes

- Fast/Slow/Idle/Stop Mode

22. On-chip Debug/ICE interface

- Use P1.2/P1.3 or P2.2 / P2.3pin, share with ICP programming pin

23. Operating Voltage and Current

- V_{BAT}=2.0V~5.5V
- 0.1uA LVR1 Current @V_{BAT}=3V
- 1.1uA SXT/SRC and System Clock Current @V_{DD}=1.5V
- 0.5uA Touch Key Current @V_{BAT}=3V
- Total 1.8uA Idle mode Current with LVR1 on and TK scan @V_{BAT}=3V, V_{DD}=1.5V

24. Operating Temperature Range

- –40℃ ~ +85℃

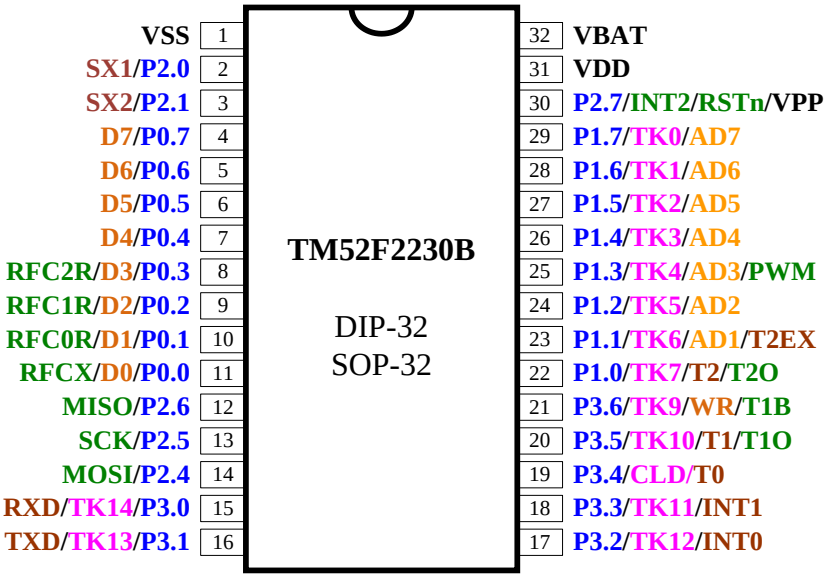
25. Package Types

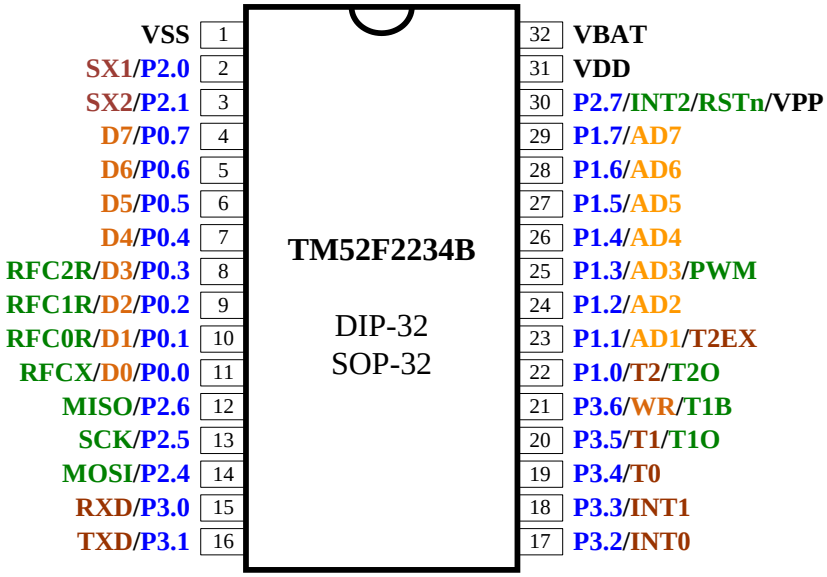
- DIP 32-pin (600 mil)
- SOP 32-pin (300 mil)
- QFN32-pin (5x5x0.75-0.5mm)

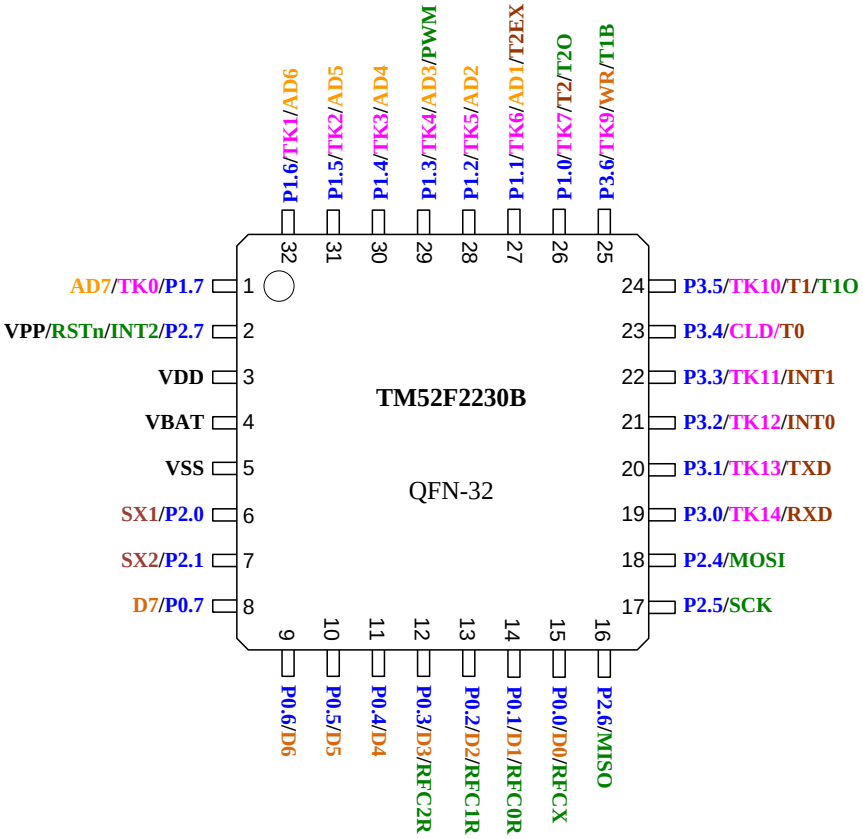
F2230/F2230B/F2234/F2234B Features comparison table

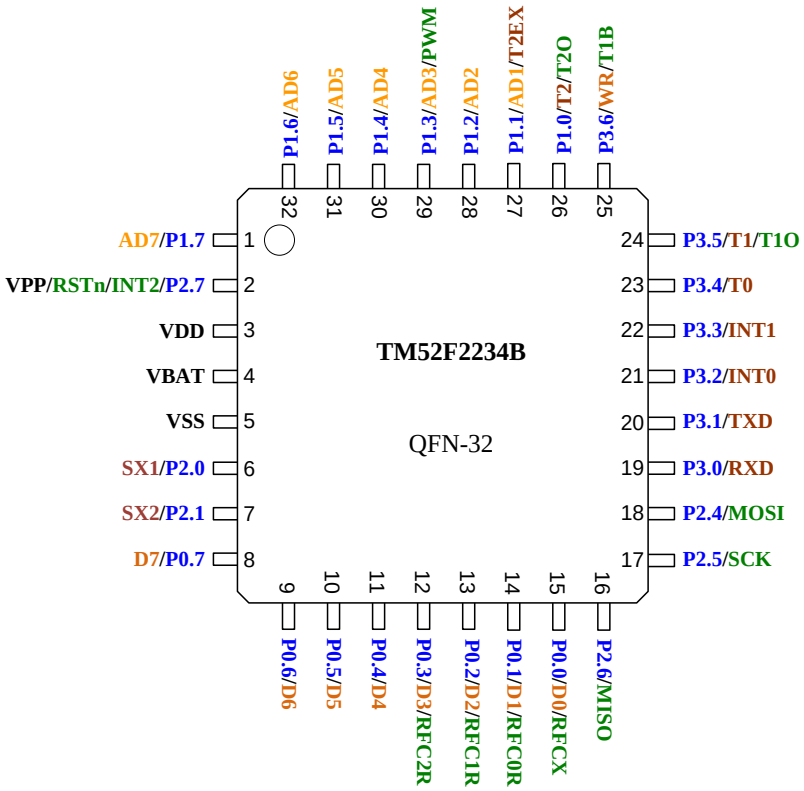
Features	F2230	F2234	F2230B	F2234B
Touch Key	Yes	n.a.	Yes	n.a.
IAP Write Control	No IAPWE constrain		Need to enable IAPWE before IAP write	
Max. System Clock	6 MHz, or FRC/2		8 MHz, or FRC/1	

PIN ASSIGNMENT






TM52F2230B
QFN-32
1 AD7/TK0/P1.7
2 VPP/RSTn/INT2/P2.7
3 VDD
4 VBAT
5 VSS
6 SX1/P2.0
7 SX2/P2.1
8 D7/P0.7
9 P0.6/D6
10 P0.5/D5
11 P0.4/D4
12 P0.3/D3/RFC2R
13 P0.2/D2/RFC1R
14 P0.1/D1/RFC0R
15 P0.0/D0/RFCX
16 P2.6/MISO
17 P2.5/SCK
18 P2.4/MOSI
19 P3.0/TK14/RXD
20 P3.1/TK13/TXD
21 P3.2/TK12/INT0
22 P3.3/TK11/INT1
23 P3.4/CLD/T0
24 P3.5/TK10/T1/T1O
25 P3.6/TK9/WR/T1B
26 P1.0/TK7/T2/T2O
27 P1.1/TK6/AD1/T2EX
28 P1.2/TK5/AD2
29 P1.3/TK4/AD3/PWM
30 P1.4/TK3/AD4
31 P1.5/TK2/AD5
32 P1.6/TK1/AD6


TM52F2234B
QFN-32
1 AD7/P1.7
2 VPP/RSTn/INT2/P2.7
3 VDD
4 VBAT
5 VSS
6 SX1/P2.0
7 SX2/P2.1
8 D7/P0.7
9 P0.6/D6
10 P0.5/D5
11 P0.4/D4
12 P0.3/D3/RFC2R
13 P0.2/D2/RFC1R
14 P0.1/D1/RFC0R
15 P0.0/D0/RFCX
16 P2.6/MISO
17 P2.5/SCK
18 P2.4/MOSI
19 P3.0/RXD
20 P3.1/TXD
21 P3.2/INT0
22 P3.3/INT1
23 P3.4/T0
24 P3.5/T1/T1O
25 P3.6/WR/T1B
26 P1.0/T2/T2O
27 P1.1/AD1/T2EX
28 P1.2/AD2
29 P1.3/AD3/PWM
30 P1.4/AD4
31 P1.5/AD5
32 P1.6/AD6

PIN DESCRIPTION

Name	In/Out	Pin Description
P1.0~P1.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software. These pin's level change can interrupt/wake up CPU from Idle/Stop mode.
P3.0~P3.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "**pseudo open drain**" output. Pull-up resistors are assignable by software.
P3.3~P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
P0.0~P0.7 P2.0~P2.6	I/O	Bit-programmable I/O port for Schmitt-trigger input or CMOS push-pull output. Pull-up resistors are assignable by software.
P2.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or "open-drain" output. Pull-up resistor is fix enable.
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Stop mode wake up input
INT2	I	External falling edge Interrupt input, Idle/Stop mode wake up input
RXD	I/O	UART Mode0 transmit & receive data, Mode1/2/3 receive data
TXD	I/O	UART Mode0 transmit clock, Mode1/2/3 transmit data. In One Wire UART mode, this pin transmits and receives serial data.
MISO	I/O	SPI data input for Master mode, data output for Slave mode
MOSI	I/O	SPI data output for Master mode, data input for Slave mode
SCK	I/O	SPI clock output for Master or clock input for Slave mode
T0, T1, T2	I	Timer0, Timer1, Timer2 event count pin input
T2EX	I	Timer2 external trigger input
PWM	O	8+2 bit PWM output
T1O, T1B	O	Positive and Negative signal pair of Timer1 overflow divided by 2/3/4 output
T2O	O	Timer2 overflow divided by 2/3/4 output
TCO	O	System Clock divided by 1/2/3/4 output
RFC0R~RFC2R	O	RFC resistor connection pin
RFCX	I	RFC clock input pin
D0~D7	I/O	I80 interface data bus
WR	O	I80 interface write enable
RD	O	I80 interface read enable
AD1~AD7	I	6 bit ADC channel input
TK0~TK14	I	Touch Key Input (F2230B only)
CLD	I/O	Touch Key charge collection capacitor connection pin (F2230B only)
RSTn	I	External active low reset input, Pull-up resistor is fixed enable
SX1, SX2	–	32768 Crystal/Resonator oscillator connection for System Clock (SXT)
FX1, FX2	–	1~8 MHz Crystal / Resonator oscillator connection for System clock (FXT)
VPP	I	Flash memory programming high voltage input
VDD	–	LDO Regulator output and internal power supply, add 1 uF capacitor to V_{SS}
VBAT, VSS	P	Power input pin and ground, V_{BAT} is the I/O pin power supply

Note: Digital I/O pins voltage swing from V_{SS} to V_{BAT}.

PIN SUMMERY

DIP/SOP-32	QFN-32	Pin Name	Type	Input		Output			Alternative Function				
				Wake up	Ext. Interrupt	CMOS P.P.	P.O.D.	O.D.	Touch Key	ADC Input	Timer Input	I80	Others
1	5	**VSS**	P										
2	6	**SX1/P2.0**	I/O			●							SXT
3	7	**SX2/P2.1**	I/O			●							SXT
4	8	**D7/P0.7**	I/O			●						●	
5	9	**D6/P0.6**	I/O			●						●	
6	10	**D5/P0.5**	I/O			●						●	
7	11	**D4/P0.4**	I/O			●						●	
8	12	**RFC2R/D3/P0.3**	I/O			●						●	RFC
9	13	**RFC1R/D2/P0.2**	I/O			●						●	RFC
10	14	**RFC0R/D2/P0.1**	I/O			●						●	RFC
11	15	**RFCX/D1/P0.0**	I/O			●					●	●	RFC
12	16	**MISO/ P2.6**	I/O			●							SPI
13	17	**SCK/ P2.5**	I/O			●							SPI
14	18	**MOSI/ P2.4**	I/O			●							SPI
15	19	**RXD/TK14/ P3.0**	I/O			●	●		●				UART
16	20	**TXD/TK13/ P3.1**	I/O			●	●		●				UART
17	21	**INT0/TK12/ P3.2**	I/O	●	●	●	●		●				
18	22	**INT1/TK11/ P3.3**	I/O	●	●	●		●	●				
19	23	**T0/CLD/P3.4**	I/O			●		●	●		●		
20	24	**T1/T1O/TK10/P3.5**	I/O			●		●	●		●		Clock out
21	25	**T1B/WR/TK9/P3.6**	I/O			●		●	●			●	Clock out
22	26	**T2/T2O/TK7/P1.0**	I/O	●	●	●		●	●		●		Clock out
23	27	**T2EX/AD1/TK6/P1.1**	I/O	●	●	●		●	●	●	●		
24	28	**AD2/TK5/P1.2**	I/O	●	●	●		●	●	●			
25	29	**PWM/AD3/TK4/P1.3**	I/O	●	●	●		●	●	●			PWM
26	30	**AD4/TK3/P1.4**	I/O	●	●	●		●	●	●			
27	31	**AD5/TK2/P1.5**	I/O	●	●	●		●	●	●			
28	32	**AD6/TK1/P1.6**	I/O	●	●	●		●	●	●			
29	1	**AD7/TK0/P1.7**	I/O	●	●	●		●	●	●			
30	2	**VPP/RSTn/INT2/P2.7**	I/O	●	●			●					Reset/VPP
31	3	**VDD**	–										
32	4	**VBAT**	P										

Symbol:

P.P. = CMOS Push-Pull Output
O.D. = Open Drain
P.O.D. = Pseudo Open Drain
PU = Pull up
DL = Drive Low

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The TM52 device features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a programg counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as “A” or “ACC” including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR **E0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC:** Accumulator

1.2 B Register (B)

The “B” register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands be in A and B.

SFR **F0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B:** B register

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer. The Stack Pointer points to the top location of the stack.

SFR **81h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP:** Stack Point

1.4 Dual Data Pointer (DPTRs)

TM52 device has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs.

SFR **82h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL:** Data Point low byte

SFR **83h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH:** Data Point high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	–	–	–	TKSOC	CLRWDT	CLRTM3	STPRFC	DPSEL
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

F8h.0 **DPSEL:** Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The instructions that affect the PSW are listed below.

Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR **D0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY:** ALU carry flag

D0h.6 **AC:** ALU auxiliary carry flag

D0h.5 **F0:** General purpose user-definable flag

D0h.4~3 **RS1, RS0:** The contents of (RS1, RS0) enable the working register banks as:

00: Bank 0 (00h~07h)

01: Bank 1 (08h~0Fh)

10: Bank 2 (10h~17h)

11: Bank 3 (18h~1Fh)

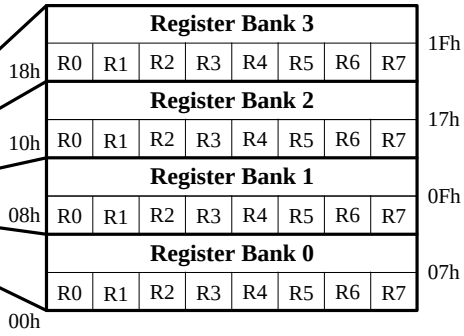
D0h.2 **OV:** ALU overflow flag

D0h.1 **F1:** General purpose user-definable flag

D0h.0 **P:** Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of "one" bits in the accumulator.

PSW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CY	**AC**	**FO**	**RS1**	**RS0**	**OV**	**F1**	**P**

RS1	**RS0**	**Bank**
1	1	3
1	0	2
0	1	1
0	0	0



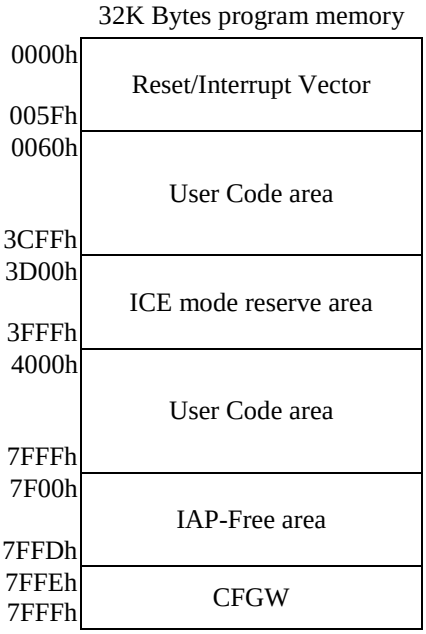
2. Memory

2.1 Program Memory

The **F2230B/34B** has a 32K Bytes Flash program memory, which can support In Circuit Programming (ICP), In Application Programming (IAP) and In System Programming (ISP) function modes. The Flash write endurance is at least 10K cycles. The Flash program memory address continuous space (0000h~7FFFh) is partitioned to several sectors for device operation.

2.1.1 Program Memory Functional Partition

The last 2 bytes (7FFEh~7FFFh) of program memory is defined as chip Configuration Word (CFGW), which is loaded into the device control registers upon power on reset (POR). The address space 7F00h~7FFDh is the IAP free area, while the 0000h~005Fh is occupied by Reset/Interrupt vectors as standard 8051 definition. In the in-circuit emulation (ICE) mode, user also needs to reserve the address space 3D00h~3FFFh for ICE System communication.



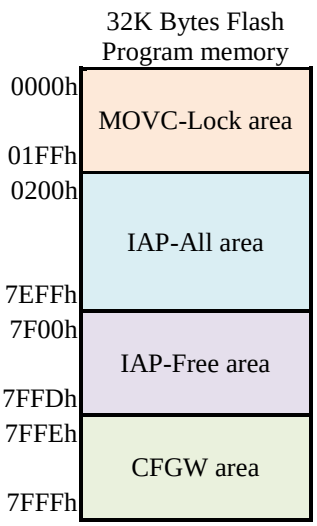
2.1.2 Flash ICP Mode

The Flash memory can be programmed by the tenx proprietary writer **(TWR98/TWR99)**, which needs at least four wires (VBAT, VSS, P1.2, and P1.3 pins) to connect to this chip. To shorten the programming time, it is recommended to connect Writer with an additional fifth wire, which is the VPP (P2.7) pin. If the user wants to program the Flash memory on the target circuit board (In Circuit Programming, ICP), these pins must be reserved sufficient freedom to be connected to the Writer. More pins connected to Writer ensure more writing efficiency and speed.

Writer wire number	Pin connection
4-Wire	VBAT, VSS, P1.2, P1.3
5-Wire	VBAT, VSS, P1.2, P1.3, VPP
6-Wire	VBAT, VSS, P1.2, P1.3, VPP, P1.0

2.1.3 Flash IAP Mode

The **F2230B/34B** has "In Application Programming" (IAP) capability, which allows software to read/write data from/to the Flash memory during CPU run time as conveniently as data EEPROM access. The IAP function is byte writable, meaning that the **F2230B/34B** does not need to erase one Flash page before write. The available IAP data space is 254 Bytes after chip reset, and can be re-defined by the "MVCLOCK" and "IAPALL" control register as shown below.



Flash memory	MVCLOCK	IAPALL	MOVC Accessible	MOVX (IAP) Accessible
0000h~01FFh	1	X	No	No
	0	0	Yes	No
	0	1	Yes	Yes
0200h~7FFFh	X	0	Yes	No
	X	1	Yes	Yes
7F00h~7FFDh	X	X	Yes	Yes
7FFEh	X	0	Yes	No
	X	1	Yes	Yes
7FFFh	X	X	Yes	No

In IAP mode, the program Flash memory is separated into four sectors: MOVC-Lock area, IAP-All area, IAP-Free area, and CFGW area. These four sectors are regulated differently.

In the **MOVC-Lock area,** IAP read/write is limited by MVCLOCK bit, which can be set to control the accessibility of the MOVC and MOVX instructions to this area. The size of this area is 512 Bytes. The lock function is made to protect the main program code against unconsciously writing Flash memory in IAP mode. Locking or unlocking the function should be performed by the tenx TWR98/99 writing to the CFGW in Flash memory.

The **IAP-All area** is protected by the IAPALL register to prevent IAP mode from writing application data to the program area, resulting in a program code error that cannot be repaired. The size of this area is 32000 Bytes. Enabling IAPALL requires writing 65h to SFR SWCMD 97h to set the IAPALL control flag. Then, software can use MOVX instructions to write application data to flash memory from 0200h to 7EFFh. If user wants to disable IAPALL function, user can write other values to SFR SWCMD 97h to clear the IAPALL control flag. User must be careful not to overwrite program code which is already resided on the same Flash memory area.

The **IAP-Free area** has no control bit to protect. It can be used to reliably store system application data that needs to be programmed once or periodically during system operation. Other areas of Flash memory can be used to store data, but this area is usually the best. The size of this area is 254 Bytes, equivalent to an EEPROM, and Flash memory can provide byte access to read and write commands. In the past, storage of configuration data required an additional EEPROM or the other storage device. However, this functionality can now be provided by on-chip Flash, reducing the chip count of embedded applications. An external EEPROM or SRAM may not be needed.

The **CFGW area** has 2 data bytes (CFGWH and CFGWL), which is located at the last 2 addresses of Flash memory. The CFGWH is not accessible to IAP, while the CFGWL can be read or written by IAP in case the IAPALL flag is set. CFGWL is copied to the SFR F7h after power on reset, software then

take over CFGWL's control capability by modifying the SFR F7h. The CFGWL is defined as FRC adjustment register in F2230B/34B.

2.1.4 IAP Mode Access Routines

Flash IAP write is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target Flash address (0~7FFEh), and the ACC contains the data being written. The F2230B/34B accepts IAP Write command only when the IAPWE SFR is enabled; but F2230/34 does not have such constrain. Flash IAP writing requires approximately 500uS. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers and others) continue running during the writing time. The software must handle the pending interrupts after an IAP write. Flash IAP writing needs slower SYSCLK frequency as well as higher V_{DD} voltage. User must make a condition of 2.8V<V_{DD}<3.6V for IAP write.

Because the Program memory and the IAP data space share the same entity, a Flash IAP read can be performed by the "MOVX A, @DPTR" or "MOVC" instruction as long as the target address points to the 0~7FFFh area. A Flash IAP read does not require extra CPU wait time.

```
; IAP example code
; need 2.8V < VDD < 3.6V
MOV     DPTR, #7F00h        ; DPTR=7F00h=target IAP address
MOV     A, #5Ah             ; A=5Ah=target IAP write data
MOV     A9h, #A0h           ;IAPWE=1 for F2230B/34B
MOVX    @DPTR, A            ; Flash [7F00h] =5Ah, after IAP write
                            ; 200µs~500µs H/W writing time, CPU wait
MOV     A9h, #00h           ; IAPWE=0 immediately after IAP write
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=5Ah
CLR     A                   ; A=0
MOVC    A, @A+DPTR          ; A=5Ah
```

Flash **7FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	MVCLOCK	WDTE	–	–	LVR1E	–

7FFFh.5 **MVCLOCK:** If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL / SWRST							
R/W	W							R/W
Reset	–							0

97h.7~0 **IAPALL (W) :** Write 65h to set IAPALL control flag; Write other value to clear IAPALL flag. It is recommended to clear it immediately after IAP access.

97h.0 **IAPALL (R) :** Flag indicates Flash memory sectors can be accessed by IAP or not. This bit combines with MVCLOCK to define the accessible IAP area.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	IAPWE			SPIE	TKIE	EX2	P1IE	TM3IE
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

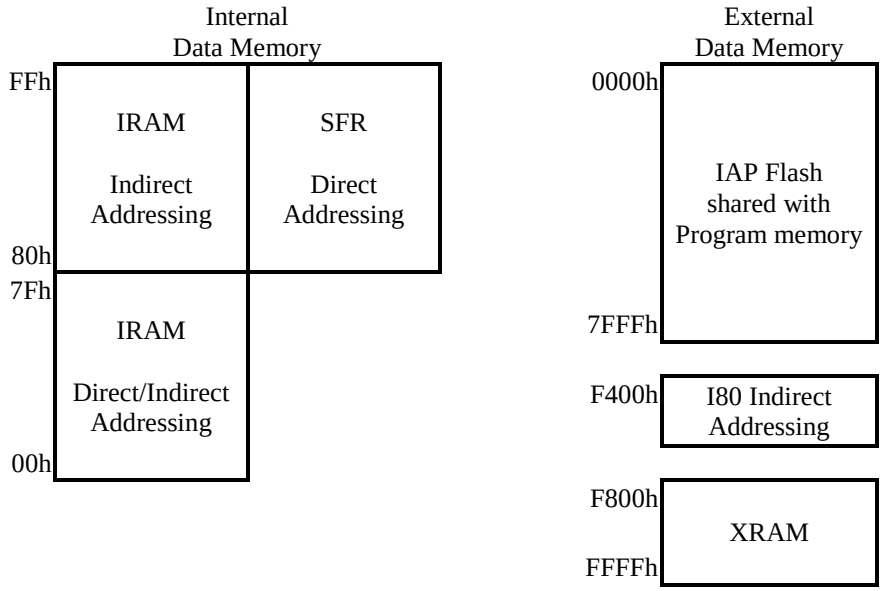
A9h.7~5 **IAPWE:** IAP write enable control (only for F2230B/34B)
101: Enable IAP write. It is recommended to clear it immediately after IAP write.
Others value: Disable IAP write.

2.1.5 Flash ISP Mode

The "In System Programming" (ISP) usage is similar to IAP, except the purpose is to refresh the Program code. User can use UART/SPI or other method to get new Program code from external host, then writes code as the same way as IAP. ISP operation is complicated; basically it needs to assign a Boot code area to the Flash which does not change during the ISP process.

2.2 Data Memory

As the standard 8051, the **F2230B/34B** has both Internal and External Data Memory space. The Internal Data Memory space consists of 256 Bytes IRAM and 68 SFRs, which are accessible through a rich instruction set. The External Data Memory space consists of 2048 Bytes XRAM, I80 indirect addressing and IAP Flash, which can be only accessed by MOVX instruction.



2.2.1 IRAM

IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

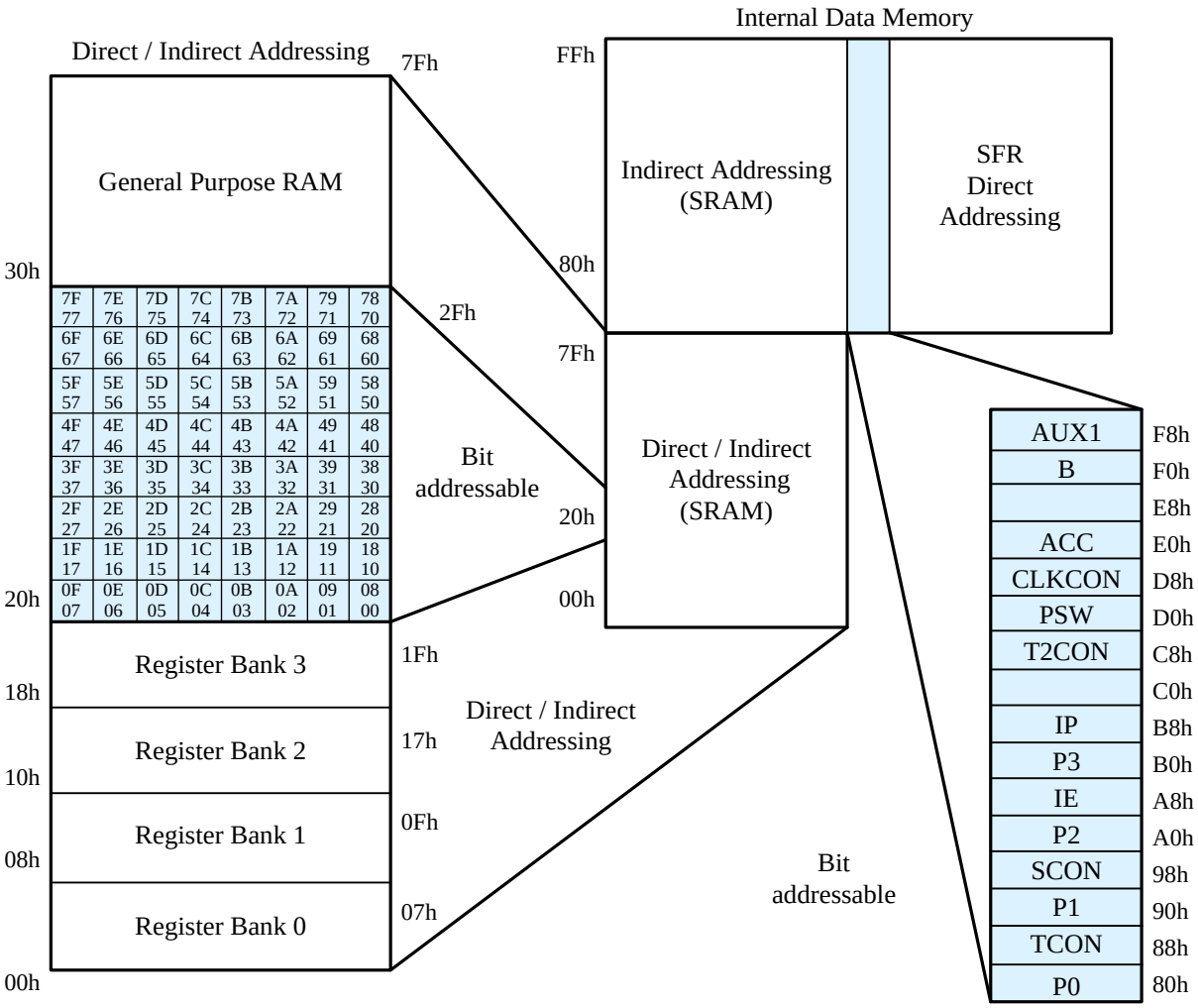
2.2.2 XRAM

XRAM is located in the 8051 external data memory space (address from F800h to FFFFh). The 2048 Bytes XRAM can be only accessed by "MOVX" instruction.

2.2.3 SFRs

All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit-addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with the resources and peripherals of the **F2230B/34B**. The TM52 series of microcontrollers provides

complete binary code with standard 8051 instruction set compatibility. Beside the standard 8051 SFRs, the **F2230B/34B** implements additional SFRs used to configure and access subsystems such as the SPI or I80, which are unique to the **F2230B/34B**.

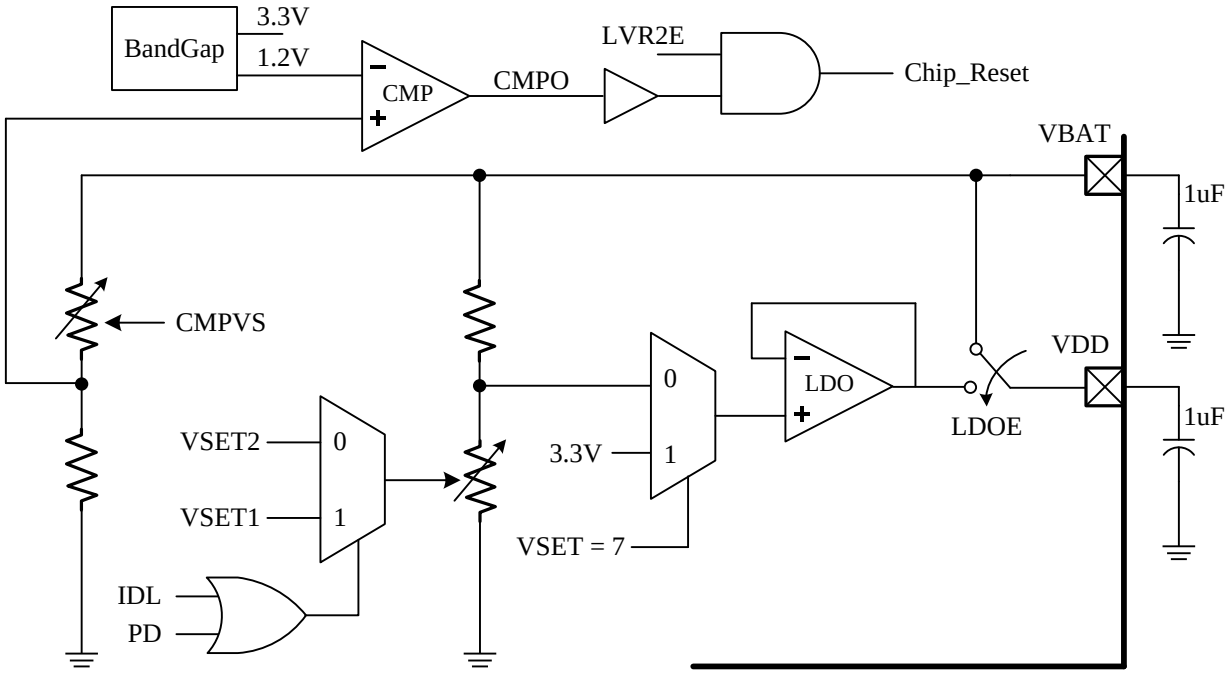


	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B							CFGWL
E8h								
E0h	ACC							
D8h	CLKCON							
D0h	PSW							
C8h	T2CON		RCP2L	RCP2H	TL2	TH2		
C0h			BGADCS	BGADCD	ATKCMP0	ATKCMP1	ATKCMP2	ATKCMP3
B8h	IP	IPH	IP1	IP1H	SPCON	SPSTA	SPDAT	PINMODE
B0h	P3			TM3SEC	TM3DL	TM3DH	TM3RLD	TM3ADJ
A8h	IE	INTE1		ATKDT	TKDL	TKCON	TKCON2	RFCON
A0h	P2	PWMCON	P1MODL	P1MODH	P3MODL	P3MODH	TOCON	VCON
98h	SCON	SBUF			PWMPRD	PWMDH		
90h	P1	P0OE		P2OE	OPTION	INTFLG	P1WKUP	SWCMD
88h	TCON	TMOD	TL0	TL1	TH0	TH1		
80h	P0	SP	DPL	DPH				PCON

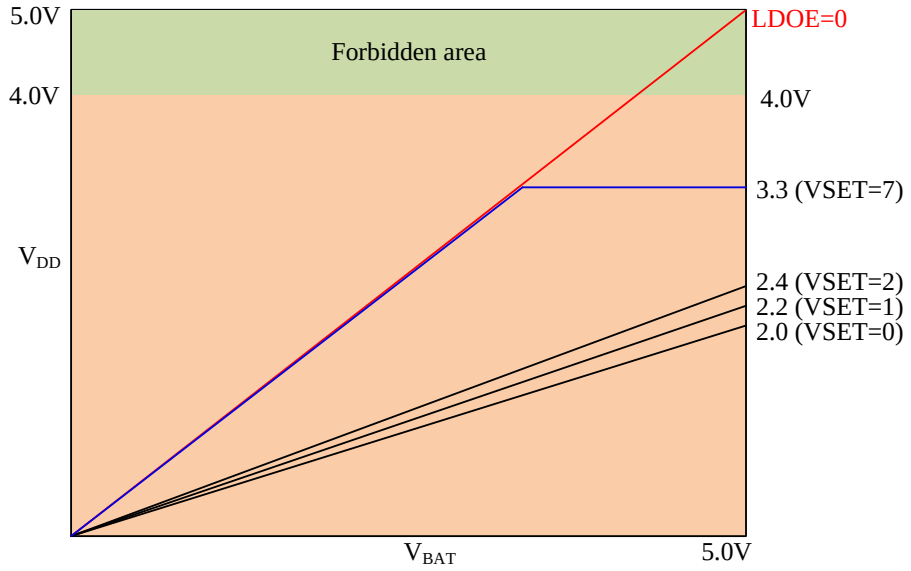
3. Power Management

VBAT pin is the power supply for this chip. It provides voltage source to the built-in tiny current LDO Regulator for chip internal operation. The VDD is the LDO output pin, which needs an external 1uF capacitor connection to VSS for voltage level stability. If LDOE=0, the LDO is disable and the VDD is shorted to VBAT. If LDOE=1, the LDO is enable and the V_{DD} voltage level is defined by VSET1/2 SFR. When VSET1/2=0~6, V_{DD} = V_{BAT}*12/30~V_{BAT}*19/30 and the LDO module only consume 0.3uA. When VSET1/2=7, V_{DD}=V_{BG}*2.75=1.2V*2.75=3.3V and the Bandgap module consumes 15uA. The lower V_{DD} voltage level causes lower chip current consumption, but user must also consider the System clock rate. Higher clock rate requires higher V_{DD} voltage level. User must keep 1.7V<V_{DD}<4.0V for the device's proper operation. In IAP write mode, user also needs to set V_{DD}>2.8V

The 1.2V BandGap Voltage Reference module also support for Low Battery Detection (LBD) and LVR2. The Battery voltage is divided by resistor to certain level then compare to the BandGap voltage. User can refer to the V_{BAT} voltage level for setting the V_{DD} level by VSET1 or VSET2 SFR. The BandGap and Comparator consume un-neglect current, so user should not use them too often. Since V_{BAT} voltage level changes very slowly, user can detect it once an hour or once a day to reduce current consumption.



LDO Regulator & Comparator



VSET	V_{BAT} 3V	V_{BAT} 5V
	V_{DD}	V_{DD}
7	3.00	3.30
6	1.88	3.13
5	1.76	2.94
4	1.65	2.75
3	1.54	2.56
2	1.43	2.38
1	1.31	2.19
0	1.2	2.00

V_{BAT} to V_{DD} selection table

Note: must keep 1.7V < V_{DD} < 4.0V

CMPO	CMPVS															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
4.5V<V_{BAT}	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4.3V<V_{BAT}<4.5V	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
4.1V<V_{BAT}<4.3V	X	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
3.9V<V_{BAT}<4.1V	X	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
3.7V<V_{BAT}<3.9V	X	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
3.5V<V_{BAT}<3.7V	X	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
3.3V<V_{BAT}<3.5V	X	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
3.1V<V_{BAT}<3.3V	X	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
3.0V<V_{BAT}<3.1V	X	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
2.9V<V_{BAT}<3.0V	X	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
2.8V<V_{BAT}<2.9V	X	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
2.7V<V_{BAT}<2.8V	X	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
2.6V<V_{BAT}<2.7V	X	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
2.5V<V_{BAT}<2.6V	X	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.4V<V_{BAT}<2.5V	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
V_{BAT}<2.4V	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Comparator Result vs V_{BAT} voltage level

SFR **A7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCON	–	LDOE	VSET2			VSET1		
R/W	–	R/W	R/W			R/W		
Reset	–	1	1	1	1	1	1	1

A7h.6 **LDOE:** Chip internal LDO Regulator enable control
0: LDO disable, $V_{DD}=V_{BAT}$
1: LDO enable, V_{DD}=LDO Regulator output

A7h.5~3 **VSET2:** V_{DD} voltage setting in Fast/Slow mode while LDOE=1.
0xx: Don't select
100: $V_{DD}=V_{BAT}$*165/300 in Fast/Slow mode
101: $V_{DD}=V_{BAT}$*176/300 in Fast/Slow mode
110: $V_{DD}=V_{BAT}$*188/300 in Fast/Slow mode
111: $V_{DD}=V_{BG}$*2.75=1.2V*2.75=3.3V in Fast/Slow mode while V_{BAT}>3.3V.

A7h.2~0 **VSET1:** V_{DD} voltage setting in Idle/Stop mode while LDOE=1.
0xx: Don't select
100: $V_{DD}=V_{BAT}$*165/300 in Idle/Stop mode
101: $V_{DD}=V_{BAT}$*176/300 in Idle/Stop mode
110: $V_{DD}=V_{BAT}$*188/300 in Idle/Stop mode
111: $V_{DD}=V_{BG}$*2.75=1.2V*2.75=3.3V in Idle/Stop mode while V_{BAT}>3.3V.

Note: If System Clock is FRC/FXT, the VCON setting should follow the rule below:
3V Mode: LDOE=0. ($V_{DD}=V_{BAT}$)
5V Mode: LDOE=1, VSET=7. ($V_{DD}=V_{BAT}$ when V_{BAT}<3.3V, V_{DD}=3.3V when V_{BAT}>3.3V)

Note: must keep 1.7V < V_{DD} < 4.0V

SFR **C2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BGADCS	LVR2E	ADCHS			CMPVS			
R/W	R/W	R/W			R/W			
Reset	0	0	0	0	0	0	0	0

C2h.3~0 **CMPVS:** Select V_{BAT} resistor divider for Comparator input to compare with the 1.2V Bandgap reference voltage. If LVR2E=1, the Low Voltage Reset #2 is triggered when V_{BAT} resistor divider is lower than 1.2V (CMPO=0).

0000: Comparator Disable
0001: the Comparator input is V_{BAT}*12 / 24, LVR2=2.4V
0010: the Comparator input is V_{BAT}*12 / 25, LVR2=2.5V
0011: the Comparator input is V_{BAT}*12 / 26, LVR2=2.6V
0100: the Comparator input is V_{BAT}*12 / 27, LVR2=2.7V
0101: the Comparator input is V_{BAT}*12 / 28, LVR2=2.8V
0110: the Comparator input is V_{BAT}*12 / 29, LVR2=2.9V
0111: the Comparator input is V_{BAT}*12 / 30, LVR2=3.0V
1000: the Comparator input is V_{BAT}*12 / 31, LVR2=3.1V
1001: the Comparator input is V_{BAT}*12 / 33, LVR2=3.3V
1010: the Comparator input is V_{BAT}*12 / 35, LVR2=3.5V
1011: the Comparator input is V_{BAT}*12 / 37, LVR2=3.7V
1100: the Comparator input is V_{BAT}*12 / 39, LVR2=3.9V
1101: the Comparator input is V_{BAT}*12 / 41, LVR2=4.1V
1110: the Comparator input is V_{BAT}*12 / 43, LVR2=4.3V
1111: the Comparator input is V_{BAT}*12 / 45, LVR2=4.5V

SFR **C3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BGADCD	CMPO	–	ADCDT					
R/W	R	–	R					
Reset	–	–	–	–	–	–	–	–

C3h.7 **CMPO:** Compare result of BandGap voltage and V_{BAT} voltage divider. CMPO = 1 means the V_{BAT} divider voltage is higher. If LVR2E = 1, the CMPO = 0 can trigger LVR2.

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	SXTGAIN		STPPCK	PWRFLT	UART1W	WDTPSC	TM3PSC	
R/W	R/W		R/W	R/W	R/W	R/W	R/W	
Reset	1	1	0	0	0	0	0	1

94h.4 **PWRFLT:** Set 1 to enhance the chip's power noise immunity

4. Reset

The **F2230B/34B** has six types of reset methods. The CFGW controls the Reset functionality. The SFRs are returned to their default value after Reset.

4.1 Power on Reset

After Power on Reset, the device stays on Reset state for 20 ms as chip warm up time, then downloads the CFGW register from Flash's last two bytes (Other Reset will not reload the CFGW). The Power on Reset needs both V_{BAT} and V_{DD} voltage first discharge to near V_{SS} level, then rise beyond 1.8V.

4.2 External Pin Reset

External Pin Reset is active low. The RSTn pin needs to keep at least 2 SRC clock cycle long to be sampled by the chip. Pin Reset can be disabled or enabled by CFGW.

4.3 Software Reset

Software Reset is activated by writing the SFR 97h with data 56h.

4.4 Watch Dog Timer Reset

WDT overflow Reset is disabled or enable by CFGW. The WDT uses SYSCLK as its counting time base. It runs in Fast/Slow mode and stops in Idle/Stop mode. WDT overflow speed can be defined by WDTPSC SFR. WDT is cleared by device Reset or CLRWDT SFR bit.

4.5 Low Voltage Reset #1 (LVR1)

LVR1 is disabled or enable by LVR1E in the CFGW. If enable, LVR1 resets the chip when $V_{BAT} < 1.5V$. LVR1 consumes very small current, typically 0.1uA @V_{BAT}=3V. It is designed to prevent the chip's abnormal function during power on-off.

4.6 Low Voltage Reset #2 (LVR2)

LVR2 is disabled or enable by LVR2E SFR bit. LVR2 is generated by the Bandgap Comparator module. When the V_{BAT} resister divider voltage is lower than the 1.2V Bandgap reference voltage (CMPO=0), the LVR2 occurs. F/W must setup the CMPVS SFR before set LVR2E=1 to prevent the LVR2 triggered during Bandgap unstable. LVR2's trigger level can be selected as V_{BAT}=2.4V~4.5V by the CMPVS SFR. Enable the LVR2 function consumes 15uA @V_{BAT}=3V.

Note: LVR1 must be enable, also refer to AP-TM52XXXXX_02S for LVR1/LVR2 setting information

System Clock frequency	8 MHz	6 MHz	4 MHz	2 MHz	1 MHz
Minimum LVR1 / 2 level	LVR2=2.9V LVR1=1.5V	LVR2=2.6V LVR1=1.5V	LVR2=2.4V LVR1=1.5V	LVR2=2.4V LVR1=1.5V	LVR1=1.5V

LVR1/2 setting table

Flash **7FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	MVCLOCK	WDTE	–	–	LVR1E	–

7FFFh.6 **XRSTE:** Pin Reset enable, 1=enable.

7FFFh.4 **WDTE:** WDT Reset enable, 1=enable.

7FFFh.1 **LVR1E:** Low Voltage Reset #1 enable, 1=enable.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL / SWRST							
R/W	W							R/W
Reset	–							0

97h.7~0 **SWRST (W) :** Write 56h to generate S/W Reset.

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	–	–	–	TKSOC	CLRWDT	CLRTM3	STPRFC	DPSEL
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

F8h.3 **CLRWDT:** Set to 1 to clear Watch Dog Timer.

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	SXTGAIN		STPPCK	PWRFLT	UART1W	WDTPSC	TM3PSC	
R/W	R/W		R/W	R/W	R/W	R/W	R/W	
Reset	1	1	0	0	0	0	0	1

94h.2 **WDTPSC:** WDT prescaler.
0: WDT overflow at 65536 System clock count
1: WDT overflow at 32768 System clock count

SFR **C2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BGADCS	LVR2E	ADCHS			CMPVS			
R/W	R/W	R/W			R/W			
Reset	0	0	0	0	0	0	0	0

C2h.7 **LVR2E:** Low Voltage Reset #2 enable, 1=enable. This bit must be set to 1 after CMPVS setting done and the Bandgap voltage stable.

C2h.3~0 **CMPVS:** Select V_{BAT} resistor divider for Comparator input to compare with the 1.2V Bandgap reference voltage. If LVR2E=1, the Low Voltage Reset #2 is triggered when V_{BAT} resistor divider is lower than 1.2V (CMPO=0).

0000: Comparator Disable
0001: the Comparator input is V_{BAT}*12/24, LVR2=2.4V
0010: the Comparator input is V_{BAT}*12/25, LVR2=2.5V
0011: the Comparator input is V_{BAT}*12/26, LVR2=2.6V
0100: the Comparator input is V_{BAT}*12/27, LVR2=2.7V
0101: the Comparator input is V_{BAT}*12/28, LVR2=2.8V
0110: the Comparator input is V_{BAT}*12/29, LVR2=2.9V
0111: the Comparator input is V_{BAT}*12/30, LVR2=3.0V
1000: the Comparator input is V_{BAT}*12/31, LVR2=3.1V
1001: the Comparator input is V_{BAT}*12/33, LVR2=3.3V
1010: the Comparator input is V_{BAT}*12/35, LVR2=3.5V
1011: the Comparator input is V_{BAT}*12/37, LVR2=3.7V
1100: the Comparator input is V_{BAT}*12/39, LVR2=3.9V
1101: the Comparator input is V_{BAT}*12/41, LVR2=4.1V
1110: the Comparator input is V_{BAT}*12/43, LVR2=4.3V
1111: the Comparator input is V_{BAT}*12/45, LVR2=4.5V

SFR **C3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BGADCD	CMPO	–	ADCDT					
R/W	R	–	R					
Reset	–	–	–	–	–	–	–	–

C3h.7 **CMPO:** Compare result of BandGap voltage and V_{BAT} voltage divider. CMPO=1 means the V_{BAT} divider voltage is higher. If LVR2E=1, the CMPO=0 can trigger LVR2.

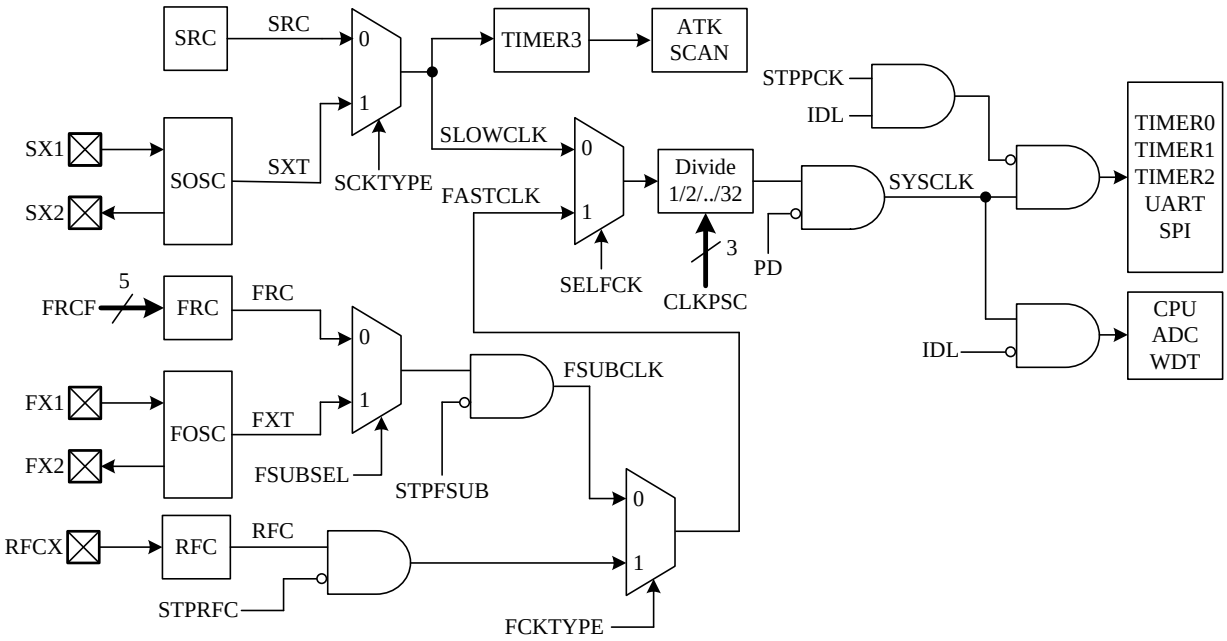
5. Clock Circuitry & Operation Mode

5.1 System Clock

The **F2230B/34B** is designed with dual-clock system. During runtime, user can directly switch the System clock from fast to slow or from slow to fast. It also can directly select a clock divider of 1, 2, 4, 8, 16 or 32. The Fast clock consists of **FRC** (Fast Internal RC, 7.3728 MHz), **FXT** (1~8 MHz) and **RFC**. The Slow clock can be selected as **SXT** (Slow Crystal, 32 KHz) or **SRC** (80 KHz @V_{DD}=3V, 40 KHz @V_{DD}=1.5V). Fast mode and Slow mode are defined as the CPU running at Fast and Slow clock speeds.

After Reset, the chip is running at Slow mode with SRC clock. Since Fast clock is useless in Slow mode, S/W can set STPFSUB=1 to stop FXT or FRC to reduce device's current consumption. Before the device switches to other clock rate, S/W must also consider the V_{DD} voltage level for device operation safety. The higher V_{DD} allows the device to run at higher System clock frequency. In typical condition, 7.3728 MHz System clock rate requires V_{DD} >2.8V.

Before entering the Fast mode, S/W must select the Fast clock type in advance. If RFC is used as the Fast clock source, S/W also has to setup the pin mode and RFC related SFRs in advance. The FRC is the default Fast clock type. Its frequency is controlled by FRCF SFR, which is automatically loaded with CFGW data at power on reset. The FRC is trimmed to 7.3728 MHz in chip manufacturing.



Clock Structure

The CLKCON SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow clock type in Fast mode, and change the Fast clock type in Slow mode. Never to write both STPFSUB=1 & SELFCK=1 in FXT/FRC mode. It is recommended to write this register bit by bit.

This chip can also output the System clock to TCO pin (in CMOS format). TCO's frequency/duty is defined by TCOCON SFR. TCO pin's output enable is defined by P3MOD7 SFR (***see section 7***).

Flash **7FFEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	–	–	FRCF				

FFEh.4~0 **FRCF:** FRC frequency adjustment.
FRC is trimmed to 7.3728 MHz in chip manufacturing. FRCF records the adjustment data.

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	–	–	FRCF				
R/W	–	–	–	R/W				
Reset	–	–	–	–	–	–	–	–

F7h.4~0 **FRCF:** FRC frequency adjustment. It is automatically loaded with Flash's 7FFEh data at power on reset and can be read/written as any other SFR register in normal mode. So the FRC clock speed can be changed on CPU run time by S/W.
00h=central frequency, 0Fh=highest frequency, 10h=lowest frequency.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	FCKTYPE	FSUBSEL	SELFCK	SCKTYPE	STPFSUB	CLKPSC		
R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	1	0	1

D8h.7 **FCKTYPE:** Fast clock type select, This bit can be changed only in Slow mode (SELFCK=0)
0: Fast clock is FSUBCLK (FRC or FXT)
1: Fast clock is RFC, S/W must setup RFC oscillating circuitry before set this bit to 1.

D8h.6 **FSUBSEL:** FSUBCLK select, This bit can be changed only in Slow mode (SELFCK=0).
0: FSUBCLK is FRC
1: FSUBCLK is FXT, P2.2 and P2.3 are crystal oscillator pins

D8h.5 **SELFCK:** System clock select. This bit can be changed only when STPFSUB=0 or FCKTYPE=1.
0: Slow clock (SRC/SXT)
1: Fast clock (FRC/FXT/RFC)

D8h.4 **SCKTYPE:** Slow clock Type. This bit can be changed only in Fast mode (SELFC =1).
0: SRC
1: SXT, P2.0 and P2.1 are crystal oscillator pins

D8h.3 **STPFSUB:** Set 1 to stop FXT/FRC for power saving in Slow/Idle mode. This bit can be changed only in Slow mode or RFC mode.

D8h.2~0 **CLKPSC:** System clock prescaler. max effective delay is 32 cycle, Refer AP-TM52XXXXX_01S.
000: System clock is Fast/Slow clock divided by 32
001: System clock is Fast/Slow clock divided by 16
010: System clock is Fast/Slow clock divided by 8
011: System clock is Fast/Slow clock divided by 4
100: System clock is Fast/Slow clock divided by 2
101: System clock is Fast/Slow clock divided by 1

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	SXTGAIN		STPPCK	PWRFLT	UART1W	WDTPSC	TM3PSC	
R/W	R/W		R/W	R/W	R/W	R/W	R/W	
Reset	1	1	0	0	0	0	0	1

94h.7~6 **SXTGAIN:** 32768 SXT oscillator gain, 3=Highest gain, 0=Lowest gain. Higher gain can shorten the Crystal oscillation warm-up time. Lower gain can reduce oscillation current.

94h.5 **STPPCK:** Set 1 to stop UART/Timer0/Timer1/Timer2 clock in Idle mode for current reducing.

Note: In crystal mode, user should set the P2.2/P2.3 (FXT) or P2.0/P2.1 (SXT) pins as Input with Pull-up (section7).

SYSCLK	CLKCON (D8h)				
	bit7 FCKTYPE	bit6 FSUBSEL	bit5 SELFCK	bit4 SCKTYPE	bit3 STPFSUB
Fast RFC (*1)	1	0/1	1	0/1	0/1
Fast FXT	0	1	1	0/1	0
Fast FRC	0	0	1	0/1	0
Slow SXT	0/1	0/1	0	1	0/1
Slow SRC	0/1	0/1	0	0	0/1
Fast type change	0 ← → 1	0 ← → 1	0	0/1	0/1
Slow type change	0/1	0/1	1	0 ← → 1	0/1(*2)
Stop FRC / FXT	0	0/1	0	0/1	0 → 1
Stop FRC / FXT	1	0/1	0/1	0/1	0 → 1
Switch to FRC/FXT	0	0/1	0 → 1	0/1	0
Switch to RFC (*1)	1	0/1	0 → 1	0/1	0/1
Switch to SRC / SXT	0	0/1	1 → 0	0/1	0
Switch to SRC / SXT	1	0/1	1 → 0	0/1	0/1

(*1) also need RFC related SFRs proper setting

(*2) STPFSUB=1 is only valid for RFC Mode, FRC/FXT Mode needs STPFSUB=0

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TOCON	T1OCON		T2OCON			TCOCON		
R/W	R/W		R/W			R/W		
Reset	0	0	0	0	0	0	0	0

A6h.2~0 **TCOCON:** TCO pin duty and frequency control

000: 1/2 duty, 1/2 SYSCLK frequency

001: 1/3 duty, 1/3 SYSCLK frequency

010: 1/4 duty, 1/4 SYSCLK frequency

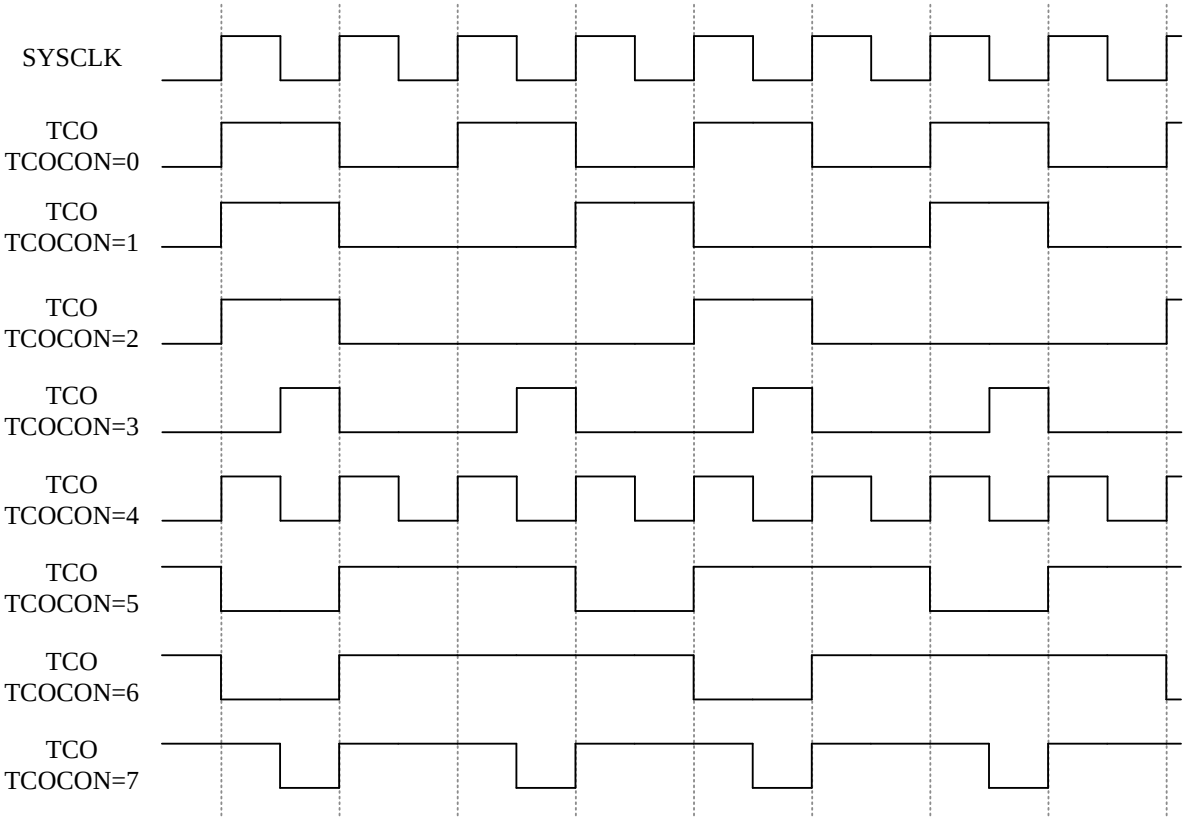
011: 1/4 duty, 1/2 SYSCLK frequency

100: 1/2 duty, 1/1 SYSCLK frequency

101: 2/3 duty, 1/3 SYSCLK frequency

110: 3/4 duty, 1/4 SYSCLK frequency

111: 3/4 duty, 1/2 SYSCLK frequency



TCO waveform with TCOCON

5.2 Operation Modes

There are four operation modes for this device. **Fast Mode** is defined as the CPU running at Fast clock speed. **Slow Mode** is defined as the CPU running at Slow clock speed. When the System clock speed is lower, the power consumption is lower.

Idle Mode is entered by setting the IDL bit in PCON SFR. Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The STPPCK bit can be set to furthermore reduce Idle mode current. If STPPCK=1, Timer0/1/2 and UART are stopped in Idle mode. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Stop Mode is entered by setting the PD bit in PCON SFR. This mode is the so-called "Power Down" mode in standard 8051. In Stop mode, all clocks stop. Stop Mode can be terminated by Reset or pin wake up.

Note: Chip cannot enter Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and Exn=1, n=0,1,2)

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter STOP mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter IDLE mode.

6. Interrupt & Wake-up

The **F2230B/34B** has an 11-source four-level priority interrupt structure. All enabled Interrupts can wake up CPU from Idle mode, but only the Pin Interrupts can wake up CPU from Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter whether its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	Flag	Description
0003	IE0	INT0 external pin Interrupt (can wake up Stop mode)
000B	TF0	Timer0 Interrupt
0013	IE1	INT1 external pin Interrupt (can wake up Stop mode)
001B	TF1	Timer1 Interrupt
0023	RI+TI	Serial Port (UART) Interrupt
002B	TF2+EXF2	Timer2 Interrupt
0033		Reserved for ICE mode use
003B	TF3	Timer3 Interrupt
0043	P1IF	Port1 external pin change Interrupt (can wake up Stop mode)
004B	IE2	INT2 external pin Interrupt (can wake up Stop mode)
0053	TKIF	Touch Key Interrupt (F2230B only)
005B	SPIF+WCOL	SPI Interrupt

Interrupt Vector & Flag

6.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The P1WKUP SFR controls the individual Port1 pin's wake-up and interrupt capability. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

SFR **96h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1WKUP	P1WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

96h.7~0 **P1WKUP:** P1.7~P1.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable control.
0: Disable all Interrupts.
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.5 **ET2:** Timer2 interrupt enable
0: Disable Timer2 interrupt
1: Enable Timer2 interrupt

A8h.4 **ES:** Serial Port (UART) interrupt enable
0: Disable Serial Port (UART) interrupt
1: Enable Serial Port (UART) interrupt

A8h.3 **ET1:** Timer1 interrupt enable
0: Disable Timer1 interrupt
1: Enable Timer1 interrupt

A8h.2 **EX1:** External INT1 pin Interrupt enable and Stop mode wake up enable
0: Disable INT1 pin Interrupt and Stop mode wake up
1: Enable INT1 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A8h.1 **ET0:** Timer0 interrupt enable
0: Disable Timer0 interrupt
1: Enable Timer0 interrupt

A8h.0 **EX0:** External INT0 pin Interrupt enable and Stop mode wake up enable
0: Disable INT0 pin Interrupt and Stop mode wake up
1: Enable INT0 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	IAPWE			SPIE	TKIE	EX2	P1IE	TM3IE
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.4 **SPIE:** SPI interrupt enable
0: Disable SPI interrupt
1: Enable SPI interrupt

A9h.3 **TKIE:** Touch Key (F2230B only) interrupt enable
0: Disable Touch Key interrupt
1: Enable Touch Key interrupt

A9h.2 **EX2:** External INT2 pin Interrupt enable and Stop mode wake up enable
0: Disable INT2 pin Interrupt and Stop mode wake up
1: Enable INT2 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A9h.1 **P1IE:** Port1 pin change interrupt enable. This bit does not affect the Port1 pin's Stop mode wake up capability.
0: Disable Port1 pin change interrupt
1: Enable Port1 pin change interrupt

A9h.0 **TM3IE:** Timer3 interrupt enable
0: Disable Timer3 interrupt
1: Enable Timer3 interrupt

SFR **B9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

SFR **B8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

B9h.5, B8h.5 **PT2H, PT2:** Timer2 Interrupt Priority control. (PT2H, PT2) =
11: Level 3 (highest priority)
10: Level 2
01: Level 1
00: Level 0 (lowest priority)

B9h.4, B8h.4 **PSH, PS:** Serial Port (UART) Interrupt Priority control. Definition as above.

B9h.3, B8h.3 **PT1H, PT1:** Timer1 Interrupt Priority control. Definition as above.

B9h.2, B8h.2 **PX1H, PX1:** External INT1 pin Interrupt Priority control. Definition as above.

B9h.1, B8h.1 **PT0H, PT0:** Timer0 Interrupt Priority control. Definition as above.

B9h.0, B8h.0 **PX0H, PX0:** External INT0 pin Interrupt Priority control. Definition as above.

SFR **BBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	–	–	–	PSPIH	PTKIH	PX2H	PP1H	PT3H
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

SFR **BAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	–	–	–	PSPI	PTKI	PX2	PP1	PT3
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

BBh.4, BAh.4 **PSPIH, PSPI:** SPI Interrupt Priority control. Definition as above.

BBh.3, BAh.3 **PTKIH, PTKI:** Touch Key Interrupt Priority control. Definition as above. (F2230B only)

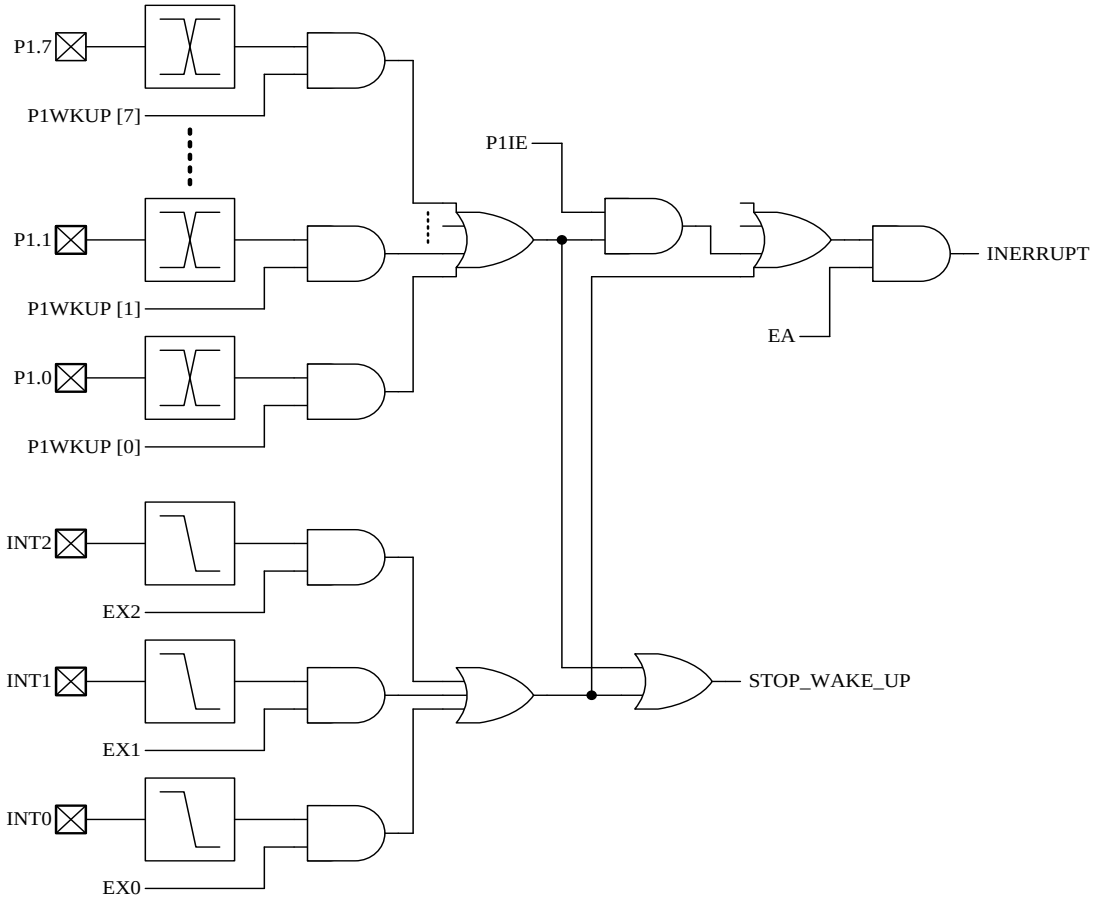
BBh.2, BAh.2 **PX2H, PX2:** External INT2 pin Interrupt Priority control. Definition as above.

BBh.1, BAh.1 **PP1H, PP1:** Port1 Pin Change Interrupt Priority control. Definition as above.

BBh.0, BAh.0 **PT3H, PT3:** Timer3 Interrupt Priority control. Definition as above.

6.2 Pin Interrupt

Pin Interrupts include INT0 (P3.2), INT1 (P3.3), INT2 (P2.7) and Port1 Change Interrupt. These pins also have the Stop mode wake up capability. INT0 and INT1 are falling edge or low level triggered as the 8051 standard. INT2 is falling edge triggered and Port1 Change Interrupt is triggered by any Port1 pin state change.



Pin Interrupt & Wake up

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag.
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin

88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	–	TKIF	IE2	P1IF	TF3
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

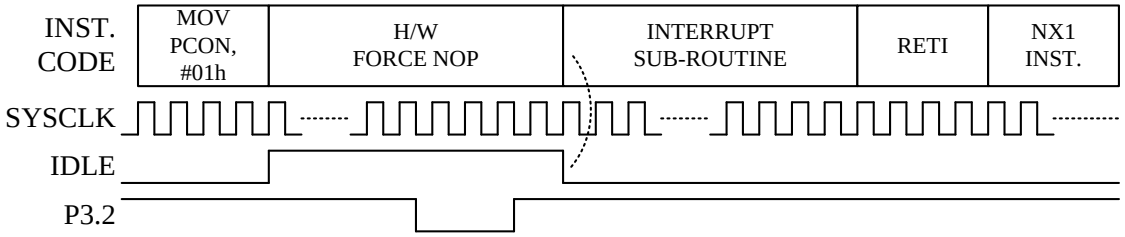
95h.2 **IE2:** External Interrupt 2 (INT2 pin) edge flag
Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FBh to INTFLG to clear this bit.

95h.1 **P1IF:** Port1 pin change interrupt flag
Set by H/W when a Port1 pin state change is detected and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FDh to INTFLG to clear this bit.

Note2: S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.

6.3 Idle mode Wake up and Interrupt

Idle mode is waked up by enabled Interrupts, which means individual interrupt enable bit (ex: EX0) and EA bit must be both set to 1 to establish Idle mode wake up capability. All enabled Interrupts (Pins, Timers, TK, SPI and UART) can wake up CPU from Idle mode. Upon Idle wake-up, Interrupt service routine is entered immediately. "The first instruction behind IDL (PCON.0) setting" is executed after interrupt service routine return.



EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

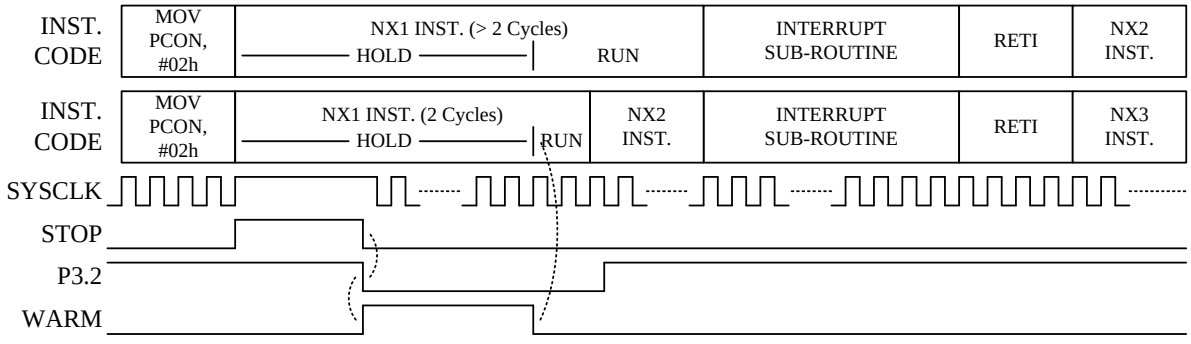
SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter STOP mode.
87h.0 **IDL:** Idle mode control bit, set 1 to enter IDLE mode.

6.4 Stop mode Wake up and Interrupt

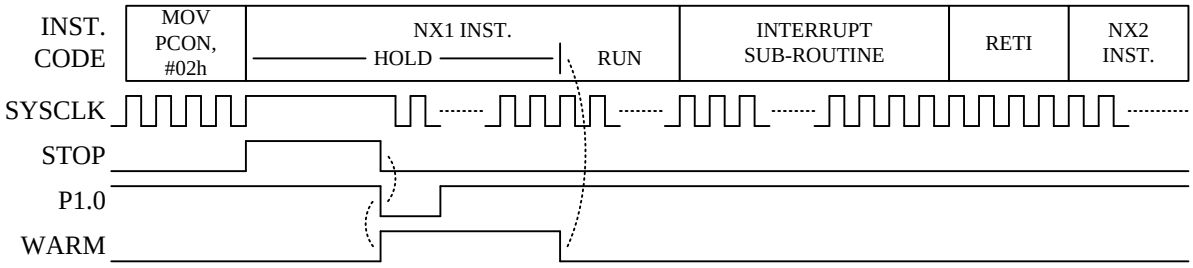
Stop mode wake up is simple, as long as the individual pin interrupt enable bit (ex: EX0) is set, the pin wake up capability is asserted. Set EX0/EX1/EX2 can enable INT0/INT1/INT2 pins' Stop mode wake up capability. Set P1WKUP bit 7~0 can enable P1.7~P1.0's Stop mode wake up capability. Upon Stop wake up, "the first instruction behind PD setting (PCON.1)" is executed immediately before Interrupt service. Interrupt entry requires EA=1 (P1WKUP also needs P1IE=1) and trigger state of the pin staying sufficiently long to be observed by the System clock. This feature allows CPU to enter or not enter Interrupt sub-routine after Stop mode wake up.

Note: Chip cannot enter Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and Exn=1, n=0,1,2)
Note: It is recommended to place the NX1/NX2 with NOP Instruction in figures below.



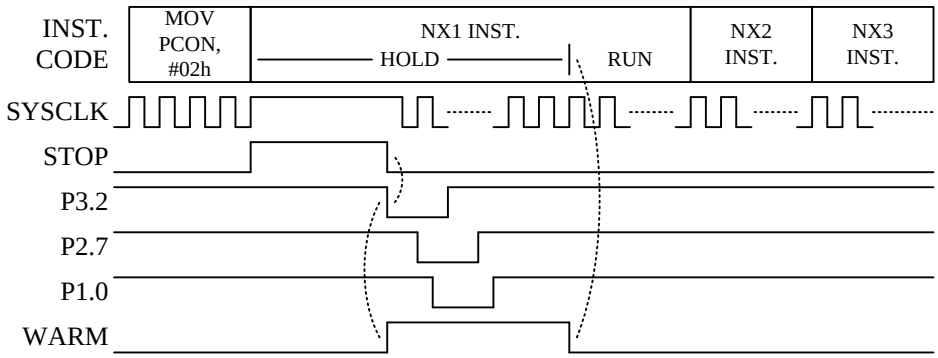
EA=EX0=1

P3.2 (INT0) is sampled after warm-up, Stop mode wake-up and Interrupt



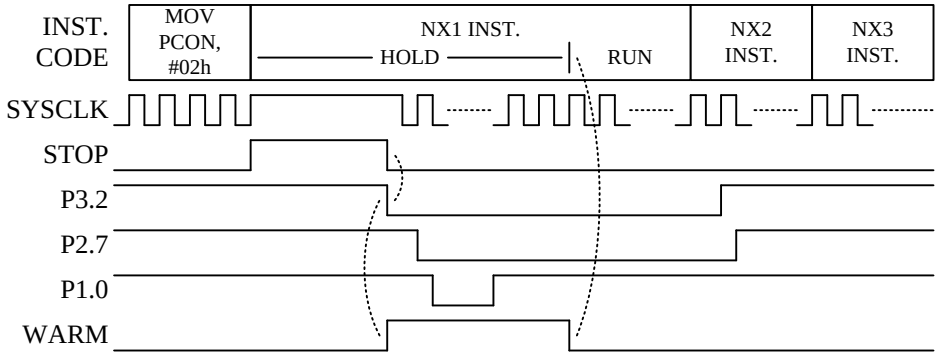
EA=P1IE=P1WKUP=1

P1.0 change (not need clock sample), Stop mode wake-up and Interrupt



EA=EX0=EX2=P1WKUP=1, P1IE=0

Stop mode wake-up but not Interrupt, P3.2/P2.7 pulse too narrow



EX0=EX2=P1WKUP=P1IE=1, EA=0

Stop mode wake-up but not Interrupt

7. I/O Ports

The **F2230B/34B** has total 32 multi-function I/O pins. All I/O pins follow the standard 8051 "Read-Modify-Write" feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR. (ex: ANL P1, A; INC P2; CPL P3.0)

7.1 Port1 & Port3

These pins can operate in four different modes as below.

Mode	Port1, Port3 pin function		P1.n / P3.n SFR data	Pin State	Resistor Pull-up	Digital Input
	P3.0~P3.2	Others				
Mode 0	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Pull-up	Y	Y
Mode 1	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Hi-Z	N	Y
Mode 2	CMOS Output		0	Drive Low	N	N
			1	Drive High	N	N
Mode 3	Alternative Function, such as ADC and Clock output		X (don't care)	–	N	N

Port1, Port3 I/O Pin Function Table

If a Port1 or Port3 pin is used for Schmitt-trigger input, S/W must set the I/O pin to Mode0 or Mode1 and set the corresponding Port Data SFR to 1 to disable the pin's output driving circuitry.

Beside I/O port function, each Port1 and Port3 pin has one or more alternative functions, such as Touch Key, ADC, I80 and Clock output. Most of the functions are activated by setting the individual pin mode control SFR to Mode3. Port1/Port3 pins also have standard 8051 auxiliary definition such as INT0/1, T0/1/2, or RXD/TXD. These pin functions need to set the pin mode SFR to Mode0 or Mode1 and keep the P1.n/P3.n SFR at 1.

Pin Name	8051	Wake-up	CKO	ADC	TK	I80	PWM	Mode3
P1.0	T2	Y	T2O		TK7			T2O
P1.1	T2EX	Y		ADC1	TK6			ADC1
P1.2		Y		ADC2	TK5			ADC2
P1.3		Y		ADC3	TK4		PWM	ADC3
P1.4		Y		ADC4	TK3			ADC4
P1.5		Y		ADC5	TK2			ADC5
P1.6		Y		ADC6	TK1			ADC6
P1.7		Y		ADC7	TK0			ADC7
P3.0	RXD				TK14			
P3.1	TXD				TK13			
P3.2	INT0	Y			TK12			
P3.3	INT1	Y			TK11			
P3.4	T0				CLD			CLD
P3.5	T1		T1O		TK10			T1O
P3.6			T1B		TK9	WR		T1B
P3.7			TCO		TK8	RD		TCO

Port1, Port3 multi-function Table

The necessary SFR setting for Port1/Port3 pin's alternative functions is list below.

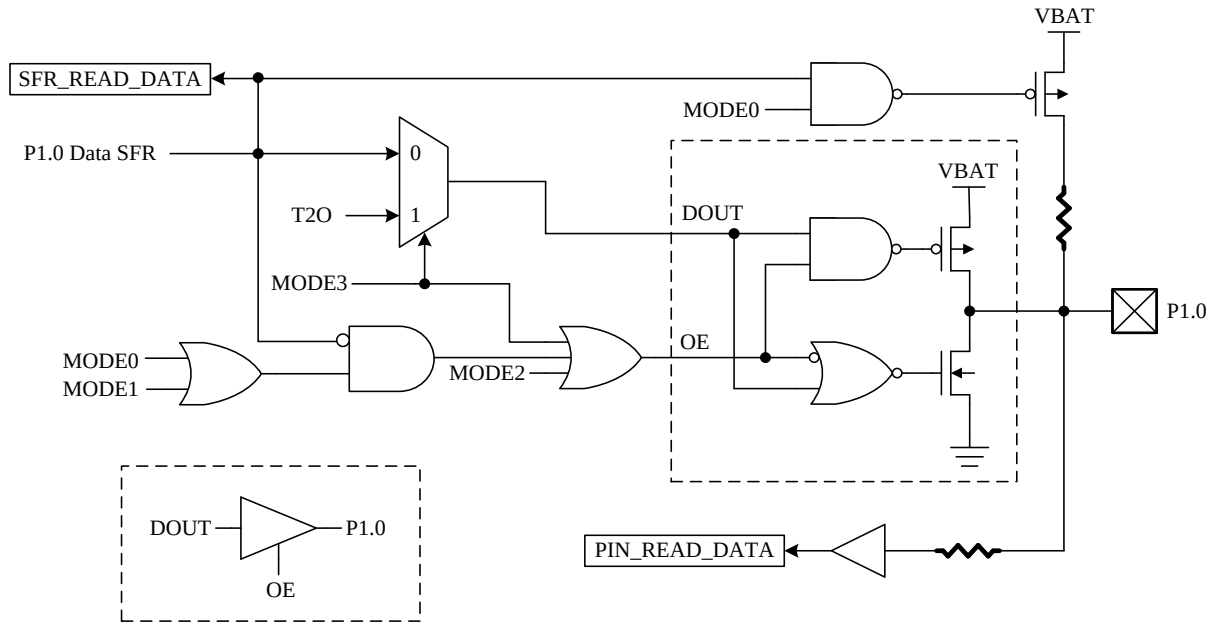
Alternative Function	Mode	Px.n SFR data	Pin State	Other necessary SFR setting
T0, T1, T2, T2EX, INT0, INT1	**0**	1	Input with Pull-up	
	1	1	Input	
RXD, TXD	**0**	1	Input with Pull-up/Pseudo Open Drain Output	
	1	1	Input/Pseudo Open Drain Output	
TCO, T1O, T1B, T2O	**3**	X	Clock Output (CMOS Push-Pull)	
RD, WR	**2**	X	I80 interface read/write enable	PINMODE
TK0~TK14	**0**	1	Touch Key Idling or Scanning	
CLD	**3**	X	Touch Key charge collection	
PWM	**0**	X	PWM Open Drain Output with Pull-up	PINMODE
	1	X	PWM Open Drain Output	
	2	X	PWM Output (CMOS Push-Pull)	
ADC1~ADC7	**3**	X	ADC analog Input	

Mode Setting for Port1, Port3 Alternative Function

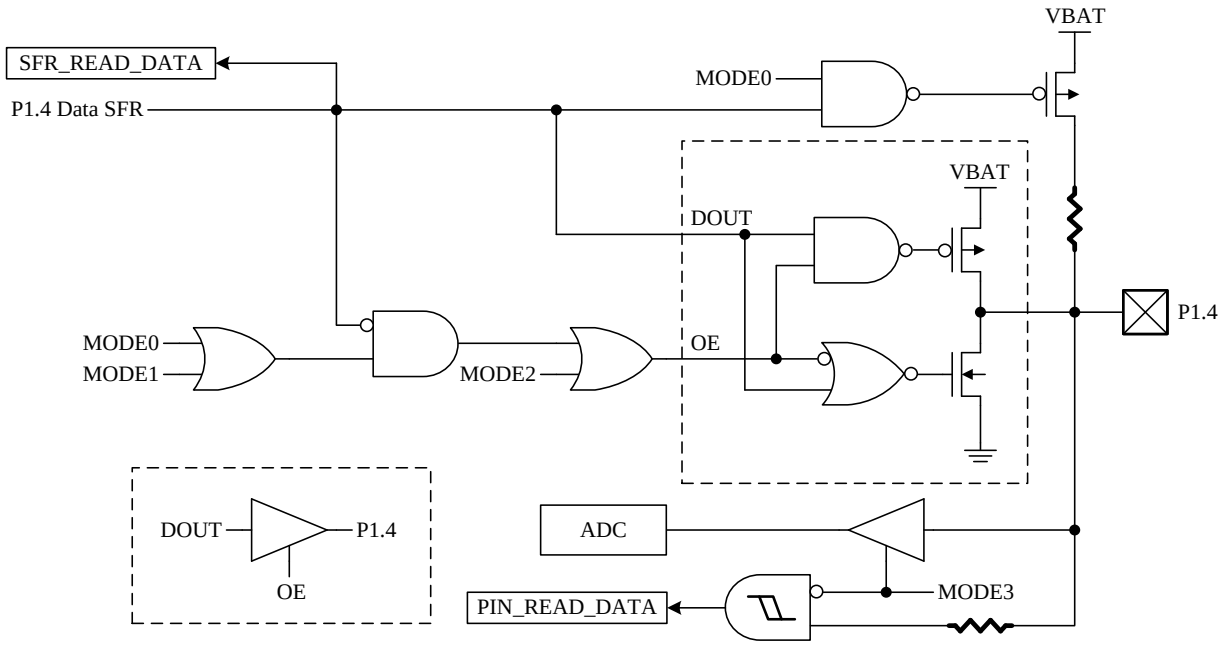
For tables above, a "**CMOS Output**" pin means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.

An "**Open Drain**" pin means it can sink at least 4mA current but only drive a small current (<20uA). It can be used as input or output function and typically needs an external pull up resistor.

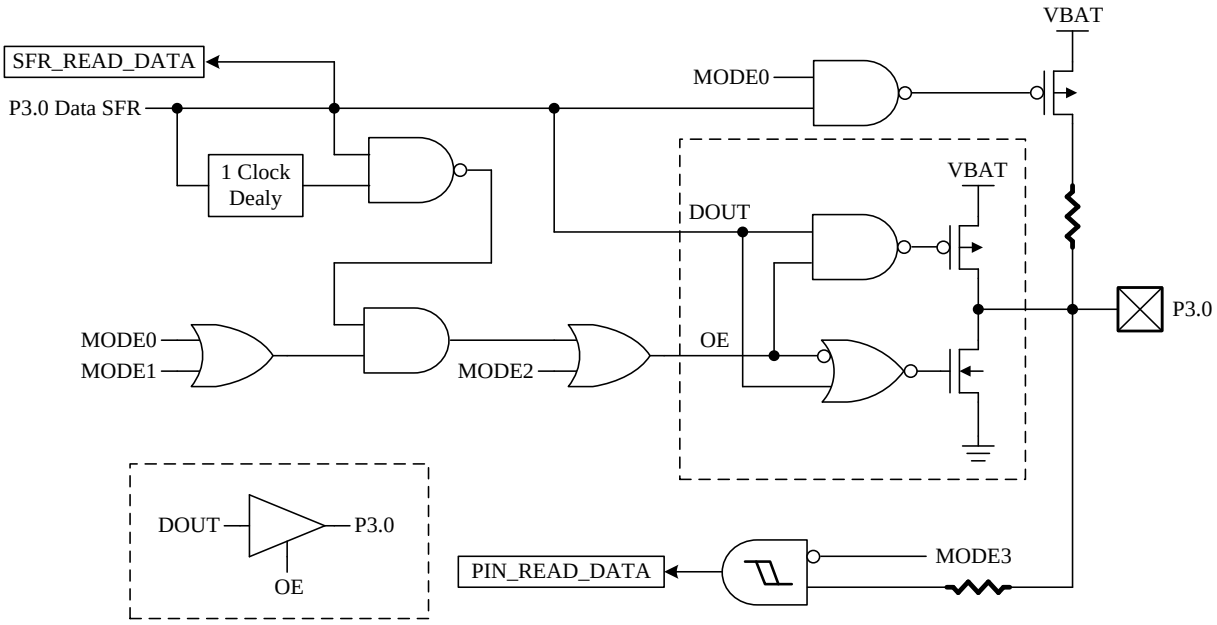
An 8051 standard pin is a "**Pseudo Open Drain**" pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 1~2 clock cycle when output transits from low to high, then keeps driving a small current (<20uA) to maintain the pin at high level. It can be used as input or output function.



P1.0 Pin Structure



P1.4 Pin Structure



P3.0 Pin Structure

SFR **90h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

90h.7~0 **P1:** Port1 data

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.7~0 **P3:** Port3 data

SFR **A2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A2h.7~6 **P1MOD3:** P1.3 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.3 is ADC input.

A2h.5~4 **P1MOD2:** P1.2 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.2 is ADC input.

A2h.3~2 **P1MOD1:** P1.1 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.1 is ADC input.

A2h.1~0 **P1MOD0:** P1.0 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.0 is “Timer2 overflow divided by 2/3/4” (T2O) CMOS push pull output.

SFR **A3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A3h.7~6 **P1MOD7:** P1.7 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.7 is ADC input.

A3h.5~4 **P1MOD6:** P1.6 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.6 is ADC input.

A3h.3~2 **P1MOD5:** P1.5 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.5 is ADC input.

A3h.1~0 **P1MOD4:** P1.4 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.4 is ADC input.

SFR **A4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A4h.7~6 **P3MOD3:** P3.3 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A4h.5~4 **P3MOD2:** P3.2 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A4h.3~2 **P3MOD1:** P3.1 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A4h.1~0 **P3MOD0:** P3.0 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A5h.7~6 **P3MOD7:** P3.7 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.7 is “SYSCLK divided by 1/2/3/4” (TCO) CMOS push pull output.

A5h.5~4 **P3MOD6:** P3.6 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.6 is “Negative Timer1 overflow divided by 2/3/4” (T1B) CMOS push pull output.

A5h.3~2 **P3MOD5:** P3.5 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.5 is “Positive Timer1 overflow divided by 2/3/4” (T1O) CMOS push pull output.

A5h.1~0 **P3MOD4:** P3.4 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.4 is Touch Key charge collection (CLD).

7.2 P2.7

P2.7 can be only used as Schmitt-trigger input or open-drain output, with pull-up resistor always enable. P2.7 pin is shared with RSTn, INT2 and Flash VPP function.

7.3 P2.6~P2.0 & Port0

These pins are shared with RFC, SPI, I80 and crystal oscillator. If a Port0/2 pin is defined as I/O pin, it can be used as CMOS push-pull output or Schmitt-trigger input. The pin's pull up function is enable while SFR bit PxOE.n=0 and Px.n=1.

P2.6~P2.0/Port0 pin function	P2OE.n/ P0OE.n	P2.n/P0.n SFR data	Pin State	Resistor Pull-up	Digital Input
Input	0	0	Hi-Z	N	Y
	0	1	Pull-up	Y	Y
CMOS Output	1	0	Drive Low	N	N
	1	1	Drive High	N	N

P2.6~P2.0 & Port0 I/O Pin Function Table

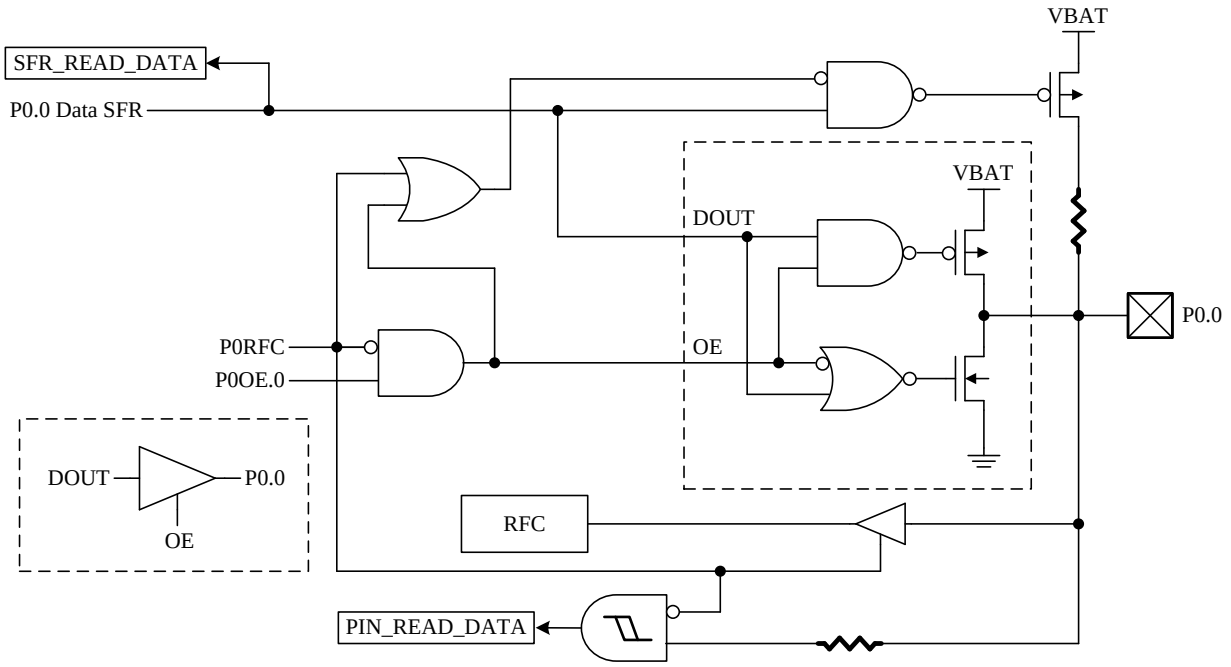
Pin Name	Wake-up	RFC	SPI	SXT/FXT	I80	Others
P0.0		RFCX			D0	
P0.1		RFC0R			D1	
P0.2		RFC1R			D2	
P0.3		RFC2R			D3	
P0.4					D4	
P0.5					D5	
P0.6					D6	
P0.7					D7	
P2.0				SX1		
P2.1				SX2		
P2.2				FX1		
P2.3				FX2		
P2.4			MOSI			
P2.5			SCK			
P2.6			MISO			
P2.7	Y					INT2, RSTn, VPP

Port0, Port2 multi-function Table

The necessary SFR setting for Port0/Port2 pin's alternative functions is list below.

Alternative Function	P2OE.n/ P0OE.n	P2.n/P0.n SFR data	Pin State	other necessary SFR setting
RFCX, RFC0R~RFC2R	0	X	RFC clock oscillation	RFCON
MOSI, SCK, MISO	0	0	SPI communication	SPCON
SX1, SX2, FX1, FX2	0	1	Crystal oscillation	CLKCON
D0~D7	0	0	I80 interface data bus without Pull up	PINMODE
	0	1	I80 interface data bus with Pull-up	

Mode Setting for Port0, Port2 Alternative Function



P0.0 Pin Structure

SFR **80h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

80h.7~0 **P0:** Port0 data, also controls the P0.n pin's pull-up function. If the P0.n SFR data is "1" and the corresponding P0OE.n= 0 (input mode), the pull-up is enabled.

SFR **A0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.7 **P2.7:** P2.7 data, 0=Open Drain output low, 1=Schmitt-trigger input with pull up

A0h.6~0 **P2.6~P2.0:** P2.6~P2.0 data, also controls the P2.n pin's pull-up function. If the P2.n SFR data is "1" and the corresponding P2OE.n=0 (input mode), the pull-up is enabled.

SFR **91h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0OE	P0OE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

91h.7~0 **P0OE:** Port0 CMOS Push-Pull output enable control, 1=Enable.

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2OE	–	P2OE						
R/W	–	R/W						
Reset	–	0	0	0	0	0	0	0

93h.6~0 **P2OE:** P2.6~P2.0 pin CMOS Push-Pull output enable control, 1=Enable.

SFR **BCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCON	SPEN	MSTR	CPOL	CPHA	–	LSBF	SPCR	
R/W	R/W	R/W	R/W	R/W	–	R/W	R/W	
Reset	0	0	0	0	–	0	0	0

BCh.7 **SPEN:** SPI Enable.
0: SPI Disable
1: SPI Enable, P2.4~P2.6 are SPI functional pins.

SFR **AFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCON	P0RFC		T0SEL		RFCPSC		RFCS	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	1	1	0	0

AFh.7~6 **P0RFC:** P0.0~P0.3 pin RFC mode control.
00: P0.0~P0.3 are not RFC pins
01: P0.0 and P0.1 are RFC pins, P0.2 and P0.3 are not RFC pins
10: P0.0~P0.2 are RFC pins, P0.3 is not RFC pin
11: P0.0~P0.3 are RFC pins

SFR **BFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMODE	I80EN	I80POL	PWMOE	–	–	–	–	–
R/W	R/W	R/W	R/W	–	–	–	–	–
Reset	0	0	0	–	–	–	–	–

BFh.7 **I80EN:** I80 interface enable.
0: Disable
1: Enable, Port0, P3.6 and P3.7 are I80 functional pin

BFh.6 **I80POL:** The polarity of RD/WR signal
0: RD/WR are low active
1: RD/WR are high active

BFh.5 **PWMOE:** PWM signal output enable
0: Disable PWM signal output to P1.3
1: Enable PWM signal output to P1.3

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	FCKTYPE	FSUBSEL	SELFCK	SCKTYPE	STPFSUB	CLKPSC		
R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	1	0	1

D8h.6 **FSUBSEL:** Set 1 to enable P2.2 and P2.3 pin's FXT oscillation mode

D8h.4 **SCKTYPE:** Set 1 to enable P2.0 and P2.1 pin's SXT oscillation mode

Note: In crystal mode, user should set the P2.2/P2.3 (FXT) or P2.0/P2.1 (SXT) pins as Input with Pull-up.

8. Timers

Timer0, Timer1 and Timer2 are provided as standard 8051 compatible timer/counter. Timer3 is provided for a real-time clock count. Compare to the traditional 12T 8051, the chip's Timer0/1/2 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every "2 System clock" rate; in counter mode, T0/T1/T2 pin input pulse must be wider than 2 System clock to be seen by this device. In addition to the standard 8051 timers function, the T1O and T1B pin can output the positive and negative "Timer1 overflow divided by 2/3/4" signal, and the T2O pin can output the "Timer2 overflow divided by 2/3/4" signal. These outputs can be used for Buzzer application. Timer0's extra utility is to supports RFC/SXT count. The RFC clock divided by 1/4/16/64 signal or SXT clock can replace T0 pin as the Timer0's event count input.

8.1 Timer0/Timer1

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs

88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR **89h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set

89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin's negative edge

89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops

89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

89h.2 **CT0N:** Timer0 Counter/Timer select bit
0: Timer mode, Timer0 data increases at 2 System clock cycle rate
1: Counter mode, Timer0 data increases at T0 pin's negative edge

89h.1~0 **TMOD0:** Timer0 mode select
00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR **8Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR **8Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

SFR **8Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

SFR **8Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

SFR **AFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCON	P0RFC		T0SEL		RFCPSC		RFCS	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	1	1	0	0

AFh.5~4 **T0SEL:** Timer0 Counter mode (CT0N=1) T0 input select
00: P3.4 pin (8051 standard)
01: RFC clock divided by 1/4/16/64
10: SXT clock
11: RFC clock divided by 1/4/16/64 gated by Timer2 overflow

AFh.3~2 **RFCPSC:** RFC clock divider to Timer0
00: divided by 64
01: divided by 16
10: divided by 4
11: divided by 1

8.2 Timer2

Timer2 is controlled through the TCON2 register with the low and high bytes of Timer/Counter2 stored in TL2 and TH2 and the low and high bytes of the Timer2 reload/capture registers stored in RCAP2L and RCAP2H.

SFR **C8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

C8h.7 **TF2:** Timer2 overflow flag
Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.

C8h.6 **EXF2:** T2EX interrupt pin falling edge flag
Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.

C8h.5 **RCLK:** UART receive clock control bit
0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3
1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3

C8h.4 **TCLK:** UART transmit clock control bit
0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3
1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3

C8h.3 **EXEN2:** T2EX pin enable
0: T2EX pin disable
1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0

C8h.2 **TR2:** Timer2 run control
0: Timer2 stops
1: Timer2 runs

C8h.1 **CT2N:** Timer2 Counter/Timer select bit
0: Timer mode, Timer2 data increases at 2 System clock cycle rate
1: Counter mode, Timer2 data increases at T2 pin's negative edge

C8h.0 **CPRL2N:** Timer2 Capture/Reload control bit
0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1.
1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1.
If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.

SFR **CAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2L	RCP2L							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CAh.7~0 **RCP2L:** Timer2 reload/capture data low byte

SFR **CBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2H	RCP2H							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CBh.7~0 **RCP2H:** Timer2 reload/capture data high byte

SFR **CCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL2	TL2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CCh.7~0 **TL2:** Timer2 data low byte

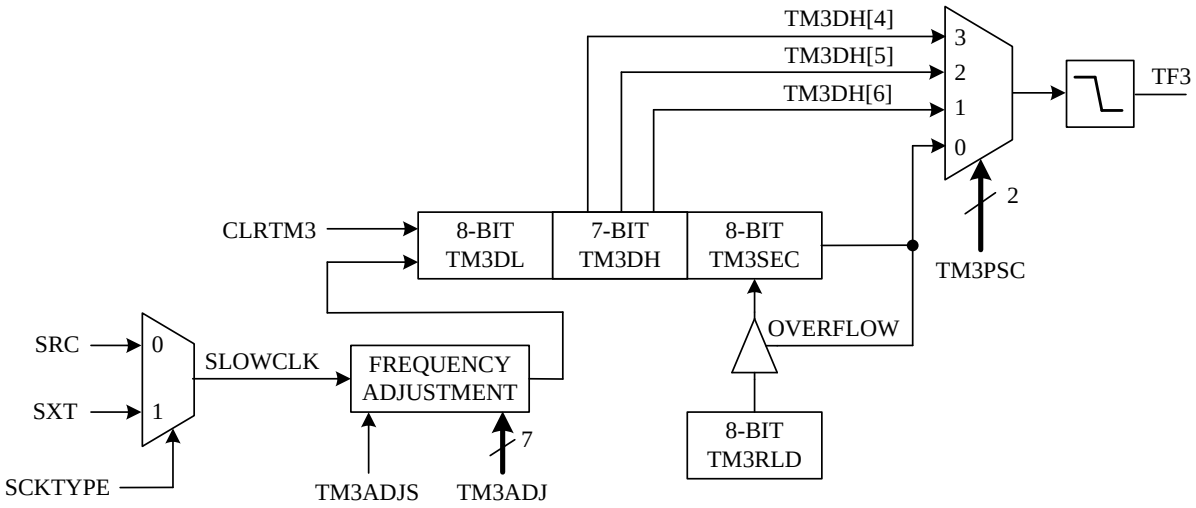
SFR **CDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH2	TH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CDh.7~0 **TH2:** Timer2 data high byte

8.3 Timer3

The 23-bit wide Timer3 is reloadable for its 8-bit MSB when overflow. Its time base is Slow clock (SRC or SXT). Timer3 can generate interrupt periodically at different rate, and its counting data can be read out by CPU. It is recommended to read Timer3 data in Slow mode. While CPU clock is switched to Fast clock, the clock source of CPU and Timer3 are different, CPU may read a "under changing Timer3 data". User F/W must have some filter mechanism to avoid such kind un-stability. On the contrast, Timer3 interrupt has no ambiguous behavior no matter what the CPU clock source is.

Timer3 can control its counting rate by the TM3ADJ SFR. This feature compensates the 32768 SXT crystal's in-accuracy. While TM3ADJ=0, Timer3 increase its data count normally at each Slow clock cycle. If TM3ADJ is set to positive adjustment, Timer3 increase its data count by 2 in particular Slow clock cycles, resulting a faster counting rate. If TM3ADJ is set to negative adjustment, Timer3 stop increase in particular Slow clock cycles, resulting a slower counting rate. The adjustment is 0.477ppm per step, and the total adjustable range is ±61ppm.



Timer3 Structure

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	–	–	–	TKSOC	CLRWDT	CLRTM3	STPRFC	DPSEL
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

F8h.2 **CLRTM3:** Set 1 to Clear Timer3 and force TM3SEC reload

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	SXTGAIN		STPPCK	PWRFLT	UART1W	WDTPSC	TM3PSC	
R/W	R/W		R/W	R/W	R/W	R/W	R/W	
Reset	1	1	0	0	0	0	0	1

94h.1~0 **TM3PSC:** Timer3 Interrupt rate

00: Timer3 interrupt occurs when 23 bit count data overflow

01: Timer3 interrupt rate is 32768 Slow clock cycles (1.0 second for SXT)

10: Timer3 interrupt rate is 16384 Slow clock cycles (0.5 second for SXT)

11: Timer3 interrupt rate is 8192 Slow clock cycles (0.25 second for SXT)

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	–	TKIF	IE2	P1IF	TF3
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

95h.0 **TF3:** Timer3 Interrupt Flag

Set by H/W when Timer3 reaches TM3PSC setting cycles. Cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit. (***Note2***)

SFR **B3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3SEC	TM3SEC							
R/W	R							
Reset	–	–	–	–	–	–	–	–

B3h.7~0 **TM3SEC:** Timer3 count data bit 22~15

SFR **B4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3DL	TM3DL							
R/W	R							
Reset	–	–	–	–	–	–	–	–

B4h.7~0 **TM3DL:** Timer3 count data bit 7~0

SFR **B5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3DH	–	TM3DH						
R/W	–	R						
Reset	–	–	–	–	–	–	–	–

B5h.6~0 **TM3DH:** Timer3 count data bit 14~8

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3RLD	TM3RLD							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

B6h.7~0 **TM3RLD:** Timer3 overflow reload data for Timer3 bit 22~15 (TM3SEC)

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3ADJ	TM3ADJS	TM3ADJ						
R/W	R/W	R/W						
Reset	0	0	0	0	0	0	0	0

B7h.7 **TM3ADJS:** Timer3 adjustment sign

0: Timer3 positive adjust, to increase Timer3 counting rate

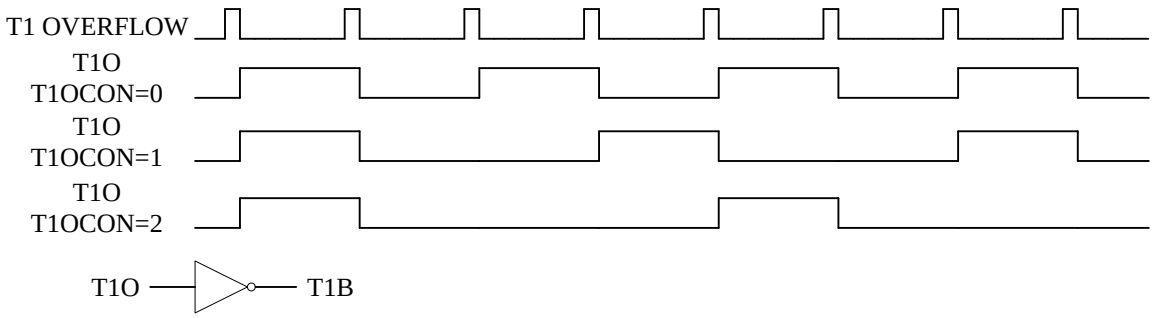
1: Timer3 negative adjust, to decrease Timer3 counting rate

B7h.6~0 **TM3ADJ:** Timer3 adjust magnitude, 0.477 ppm per LSB.

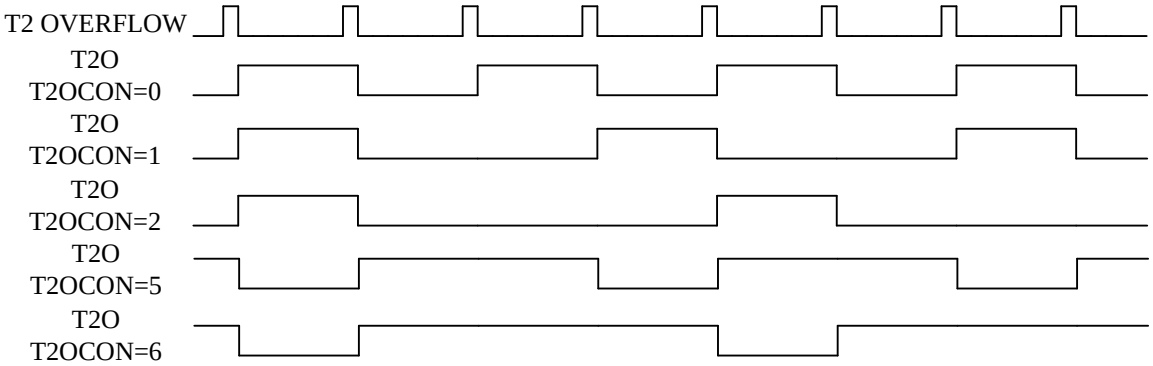
The adjustment is calculated as ±TM3ADJ*0.477ppm. The total adjustable range is ±61ppm.

8.4 T1O, T1B and T2O output Control

This device can generate various frequency or duty cycle waveform output (in CMOS push pull format) for Buzzer or Remote IR control application. The T1O, T1B and T2O waveform is derived by Timer1/Timer2 overflow signal. User can control their frequency by Timers auto reload value, as well as set their duty cycle by TOCON SFR. The pin output function is enabled by setting the P3MODH SFR to Mode3 for each pin (***see Section 7***).



T1O, T1B waveform with T1OCON



T2O waveform with T2OCON

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TOCON	T1OCON		T2OCON			TCOCON		
R/W	R/W		R/W			R/W		
Reset	0	0	0	0	0	0	0	0

A6h.7~6 **T1OCON:** T1O pin duty and frequency control
00: 1/2 duty, 1/2 Timer1 overflow frequency
01: 1/3 duty, 1/3 Timer1 overflow frequency
10: 1/4 duty, 1/4 Timer1 overflow frequency

A6h.5~3 **T2OCON:** T2O pin duty and frequency control
000: 1/2 duty, 1/2 Timer2 overflow frequency
001: 1/3 duty, 1/3 Timer2 overflow frequency
010: 1/4 duty, 1/4 Timer2 overflow frequency
101: 2/3 duty, 1/3 Timer2 overflow frequency
110: 3/4 duty, 1/4 Timer2 overflow frequency

Note6: also refer to Section 6 for more information about Timer0/1/2/3 Interrupt enable and priority.

9. UART

The UART uses SCON and SBUF SFRs. SCON is the control register, SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are completely independent. In addition to standard 8051's full duplex mode, this chip also provides one wire mode. If the UART1W bit is set, both transmit and receive data use P3.1 pin.

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.7 **SMOD:** UART double baud rate control bit
0: Disable UART double baud rate
1: Enable UART double baud rate

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	SXTGAIN		STPPCK	PWRFLT	UART1W	WDTPSC	TM3PSC	
R/W	R/W		R/W	R/W	R/W	R/W	R/W	
Reset	1	1	0	0	0	0	0	1

94h.3 **UART1W:** One wire UART mode enable, both TXD / RXD use P3.1 pin
0: Disable one wire UART mode
1: Enable one wire UART mode

SFR **98h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** Serial port mode select bit 0,1
00: Mode0: 8 bit shift register, Baud Rate=$F_{SYSCLK}/2$
01: Mode1: 8 bit UART, Baud Rate is variable
10: Mode2: 9 bit UART, Baud Rate=F_{SYSCLK} / 32 or/64
11: Mode3: 9 bit UART, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2
SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART reception enable
0: Disable reception
1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR **99h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

99h.7~0 **SBUF:** UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

F_{SYSCLK} denotes System clock frequency, the UART baud rate is calculated as below.

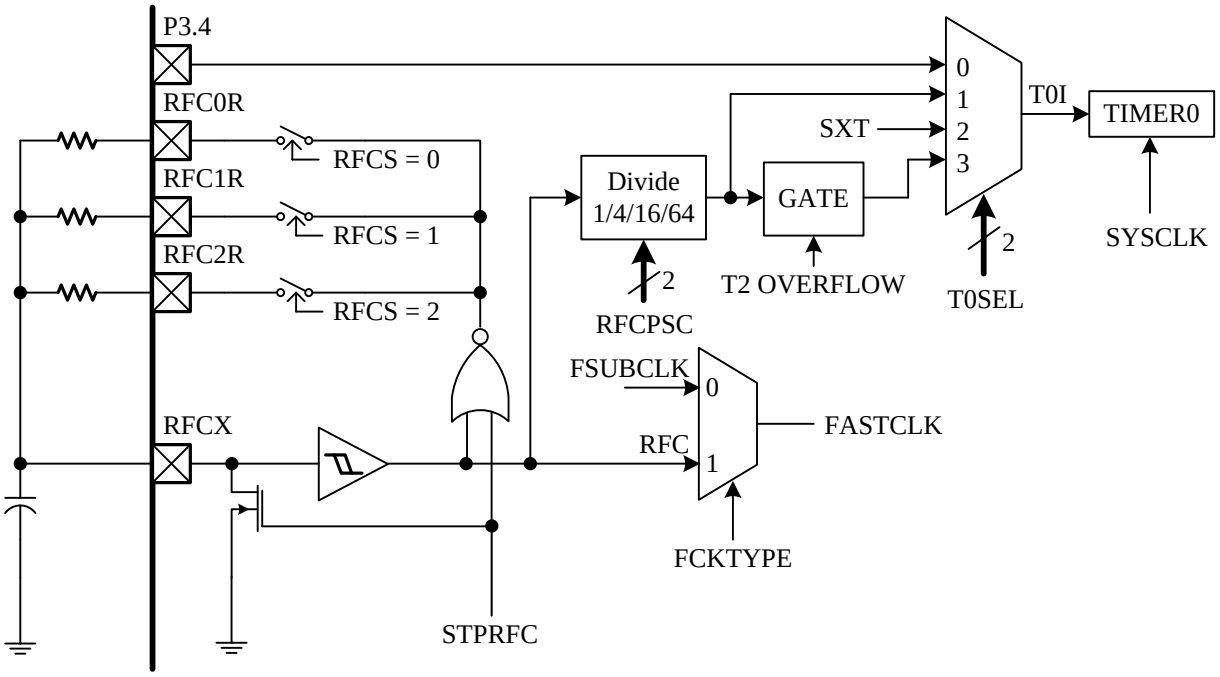
- **Mode 0:**
  Baud Rate=$F_{SYSCLK}/2$
- **Mode 1, 3:** if using Timer1 auto reload mode
  Baud Rate= (SMOD+1) xF_{SYSCLK}/ (32x2x (256–TH1))
- **Mode 1, 3:** if using Timer2
  Baud Rate=Timer2 overflow rate/16=F_{SYSCLK}/ (32x (65536–RCP2H, RCP2L))
- **Mode 2:**
  Baud Rate= (SMOD+1) x $F_{SYSCLK}/64$

Note6: also refer to Section 6 for more information about UART Interrupt enable and priority.

Note8: also refer to Section 8 for more information about how Timer2 controls UART clock.

10. Resistance to Frequency Converter (RFC)

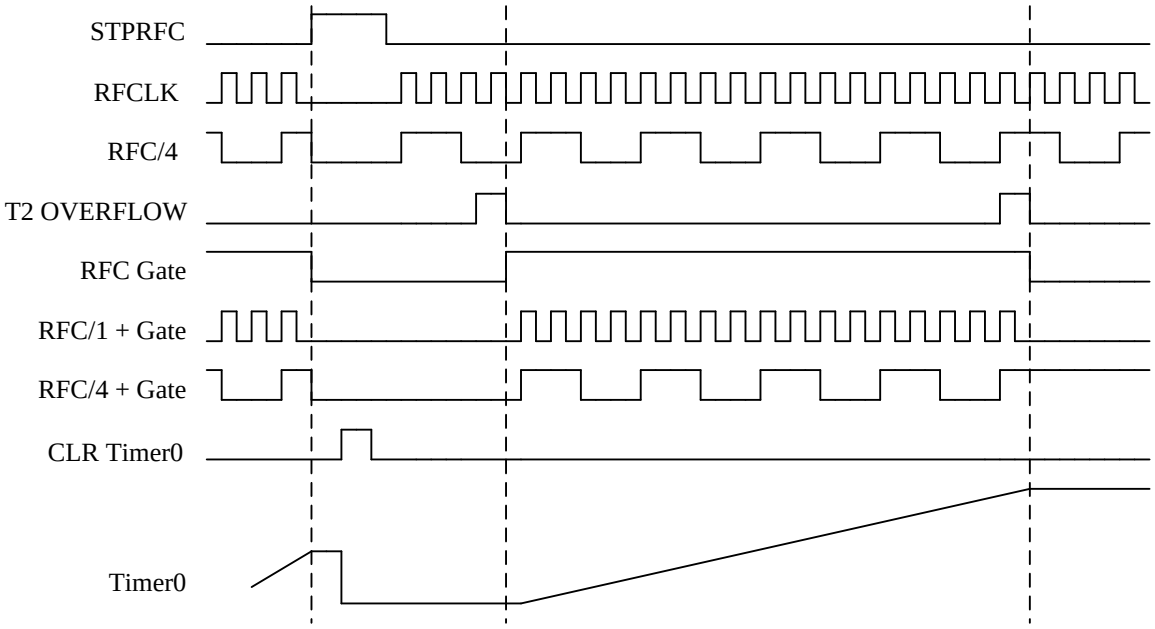
The RFC module can build the RC oscillation circuitry with RFCX pin and RFC0R, RFC1R or RFC2R pins. Only one RC oscillation circuitry is active at a time. There are 2 methods to measure the RFC clock frequency. One is to set the RFC as the Timer0 Counter mode input, the other one is to set RFC as the System clock. Since SXT/FXT is a precise timing source, user can derive the RFC frequency by comparing the Timer's count data which running by RFC and SXT/FXT.



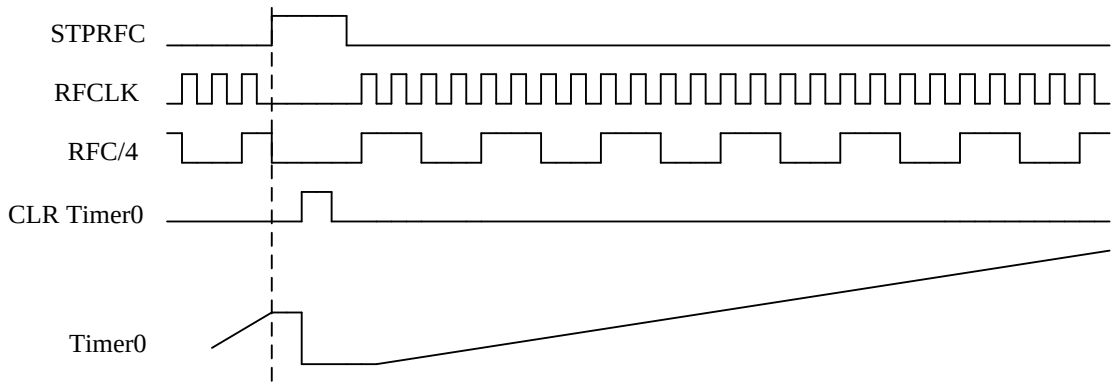
RFC Structure

The Timer0's event count input can be selected by T0SEL SFR. When T0SEL=3, the RFC clock is gated by Timer2's overflow period then go into the Timer0 for event counting. This function helps Timer0 to count the RFC clock with more accuracy by H/W automatically start and stop gating the RFC clock. The steps of this usage are described below.

1. Proper setting the RFCON SFR to setup the RFC oscillation circuitry.
2. CT0N=1 (Timer0 counter mode), CT2N=0 (Timer2 timer mode), T0SEL=3, FCKTYPE=0.
3. STPRFC=1, RFC gating is cleared and waiting for next Timer2 overflow to start
4. Clear Timer0, write TH2/TL2 with a data to accelerate Timer2 overflow (ex: FF00)
5. STPRFC=0, RFC starts, wait for next two Timer2 overflows.
6. The Timer0 counting the RFC clock only in between the two Timer2 overflows time slot.



RFC clock to Timer0, T0SEL=3



RFC clock to Timer0, T0SEL=1

SFR **AFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCON	P0RFC		T0SEL		RFCPSC		RFCS	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	1	1	0	0

AFh.7~6 **P0RFC:** P0.0~P0.3 pin RFC mode control.
00: P0.0~P0.3 are not RFC pins
01: P0.0 and P0.1 are RFC pins, P0.2 and P0.3 are not RFC pins
10: P0.0~P0.2 are RFC pins, P0.3 is not RFC pin
11: P0.0~P0.3 are RFC pins

AFh.5~4 **T0SEL:** Timer0 Counter mode (CT0N=1) T0 input select
00: P3.4 pin (8051 standard)
01: RFC clock divided by 1/4/16/64
10: SXT clock
11: RFC clock divided by 1/4/16/64 gated by Timer2 overflow

AFh.3~2 **RFCPSC:** RFC clock divider to Timer0
00: divided by 64
01: divided by 16
10: divided by 4
11: divided by 1

AFh.1~0 **RFCS:** Select RFC convert channel.
00: RFC0R (P0.1)
01: RFC1R (P0.2)
10: RFC2R (P0.3)

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	–	–	–	TKSOC	CLRWDT	CLRTM3	STPRFC	DPSEL
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

F8h.1 **STPRFC:** Set 1 to stop RFC clock oscillating

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	FCKTYPE	FSUBSEL	SELFCK	SCKTYPE	STPFSUB	CLKPSC		
R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	1	0	1

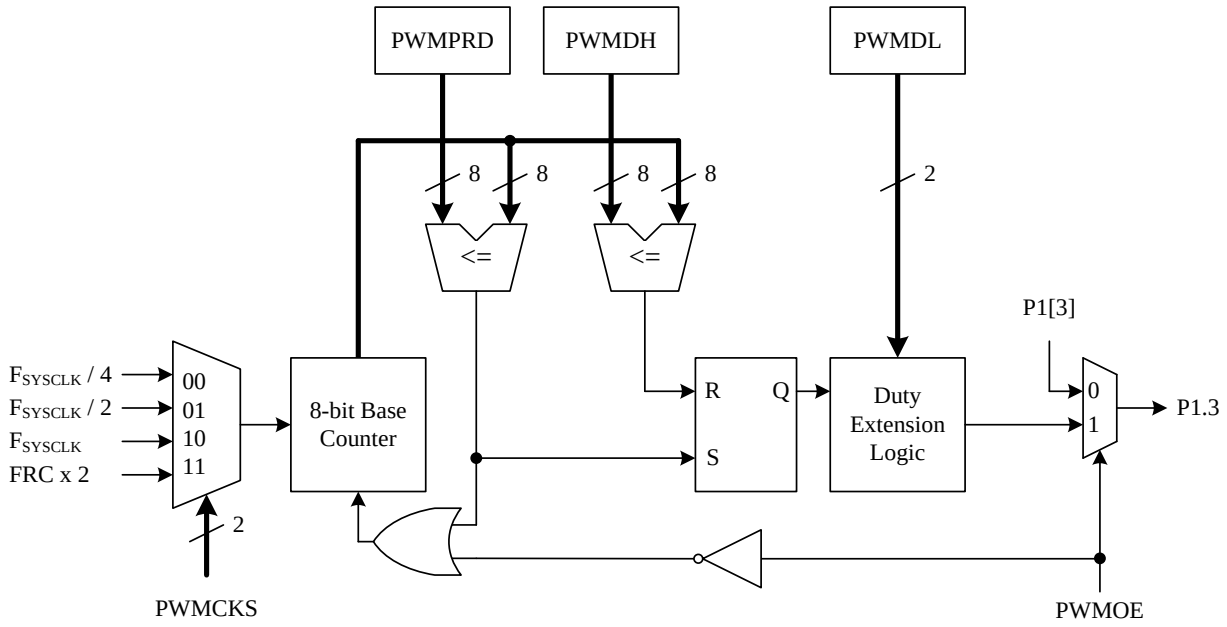
D8h.7 **FCKTYPE:** Fast clock type select, This bit can be changed only in Slow mode (SELFCK=0)
0: Fast clock is FSUBCLK (FRC or FXT)
1: Fast clock is RFC, S/W must setup RFC oscillating circuitry before set this bit to 1.

11. PWM

The **F2230B/34B** has an independent PWM module. The PWM can generate a fixed frequency waveform with 1024 duty resolution on the basis of the PWM clock. The PWM clock can select FRC double frequency (FRCx2) or F_{SYSCLK} divided by 1, 2, or 4 as its clock source. A spread LSB technique allows PWM to run its frequency at the "PWM clock divided by 256" instead of at the "PWM clock divided by 1024", which means the PWM is four times faster than normal. The advantage of a higher PWM frequency is that the post RC filter can transform the PWM signal to a more stable DC voltage level.

The PWM output signal resets to a low level whenever the 8-bit base counter matches the 8-bit MSB of the PWM duty register. When the base counter rolls over, the 2-bit LSB of the PWM duty register decides whether to set the PWM output signal high immediately or set it high after one clock cycle delay. The PWM period can be set by writing the period value to the 8-bit PWM period register.

The pin mode SFR controls the PWM output waveform format. Mode1 makes the PWM open drain output and Mode2 makes the PWM CMOS push-pull output. (see section 7)



PWM Structure

SFR **9Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMPRD	PWMPRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Ch.7~0 **PWMPRD:** PWM 8-bit period register

SFR **9Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMDH	PWMDH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

9Dh.7~0 **PWMDH:** bits 9~2 of the PWM 10-bit duty register

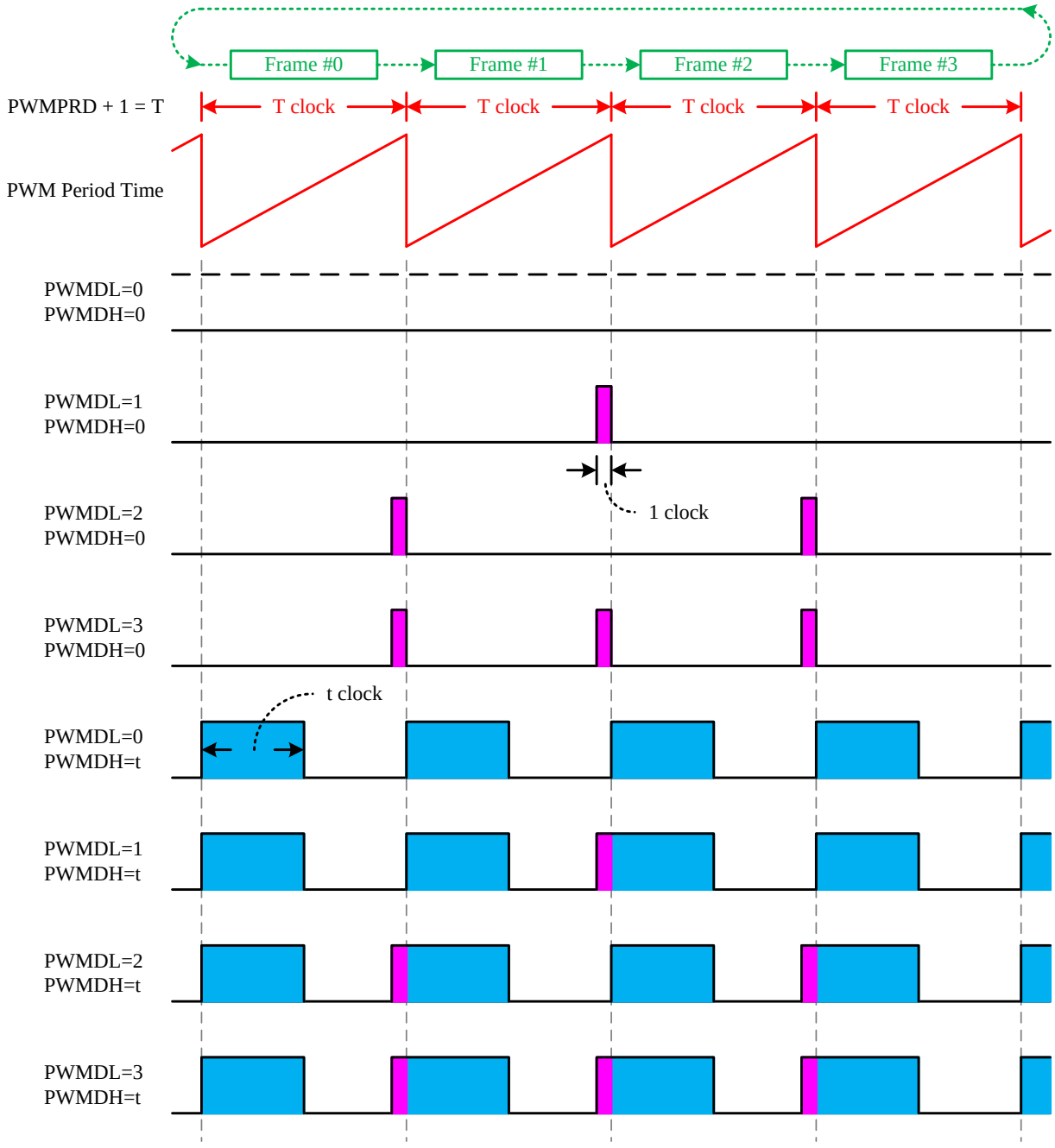
SFR **A1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON	PWMCKS		PWMDL		–	–	–	–
R/W	R/W		R/W		–	–	–	–
Reset	1	0	0	0	–	–		

A1h.7~6 **PWMCKS:** PWM clock source
00: $F_{SYSCLK}/4$
01: $F_{SYSCLK}/2$
10: F_{SYSCLK}
11: FRCx2

A1h.5~4 **PWMDL:** bits 1~0 of the PWM 10-bit duty register

SFR **BFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMODE	I80EN	I80POL	PWMOE	–	–	–	–	–
R/W	R/W	R/W	R/W	–	–	–	–	–
Reset	0	0	0	–	–	–	–	–

BFh.5 **PWMOE:** PWM signal output enable
0: Disable PWM signal output to P1.3
1: Enable PWM signal output to P1.3



PWM Waveform

12. I80 interface

The **F2230B/34B** provides an easy way to access LCD module using I80 interface. If I80EN is set, Port 0, P36 and P37 switch to I80 DATA, I80 WR and I80 RD. I80 interface provide an easy way to read or write data from LCD module just only access from external ram address at 0xF400. It is simply achieved write/read LCD module by "MOVX @DPTR, A" or "MOVX A, @DPTR" instruction.

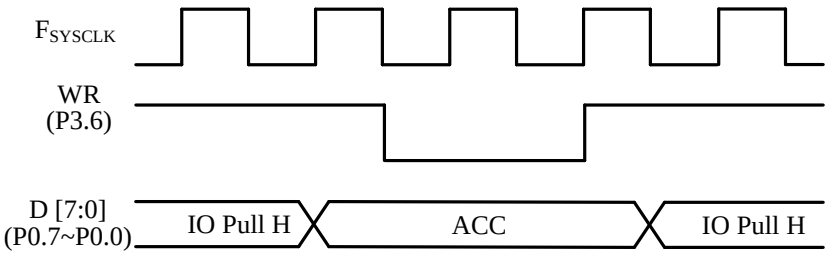
Pin Name	I80	P0OE.n	P0.n	Pin State
P07~P00	D7~D0	0	0	I80 interface data bus without Pull-up
		0	1	I80 interface data bus with Pull-up

Pin Name	I80	Mode	P3.n	Pin State
P36	WR	2	x	I80 interface write enable, without Pull-up
P37	RD	2	x	I80 interface read enable, without Pull-up

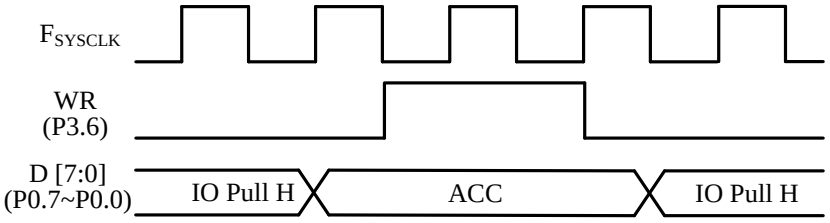
After access external ram address at 0xF400, D7~D0, WR and RD will automatic generate read/write waveform as following figure. There are some control pins at LCM module such as CS and A0 need to be connected to GPIO and set manual.

```
;I80 Write example code
MOV     PINMODE, #80h       ; Enable I80 interface & low enable
MOV     DPTR, #F400h        ; DPTR=F400h=target I80 address
MOV     A, #5Ah             ; A=5Ah=target I80 write data
MOVX    @DPTR, A            ; Write 5A to LCM
```

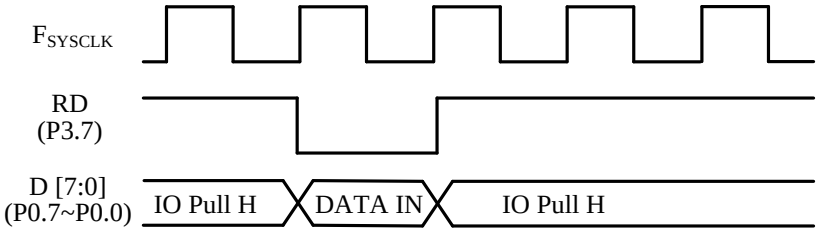
```
;I80 Read example code
MOV     PINMODE, #80h       ; Enable I80 interface & low enable
MOV     DPTR, #F400h        ; DPTR=F400h=target I80 address
MOVX    A, @DPTR            ; Read LCM data to A
```



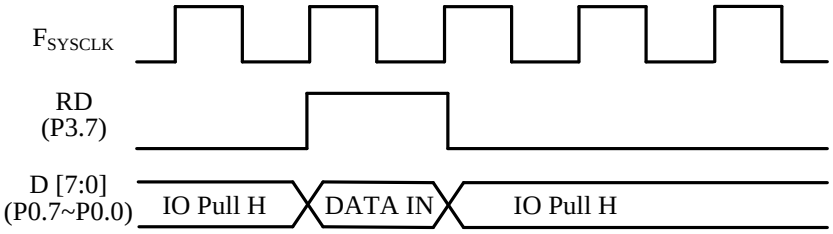
I80EN=1, I80POL=0, Write timing



I80EN=1, I80POL=1, Write timing



I80EN=1, I80POL=0, Read timing



I80EN=1, I80POL=1, Read timing

SFR **BFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMODE	I80EN	I80POL	PWMOE	–	–	–	–	–
R/W	R/W	R/W	R/W	–	–	–	–	–
Reset	0	0	0	–	–	–	–	–

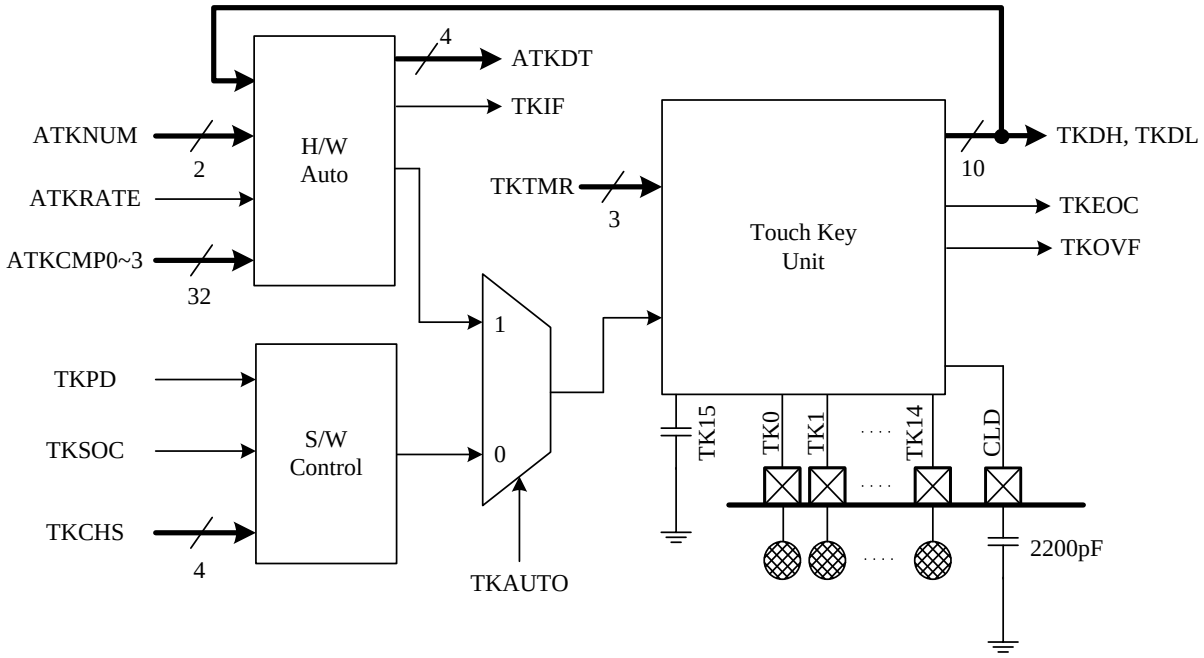
BFh.7 **I80EN:** I80 interface enable.
0: Disable
1: Enable

BFh.6 **I80POL:** The polarity of RD/WR signal
0: RD/WR are low active
1: RD/WR are high active

Note: also refer to Section 7 for more information about I80 pins share with I/O pins

13. Touch Key (F2230B only)

The Touch Key offers an easy, simple and reliable method to implement finger touch detection. During the key scan operation, it only requires an external capacitor component on CLD pin. The device support 15 channels touch key detection with S/W manual mode and H/W Auto Mode (ATK). Only one mode can be active at a time.



Touch Key Structure

To use the Touch Key, user must setup the Pin Mode (***see Section 7***) correctly as below table. Setting Mode0 for a Touch Key pin can pull up the pin during idling and reduce the mutual interference between the adjacent keys. While a TK pin is under scanning, either being in S/W manual mode or H/W ATK mode, the Touch Key module automatically disable the pin's pull-up resistor.

P1MODx/P3MODx setting for Touch Key	TK0~TK3	TK4~TK14	CLD
Pin is Touch Key, Idling	Mode0	Mode0	Mode3
Pin is Touch Key, S/W Scanning	Mode0	Mode0	Mode3
Pin is Touch Key, H/W Auto Scan (ATK)	Mode0	–	Mode3

S/W Manual Mode Touch Key Detection

All Touch Key (TK0~TK14) can be used for S/W manual mode. To start a S/W scan mode, user assigns TKAUTO=0 and TKPD=0, then set the TKSOC bit to start touch key conversion, the TKSOC bit can be automatically cleared while end of conversion. However, if the SYSCLK is too slow, H/W might fail to clear TKSOC due to clock sampling rate. TKEOC=0 means conversion is in process. TKEOC=1 means the conversion is finish, and the touch key counting result is stored into the 10 bits TK Data Counter TKDH and TKDL. The larger TK pin capacitance is the smaller TK data counter is. After TKEOC=1, user must wait at least 50 us for next conversion. If TKOVF=1, means the conversion transaction exceeds period time. Reduce/Increase TKTMR can reduce/increase TK Data Count to adapt the system board circumstances.

The Touch Key unit has an internal built-in reference capacitor to simulate the KEY behavior. Set TKCHS=15 and start the S/W scan mode can get the TK Data Count of this capacitor. Since the internal capacitor would not be affected by water or mobile phone, it is useful for comparing the environment background noise.

Note: CLD discharge time is in proportion to CLD capacitance, refer to AP-TM52_57XX_Touch_02S

H/W Auto Touch Key Detection (ATK)

Only TK0~TK3 are eligible for H/W auto mode. This function can work in Fast/Slow/Idle mode and save the S/W effort as well as minimize the chip current consumption. To use this function, user need to set TKAUTO=1 and TKPD=1 to enable H/W fully control the TK unit. H/W then automatically detects the TK0~TK3's TK Data Count at every 62ms or 125ms rate. If a Key's TK Data Count is less than the pre-set compare threshold (ATKCMP0~3), H/W generates interrupt and wake up CPU. User can switch the TK module back to S/W Manual Mode after the TK interrupt and identify/confirm the Key touch event.

SFR **ADh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON	TKPD	TKTMR			TKCHS			
R/W	R/W	R/W			R/W			
Reset	1	1	0	0	1	1	1	1

ADh.7 **TKPD:** Touch Key Power Down (for S/W mode)
0: Touch Key enable
1: Touch Key disable

ADh.6~4 **TKTMR:** Touch Key Conversion Time (for both S/W and H/W ATK mode)
000: Conversion time shortest
…
111: Conversion time longest

ADh.3~0 **TKCHS:** Touch Key Channel Select (for S/W Mode)
0000: TK0 (P1.7)
0001: TK1 (P1.6)
0010: TK2 (P1.5)
0011: TK3 (P1.4)
0100: TK4 (P1.3)
0101: TK5 (P1.2)
0110: TK6 (P1.1)
0111: TK7 (P1.0)
1000: TK8 (P3.7)
1001: TK9 (P3.6)
1010: TK10 (P3.5)
1011: TK11 (P3.3)
1100: TK12 (P3.2)
1101: TK13 (P3.1)
1110: TK14 (P3.0)
1111: Internal Reference Capacitor

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	–	–	–	TKSOC	CLRWDT	CLRTM3	STPRFC	DPSEL
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

F8h.4 **TKSOC:** Rising edge of this bit will trigger a Touch Key conversion (for S/W Mode). Basically, this bit is automatically cleared by H/W after end of conversion. However, if the SYSCLK is too slow, H/W might fail to clear TKSOC due to clock sampling rate issue.

SFR **ABh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKDT	TKEOC	TKOVF	TKDH		ATKDT			
R/W	R	R	R		R			
Reset	–	–	–	–	–	–	–	–

ABh.7 **TKEOC:** Touch Key End of Conversion (for S/W Mode), TKEOC may have 3uS delay after TKSOC=1, so F/W must wait enough time before polling this Flag.
0: Indicates conversion is in progress
1: Indicates conversion is finished

ABh.6 **TKOVF:** Touch Key Counter Overflow (for S/W Mode)

ABh.5~4 **TKDH:** Touch Key Counter Data 9~8 (for S/W Mode)

ABh.3~0 **ATKDT:** Touch Key Auto Scan Result (for H/W ATK Mode)
xxx1: TK0 has a Touch event
xx1x: TK1 has a Touch event
x1xx: TK2 has a Touch event
1xxx: TK3 has a Touch event

SFR **ACh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKDL	TKDL							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ACh.7~0 **TKDL:** Touch Key Counter Data 7~0 (for S/W Mode)

SFR **AEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON2	–	–	–	–	TKAUTO	ATKRATE	ATKNUM	
R/W	–	–	–	–	R/W	R/W	R/W	
Reset	–	–	–	–	0	0	1	1

AEh.3 **TKAUTO:** Touch Key Auto Scan Mode Enable
0: S/W Mode
1: H/W ATK Mode

AEh.2 **ATKRATE:** Touch Key Scan Rate (for H/W ATK Mode)
0: ATK scan rate is 4096 Slow clock cycles (125ms if Slow clock is SXT)
1: ATK scan rate is 2048 Slow clock cycles (62ms if Slow clock is SXT)

AEh.1~0 **ATKNUM:** Touch Key Auto Scan Channel Number (for H/W ATK Mode)
00: ATK only detect TK0
01: ATK detect TK0 and TK1
10: ATK detect TK0~TK2
11: ATK detect TK0~TK3

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	–	TKIF	IE2	P1IF	TF3
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

95h.3 **TKIF:** Touch Key Interrupt Flag (for H/W ATK Mode)
Set by H/W when a TK channel's touch event is detected.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write F7h to INTFLG to clear this bit. (***Note2***)

SFR **C4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKCMP0	ATKCMP0							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

C4h.7~0 **ATKCMP0:** Data Threshold Compared with TK0 scan (for H/W ATK Mode)

SFR **C5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKCMP1	ATKCMP1							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

C5h.7~0 **ATKCMP1:** Data Threshold Compared with TK1 scan (for H/W ATK Mode)

SFR **C6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKCMP2	ATKCMP2							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

C6h.7~0 **ATKCMP2:** Data Threshold Compared with TK2 scan (for H/W ATK Mode)

SFR **C7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKCMP3	ATKCMP3							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

C7h.7~0 **ATKCMP3:** Data Threshold Compared with TK3 scan (for H/W ATK Mode)

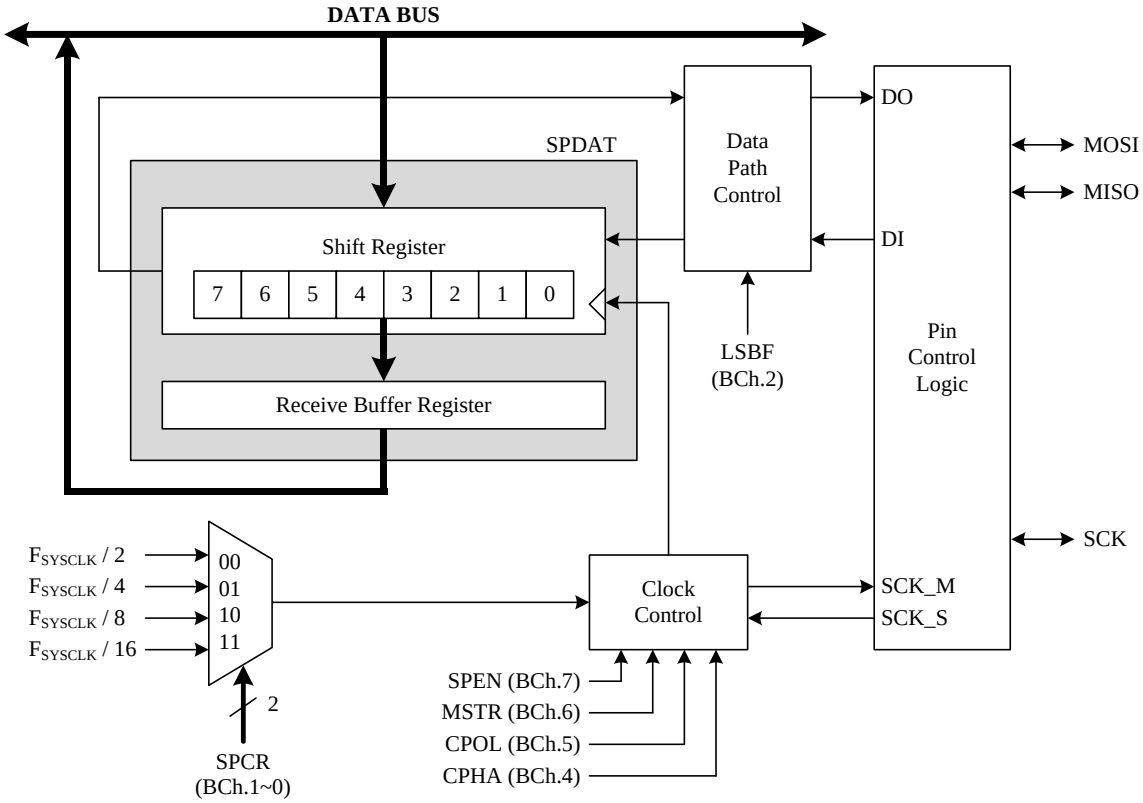
Note6: also refer to Section 6 for more information about Touch Key Interrupt enable and priority.

14. Serial Peripheral Interface (SPI)

The SPI module is capable of full-duplex, synchronous, serial communication between the **F2230B/34B** and peripheral devices. The peripheral devices can be other MCUs, A/D converter, sensors, or Flash memory, etc. The SPI runs at a baud rate up to the system clock divided by two. Firmware can read the status flags, or the operation can be interrupt driven.

The features of the SPI module include:

- Master or Slave mode operation
- 3-wire mode operation
- Full-duplex operation
- Programmable transmit bit rate
- Single Buffer receive
- Serial clock phase and polarity options
- MSB-first or LSB-first shifting selectable



SPI System Block Diagram

The MOSI (P2.4) signal is an output when SPI is operating in Master mode and an input when SPI is operating in Slave mode. The MISO (P2.6) signal is an input when SPI is operating in Master mode and an output when SPI is operating in Slave mode. Data is transferred MSB or LSB first by setting the LSBF bit. The SCK (P2.5) signal is an output from a Master device and an input to Slave devices. It is used to synchronize the data on the MOSI and MISO lines of Master and Slave. SPI generates the signal with eight programmable clock rates in Master mode.

Master Mode

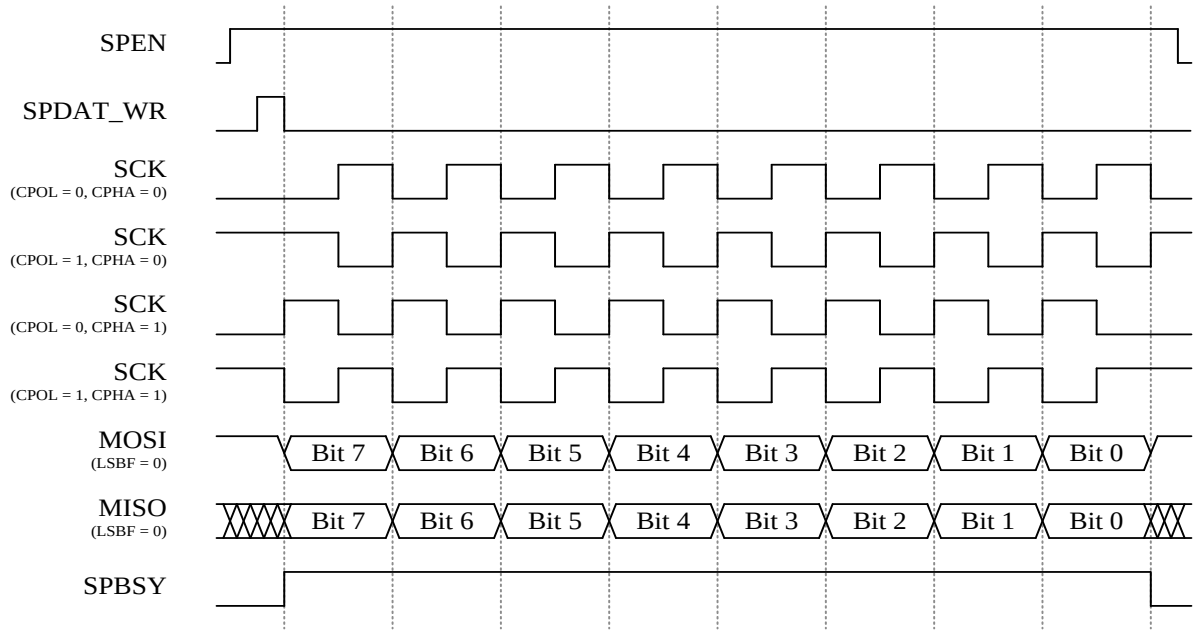
The SPI operates in Master mode by setting the MSTR bit in the SPCON. To start transmit, writing a data to the SPDAT. If SPBSY=0, the data will be transferred to the shift register and starts shift out on the MOSI line. The data of the Slave shift in from the MISO line at the same time. When the SPIF bit becomes set at the end of transfer, the receive data is written to receiver buffer and the RCVBF bit in the SPSTA is set. To prevent an overrun condition, software must read the SPDAT before next byte enters the shift register. The SPBSY bit will be set when writing a data to SPDAT to start transmit, and be cleared at the end of the eighth SCK period in Master mode.

Slave Mode

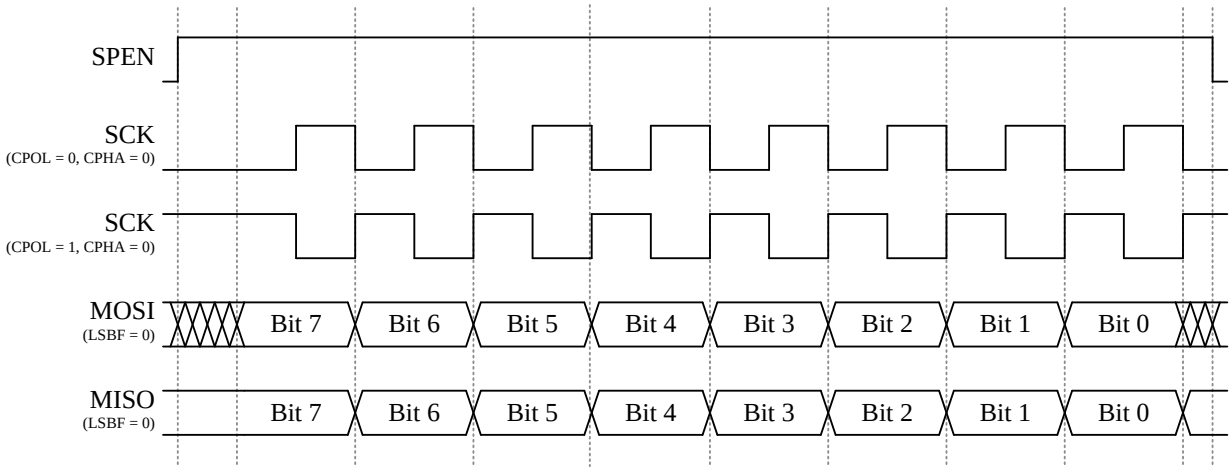
The SPI operates in Slave mode by clearing the MSTR bit in the SPCON. The transmission will start when the SPEN bit in the SPCON is set. The data from a Master will shift into the shift register through the MOSI line, and shift out from the shift register on the MISO line. When a byte enters the shift register, the data will be transferred to receiver buffer if RCVBF=0. If RCVBF=1, the newer received data will not be transferred to receiver buffer and the RCVOVF bit is set. After a byte enters the shift register, the SPIF and RCVBF bits are set. To prevent an overrun condition, software must read the SPDAT or write 0 to RCVBF before next byte enters the shift register. The maximum SCK frequency allowed in Slave mode is $F_{SYSCLK}/4$.

Serial Clock

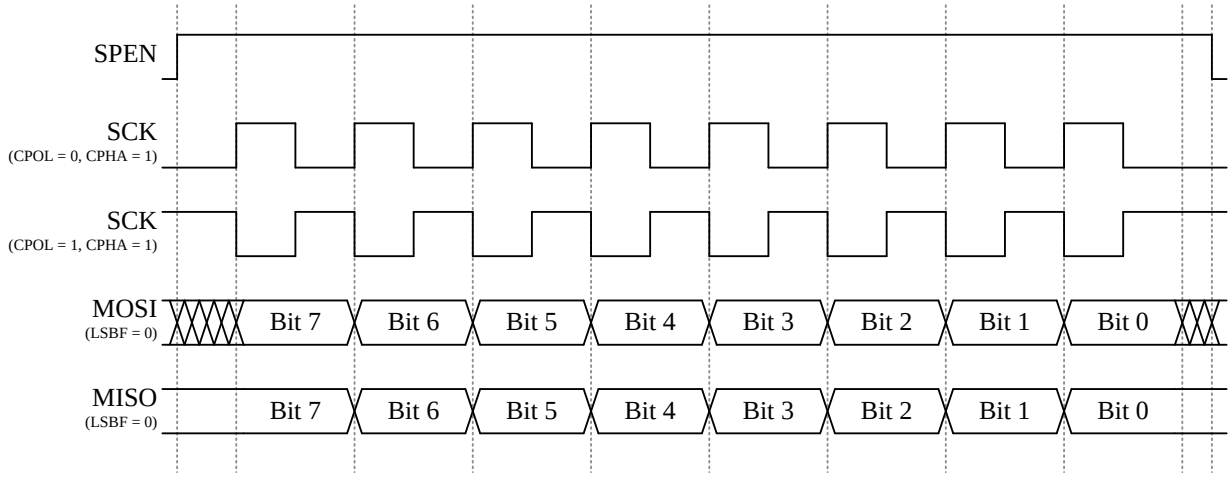
The SPI has four clock types by setting the CPOL and CPHA bits in the SPCON register. The CPOL bit defines the level of the SCK in SPI idle state. The level of the SCK in idle state is low when CPOL=0, and is high when CPOL=1. The CPHA bit defines the edges used to sample and shift data. The SPI sample data on the first edge of SCK period and shift data on the second edge of SCK period when CPHA=0. The SPI sample data on the second edge of SCK period and shift data on first edge of SCK period when CPHA=1. Figures below show the detail timing in Master and Slave modes. Both Master and Slave devices must be configured to use the same clock type before the SPEN bit is set. The SPCR controls the Master mode serial clock frequency. This register is ignored when operating in Slave mode. The SPI clock can select System clock divided by 2, 4, 8, or 16 in Master mode.



Master Mode Timing



Slave Mode Timing (CPHA=0)



Slave Mode Timing (CPHA=1)

In both Master and Slave modes, the SPIF interrupt flag is set by H/W at the end of a data transfer. If write data to SPDAT when SPBSY=1, the WCOL interrupt flag will be set by H/W. When this occurs, the data write to SPDAT will be ignored, and shift register will not be written.

SFR **BCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCON	SPEN	MSTR	CPOL	CPHA	–	LSBF	SPCR	
R/W	R/W	R/W	R/W	R/W	–	R/W	R/W	
Reset	0	0	0	0	–	0	0	0

BCh.7 **SPEN:** SPI Enable.
0: SPI Disable
1: SPI Enable, P2.4~P2.6 are SPI functional pins.

BCh.6 **MSTR:** Master Mode Enable.
0: Slave Mode
1: Master Mode

BCh.5 **CPOL:** SPI Clock Polarity
0: SCK is low in idle state
1: SCK is high in idle state

BCh.4 **CPHA:** SPI Clock Phase
0: Data sampled on first edge of SCK period
1: Data sampled on second edge of SCK period

BCh.2 **LSBF:** LSB First.
0: MSB first
1: LSB first

BCh.1~0 **SPCR:** SPI Clock Rate.
00: $F_{SYSCLK}/2$
01: $F_{SYSCLK}/4$
10: $F_{SYSCLK}/8$
11: $F_{SYSCLK}/16$

SFR **BDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPSTA	SPIF	WCOL	–	RCVOVF	RCVBF	SPBSY	–	–
R/W	R/W	R/W	–	R/W	R/W	R	–	–
Reset	0	0	–	0	0	–	–	–

BDh.7 **SPIF:** SPI Interrupt Flag
Set by H/W at the end of a data transfer. Cleared by H/W when interrupt is vectored into. Write 0 to this bit will clear this flag.

BDh.6 **WCOL:** Write Collision Interrupt Flag
Set by H/W if write data to SPDAT when SPBSY=1. Write 0 to this bit or rewrite data to SPDAT when SPBSY=0 will clear this flag.

BDh.4 **RCVOVF:** Receive Buffer Overrun Flag
Set by H/W at the end of a data transfer and RCVBF=1. Write 0 to this bit or read SPDAT register will clear this flag.

BDh.3 **RCVBF:** Receive Buffer Full Flag
Set by H/W at the end of a data transfer. Write 0 to this bit or read SPDAT register will clear this flag.

BDh.2 **SPBSY:** SPI Busy Flag (Read Only)
Set by H/W when a SPI transfer is in progress.

SFR **BEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPDAT	SPDAT							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

BEh.7~0 **SPDAT:** SPI Transmit and Receive Data
The SPDAT register is used to transmit and receive data. Writing data to SPDAT place the data into shift register and start a transfer when in Master mode. Reading SPDAT returns the contents of the receive buffer.

Note6: also refer to Section 6 for more information about SPI Interrupt enable and priority.

Note7: also refer to Section 7 for more information about SPI pins share with I/O pins

15. 6-bit SAR ADC

The 6-bit SAR ADC supports 7 channel analog inputs. To use the ADC, user only needs to select the ADC channel by setting ADCHS SFR. If ADCHS=0, The ADC stop converting and enters the power down mode. The ADC module uses 10 System clock cycles to make a conversion and launches next conversion immediately after the ADC convert result data latched. Lower System clock frequency may get more stable ADC performance. The ADC channel requires Mode3 pin setting to disable the pin's digital input path for power saving. User should not configure ADC and Touch Key channel on the same pin because of the channel input sensitivity issue.

SFR **C2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BGADCS	LVR2E	ADCHS			CMPVS			
R/W	R/W	R/W			R/W			
Reset	0	0	0	0	0	0	0	0

C2h.6~4 **ADCHS:** ADC channel select
000: ADC disable
001: AD1 (P1.1)
010: AD2 (P1.2)
011: AD3 (P1.3)
100: AD4 (P1.4)
101: AD5 (P1.5)
110: AD6 (P1.6)
111: AD7 (P1.7)

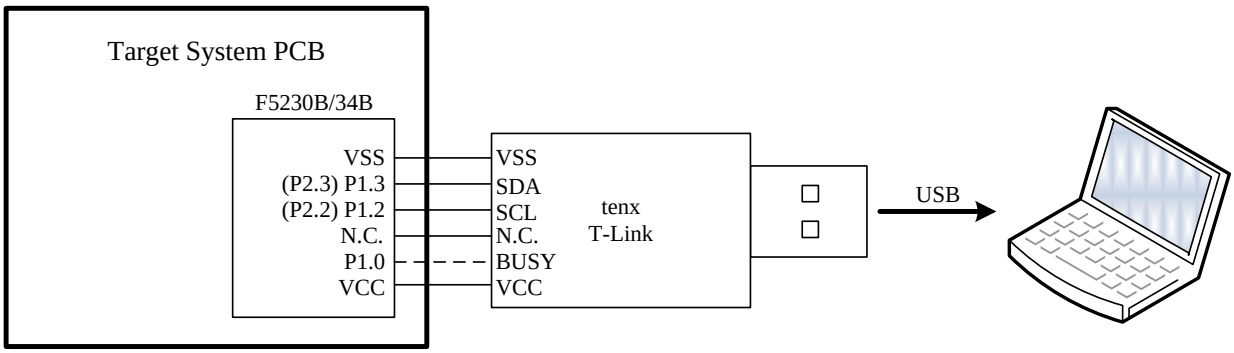
SFR **C3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BGADCD	CMPO	–	ADCDT					
R/W	R	–	R					
Reset	–	–	–	–	–	–	–	–

C3h.5~0 **ADCDT:** ADC convert data result

16. In Circuit Emulation (ICE) Mode

The **F2230B/34B** can support the In Circuit Emulation mode. To use the ICE Mode, user just needs to connect P1.2 and P1.3 pin to the tenx proprietary EV module. The benefit is that user can emulate the whole system without changing the on board target device. But there are some limits for the ICE mode as below.

1. The device must be un-protect.
2. The device's P1.2 and P1.3 pins must work in input Mode (P1MOD2=0/1 and P1MOD3=0/1).
3. During Program Code download, P1.0 sent acknowledge signal to T-Link unit. After download stage, P1.0 can be emulated as any other pins.
4. The Program ROM's addressing space 3D00h~3FFFh and 0033h~003Ah are occupied by tenx EV Module. So user Program cannot access these spaces.
5. The P1.2 and P1.3 pin's function cannot be emulated.
6. The P1.2 and P1.3 pin's can be replaced by P2.2 and P2.3.
7. The V_{DD} level and VCON SFR are controlled by T-Link module.



ICE Mode Connection

SFR & CFGW MAP

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	1111-1111	**P0**	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	**SP**	SP							
82h	0000-0000	**DPL**	DPL							
83h	0000-0000	**DPH**	DPH							
87h	0xxx-0000	**PCON**	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	**TMOD**	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	**TL0**	TL0							
8Bh	0000-0000	**TL1**	TL1							
8Ch	0000-0000	**TH0**	TH0							
8Dh	0000-0000	**TH1**	TH1							
90h	1111-1111	**P1**	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
91h	0000-0000	**P0OE**	P0OE							
93h	x000-0000	**P2OE**	–	P2OE						
94h	1100-0001	**OPTION**	SXTGAIN		STPPCK	PWRFLT	UART1W	WDTPSC	TM3PSC	
95h	xxxx-0000	**INTFLG**	–	–	–	–	TKIF	IE2	P1IF	TF3
96h	0000-0000	**P1WKUP**	P1WKUP							
97h	xxxx-xxx0	**SWCMD**	IAPALL / SWRST							
98h	0000-0000	**SCON**	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	**SBUF**	SBUF							
9Ch	1111-1111	**PWMPRD**	PWMPRD							
9Dh	1000-0000	**PWMDH**	PWMDH							
A0h	1111-1111	**P2**	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
A1h	1000-xxxx	**PWMCON**	PWMCKS		PWMDL		–	–	–	–
A2h	0000-0000	**P1MODL**	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
A3h	0000-0000	**P1MODH**	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
A4h	0000-0000	**P3MODL**	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
A5h	0000-0000	**P3MODH**	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
A6h	0000-0000	**TOCON**	T1OCON		T2OCON			TCOCON		
A7h	x111-1111	**VCON**	–	LDOE	VSET2			VSET1		
A8h	0x00-0000	**IE**	EA	–	ET2	ES	ET1	EX1	ET0	EX0
A9h	0000-0000	**INTE1**	IAPWE			SPIE	TKIE	EX2	P1IE	TM3IE
ABh	xxxx-xxxx	**ATKDT**	TKEOC	TKOVF	TKDH		ATKDT			
ACh	xxxx-xxxx	**TKDL**	TKDL							
ADh	1100-1111	**TKCON**	TKPD	TKTMR			TKCHS			
AEh	xxxx-0011	**TKCON2**	–	–	–	–	TKAUTO	ATKRATE	ATKNUM	
AFh	0000-1100	**RFCON**	P0RFC		T0SEL		RFCPSC		RFCS	
B0h	1111-1111	**P3**	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
B3h	xxxx-xxxx	**TM3SEC**	TM3SEC							
B4h	xxxx-xxxx	**TM3DL**	TM3DL							
B5h	xxxx-xxxx	**TM3DH**	–	TM3DH						
B6h	0000-0000	**TM3RLD**	TM3RLD							
B7h	0000-0000	**TM3ADJ**	TM3ADJS	TM3ADJ						
B8h	xx00-0000	**IP**	–	–	PT2	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	**IPH**	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
BAh	xxx0-0000	**IP1**	–	–	–	PSPI	PTKI	PX2	PP1	PT3

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BBh	xxx0-0000	**IP1H**	–	–	–	PSPIH	PTKIH	PX2H	PP1H	PT3H
BCh	0000-x000	**SPCON**	SPEN	MSTR	CPOL	CPHA	–	LSBF	SPCR	
BDh	00x0-0xxx	**SPSTA**	SPIF	WCOL	–	RCVOVF	RCVBF	SPBSY	–	–
BEh	0000-0000	**SPDAT**	SPDAT							
BFh	000x-xxxx	**PINMODE**	I80EN	I80POL	PWMOE	–	–	–	–	–
C2h	0000-0000	**BGADCS**	LVR2E	ADCHS			CMPVS			
C3h	xxxx-xxxx	**BGADCD**	CMPO	–	ADCDT					
C4h	0100-0000	**ATKCMP0**	ATKCMP0							
C5h	0100-0000	**ATKCMP1**	ATKCMP1							
C6h	0100-0000	**ATKCMP2**	ATKCMP2							
C7h	0100-0000	**ATKCMP3**	ATKCMP3							
C8h	0000-0000	**T2CON**	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
CAh	0000-0000	**RCP2L**	RCP2L							
CBh	0000-0000	**RCP2H**	RCP2H							
CCh	0000-0000	**TL2**	TL2							
CDh	0000-0000	**TH2**	TH2							
D0h	0000-0000	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
D8h	0000-0101	**CLKCON**	FCKTYPE	FSUBSEL	SELFCK	SCKTYPE	STPFSUB	CLKPSC		
E0h	0000-0000	**ACC**	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
F0h	0000-0000	**B**	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F7h	xxxx-xxxx	**CFGWL**	–	–	–	FRCF				
F8h	xxx0-0000	**AUX1**	–	–	–	TKSOC	CLRWDT	CLRTM3	STPRFC	DPSEL

Flash Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7FFEh	**CFGWL**	–	–	–	FRCF				
7FFFh	**CFGWH**	PROT	XRSTE	MVCLOCK	WDTE	–	–	LVR1E	–

SFR & CFGW DESCRIPTION

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
80h	**P0**	7~0	P0	R/W	FFh	Port0 data, also controls the P0.n pin's pull-up function. If the P0.n SFR data is "1" and the corresponding P0OE.n=0 (input mode), the pull-up is enabled.
81h	**SP**	7~0	SP	R/W	07h	Stack Point
82h	**DPL**	7~0	DPL	R/W	00h	Data Point low byte
83h	**DPH**	7~0	DPH	R/W	00h	Data Point high byte
87h	**PCON**	7	SMOD	R/W	0	Set 1 to enable UART double baud rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit
		1	PD	R/W	0	Power down control bit, set 1 to enter STOP mode
		0	IDL	R/W	0	Idle control bit, set 1 to enter IDLE mode
88h	**TCON**	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control. 1: timer runs; 0: timer stops
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control. 1:timer runs; 0:timer stops
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin
89h	**TMOD**	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin's negative edge
		5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	**TL0**	7~0	TL0	R/W	00h	Timer0 data low byte

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
8Bh	**TL1**	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	**TH0**	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	**TH1**	7~0	TH1	R/W	00h	Timer1 data high byte
90h	**P1**	7~0	P1	R/W	FFh	Port1 data
91h	**P0OE**	7~0	P0OE	R/W	00h	Port0 CMOS Push-Pull output enable control, 1=Enable.
93h	**P2OE**	6~0	P2OE	R/W	00h	P2.6~P2.0 pin CMOS Push-Pull output enable control, 1=Enable.
94h	**OPTION**	7~6	SXTGAIN	R/W	11	SXT oscillator gain 0=Lowest gain, 3=Highest Gain
		5	STPPCK	R/W	0	Set 1 to stop UART/Timer0/1/2 clock in Idle mode for current reducing.
		4	PWRFLT	R/W	0	Set 1 to enhance the chip's power noise immunity
		3	UART1W	R/W	0	Set 1 to enable one wire UART mode, both TXD/RXD use P3.1 pin.
		2	WDTPSC	R/W	0	WDT Prescaler 0: WDT overflow at 65536 System clock count 1: WDT overflow at 32768 System clock count
		1~0	TM3PSC	R/W	01	Timer3 Interrupt rate 00: Timer3 interrupt occurs when 23 bit count data overflow 01: Timer3 interrupt rate is 32768 Slow clock cycles (1.0 second for SXT) 10: Timer3 interrupt rate is 16384 Slow clock cycles (0.5 second for SXT) 11: Timer3 interrupt rate is 8192 Slow clock cycles (0.25 second for SXT)
95h	**INTFLG**	3	TKIF	R/W	0	Touch Key Interrupt Flag (for H/W ATK Mode) Set by H/W when a TK channel's touch event is detected. It is cleared automatically when the program performs the interrupt service routine. S/W can write F7h to INTFLG to clear this bit.
		2	IE2	R/W	0	External Interrupt 2 (INT2 pin) edge flag Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine. S/W can write FBh to INTFLG to clear this bit.
		1	P1IF	R/W	0	Port1 pin change Interrupt flag Set by H/W when a Port1 pin state change is detected and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting. It is cleared automatically when the program performs the interrupt service routine. S/W can write FDh to INTFLG to clear this bit.
		0	TF3	R/W	0	Timer3 Interrupt Flag Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.
96h	**P1WKUP**	7~0	P1WKUP	R/W	00h	P1.7~P1.0 pin individual Wake-up / Interrupt enable control 0: Disable; 1: Enable.
97h	**SWCMD**	7~0	SWRST	W	–	Write 56h to generate S/W Reset
		7~0	IAPALL	W	–	Write 65h to set IAPALL flag; Write other value to clear IAPALL flag. It is recommended to clear it immediately after IAP access.
		0	IAPALL	R	0	Flag indicates whole Flash can be access by IAP or not

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
98h	**SCON**	7	SM0	R/W	0	Serial port mode select bit 0, 1 (SM0, SM1) = 00: Mode0: 8 bit shift register, Baud Rate = $F_{SYSCLK}/2$ 01: Mode1: 8 bit UART, Baud Rate is variable 10: Mode2: 9 bit UART, Baud Rate=$F_{SYSCLK}/32$ or/64 11: Mode3: 9 bit UART, Baud Rate is variable
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	Set 1 to enable UART Reception
		3	TB8	R/W	0	Transmitter bit 8, ninth bit to transmit in Modes 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0
		1	TI	R/W	0	Transmit Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W
		0	RI	R/W	0	Receive Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.
99h	**SBUF**	7~0	SBUF	R/W	–	UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
9Ch	**PWMPRD**	7~0	PWMPRD	R/W	FFh	PWM 8-bit period register
9Dh	**PWMDH**	7~0	PWMDH	R/W	80h	bits 9~2 of the PWM 10-bit duty register
A0h	**P2**	7	P2.7	R/W	1	P2.7 data 0: Open Drain output low 1: Schmitt-trigger input with pull up
		6~0	P2.6~P2.0	R/W	7Fh	P2.6~P2.0 data, also controls the P2.n pin's pull-up function. If the P2.n SFR data is "1" and the corresponding P2OE.n=0 (input mode), the pull-up is enabled.
A1h	**PWMCON**	7~6	PWMCKS	R/W	10	PWM clock source 00: $F_{SYSCLK}/4$ 01: $F_{SYSCLK}/2$ 10: F_{SYSCLK} 11: FRCx2
		5~4	PWMDL	R/W	00	bits 1~0 of the PWM 10-bit duty register
A2h	**P1MODL**	7~6	P1MOD3	R/W	00	P1.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.3 is ADC input
		5~4	P1MOD2	R/W	00	P1.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.2 is ADC input
		3~2	P1MOD1	R/W	00	P1.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.1 is ADC input
		1~0	P1MOD0	R/W	00	P1.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.0 is T2O output
A3h	**P1MODH**	7~6	P1MOD7	R/W	00	P1.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.7 is ADC input
		5~4	P1MOD6	R/W	00	P1.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.6 is ADC input
		3~2	P1MOD5	R/W	00	P1.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.5 is ADC input
		1~0	P1MOD4	R/W	00	P1.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.4 is ADC input

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A4h	**P3MODL**	7~6	P3MOD3	R/W	00	P3.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
		5~4	P3MOD2	R/W	00	P3.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
		3~2	P3MOD1	R/W	00	P3.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
		1~0	P3MOD0	R/W	00	P3.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3
A5h	**P3MODH**	7~6	P3MOD7	R/W	00	P3.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.7 is TCO output
		5~4	P3MOD6	R/W	00	P3.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.6 is T1B output
		3~2	P3MOD5	R/W	00	P3.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.5 is T1O output
		1~0	P3MOD4	R/W	00	P3.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.4 is Touch Key charge collection (CLD)
A6h	**TOCON**	7~6	T1OCON	R/W	00	T1O pin duty and frequency control 00: 1/2 duty, 1/2 Timer1 overflow frequency 01: 1/3 duty, 1/3 Timer1 overflow frequency 10: 1/4 duty, 1/4 Timer1 overflow frequency
		5~3	T2OCON	R/W	000	T2O pin duty and frequency control 000: 1/2 duty, 1/2 Timer2 overflow frequency 001: 1/3 duty, 1/3 Timer2 overflow frequency 010: 1/4 duty, 1/4 Timer2 overflow frequency 101: 2/3 duty, 1/3 Timer2 overflow frequency 110: 3/4 duty, 1/4 Timer2 overflow frequency
		2~0	TCOCON	R/W	000	TCO pin duty and frequency control 000: 1/2 duty, 1/2 SYSCLK frequency 001: 1/3 duty, 1/3 SYSCLK frequency 010: 1/4 duty, 1/4 SYSCLK frequency 011: 1/4 duty, 1/2 SYSCLK frequency 100: 1/2 duty, 1/1 SYSCLK frequency 101: 2/3 duty, 1/3 SYSCLK frequency 110: 3/4 duty, 1/4 SYSCLK frequency 111: 3/4 duty, 1/2 SYSCLK frequency
A7h	**VCON**	6	LDOE	R/W	1	Chip internal LDO Regulator enable control 0: LDO disable, $V_{DD}=V_{BAT}$ 1: LDO enable, V_{DD}=LDO Regulator output
		5~3	VSET2	R/W	111	V_{DD} voltage setting in Fast/Slow mode while LDOE=1. 0xx: Don't select 100: $V_{DD}=V_{BAT}$*165/300 in Fast/Slow mode 101: $V_{DD}=V_{BAT}$*176/300 in Fast/Slow mode 110: $V_{DD}=V_{BAT}$*188/300 in Fast/Slow mode 111: $V_{DD}=V_{BG}$*2.75=1.2V*2.75=3.3V in Fast/Slow mode while V_{BAT}>3.3V.
		2~0	VSET1	R/W	111	V_{DD} voltage setting in Idle/Stop mode while LDOE=1. Definition is the same as VSET2.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A8h	**IE**	7	EA	R/W	0	Global interrupt enable control. 0: Disable all Interrupts. 1: Each interrupt is enabled or disabled by its own interrupt control bit.
		5	ET2	R/W	0	Set 1 to enable Timer2 interrupt
		4	ES	R/W	0	Set 1 to enable Serial Port (UART) Interrupt
		3	ET1	R/W	0	Set 1 to enable Timer1 Interrupt
		2	EX1	R/W	0	Set 1 to enable external INT1 pin Interrupt & Stop mode wake up capability
		1	ET0	R/W	0	Set 1 to enable Timer0 Interrupt
		0	EX0	R/W	0	Set 1 to enable external INT0 pin Interrupt & Stop mode wake up capability
A9h	**INTE1**	7~5	IAPWE	R/W	000	Set to 101 to enable IAP write for F2230B/34B, don't care for F2230/34. It is recommended to clear it immediately after IAP write.
		4	SPIE	R/W	0	Set 1 to enable SPI Interrupt
		3	TKIE	R/W	0	Set 1 to enable Touch Key Interrupt
		2	EX2	R/W	0	Set 1 to enable external INT2 pin Interrupt & Stop mode wake up capability
		1	P1IE	R/W	0	Set 1 to enable Port1 Pin Change Interrupt
		0	TM3IE	R/W	0	Set 1 to enable Timer3 Interrupt
ABh	**ATKDT**	7	TKEOC	R	–	Touch Key End of Conversion (for S/W Mode), TKEOC may have 3uS delay after TKSOC=1, so F/W must wait enough time before polling this Flag. 0: Indicates conversion is in progress 1: Indicates conversion is finished
		6	TKOVF	R	–	Touch Key Counter Overflow (for S/W Mode)
		5~4	TKDH	R	–	Touch Key Counter Data 9~8 (for S/W Mode)
		3~0	ATKDT	R	–	Touch Key Auto Scan Result (for H/W ATK Mode) xxx1: TK0 has a Touch event xx1x: TK1 has a Touch event x1xx: TK2 has a Touch event 1xxx: TK3 has a Touch event
ACh	**TKDL**	7~0	TKDL	R	–	Touch Key Counter Data 7~0 (for S/W Mode)
ADh	**TKCON**	7	TKPD	R/W	1	Touch Key Power Down (for S/W mode) 0: Touch Key enable; 1: Touch Key disable
		6~4	TKTMR	R/W	100	Touch Key Conversion Time (for both S/W and H/W ATK mode) 000: Conversion time shortest … 111: Conversion time longest
		3~0	TKCHS	R/W	1111	Touch Key Channel Select (for S/W Mode) 0000: TK0 (P1.7) 0001: TK1 (P1.6) 0010: TK2 (P1.5) 0011: TK3 (P1.4) 0100: TK4 (P1.3) 0101: TK5 (P1.2) 0110: TK6 (P1.1) 0111: TK7 (P1.0) 1000: TK8 (P3.7) 1001: TK9 (P3.6) 1010: TK10 (P3.5) 1011: TK11 (P3.3) 1100: TK12 (P3.2) 1101: TK13 (P3.1) 1110: TK14 (P3.0) 1111: Internal Reference Capacitor

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
AEh	**TKCON2**	3	TKAUTO	R/W	0	Touch Key Auto Scan Mode Enable 0: S/W Mode 1: H/W ATK Mode
		2	ATKRATE	R/W	0	Touch Key Scan Rate (for H/W ATK Mode) 0: ATK scan rate is 4096 Slow clock cycles (125ms if Slow clock is SXT) 1: ATK scan rate is 2048 Slow clock cycles (62ms if Slow clock is SXT)
		1~0	ATKNUM	R/W	11	Touch Key Auto Scan Channel Number (for H/W ATK Mode) 00: ATK only detect TK0 01: ATK detect TK0 and TK1 10: ATK detect TK0~TK2 11: ATK detect TK0~TK3
AFh	**RFCON**	7~6	P0RFC	R/W	00	P0.0~P0.3 pin RFC mode control. 00: P0.0~P0.3 are not RFC pins 01: P0.0 and P0.1 are RFC pins, P0.2 and P0.3 are not RFC pins 10: P0.0~P0.2 are RFC pins, P0.3 is not RFC pin 11: P0.0~P0.3 are RFC pins
		5~4	T0SEL	R/W	00	Timer0 Counter mode (CT0N=1) T0 input select 00: P3.4 pin (8051 standard) 01: RFC clock divided by 1/4/16/64 10: SXT clock 11: RFC clock divided by 1/4/16/64 gated by Timer2 overflow
		3~2	RFCPSC	R/W	11	RFC clock divider to Timer0 00: divided by 64 01: divided by 16 10: divided by 4 11: divided by 1
		1~0	RFCS	R/W	00	Select RFC convert channel. 00: RFC0R (P0.1) 01: RFC1R (P0.2) 10: RFC2R (P0.3)
B0h	**P3**	7~0	P3	R/W	FFh	Port 3 data
B3h	**TM3SEC**	7~0	TM3SEC	R	–	Timer3 count data bit 22~15
B4h	**TM3DL**	7~0	TM3DL	R	–	Timer3 count data bit 7~0
B5h	**TM3DH**	6~0	TM3DH	R	–	Timer3 count data bit 14~8
B6h	**TM3RLD**	7~0	TM3RLD	R/W	00h	Timer3 overflow reload data for Timer3 bit 22~15 (TM3SEC)
B7h	**TM3ADJ**	7	TM3ADJS	R/W	0	Timer3 adjustment sign 0: Timer3 positive adjust, to increase Timer3 counting rate 1: Timer3 negative adjust, to decrease Timer3 counting rate
		6~0	TM3ADJ	R/W	00h	Timer3 adjust magnitude, 0.477 ppm per LSB. The adjustment is calculated as ±TM3ADJ*0.477ppm. The total adjustable range is ± 61ppm.
B8h	**IP**	5	PT2	R/W	0	Timer2 Interrupt Priority Low bit
		4	PS	R/W	0	Serial Port (UART) Interrupt Priority Low bit
		3	PT1	R/W	0	Timer1 Interrupt Priority Low bit
		2	PX1	R/W	0	External INT1 Pin Interrupt Priority Low bit
		1	PT0	R/W	0	Timer0 Interrupt Priority Low bit
		0	PX0	R/W	0	External INT0 Pin Interrupt Priority Low bit
B9h	**IPH**	5	PT2H	R/W	0	Timer2 Interrupt Priority High bit
		4	PSH	R/W	0	Serial Port (UART) Interrupt Priority High bit
		3	PT1H	R/W	0	Timer1 Interrupt Priority High bit
		2	PX1H	R/W	0	External INT1 Pin Interrupt Priority High bit
		1	PT0H	R/W	0	Timer0 Interrupt Priority High bit
		0	PX0H	R/W	0	External INT0 Pin Interrupt Priority High bit
BAh	**IP1**	4	PSPI	R/W	0	SPI Interrupt Priority Low bit
		3	PTKI	R/W	0	Touch Key Interrupt Priority Low bit
		2	PX2	R/W	0	External INT2 Pin Interrupt Priority Low bit
		1	PP1	R/W	0	Port1 pin change Interrupt Priority Low bit
		0	PT3	R/W	0	Timer3 Interrupt Priority Low bit

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
BBh	**IP1H**	4	PSPIH	R/W	0	SPI Interrupt Priority High bit
		3	PTKIH	R/W	0	Touch Key Interrupt Priority High bit
		2	PX2H	R/W	0	External INT2 Pin Interrupt Priority High bit
		1	PP1H	R/W	0	Port1 Interrupt Priority High bit
		0	PT3H	R/W	0	Timer3 Interrupt Priority High bit
BCh	**SPCON**	7	SPEN	R/W	0	Set 1 to enable SPI & P2.4~P2.6 SPI pin function
		6	MSTR	R/W	0	SPI Master Mode Enable. 0: Slave Mode; 1: Master Mode
		5	CPOL	R/W	0	SPI Clock Polarity 0: SCK is low in idle state; 1: SCK is high in idle state
		4	CPHA	R/W	0	SPI Clock Phase 0: Data sampled on first edge of SCK period 1: Data sampled on second edge of SCK period
		2	LSBF	R/W	0	SPI LSB First. 0: MSB first; 1: LSB first
		1~0	SPCR	R/W	00	SPI Clock Rate. 00: F_{SYSCLK}/2; 01: F_{SYSCLK}/4; 10: F_{SYSCLK}/8; 11: F_{SYSCLK}/16
BDh	**SPSTA**	7	SPIF	R/W	0	SPI Interrupt Flag Set by H/W at the end of a data transfer. Cleared by H/W when interrupt is vectored into. Write 0 to this bit will clear this flag.
		6	WCOL	R/W	0	Write Collision Interrupt Flag Set by H/W if write data to SPDAT when SPBSY=1. Write 0 to this bit or rewrite data to SPDAT when SPBSY=0 will clear this flag.
		4	RCVOVF	R/W	0	Receive Buffer Overrun Flag Set by H/W at the end of a data transfer and RCVBF=1. Write 0 to this bit or read SPDAT register will clear this flag.
		3	RCVBF	R/W	0	Receive Buffer Full Flag Set by H/W at the end of a data transfer. Write 0 to this bit or read SPDAT register will clear this flag.
		2	SPBSY	R	–	SPI Busy Flag (Read Only) Set by H/W when a SPI transfer is in progress.
BEh	**SPDAT**	7~0	SPDAT	R/W	00h	SPI Transmit and Receive Data The SPDAT register is used to transmit and receive data. Writing data to SPDAT place the data into shift register and start a transfer when in Master mode. Reading SPDAT returns the contents of the receive buffer.
BFh	**PINMODE**	7	I80EN	R/W	0	I80 interface enable. 0: Disable 1: Enable; Port0, P3.6 and P3.7 are I80 functional pin
		6	I80POL	R/W	0	The polarity of RD/WR signal 0: RD/WR are low active 1: RD/WR are high active
		5	PWMOE	R/W	0	PWM signal output enable 0: Disable PWM signal output to P1.3 1: Enable PWM signal output to P1.3

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
C2h	**BGADCS**	7	LVR2E	R/W	0	Low Voltage Reset #2 enable, 1=enable. This bit must be set to 1 after the CMPVS setting done and the Bandgap voltage stable.
		6~4	ADCHS	R/W	000	ADC channel select 000: ADC disable; 001: AD1 (P1.1); 010: AD2 (P1.2); 011: AD3 (P1.3); 100: AD4 (P1.4); 101: AD5 (P1.5); 110: AD6 (P1.6); 111: AD7 (P1.7)
		3~0	CMPVS	R/W	0000	Select V_{BAT} resistor divider for Comparator input to compare with the 1.2V Bandgap reference voltage. If LVR2E=1, the Low Voltage Reset #2 is triggered when V_{BAT} resistor divider is lower than 1.2V (CMPO=0). 0000: Comparator Disable 0001: the Comparator input is V_{BAT}*12/24, LVR2=2.4V 0010: the Comparator input is V_{BAT}*12/25, LVR2=2.5V 0011: the Comparator input is V_{BAT}*12/26, LVR2=2.6V 0100: the Comparator input is V_{BAT}*12/27, LVR2=2.7V 0101: the Comparator input is V_{BAT}*12/28, LVR2=2.8V 0110: the Comparator input is V_{BAT}*12/29, LVR2=2.9V 0111: the Comparator input is V_{BAT}*12/30, LVR2=3.0V 1000: the Comparator input is V_{BAT}*12/31, LVR2=3.1V 1001: the Comparator input is V_{BAT}*12/33, LVR2=3.3V 1010: the Comparator input is V_{BAT}*12/35, LVR2=3.5V 1011: the Comparator input is V_{BAT}*12/37, LVR2=3.7V 1100: the Comparator input is V_{BAT}*12/39, LVR2=3.9V 1101: the Comparator input is V_{BAT}*12/41, LVR2=4.1V 1110: the Comparator input is V_{BAT}*12/43, LVR2=4.3V 1111: the Comparator input is V_{BAT}*12/45, LVR2=4.5V
C3h	**BGADCD**	7	CMPO	R	–	Compare result of BandGap voltage and V_{BAT} voltage divider. CMPO=1 means the V_{BAT} divider voltage is higher. If LVR2E=1, the CMPO=0 can trigger LVR2.
		5~0	ADCDT	R	–	ADC convert data result
C4h	**ATKCMP0**	7~0	ATKCMP0	R/W	40h	Data Threshold Compared with TK0 scan (for H/W ATK Mode)
C5h	**ATKCMP1**	7~0	ATKCMP1	R/W	40h	Data Threshold Compared with TK1 scan (for H/W ATK Mode)
C6h	**ATKCMP2**	7~0	ATKCMP2	R/W	40h	Data Threshold Compared with TK2 scan (for H/W ATK Mode)
C7h	**ATKCMP3**	7~0	ATKCMP3	R/W	40h	Data Threshold Compared with TK3 scan (for H/W ATK Mode)
C8h	**T2CON**	7	TF2	R/W	0	Timer2 overflow flag Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
		6	EXF2	R/W	0	T2EX interrupt pin falling edge flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
		5	RCLK	R/W	0	UART receive clock control bit 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3
		4	TCLK	R/W	0	UART transmit clock control bit 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
		3	EXEN2	R/W	0	T2EX pin enable 0: T2EX pin disable 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0
		2	TR2	R/W	0	Timer2 run control. 1:timer runs; 0:timer stops
		1	CT2N	R/W	0	Timer2 Counter/Timer select bit 0: Timer mode, Timer2 data increases at 2 System clock cycle rate 1: Counter mode, Timer2 data increases at T2 pin's negative edge
		0	CPRL2N	R/W	0	Timer2 Capture/Reload control bit 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1. 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1. If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.
CAh	**RCP2L**	7~0	RCP2L	R/W	00h	Timer2 reload/capture data low byte

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
CBh	**RCP2H**	7~0	RCP2H	R/W	00h	Timer2 reload/capture data high byte
CCh	**TL2**	7~0	TL2	R/W	00h	Timer2 data low byte
CDh	**TH2**	7~0	TH2	R/W	00h	Timer2 data high byte
D0h	**PSW**	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	Register Bank Select bit 1
		3	RS0	R/W	0	Register Bank Select bit 0
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag
D8h	**CLKCON**	7	FCKTYPE	R/W	0	Fast clock select, This bit can be changed only in Slow mode (SELFCK=0) 0: Fast clock is FSUBCLK (FRC or FXT) 1: Fast clock is RFC, S/W must setup RFC circuitry before set this bit to 1
		6	FSUBSEL	R/W	0	FSUBCLK select, This bit can be changed only in Slow mode (SELFCK=0). 0: FSUBCLK is FRC 1: FSUBCLK is FXT, P2.2 and P2.3 are crystal oscillator pins
		5	SELFCK	R/W	0	System clock select. This bit can be changed only when STPFSUB=0 or FCKTYPE=1. 0: Slow clock (SRC/SXT) 1: Fast clock (FRC/FXT/RFC)
		4	SCKTYPE	R/W	0	Slow clock Type. This bit can be changed only in Fast mode (SELFCK=1). 0: SRC 1: SXT, P2.0 and P2.1 are crystal oscillator pins
		3	STPFSUB	R/W	0	Set 1 to stop FXT/FRC for power saving in Slow/Idle mode. This bit can be changed only in Slow mode or RFC mode.
		2~0	CLKPSC	R/W	101	System clock prescaler. 000: System clock is Fast/Slow clock divided by 32 001: System clock is Fast/Slow clock divided by 16 010: System clock is Fast/Slow clock divided by 8 011: System clock is Fast/Slow clock divided by 4 100: System clock is Fast/Slow clock divided by 2 101: System clock is Fast/Slow clock divided by 1
E0h	**ACC**	7~0	ACC	R/W	00h	Accumulator
F0h	**B**	7~0	B	R/W	00h	B register
F7h	**CFGWL**	4~0	FRCF	R/W	–	FRC frequency adjustment 00h=central frequency; 0Fh=highest frequency; 10h=lowest frequency
F8h	**AUX1**	4	TKSOC	R/W	0	Rising edge of this bit will trigger a Touch Key conversion (for S/W Mode). Basically, this bit is automatically cleared by H/W after end of conversion. However, if the SYSCLK is too slow, H/W might fail to clear TKSOC due to clock sampling rate issue.
		3	CLRWDT	R/W	0	Set to 1 to clear Watch Dog Timer
		2	CLRTM3	R/W	0	Set 1 to Clear Timer3 and force TM3SEC reload
		1	STPRFC	R/W	0	Set 1 to stop RFC clock oscillating
		0	DPSEL	R/W	0	Active DPTR Select

Adr	Flash	Bit#	Bit Name	Description
7FFEh	**CFGWL**	4~0	FRCF	FRC frequency adjustment. FRC is trimmed to 7.3728 MHz in chip manufacturing. FRCF records the adjustment data.
7FFFh	**CFGWH**	7	PROT	Flash Code Protect, 1=Protect
		6	XRSTE	Pin Reset enable, 1=enable.
		5	MVCLOCK	If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.
		4	WDTE	WDT Reset enable, 1=enable.
		1	LVR1E	Low Voltage Reset #1 enable, 1=enable.

INSTRUCTION SET

Instructions are 1, 2 or 3 bytes long as listed in the 'byte' column below. Each instruction takes 1~8 System clock cycles to execute as listed in the 'cycle' column below.

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ADD A,Rn	Add register to A	1	2	28-2F
ADD A,dir	Add direct byte to A	2	2	25
ADD A,@Ri	Add indirect memory to A	1	2	26-27
ADD A,#data	Add immediate to A	2	2	24
ADDC A,Rn	Add register to A with carry	1	2	38-3F
ADDC A,dir	Add direct byte to A with carry	2	2	35
ADDC A,@Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A,#data	Add immediate to A with carry	2	2	34
SUBB A,Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	2	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8	A4
DIV AB	Divide A by B	1	8	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ANL A,Rn	AND register to A	1	2	58-5F
ANL A,dir	AND direct byte to A	2	2	55
ANL A,@Ri	AND indirect memory to A	1	2	56-57
ANL A,#data	AND immediate to A	2	2	54
ANL dir,A	AND A to direct byte	2	2	52
ANL dir,#data	AND immediate to direct byte	3	4	53
ORL A,Rn	OR register to A	1	2	48-4F
ORL A,dir	OR direct byte to A	2	2	45
ORL A,@Ri	OR indirect memory to A	1	2	46-47
ORL A,#data	OR immediate to A	2	2	44
ORL dir,A	OR A to direct byte	2	2	42
ORL dir,#data	OR immediate to direct byte	3	4	43
XRL A,Rn	Exclusive-OR register to A	1	2	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A,#data	Exclusive-OR immediate to A	2	2	64
XRL dir,A	Exclusive-OR A to direct byte	2	2	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
SWAP A	Swap Nibbles of A	1	2	C4
RL A	Rotate A left	1	2	23
RLC A	Rotate A left through carry	1	2	33
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MOV A,Rn	Move register to A	1	2	E8-EF
MOV A,dir	Move direct byte to A	2	2	E5
MOV A,@Ri	Move indirect memory to A	1	2	E6-E7
MOV A,#data	Move immediate to A	2	2	74
MOV Rn,A	Move A to register	1	2	F8-FF
MOV Rn,dir	Move direct byte to register	2	4	A8-AF
MOV Rn,#data	Move immediate to register	2	2	78-7F
MOV dir,A	Move A to direct byte	2	2	F5
MOV dir,Rn	Move register to direct byte	2	4	88-8F
MOV dir,dir	Move direct byte to direct byte	3	4	85
MOV dir,@Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir,#data	Move immediate to direct byte	3	4	75
MOV @Ri,A	Move A to indirect memory	1	2	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	2	76-77
MOV DPTR,#data	Move immediate to data pointer	3	4	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4	93
MOVC A,@A+PC	Move code byte relative PC to A	1	4	83
MOVX A,@Ri	Move external data(A8) to A	1	4	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	4	E0
MOVX @Ri,A	Move A to external data(A8)	1	4	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	4	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A,Rn	Exchange A and register	1	2	C8-CF
XCH A,dir	Exchange A and direct byte	2	2	C5
XCH A,@Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C,bit	AND direct bit to carry	2	4	82
ANL C,/bit	AND direct bit inverse to carry	2	4	B0
ORL C,bit	OR direct bit to carry	2	4	72
ORL C,/bit	OR direct bit inverse to carry	2	4	A0
MOV C,bit	Move direct bit to carry	2	2	A2
MOV bit,C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ACALL addr 11	Absolute jump to subroutine	2	4	11-F1
LCALL addr 16	Long jump to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	4	01-E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	4	80
JC rel	Jump on carry=1	2	4	40
JNC rel	Jump on carry=0	2	4	50
JB bit,rel	Jump on direct bit=1	3	4	20
JNB bit,rel	Jump on direct bit=0	3	4	30
JBC bit,rel	Jump on direct bit=1 and clear	3	4	10
JMP @A+DPTR	Jump indirect relative DPTR	1	4	73
JZ rel	Jump on accumulator=0	2	4	60
JNZ rel	Jump on accumulator≠0	2	4	70
CJNE A,dir,rel	Compare A,direct, jump not equal relative	3	4	B5
CJNE A,#data,rel	Compare A,immediate, jump not equal relative	3	4	B4
CJNE Rn,#data,rel	Compare register,immediate, jump not equal relative	3	4	B8-BF
CJNE @Ri,#data,rel	Compare indirect,immediate, jump not equal relative	3	4	B6-B7
DJNZ Rn,rel	Decrement register, jump not zero relative	2	4	D8-DF
DJNZ dir,rel	Decrement direct byte, jump not zero relative	3	4	D5

MISCELLANEOUS				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply voltage	V_{SS} –0.3 ~ V_{SS} +5.5	V
Input voltage	V_{SS} –0.3 ~ V_{BAT} +0.3	
Output voltage	V_{SS} –0.3 ~ V_{BAT} +0.3	
Output current high per 1 pin	–20	mA
Output current high per all pins	–50	
Output current low per 1 pin	+30	
Output current low per all pins	+100	
Maximum Operating Voltage	5.5	V
Operating temperature	–40 ~ +85	℃
Storage temperature	–65 ~ +150	

DC Characteristics (T_A=25℃)

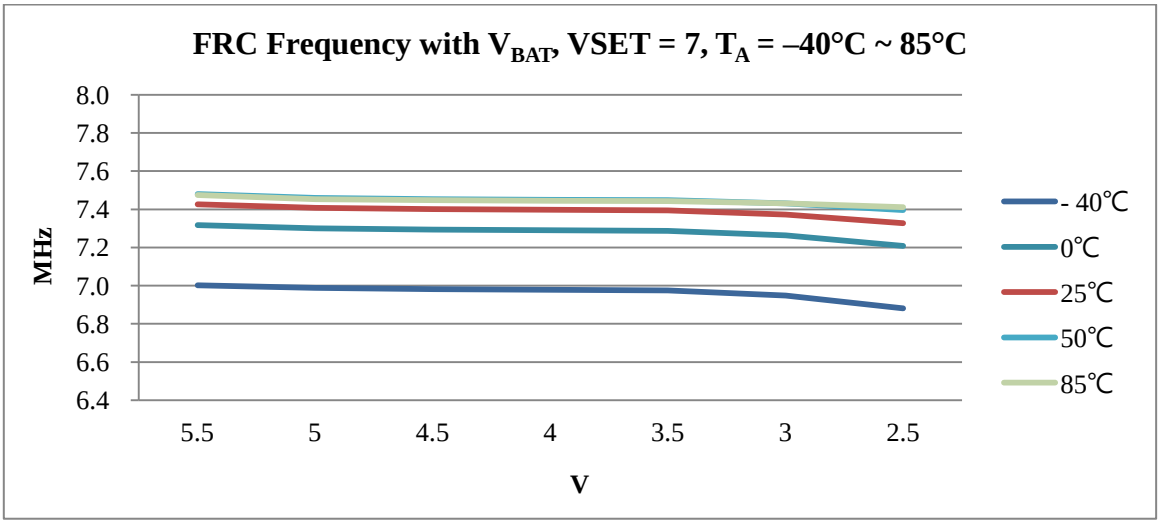
Parameter	Sym	Conditions		Min	Typ	Max	Unit
Input High Voltage	V_{IH}	all except P2.7	V_{BAT}=3V	0.6V_{BAT}	–	–	V
		P2.7	V_{BAT}=3V	0.8V_{BAT}	–	–	
Input Low Voltage	V_{IL}	all Input	V_{BAT}=3V	–	–	0.2V_{BAT}	
I/O Port Source Current	I_{OH}	all except P2.7	V_{BAT}=3V V_{OH}=2.7V	2	4	–	mA
			V_{BAT}=5V V_{OH}=4.5V	5	10	–	
I/O Port Sink Current	I_{OL}	all	V_{BAT}=3V V_{OL}=0.3V	6	12	–	
		all	V_{BAT}=5V V_{OL}=0.5V	12	24	–	
Input Leakage Current (pin high)	I_{ILH}	all Input	V_{IN}=V_{BAT}	–	–	1	uA
Input Leakage Current (pin low)	I_{ILL}		Vin=0V	–	–	–1	
Power Supply Current	I_{BAT}	FRC, 7.37 MHz	V_{BAT}=5V V_{DD}=3.3V	–	3.3	–	mA
		FXT, 8 MHz		–	3.9	–	
		SRC, 40 KHz	V_{BAT}=3V V_{DD}=1.5V ATK On LVR1 On	–	4	–	uA
		SXT, 32 KHz		–	6.1	–	
		Idle, 32 KHz		–	1.8	–	
		Idle, 2 KHz		–	1.3	–	
		Idle, 32 KHz	V_{BAT}=3V V_{DD}=1.5V ATK Off LVR1 On	–	1.4	–	
		Idle, 2 KHz		–	0.9	–	
		Stop		–	0.4	–	
System Clock Frequency	F_{SYSCLK}	2.8V<V_{DD}<4.0V		–	–	7.37	MHz
		2.0V<V_{DD}<4.0V		–	–	3.7	
Pull-Up Resistor	R_{PU}	all except P2.7	V_{BAT}=3V V_{IN}=0V	–	420	–	KΩ
		P2.7		–	270	–	

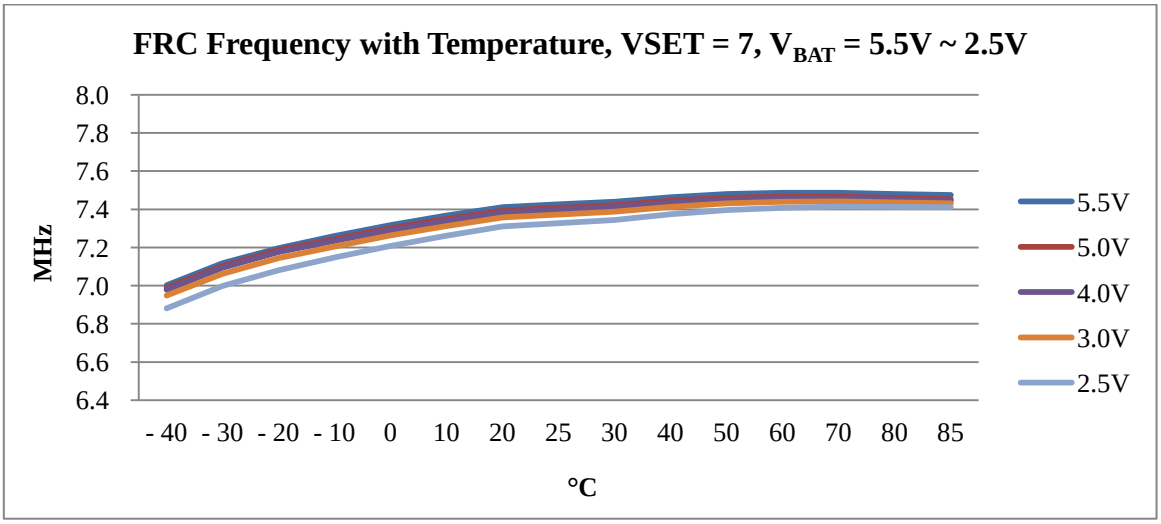
BandGap Reference Voltage

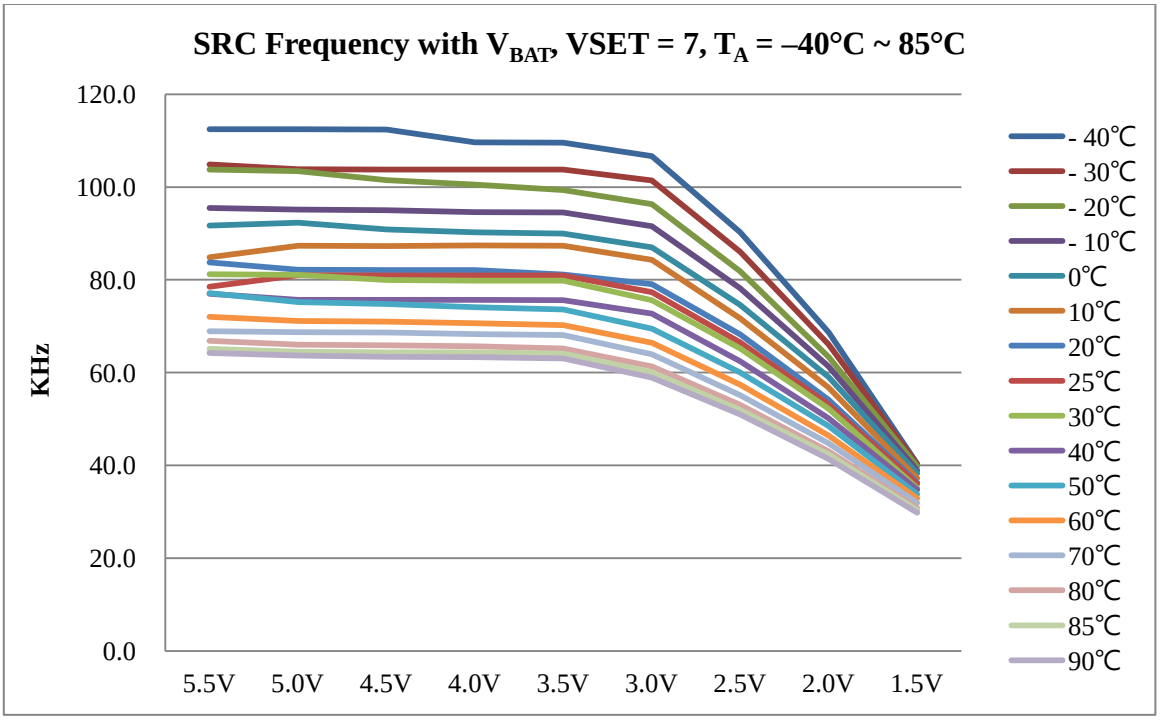
Parameter	Sym	Conditions	Min	Typ	Max	Unit
BandGap Voltage	V_{BG}	V_{BAT}=3V, 25℃	1.14	1.2	1.26	V
		V_{BAT}=3V, –40℃~85℃	1.12	1.2	1.28	
		V_{BAT}=5V, 25℃	1.18	1.25	1.33	
		V_{BAT}=5V, –40℃~85℃	1.16	1.25	1.35	

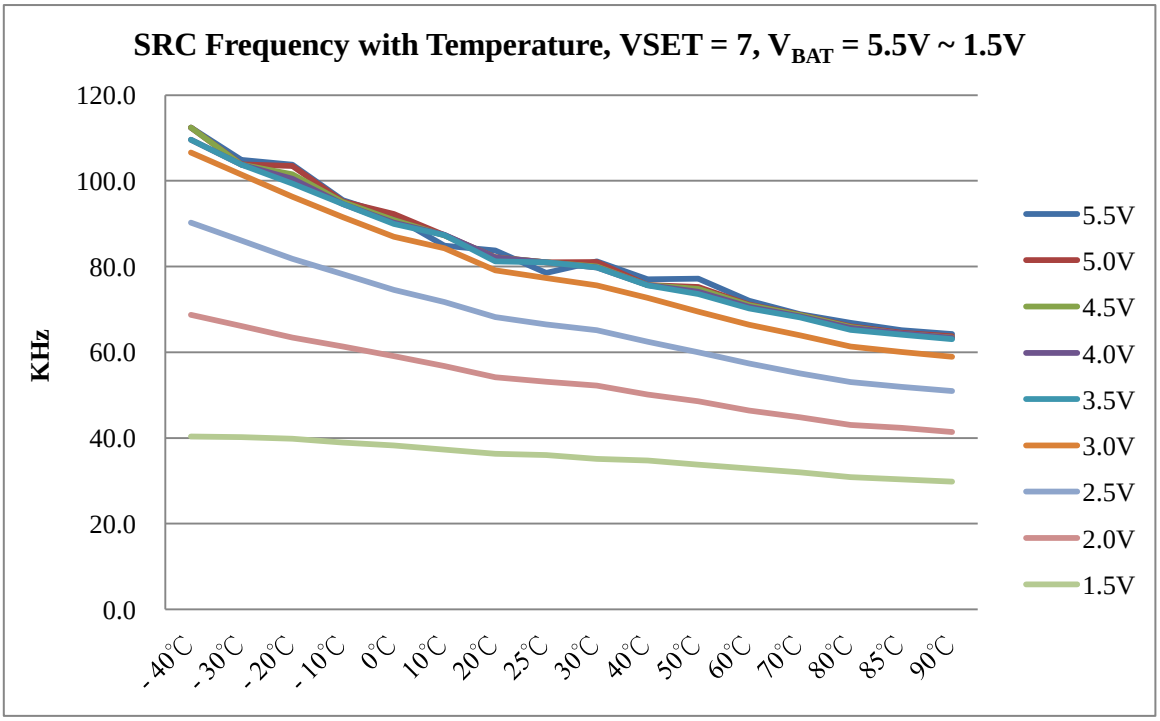
Clock Timing (T_A=25℃)

Parameter	Sym	Conditions		Min	Typ	Max	Unit
FRC Clock Frequency	F_{FRC}	VSET=7	V_{BAT}=5V ,V_{DD}=3.3V	–	7.38	–	MHz
			V_{BAT}=3V,V_{DD}=3V	–	7.37	–	
			V_{BAT}=2.5V,V_{DD}=2.5V	–	7.33	–	
SRC Clock Frequency	F_{SRC}	V_{DD}=3V		–	80	–	KHz
		V_{DD}=1.5V		–	40	–	



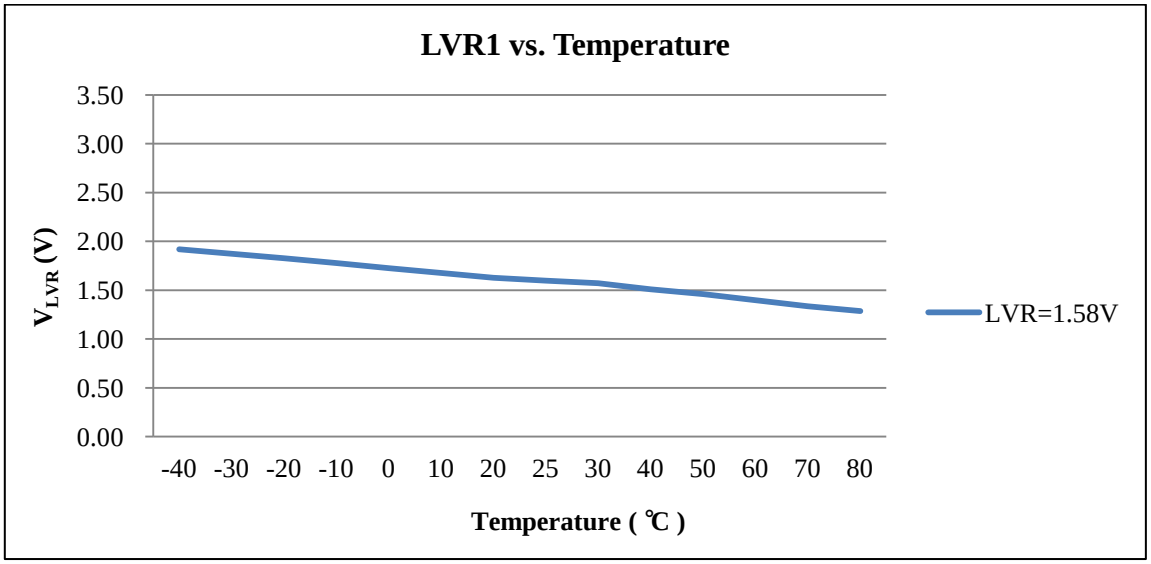



SRC Frequency with V_{BAT}, VSET = 7, T_A = –40°C ~ 85°C
KHz
120.0
100.0
80.0
60.0
40.0
20.0
0.0
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
- 40℃
- 30℃
- 20℃
- 10℃
0℃
10℃
20℃
25℃
30℃
40℃
50℃
60℃
70℃
80℃
85℃
90℃

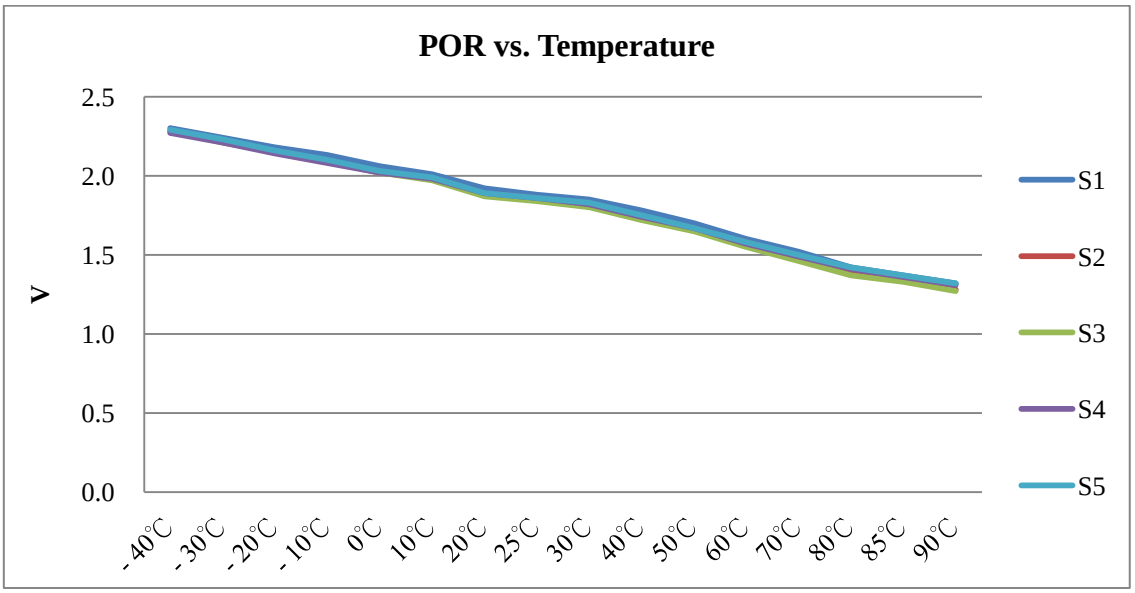

SRC Frequency with Temperature, VSET = 7, V_{BAT} = 5.5V ~ 1.5V
KHz
120.0
100.0
80.0
60.0
40.0
20.0
0.0
- 40℃
- 30℃
- 20℃
- 10℃
0℃
10℃
20℃
25℃
30℃
40℃
50℃
60℃
70℃
80℃
85℃
90℃
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V

LVR1/POR Level

Parameter	Sym	Conditions	Min	Typ	Max	Unit
LVR1 Voltage Level	V_{LVR}	25℃	1.43	1.58	1.75	V
Power On Reset Voltage	V_{POR}	25℃	1.6	1.8	2.0	V



LVR1 with Temperature, T_A= –40℃~80℃



POR with Temperature (Power on Reset needs V_{BAT}>V_{POR})

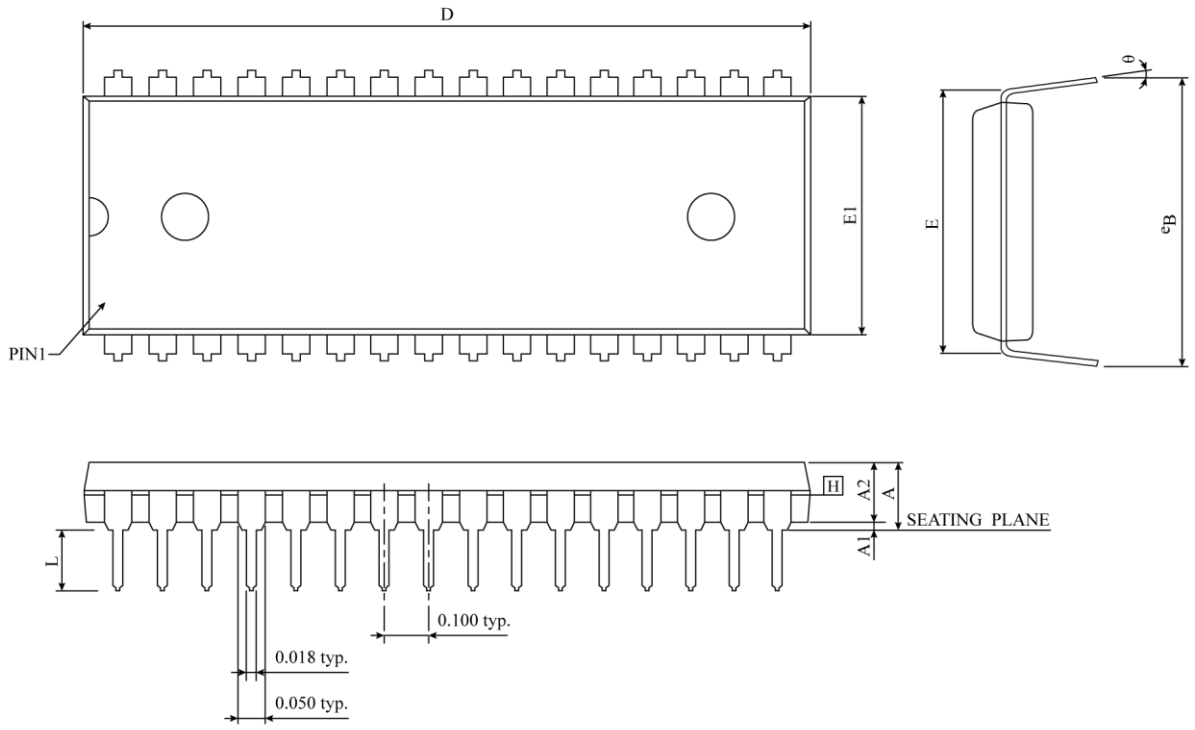
PACKAGE INFORMATION

Ordering Information

Ordering Number	Package
TM52F2230B-MTP	Wafer/Dice blank chip
TM52F2230B-COD	Wafer/Dice with code
TM52F2230B-MTP-09	DIP 32-pin (600 mil)
TM52F2230B-MTP-24	SOP 32-pin (300 mil)
TM52F2230B-MTP-98	QFN 32-pin (5x5x0.75-0.5mm)
TM52F2234B-MTP	Wafer/Dice blank chip
TM52F2234B-COD	Wafer/Dice with code
TM52F2234B-MTP-09	DIP 32-pin (600 mil)
TM52F2234B-MTP-24	SOP 32-pin (300 mil)
TM52F2234B-MTP-98	QFN 32-pin (5x5x0.75-0.5mm)

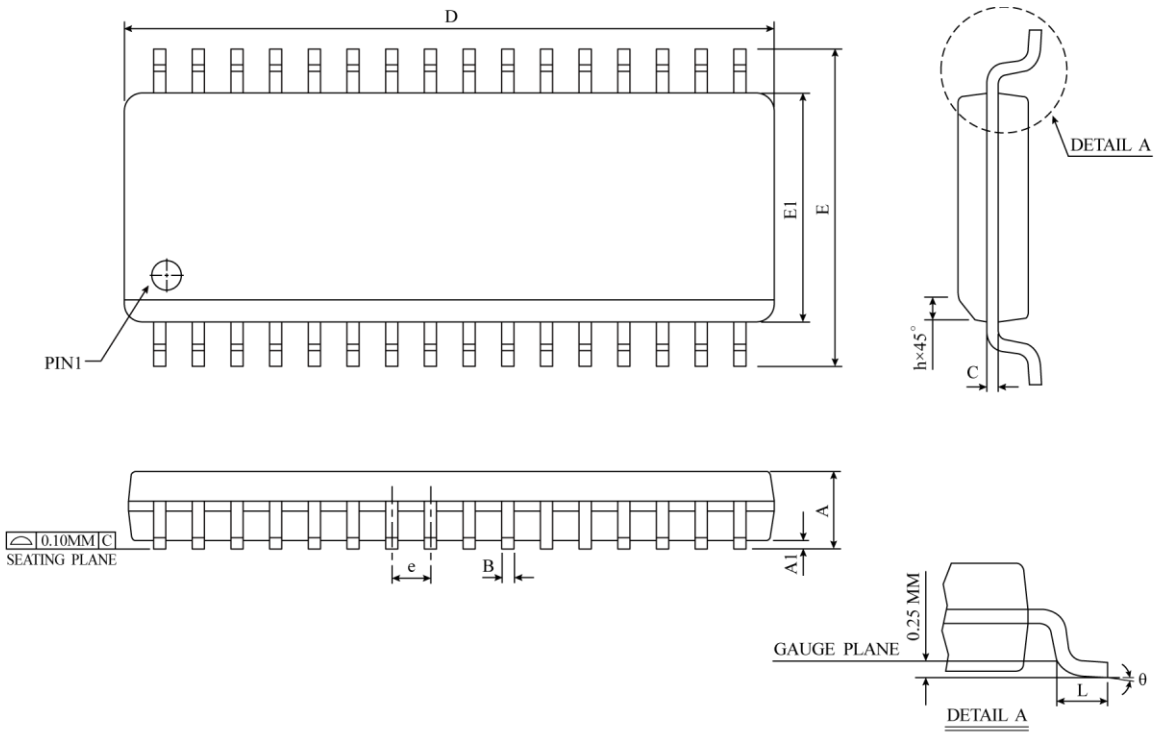
Package Information

DIP 32-pin (600 mil) Package Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	5.588	-	-	0.220
A1	0.381	-	-	0.015	-	-
A2	3.810	3.937	4.064	0.150	0.155	0.160
D	41.783	41.974	42.164	1.645	1.653	1.660
E	15.240 BSC			0.600 BSC		
E1	13.716	13.843	13.970	0.540	0.545	0.550
L	2.921	4.001	5.080	0.115	0.158	0.200
^{e}B	16.002	16.51	17.018	0.630	0.650	0.670
θ	0°	7.5°	15°	0°	7.5°	15°
JEDEC	MO-015 (AP)					

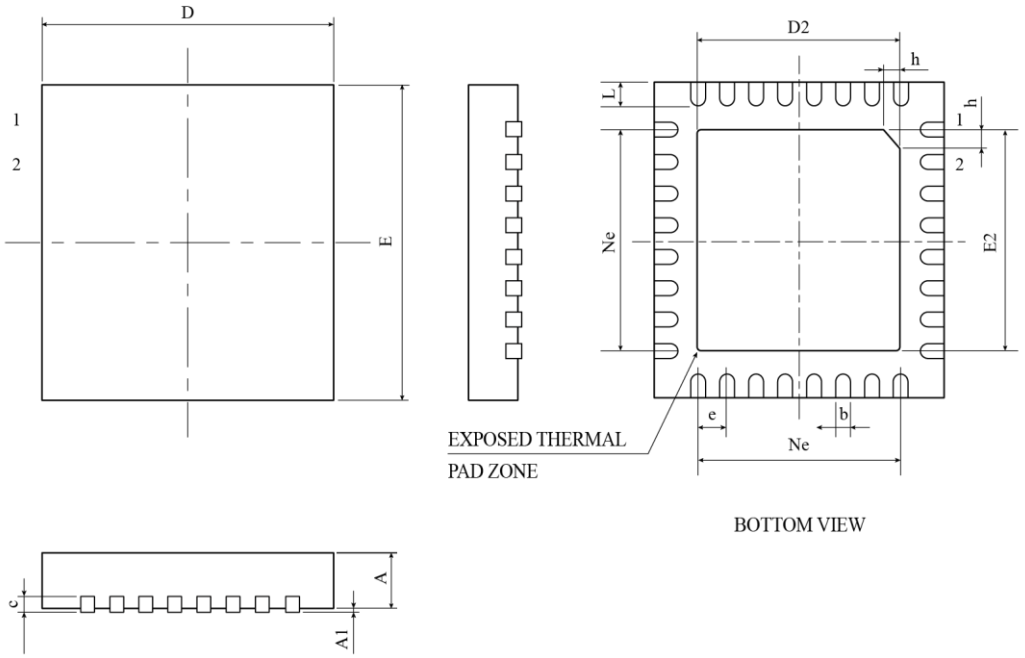
SOP 32-pin (300 mil) Package Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	20.32	20.53	20.73	0.8000	0.8080	0.8160
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	-	8°	0°	-	8°

△ * NOTES：DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

QFN 32pin (5x5x0.75-0.5mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	--	0.02	0.05	--	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
c	0.18	0.20	0.25	0.007	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	3.40	3.50	3.60	0.134	0.138	0.142
e	0.50 BSC			0.020 BSC		
Ne	3.50 BSC			0.138 BSC		
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	3.40	3.50	3.60	0.134	0.138	0.142
L	0.35	0.40	0.45	0.014	0.016	0.018
h	0.30	0.35	0.40	0.012	0.014	0.016