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TM52F2260

DATA SHEET

Rev 0.93

AMENDMENT HISTORY

Version	Date	Description
V0.90	Jan, 2015	New release.
V0.91	Nov, 2015	Add POR vs Temperature Diagram (page 68)
V0.92	Mar, 2016	Modify ICE mode pin connection diagram (page 54)
V0.93	Apr, 2017	1. Add LQFP64 (7X7) ordering/package info. 2. modify Flash endurance 3. VCON limitation in ICE mode 4. Stop mode entry limitation 5. other details

CONTENTS

TM52 F22xx FAMILY

Common Feature

CPU	Flash Program memory	RAM bytes	Dual Clock	Operation Mode	Timer0 Timer1 Timer2	UART	Real-time Timer3	LBD	LVR
Fast 8051 (2T)	8K~32K with IAP, ISP, ICP	512 ~ 2304	SXT SRC FXT FRC	Fast Slow Idle Stop	8051 Standard		0.5~61ppm Adjustable	2.4V ~ 3.1V	1.6V

Family Members Features

P/N	Flash	RAM bytes	IO Pin	RFC ADC	SAR ADC	Touch Key	LCD	LED	SPI	others	Status
TM52-F2261	16K	768	32	3-ch	–	14-ch	43 x 10 1.0~1.5V adj.-Bias	30x6 40mA hi-Sink	Yes	–	Product
TM52-F2264						–					
TM52-F2260	16K	1280	25	3-ch	–	–	36 x 4 1.0V Bias	–	–	–	Product
TM52-F2280	8K	512	32	3-ch	6bit 7-ch	15-ch	23 x 8 1.0~1.5V adj.-Bias	10x4 40mA hi-Sink	Yes	–	Product
TM52-F2284						–					
TM52-F2230	32K	2304	32	3-ch	6bit 7-ch	15-ch	–	–	Yes	PWM	Sample

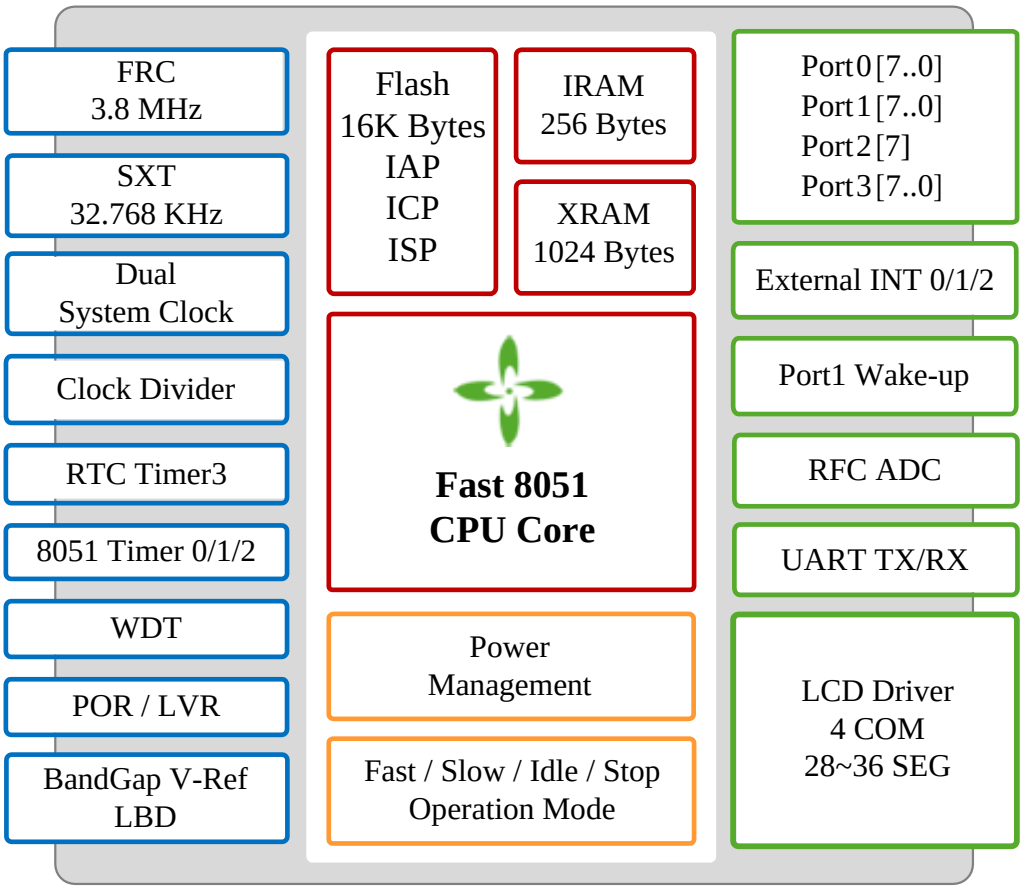
P/N	Operation Voltage	Idle Mode Current (V_{BAT}=3V) with 32 KHz wake-up & LVR On				Max. System Clock (Hz)			
		TK Off LCD Off	TK Off LCD On	TK On LCD Off	TK On LCD On	SXT	SRC	FXT	FRC
TM52-F2261	2.0~4.2V	0.8uA	1.4uA	1.3uA	1.9uA	32K	–	–	4M
TM52-F2264				–	–				
TM52-F2260	2.0~4.2V	0.7uA	1.0uA	–	–	32K	–	–	4M
TM52-F2280	2.0~5.5V	1.0uA	2.5uA	1.5uA	3.0uA	32K	80K	8M	7.4M
TM52-F2284				–	–				
TM52-F2230	2.0~5.5V	1.0uA	–	1.5uA	–	32K	80K	8M	7.4M

GENERAL DESCRIPTION

TM52 series F2260 is a version of a new, fast 8051 architecture for an 8-bit microcontroller single chip with an instruction set fully compatible with industry standard 8051, C language development platform, and retains most 8051 peripheral's functional block. Typically, the **TM52-F2260** executes instructions six times faster than the standard 8051 architecture.

The **TM52-F2260** provides improved performance, lower cost and fast time-to-market by integrating features on the chip, including 16K Bytes Flash program memory, 1280 Bytes SRAM, Low Voltage Reset (LVR), Low Battery Detector (LBD), dual clock power saving operation mode, 8051 standard UART and Timer0/1/2, adjustable real time clock Timer3, LCD driver, Watch Dog Timer and Resistance to Frequency Converter (RFC). Its high reliability and low power consumption feature can be widely applied in consumer and battery appliance products.

BLOCK DIAGRAM



TM52F2260

FEATURES

1. **Standard 8051 Instruction set, fast machine cycle**
   - Executes instructions six times faster than the standard 8051.
2. **16K Bytes Flash Program Memory**
   - Support “In Circuit Programming” (ICP) or “In System Programming” (ISP) for the Flash code
   - Byte Write “In Application Programming” (IAP) mode is convenient as Data EEPROM access
   - Code Protection Capability
3. **Total 1280 Bytes SRAM (IRAM + XRAM)**
   - 256 Bytes IRAM in the 8051 internal data memory area
   - 1024 Bytes XRAM in the 8051 external data memory area (accessed by MOVX Instruction)
4. **Three System Clock type Selections**
   - Fast clock from Internal RC (FRC, 3.75MHz @V_{DD}=3V)
   - Slow clock from 32768Hz Crystal (SXT)
   - Slow clock from RFC
   - System Clock can be divided by 1/4/16/64 option
   - System Clock output pin (TCO) for EL / IR application
5. **8051 Standard Timer – Timer0 / 1 / 2**
   - 16-bit Timer0, also supports RFC clock input counting
   - 16-bit Timer1, also supports T1O / T1B clock output for Buzzer / IR application
   - 16-bit Timer2, also supports T2O clock output for Buzzer / IR application
6. **23-bit Timer3 used for Real Time 32768Hz Crystal counting**
   - ± 0.5 ppm ~ 61 ppm interrupt rate adjustable
   - MSB 8-bit overflow auto-reload
   - 0.25 sec, 0.5 sec, 1.0 sec or overflow Interrupt
7. **9-Sources, 4-level priority Interrupt**
   - Timer0 / Timer1 / Timer2 / Timer3 Interrupt
   - INT0 / INT1 Falling-Edge / Low-Level Interrupt
   - Port1 Pin Change Interrupt
   - UART TX/RX Interrupt
   - P2.7 (INT2) Interrupt
8. **Pin Interrupt can Wake up CPU from Power-Down (Stop) mode**
   - P3.2 / P3.3 (INT0 / INT1) Interrupt & Wake-up
   - P2.7 (INT2) Interrupt & Wake-up
   - Each Port1 pin can be defined as Interrupt & Wake-up pin (by pin change)

9. **8051 Standard UART**
   - One Wire UART option can be used for ISP or other application
10. **Max. 25 Programmable I/O pins**
   - CMOS Output
   - Pseudo-Open-Drain, or Open-Drain Output
   - Schmitt Trigger Input
   - Pin Pull-up can be Enabled or Disabled
11. **Resistance to Frequency Converter (RFC)**
   - RFC clock divided by 1/4/16/64 signal can be assigned as Timer0 event count input
   - RFC clock can be used as System clock source
12. **LCD Controller / Driver**
   - 1/3 or 1/4 Duty
   - 4 COM, 28 ~ 36 SEG
   - 1/3 Bias, VL1 = V_{BAT} / 3
   - Frame Rate = 40Hz ~ 90Hz
13. **BandGap Voltage Reference for Low Battery Detection (LBD)**
   - Detect V_{BAT} voltage level from 2.5V to 3.1V
14. **Built-in tiny current LDO Regulator for chip internal power supply (V_{DD})**
   - V_{DD} voltage level can be set from 1.2V to 1.9V
15. **Watch Dog Timer based on System Clock**
   - Running in Fast / Slow Mode, Stop counting in Idle / Stop Mode
   - 32K or 64K counts overflow Reset
16. **5-types Reset**
   - Power on Reset
   - Selectable External Pin Reset
   - Selectable Watch Dog Reset
   - Software Command Reset
   - Selectable Battery Low Voltage Reset (when V_{BAT} < 1.6V)
17. **4-types Power Operation Modes**
   - Fast / Slow / Idle / Stop Mode
18. **On-chip Debug / ICE interface**
   - Use P1.2 / P1.3 pin
   - Share with ICP programming pin

19. Operating Voltage and Current

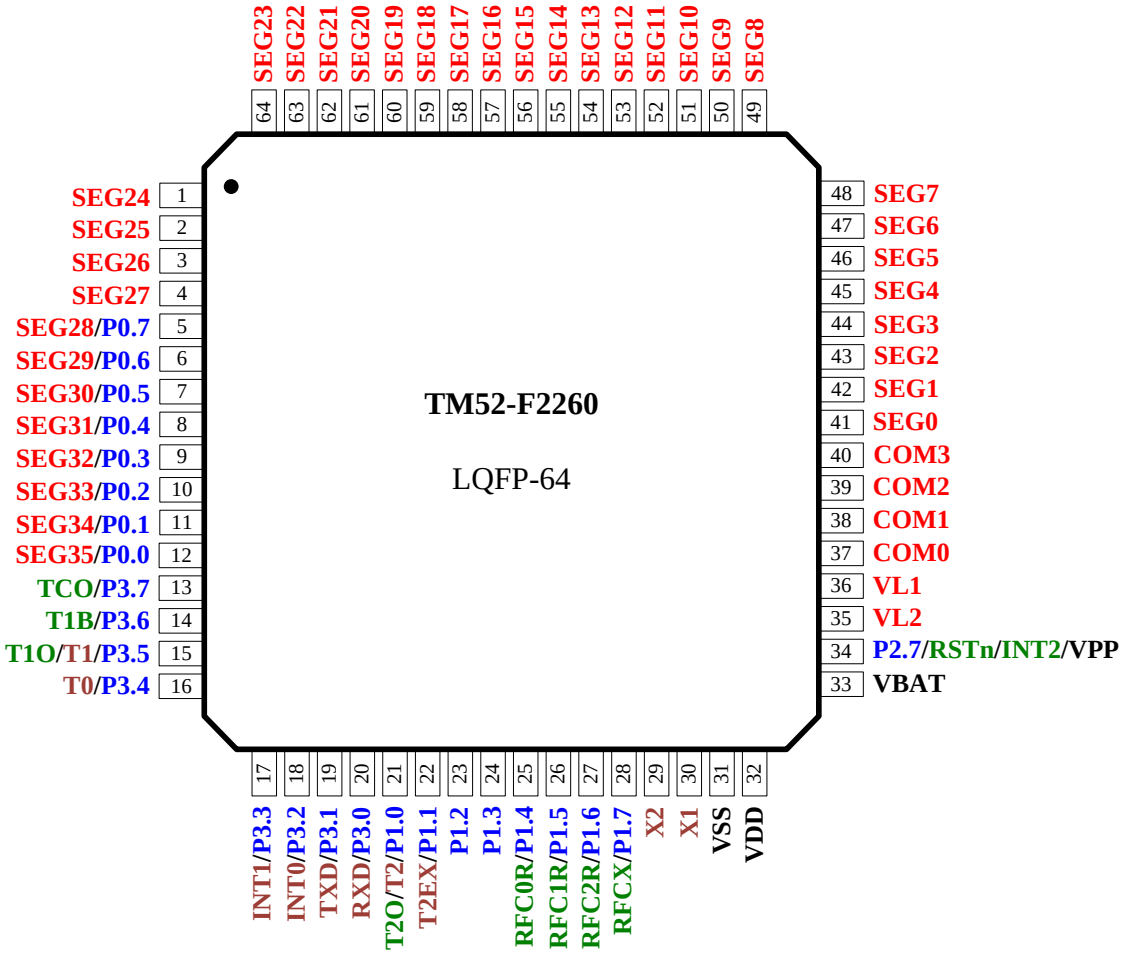
- V_{BAT} = 2.0V ~ 4.2V
- 0.3uA LCD Current @V_{BAT} = 3V
- 0.1uA LVR Current @V_{BAT} = 3V
- 0.6uA 32K Crystal and System Clock Current @V_{DD} = 1.5V
- Total 1.0uA Idle mode Current with LCD on and LVR on, @V_{BAT} = 3V, V_{DD} = 1.5V

20. Operating Temperature Range

- –40℃ ~ +85℃

21. 64-pin LQFP Package

PIN ASSIGNMENT



PIN DESCRIPTION

Name	In/Out	Pin Description
P1.0~P1.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software. These pin's level change can interrupt/wake up CPU from Idle/Stop mode.
P3.0~P3.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "**pseudo open drain**" output. Pull-up resistors are assignable by software.
P3.3~P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
P0.0~P0.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or CMOS push-pull output. Pull-up resistors are assignable by software.
P2.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or "open-drain" output. Pull-up resistor is fix enable.
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Stop mode wake up input
INT2	I	External falling edge Interrupt input, Idle / Stop mode wake up input
RXD	I/O	UART Mode0 transmit & receive data, Mode1/2/3 receive data
TXD	I/O	UART Mode0 transmit clock, Mode1/2/3 transmit data. In One Wire UART mode, this pin transmits and receives serial data.
T0, T1, T2	I	Timer0, Timer1, Timer2 event count pin input
T2EX	I	Timer2 external trigger input
T1O, T1B	O	Positive and Negative signal pair of Timer1 overflow divided by 2/3/4 output
T2O	O	Timer2 overflow divided by 2/3/4 output
TCO	O	System Clock divided by 1/2/3/4 output
RFC0R~RFC2R	O	RFC resistor connection pin
RFCX	I	RFC clock input pin
SEG0~SEG35	O	LCD segment output
COM0~COM3	O	LCD common output
VL1, VL2	–	LCD Bias Voltage Regulator output, add 0.1uF capacitor for each pin to VSS
RSTn	I	External active low reset input, Pull-up resistor is fixed enable
X1, X2	–	32768 Crystal / Resonator oscillator connection for System Clock
VPP	I	Flash memory programming high voltage input
VDD	–	LDO Regulator output and internal power supply, add 1uF capacitor to VSS
VBAT, VSS	P	Power input pin and ground, VBAT is the I/O pin power supply

Note: Digital I/O pins voltage swing from V_{SS} to V_{BAT}.

PIN SUMMERY

LQFP-64	Pin Name	Type	After Reset		Input		Output			Alternative Function					
			Function	State	Wake up	Ext. Interrupt	CMOS P.P.	P.O.D.	O.D.	LCD	RFC	UART	Clock Output	Timer Input	Others
1	SEG24	O	LCD	DL						●					
2	SEG25	O	LCD	DL						●					
3	SEG26	O	LCD	DL						●					
4	SEG27	O	LCD	DL						●					
5	SEG28/P0.7	I/O	LCD	DL			●			●					
6	SEG29/P0.6	I/O	LCD	DL			●			●					
7	SEG30/P0.5	I/O	LCD	DL			●			●					
8	SEG31/P0.4	I/O	LCD	DL			●			●					
9	SEG32/P0.3	I/O	LCD	DL			●			●					
10	SEG33/P0.2	I/O	LCD	DL			●			●					
11	SEG34/P0.1	I/O	LCD	DL			●			●					
12	SEG35/P0.0	I/O	LCD	DL			●			●					
13	TCO/P3.7	I/O	I/O Input	PU			●		●				●		
14	T1B/P3.6	I/O	I/O Input	PU			●		●				●		
15	T1O/T1/P3.5	I/O	I/O Input	PU			●		●				●	●	
16	T0/P3.4	I/O	I/O Input	PU			●		●					●	
17	INT1/P3.3	I/O	I/O Input	PU	●	●	●		●						
18	INT0/P3.2	I/O	I/O Input	PU	●	●	●	●							
19	TXD/P3.1	I/O	I/O Input	PU			●	●				●			
20	RXD/P3.0	I/O	I/O Input	PU			●	●				●			
21	T2O/T2/ P1.0	I/O	I/O Input	PU	●	●	●		●				●	●	
22	T2EX/P1.1	I/O	I/O Input	PU	●	●	●		●					●	
23	P1.2	I/O	I/O Input	PU	●	●	●		●						
24	P1.3	I/O	I/O Input	PU	●	●	●		●						
25	RFC0R/P1.4	I/O	I/O Input	PU	●	●	●		●		●				
26	RFC1R/P1.5	I/O	I/O Input	PU	●	●	●		●		●				
27	RFC2R/P1.6	I/O	I/O Input	PU	●	●	●		●		●				
28	RFCX/P1.7	I/O	I/O Input	PU	●	●	●		●		●			●	
29	X2	–	Crystal	–											Crystal
30	X1	–	Crystal	–											Crystal
31	VSS	P	V_{SS}	–											
32	VDD	–	V_{DD}	–											
33	VBAT	P	V_{BAT}	–											
34	VPP/RSTn/INT2/P2.7	I/O	I/O Input	PU	●	●			●						Reset/VPP

LQFP-64	Pin Name	Type	After Reset		Input		Output			Alternative Function					
			Function	State	Wake up	Ext. Interrupt	CMOS P.P.	P.O.D.	O.D.	LCD	RFC	UART	Clock Output	Timer Input	Others Misc.
35	**VL2**	–	LCD	–						●					
36	**VL1**	–	LCD	–						●					
37	**COM0**	O	LCD	DL						●					
38	**COM1**	O	LCD	DL						●					
39	**COM2**	O	LCD	DL						●					
40	**COM3**	O	LCD	DL						●					
41	**SEG0**	O	LCD	DL						●					
42	**SEG1**	O	LCD	DL						●					
43	**SEG2**	O	LCD	DL						●					
44	**SEG3**	O	LCD	DL						●					
45	**SEG4**	O	LCD	DL						●					
46	**SEG5**	O	LCD	DL						●					
47	**SEG6**	O	LCD	DL						●					
48	**SEG7**	O	LCD	DL						●					
49	**SEG8**	O	LCD	DL						●					
50	**SEG9**	O	LCD	DL						●					
51	**SEG10**	O	LCD	DL						●					
52	**SEG11**	O	LCD	DL						●					
53	**SEG12**	O	LCD	DL						●					
54	**SEG13**	O	LCD	DL						●					
55	**SEG14**	O	LCD	DL						●					
56	**SEG15**	O	LCD	DL						●					
57	**SEG16**	O	LCD	DL						●					
58	**SEG17**	O	LCD	DL						●					
59	**SEG18**	O	LCD	DL						●					
60	**SEG19**	O	LCD	DL						●					
61	**SEG20**	O	LCD	DL						●					
62	**SEG21**	O	LCD	DL						●					
63	**SEG22**	O	LCD	DL						●					
64	**SEG23**	O	LCD	DL						●					

Symbol:

P.P. = CMOS Push-Pull Output
O.D. = Open Drain
P.O.D. = Pseudo Open Drain
PU = Pull up
DL = Drive Low

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The **F2260** features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a program counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as “A” or “ACC,” including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR **E0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC:** Accumulator

1.2 B Register (B)

The “B” register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands be in A and B.

SFR **F0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B:** B register

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer. The Stack Pointer points to the top location of the stack.

SFR **81h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP:** Stack Point

1.4 Dual Data Pointer (DPTRs)

F2260 has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs.

SFR **82h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL:** Data Point low byte

SFR **83h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH:** Data Point high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	–	–	–	–	CLRWDT	CLRTM3	STPRFC	DPSEL
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

F8h.0 **DPSEL:** Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The instructions that affect the PSW are listed below.

Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR **D0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY:** ALU carry flag

D0h.6 **AC:** ALU auxiliary carry flag

D0h.5 **F0:** General purpose user-definable flag

D0h.4~3 **RS1, RS0:** The contents of (RS1, RS0) enable the working register banks as:

00: Bank 0 (00h~07h)

01: Bank 1 (08h~0Fh)

10: Bank 2 (10h~17h)

11: Bank 3 (18h~1Fh)

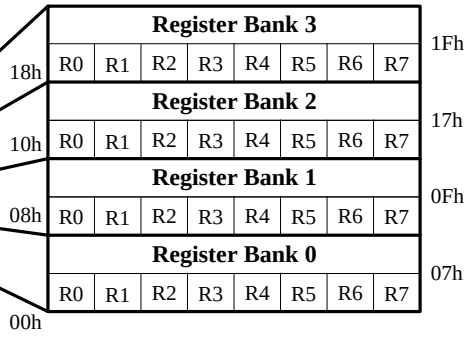
D0h.2 **OV:** ALU overflow flag

D0h.1 **F1:** General purpose user-definable flag

D0h.0 **P:** Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of "one" bits in the accumulator.

PSW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CY	**AC**	**FO**	**RS1**	**RS0**	**OV**	**F1**	**P**

RS1	RS0	Bank
1	1	3
1	0	2
0	1	1
0	0	0



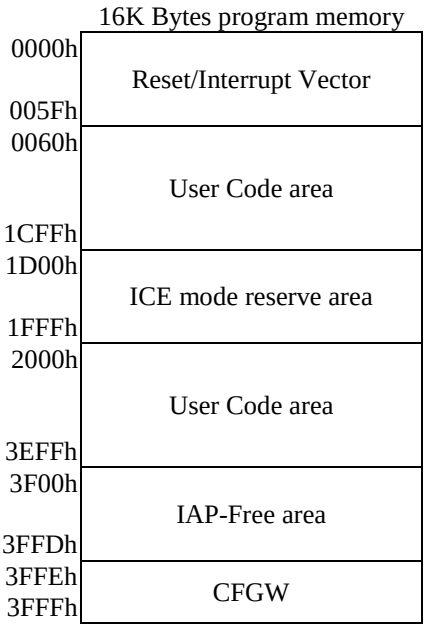
2. Memory

2.1 Program Memory

The **F2260** has a 16K Bytes Flash program memory, which can support In Circuit Programming (ICP), In Application Programming (IAP) and In System Programming (ISP) function modes. The Flash write endurance is at least 50K cycles. The Flash program memory address continuous space (0000h~3FFFh) is partitioned to several sectors for device operation.

2.1.1 Program Memory Functional Partition

The last 2 bytes (3FFEh~3FFFh) of program memory is defined as chip Configuration Word (CFGW), which is loaded into the device control registers upon power on reset (POR). The address space 3F00h~3FFDh is the IAP free area, while the 0000h~005Fh is occupied by Reset/Interrupt vectors as standard 8051 definition. In the in-circuit emulation (ICE) mode, user also needs to reserve the address space 1D00h~1FFFh for ICE System communication.



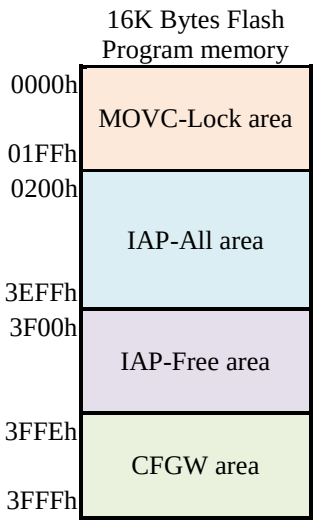
2.1.2 Flash ICP Mode

The Flash memory can be programmed by the tenx proprietary writer **(TWR98/TWR99)**, which needs at least four wires (VBAT, VSS, P1.2, and P1.3 pins) to connect to this chip. To shorten the programming time, it is recommended to connect Writer with an additional fifth wire, which is the VPP (P2.7) pin. If the user wants to program the Flash memory on the target circuit board (In Circuit Program, ICP), these pins must be reserved sufficient freedom to be connected to the Writer. More pins connected to Writer ensure more writing efficiency and speed.

Writer wire number	Pin connection
4-Wire	VBAT, VSS, P1.2, P1.3
5-Wire	VBAT, VSS, P1.2, P1.3, VPP
6-Wire	VBAT, VSS, P1.2, P1.3, VPP, P1.0. ***Note:*** P1.1 always output Low in this mode

2.1.3 Flash IAP Mode

The **F2260** has "In Application Program" (IAP) capability, which allows software to read/write data from/to the Flash memory during CPU run time as conveniently as data EEPROM access. The IAP function is byte writable, meaning that the **F2260** does not need to erase one Flash page before write. The available IAP data space is 254 Bytes after chip reset, and can be re-defined by the "MVCLOCK" and "IAPALL" control register as shown below.



Flash memory	MVCLOCK	IAPALL	MOVC Accessible	MOVX (IAP) Accessible
0000h~01FFh	1	X	No	No
	0	0	Yes	No
	0	1	Yes	Yes
0200h~3EFFh	X	0	Yes	No
	X	1	Yes	Yes
3F00h~3FFDh	X	X	Yes	Yes
3FFEh	X	0	Yes	No
	X	1	Yes	Yes
3FFFh	X	X	Yes	No

In IAP mode, the program Flash memory is separated into four sectors: MOVC-Lock area, IAP-All area, IAP-Free area, and CFGW area. These four sectors are regulated differently.

In the **MOVC-Lock area,** IAP read/write is limited by MVCLOCK bit, which can be set to control the accessibility of the MOVC and MOVX instructions to this area. The size of this area is 512 Bytes. The lock function is made to protect the main program code against unconsciously writing Flash memory in IAP mode. Locking or unlocking the function should be performed by the tenx TWR98/99 writing to the CFGW in Flash memory.

The **IAP-All area** is protected by the IAPALL register to prevent IAP mode from writing application data to the program area, resulting in a program code error that cannot be repaired. The size of this area is 15,616 Bytes. Enabling IAPALL requires writing 65h to SFR SWCMD 97h to set the IAPALL control flag. Then, software can use MOVX instructions to write application data to flash memory from 0200h to 3EFFh. If user wants to disable IAPALL function, user can write other values to SFR SWCMD 97h to clear the IAPALL control flag. User must be careful not to overwrite program code which is already resided on the same Flash memory area.

The **IAP-Free area** has no control bit to protect. It can be used to reliably store system application data that needs to be programmed once or periodically during system operation. Other areas of Flash memory can be used to store data, but this area is usually the best. The size of this area is 254 Bytes, equivalent to an EEPROM, and Flash memory can provide byte access to read and write commands. In the past, storage of configuration data required an additional EEPROM or the other storage device. However, this functionality can now be provided by on-chip Flash, reducing the chip count of embedded applications. An external EEPROM or SRAM may not be needed.

The **CFGW area** has 2 data bytes (CFGWH and CFGWL), which is located at the last 2 addresses of Flash memory. The CFGWH is not accessible to IAP, while the CFGWL can be read or written by IAP in case the IAPALL flag is set. CFGWL is copied to the SFR F7h after power on reset, software then

take over CFGWL's control capability by modifying the SFR F7h. The CFGWL is applied in many other TM52 series MCU. However, it is not defined in F2260.

Flash **3FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	MVCLOCK	WDTE	–	–	LVRE	–

3FFFh.5 **MVCLOCK:** If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL / SWRST							
R/W	W							R/W
Reset	–							0

97h.7~0 **IAPALL (W):** Write 65h to set IAPALL control flag; Write other value to clear IAPALL flag.

97h.0 **IAPALL (R):** Flag indicates Flash memory sectors can be accessed by IAP or not. This bit combines with MVCLOCK to define the accessible IAP area.

2.1.4 IAP Mode Access Routines

Flash IAP write is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target Flash address (0~3FFEh), and the ACC contains the data being written. Flash IAP writing requires approximately 500uS. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers, LCD, and others) continue running during the writing time. The software must handle the pending interrupts after an IAP write. Flash IAP writing needs slower SYSCLK frequency as well as higher V_{DD} voltage. User must clear "PWRSAV" control bit to let $V_{DD}=V_{BAT}$ and $V_{BAT}>2.8V$.

Because the Program memory and the IAP data space share the same entity, a Flash IAP read can be performed by the "MOVX A, @DPTR" or "MOVC" instruction as long as the target address points to the 0~3FFFh area. A Flash IAP read does not require extra CPU wait time.

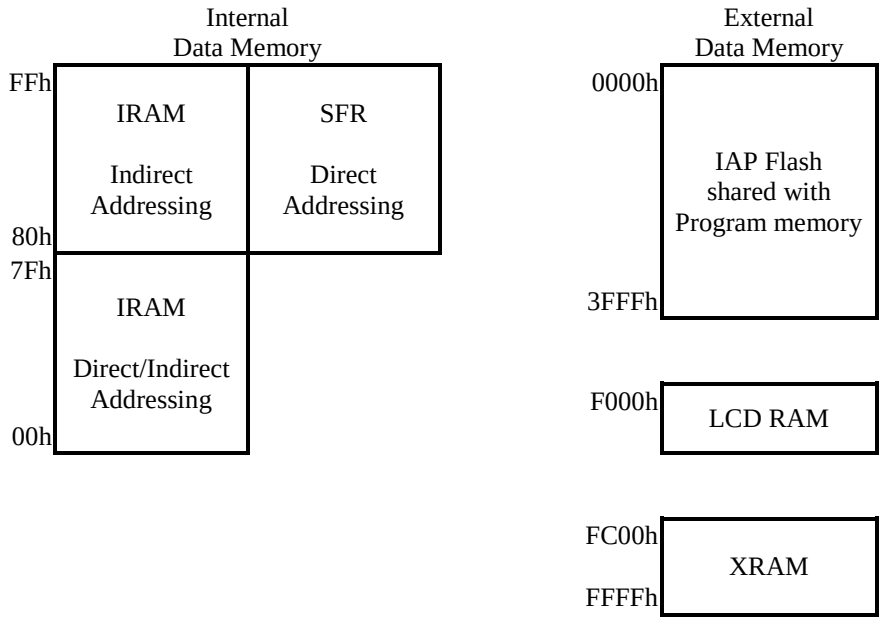
```
; IAP example code
; need VDD > 2.8V and slower System clock
MOV     DPTR, #3F00h        ; DPTR=3F00h=target IAP address
MOV     A, #5Ah             ; A=5Ah=target IAP write data
MOVX    @DPTR, A            ; Flash[3F00h]=5Ah, after IAP write
                            ; 200µs~500µs H/W writing time, CPU wait
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=5Ah
CLR     A                   ; A=0
MOVC    A, @A+DPTR          ; A=5Ah
```

2.1.5 Flash ISP Mode

The "In System Programming" (ISP) usage is similar to IAP, except the purpose is to refresh the Program code. User can use UART or other method to get new Program code from external host, then writes code as the same way as IAP. ISP operation is complicated; basically it needs to assign a Boot code area to the Flash which does not change during the ISP process.

2.2 Data Memory

As the standard 8051, the **F2260** has both Internal and External Data Memory space. The Internal Data Memory space consists of 256 Bytes IRAM and 50 SFRs, which are accessible through a rich instruction set. The External Data Memory space consists of 1024 Bytes XRAM, LCDRAM and IAP Flash, which can be only accessed by MOVX instruction.



2.2.1 IRAM

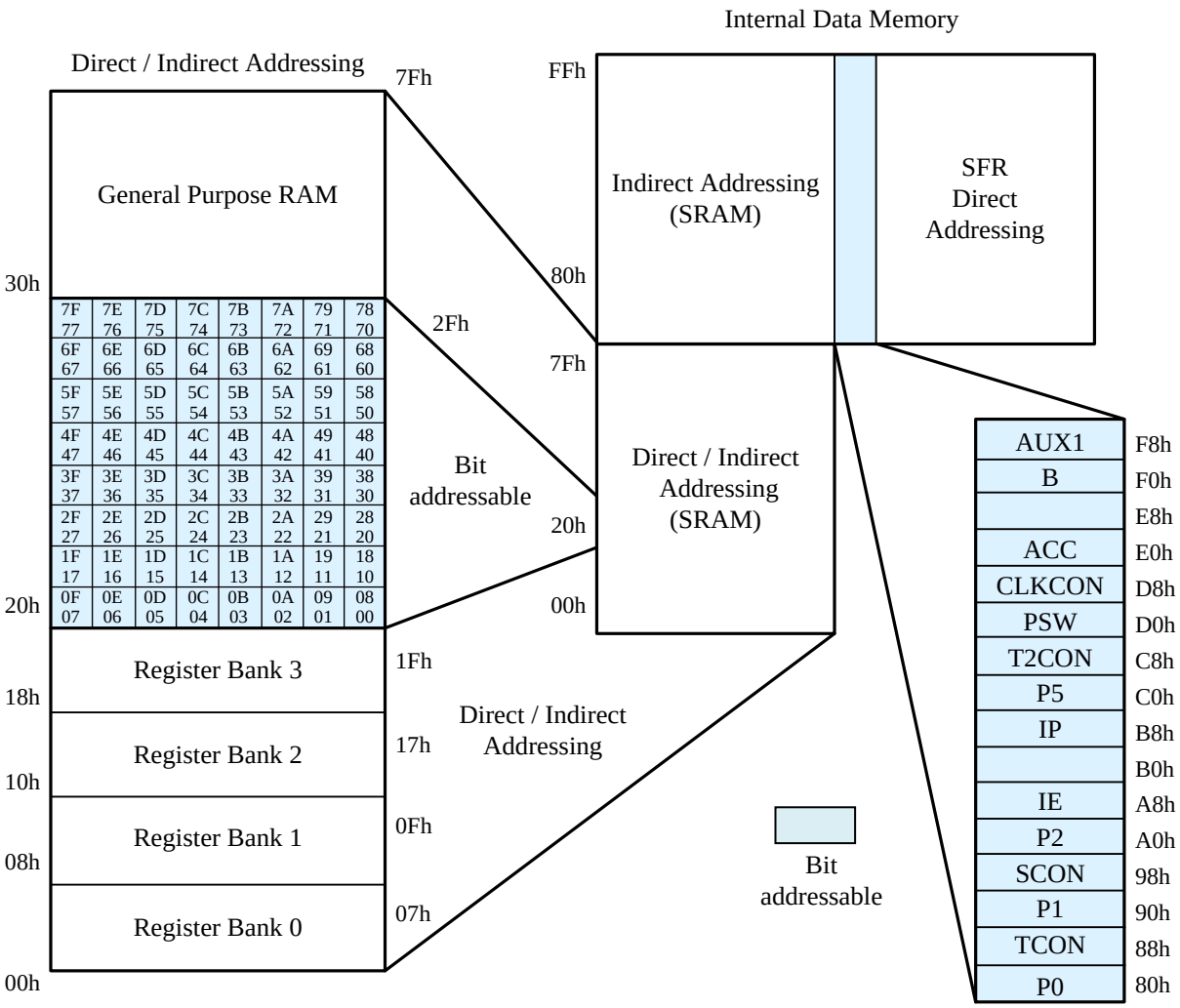
IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

2.2.2 XRAM

XRAM is located in the 8051 external data memory space (address FC00h to FFFFh). The 1024 Bytes XRAM can be only accessed by "MOVX" instruction.

2.2.3 SFRs

All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit-addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with the resources and peripherals of the **F2260**. The TM52 series of microcontrollers provides complete binary code with standard 8051 instruction set compatibility. Beside the standard 8051 SFRs, the **F2260** implements additional SFRs used to configure and access subsystems such as the Timer3, RFC and LCD, which are unique to the **F2260**.

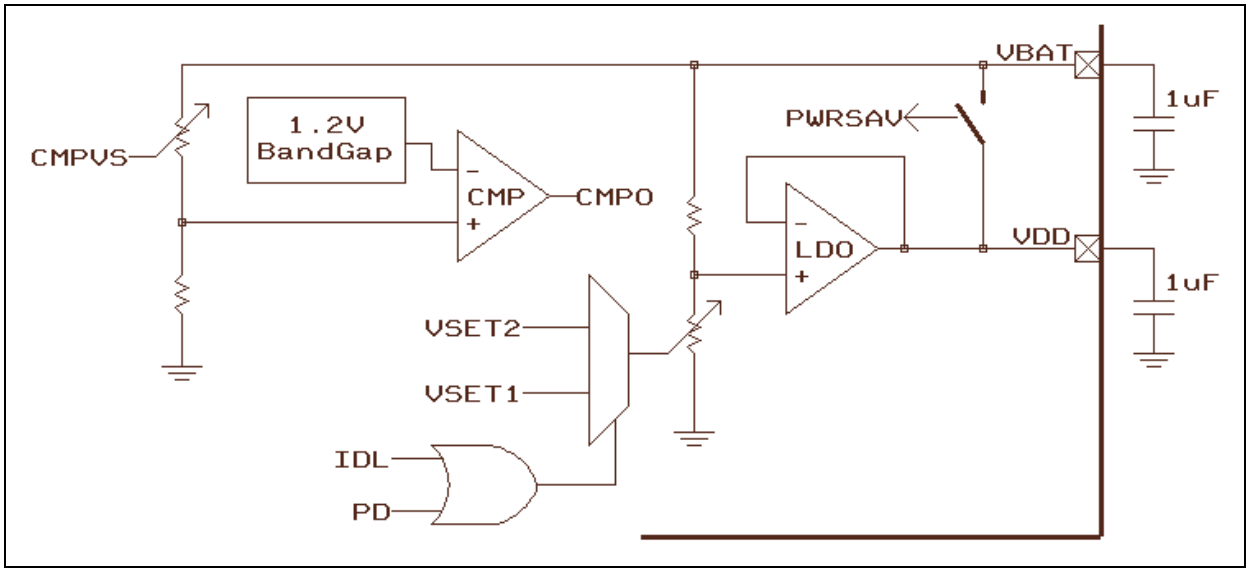


	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B							
E8h								
E0h	ACC							
D8h	CLKCON							
D0h	PSW							
C8h	T2CON		RCP2L	RCP2H	TL2	TH2		
C0h								
B8h	IP	IPH	IP1	IP1H				
B0h	P3	LCON		TM3SEC	TM3DL	TM3DH	TM3RLD	TM3ADJ
A8h	IE	INTE1						RFCON
A0h	P2		P1MODL	P1MODH	P3MODL	P3MODH	TOCON	VCON
98h	SCON	SBUF						
90h	P1	P0OE			OPTION	INTFLG	P1WKUP	SWCMD
88h	TCON	TMOD	TL0	TL1	TH0	TH1		
80h	P0	SP	DPL	DPH				PCON

3. Power

VBAT pin is the power supply for this chip. It provides voltage source to the built-in tiny current LDO Regulator for chip internal operation. The VDD is the LDO output pin, which needs an external 1uF capacitor connection to VSS for voltage level stability. The PWRSAV and VSET1/VSET2 SFR bits control the V_{DD} voltage level. If PWRSAV=0 (chip reset default), V_{DD} voltage level is the same as V_{BAT}. If PWRSAV=1, the V_{DD} voltage level can be switched from V_{BAT}*115/300 to V_{BAT}*192/300 range. The VSET1/VSET2 SFR can set the V_{DD} voltage level in different operation mode. The lower V_{DD} voltage level causes lower chip current consumption, but user must also consider the System clock rate. Higher clock rate needs higher V_{DD} voltage level. User must keep $1.4V<V_{DD}<4.2V$ for the device's proper operation. In IAP write mode, user also needs to set $V_{DD} > 2.8V$, which means PWRSAV bit must be 0.

The **F2260** also has a built-in 1.2V BandGap Voltage Reference for Low Battery Detection (LBD). The Battery voltage is divided by resistor to certain level then compare to the BandGap voltage. User can refer to the V_{BAT} voltage level for setting the V_{DD} level by VSET1 or VSET2 SFR. The BandGap and Comparator consume un-neglect current, so user should not use them too often. Since V_{BAT} voltage level changes very slowly, user can detect it once an hour or once a day to reduce current consumption.



LDO Regulator & Comparator

CMPO	CMPVS						
	1	2	3	4	5	6	7
$3.1V < V_{BAT}$	1	1	1	1	1	1	1
$3.0 < V_{BAT} < 3.1V$	1	1	1	1	1	1	0
$2.9 < V_{BAT} < 3.0V$	1	1	1	1	1	0	0
$2.8 < V_{BAT} < 2.9V$	1	1	1	1	0	0	0
$2.7 < V_{BAT} < 2.8V$	1	1	1	0	0	0	0
$2.6 < V_{BAT} < 2.7V$	1	1	0	0	0	0	0
$2.5 < V_{BAT} < 2.6V$	1	0	0	0	0	0	0
$V_{BAT} < 2.5V$	0	0	0	0	0	0	0

Comparator Result vs V_{BAT} voltage level

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	CMPO	CMPVS			UART1W	WDTPSC	TM3PSC	
R/W	R	R/W			R/W	R/W	R/W	
Reset	–	0	0	0	0	0	0	1

94h.7 **CMPO:** Compare result of BandGap voltage and V_{BAT} voltage divider. "1" means the V_{BAT} divider voltage is higher.

94h.6~4 **CMPVS:** Select V_{BAT} resistor divider for Comparator input to compare with the 1.2V reference.

000: Comparator Disable
001: the Comparator input is V_{BAT}*12/25
010: the Comparator input is V_{BAT}*12/26
011: the Comparator input is V_{BAT}*12/27
100: the Comparator input is V_{BAT}*12/28
101: the Comparator input is V_{BAT}*12/29
110: the Comparator input is V_{BAT}*12/30
111: the Comparator input is V_{BAT}*12/31

SFR **A7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCON	–	PWRSAV	VSET2			VSET1		
R/W	–	R/W	R/W			R/W		
Reset	–	0	1	0	0	0	1	0

A7h.6 **PWRSAV:** V_{DD} voltage control.

0: $V_{DD} = V_{BAT}$
1: $V_{DD} = V_{BAT}$*115/300 ~ V_{BAT}*192/300

A7h.5~3 **VSET2:** V_{DD} voltage setting in Fast/Slow mode while PWRSAV=1.

000: $V_{DD} = V_{BAT}$*115/300 in Fast/Slow mode
001: $V_{DD} = V_{BAT}$*126/300 in Fast/Slow mode
010: $V_{DD} = V_{BAT}$*137/300 in Fast/Slow mode
011: $V_{DD} = V_{BAT}$*148/300 in Fast/Slow mode
100: $V_{DD} = V_{BAT}$*159/300 in Fast/Slow mode
101: $V_{DD} = V_{BAT}$*170/300 in Fast/Slow mode
110: $V_{DD} = V_{BAT}$*181/300 in Fast/Slow mode
111: $V_{DD} = V_{BAT}$*192/300 in Fast/Slow mode

A7h.2~0 **VSET1:** V_{DD} voltage setting in Idle/Stop mode while PWRSAV=1.

000: $V_{DD} = V_{BAT}$*115/300 in Idle/Stop mode
001: $V_{DD} = V_{BAT}$*126/300 in Idle/Stop mode
010: $V_{DD} = V_{BAT}$*137/300 in Idle/Stop mode
011: $V_{DD} = V_{BAT}$*148/300 in Idle/Stop mode
100: $V_{DD} = V_{BAT}$*159/300 in Idle/Stop mode
101: $V_{DD} = V_{BAT}$*170/300 in Idle/Stop mode
110: $V_{DD} = V_{BAT}$*181/300 in Idle/Stop mode
111: $V_{DD} = V_{BAT}$*192/300 in Idle/Stop mode

***Note*:** the VCON is stuck at 0x22 (reset default state) in ICE mode.

4. Reset

The **F2260** has five types of reset methods. The CFGW controls the Reset functionality. The SFRs are returned to their default value after Reset.

4.1 Power on Reset

After Power on Reset, the device stays on Reset state for 8 ms as chip warm up time, then downloads the CFGW register from Flash's last two bytes (Other Reset will not reload the CFGW). The Power on Reset needs both V_{BAT} and V_{DD}'s voltage first discharge to near V_{SS} level, then rise beyond 1.8V.

4.2 External Pin Reset

External Pin Reset is active low. The RSTn pin needs to keep at least 2 FRC clock cycle long to be sampled by the chip. Pin Reset can be disabled or enabled by CFGW.

4.3 Software Reset

Software Reset is activated by writing the SFR 97h with data 56h.

4.4 Watch Dog Timer Reset

WDT overflow Reset is disabled or enable by CFGW. The WDT uses SYSCLK as its counting time base. It runs in Fast / Slow mode and stops in Idle / Stop mode. WDT overflow speed can be defined by WDTPSC SFR. WDT is cleared by device Reset or CLRWDT SFR bit.

4.5 Low Voltage Reset

LVR is disabled or enable by CFGW. If enable, LVR resets the device when $V_{BAT} < 1.5V$.

Flash **3FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	MVCLOCK	WDTE	–	–	LVRE	–

3FFFh.6 **XRSTE:** Pin Reset enable, 1=enable.

3FFFh.4 **WDTE:** WDT Reset enable, 1=enable.

3FFFh.1 **LVRE:** Low Voltage Reset enable, 1=enable.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL / SWRST							
R/W	W							R/W
Reset	–							0

97h.7~0 **SWRST (W):** Write 56h to generate S/W Reset.

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	–	–	–	–	CLRWDT	CLRTM3	STPRFC	DPSEL
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

F8h.3 **CLRWDT:** Set to 1 to clear Watch Dog Timer.

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	CMPO	CMPVS			UART1W	WDTPSC	TM3PSC	
R/W	R	R/W			R/W	R/W	R/W	
Reset	–	0	0	0	0	0	0	1

94h.2 **WDTPSC:** WDT Prescaler.
0: WDT overflow at 65536 System clock count
1: WDT overflow at 32768 System clock count

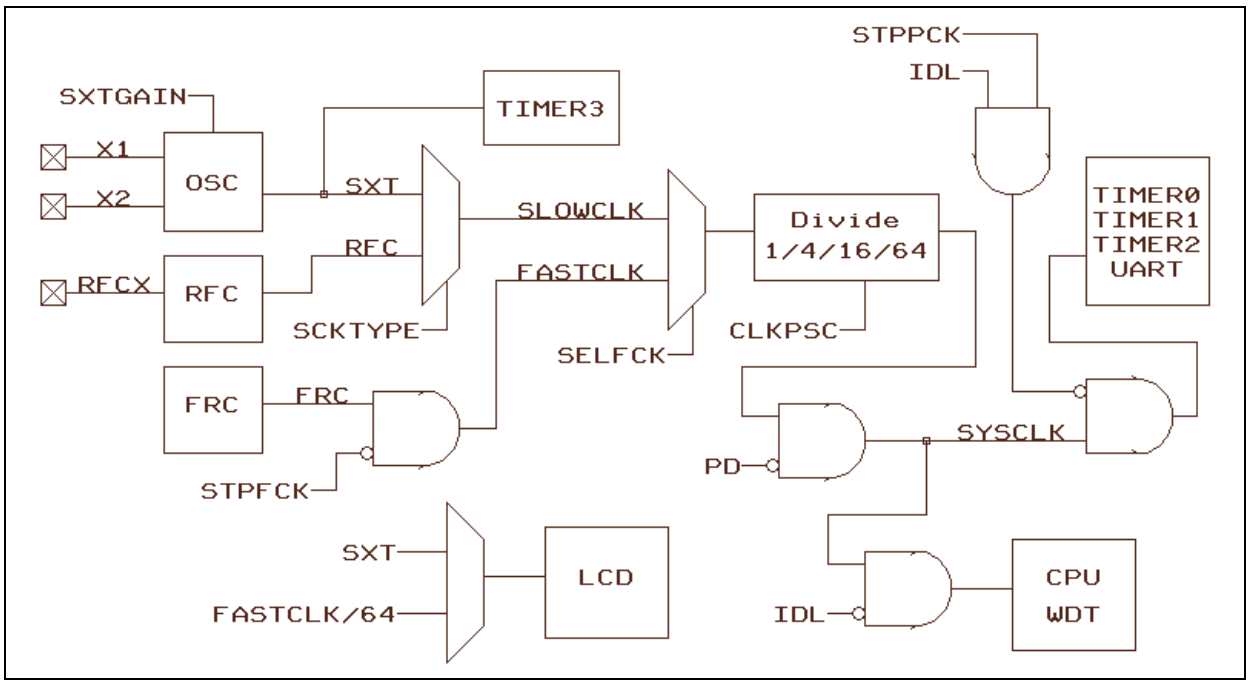
5. Clock Circuitry & Operation Mode

5.1 System Clock

The **F2260** is designed with dual-clock system. During runtime, user can directly switch the System clock from fast to slow or from slow to fast. It also can directly select a clock divider of 1, 4, 16 or 64. The Fast clock is fixed to **FRC** (Fast Internal RC, 3.75MHz at V_{DD}=3V). The Slow clock can be selected as **SXT** (Slow Crystal, 32KHz) or **RFC** (oscillation with external R and C). Fast mode and Slow mode are defined as the CPU running at Fast and Slow clock speeds.

After Reset, V_{DD}=V_{BAT} and the device is running at Fast mode with 3.75MHz FRC. If user set the PWRSAV bit, V_{DD} drops to 1.1V~1.9V, and the FRC clock frequency also reduces with the V_{DD} voltage level. The lower V_{DD} level makes the lower FRC frequency. In typical condition, FRC=1.5MHz at V_{DD}=1.5V.

SXT is the default Slow clock type. Before entering the Slow mode, software must select the Slow clock type in advance. If RFC is used as the Slow clock source, software also has to setup the pin mode and RFC related SFRs in advance. Since Fast clock is useless in Slow mode, software can set the STPFCK bit (after SELFCK=0) to stop Fast clock and reduce chip current consumption.



Clock Structure

The **CLKCON** SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow Clock type in Fast mode. Never to write both STPFCK=1 & SELFCK=1. It is recommended to write this SFR bit by bit.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	SXTGAIN		STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W		R/W	R/W	R/W	R/W	
Reset	0	1	1	0	0	1	1	1

D8h.7 **SCKTYPE:** Slow clock Type. This bit can be changed only in Fast mode (SELFCK=1).
0: SXT
1: RFC, S/W must setup RFC oscillating circuitry before set this bit to 1

D8h.6~5 **SXTGAIN:** 32768 SXT oscillator gain, 3=Highest gain, 0=Lowest gain. Higher gain can shorten the Crystal oscillation warm-up time. Lower gain can reduce oscillation current.

D8h.4 **STPPCK:** Set 1 to stop UART/Timer0/Timer1/Timer2 clock in Idle mode for current reducing.

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler.
00: System clock is Fast/Slow clock divided by 64
01: System clock is Fast/Slow clock divided by 16
10: System clock is Fast/Slow clock divided by 4
11: System clock is Fast/Slow clock divided by 1

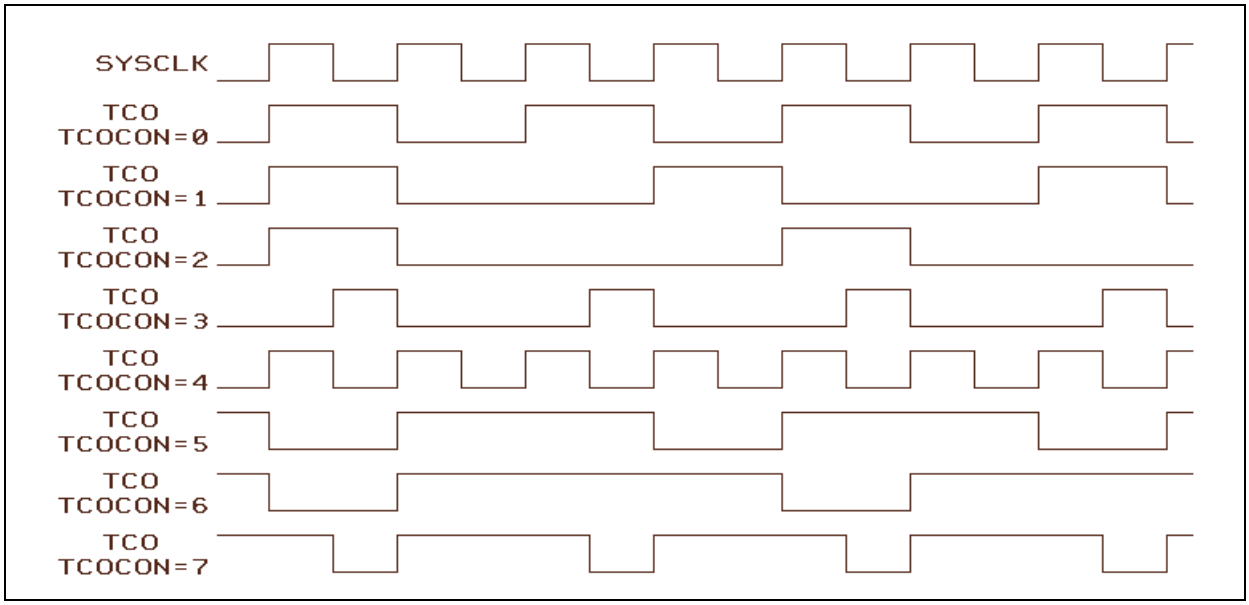
SYSCLK	CLKCON (D8h)		
	bit7	bit3	Bit2
	SCKTYPE	STPFCK	SELFCK
Slow SXT	0	0/1	0
Slow RFC (*1)	1	0/1	0
Fast FRC	0/1	0	1
Slow type change	0 ← → 1	0	1
Stop FRC	0/1	0 → 1	0
Switch to fast FRC	0/1	0	0 → 1
Switch to slow SRC/RFC	0/1	0	1 → 0

(*1) also need RFC related SFRs proper setting

This device can also output the System clock to TCO pin (in CMOS format). TCO's frequency/duty is defined by TCOCON SFR. TCO pin's output enable is defined by P3MOD7 SFR (***see section 7***).

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TOCON	T1OCON		T2OCON			TCOCON		
R/W	R/W		R/W			R/W		
Reset	0	0	0	0	0	0	0	0

A6h.2~0 **TCOCON:** TCO pin duty and frequency control
000: 1/2 duty, 1/2 SYSCLK frequency
001: 1/3 duty, 1/3 SYSCLK frequency
010: 1/4 duty, 1/4 SYSCLK frequency
011: 1/4 duty, 1/2 SYSCLK frequency
100: 1/2 duty, 1/1 SYSCLK frequency
101: 2/3 duty, 1/3 SYSCLK frequency
110: 3/4 duty, 1/4 SYSCLK frequency
111: 3/4 duty, 1/2 SYSCLK frequency



TCO waveform with TCOCON

5.2 Operation Modes

There are four operation modes for this device. **Fast Mode** is defined as the CPU running at Fast clock speed. **Slow Mode** is defined as the CPU running at Slow clock speed. When the System clock speed is lower, the power consumption is lower.

Idle Mode is entered by setting the IDL bit in PCON SFR. Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The "STPPCK" bit in CLKCON SFR can be set to furthermore reduce Idle mode current. If STPPCK=1, Timer0/1/2 and UART are stopped in Idle mode. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Stop Mode is entered by setting the PD bit in PCON SFR. This mode is the so-called "Power Down" mode in standard 8051. In Stop mode, all clocks stop. Stop Mode can be terminated by Reset or pin wake up.

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter STOP mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter IDLE mode.

Note: Chip cannot enter Stop Mode if INTn pin is low and wakeup is enable. (INTn=0 and EXn=1, n=0,1,2)

6. Interrupt & Wake-up

The **F2260** has an 9-source four-level priority interrupt structure. All enabled Interrupts can wake up CPU from Idle mode, but only the Pin Interrupts can wake up CPU from Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	Flag	Description
0003	IE0	INT0 external pin Interrupt (can wake up Stop mode)
000B	TF0	Timer0 Interrupt
0013	IE1	INT1 external pin Interrupt (can wake up Stop mode)
001B	TF1	Timer1 Interrupt
0023	RI+TI	Serial Port (UART) Interrupt
002B	TF2+EXF2	Timer2 Interrupt
0033		Reserved for ICE mode use
003B	TF3	Timer3 Interrupt
0043	P1IF	Port1 external pin change Interrupt (can wake up Stop mode)
004B	IE2	INT2 external pin Interrupt (can wake up Stop mode)

Interrupt Vector & Flag

6.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The P1WKUP SFR controls the individual Port1 pin's wake-up and interrupt capability. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

SFR **96h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1WKUP	P1WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

96h.7~0 **P1WKUP:** P1.7~P1.0 pin individual Wake-up / Interrupt enable control
0: Disable
1: Enable

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable control.
0: Disable all Interrupts.
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.5 **ET2:** Timer2 interrupt enable
0: Disable Timer2 interrupt
1: Enable Timer2 interrupt

A8h.4 **ES:** Serial Port (UART) interrupt enable
0: Disable Serial Port (UART) interrupt
1: Enable Serial Port (UART) interrupt

A8h.3 **ET1:** Timer1 interrupt enable
0: Disable Timer1 interrupt
1: Enable Timer1 interrupt

A8h.2 **EX1:** External INT1 pin Interrupt enable and Stop mode wake up enable
0: Disable INT1 pin Interrupt and Stop mode wake up
1: Enable INT1 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A8h.1 **ET0:** Timer0 interrupt enable
0: Disable Timer0 interrupt
1: Enable Timer0 interrupt

A8h.0 **EX0:** External INT0 pin Interrupt enable and Stop mode wake up enable
0: Disable INT0 pin Interrupt and Stop mode wake up
1: Enable INT0 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	–	–	–	–	–	EX2	P1IE	TM3IE
R/W	–	–	–	–	–	R/W	R/W	R/W
Reset	–	–	–	–	–	0	0	0

A9h.2 **EX2:** External INT2 pin Interrupt enable and Stop mode wake up enable
0: Disable INT2 pin Interrupt and Stop mode wake up
1: Enable INT2 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A9h.1 **P1IE:** Port1 pin change interrupt enable. This bit does not affect the Port1 pin's Stop mode wake up capability.
0: Disable Port1 pin change interrupt
1: Enable Port1 pin change interrupt

A9h.0 **TM3IE:** Timer3 interrupt enable
0: Disable Timer3 interrupt
1: Enable Timer3 interrupt

SFR **B9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

SFR **B8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

B9h.5, B8h.5 **PT2H, PT2 :** Timer2 Interrupt Priority control. (PT2H, PT2)=
11: Level 3 (highest priority)
10: Level 2
01: Level 1
00: Level 0 (lowest priority)

B9h.4, B8h.4 **PSH, PS :** Serial Port (UART) Interrupt Priority control. Definition as above.

B9h.3, B8h.3 **PT1H, PT1 :** Timer1 Interrupt Priority control. Definition as above.

B9h.2, B8h.2 **PX1H, PX1 :** External INT1 pin Interrupt Priority control. Definition as above.

B9h.1, B8h.1 **PT0H, PT0 :** Timer0 Interrupt Priority control. Definition as above.

B9h.0, B8h.0 **PX0H, PX0 :** External INT0 pin Interrupt Priority control. Definition as above.

SFR **BBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	–	–	–	–	–	PX2H	PP1H	PT3H
R/W	–	–	–	–	–	R/W	R/W	R/W
Reset	–	–	–	–	–	0	0	0

SFR **BAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	–	–	–	–	–	PX2	PP1	PT3
R/W	–	–	–	–	–	R/W	R/W	R/W
Reset	–	–	–	–	–	0	0	0

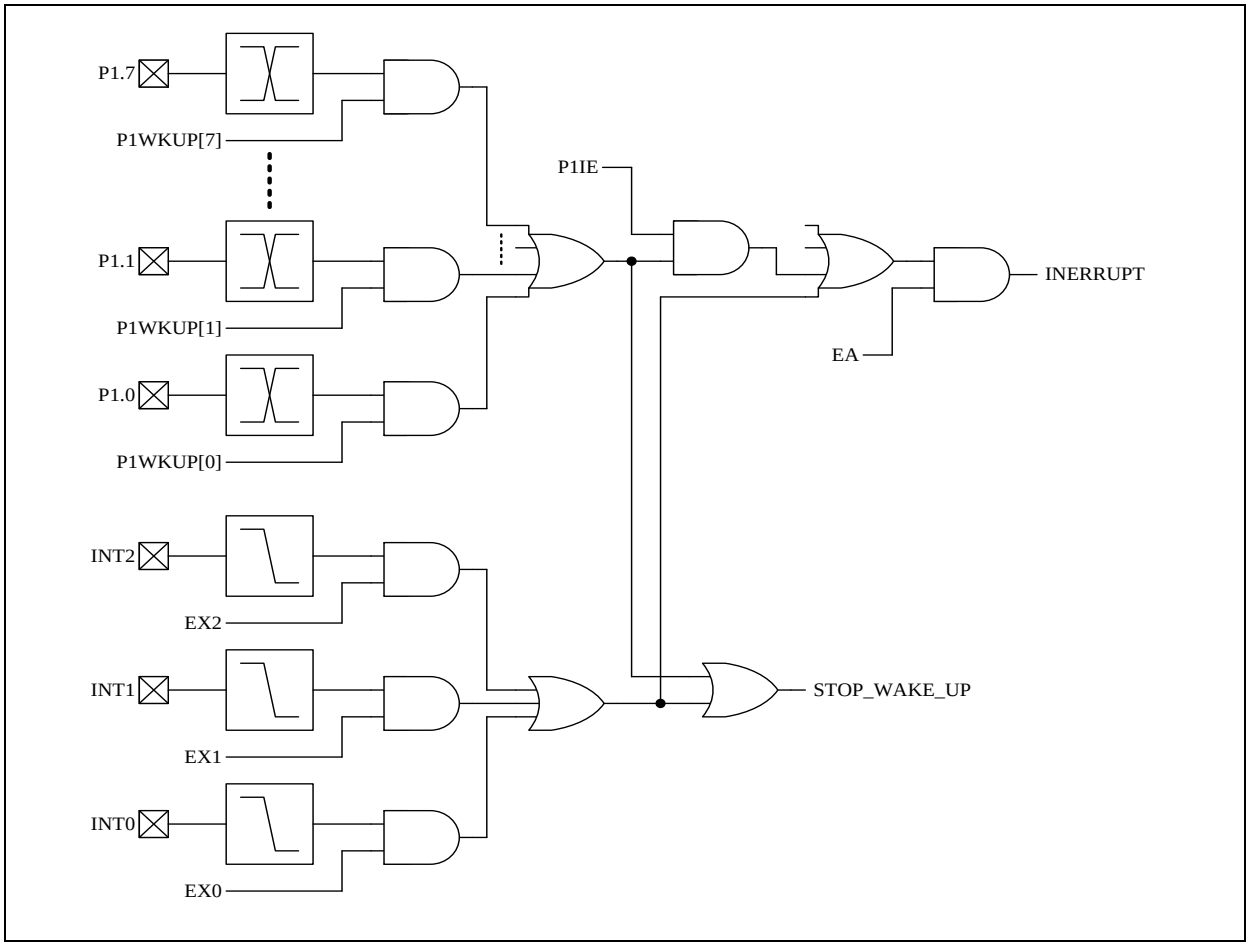
BBh.2, BAh.2 **PX2H, PX2 :** External INT2 pin Interrupt Priority control. Definition as above.

BBh.1, BAh.1 **PP1H, PP1 :** Port1 Pin Change Interrupt Priority control. Definition as above.

BBh.0, BAh.0 **PT3H, PT3 :** Timer3 Interrupt Priority control. Definition as above.

6.2 Pin Interrupt

Pin Interrupts include INT0 (P3.2), INT1 (P3.3), INT2 (P2.7) and Port1 Change Interrupt. These pins also have the Stop mode wake up capability. INT0 and INT1 are falling edge or low level triggered as the 8051 standard. INT2 is falling edge triggered, and Port1 Change Interrupt is triggered by any Port1 pin state change.



Pin Interrupt & Wake up

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag.
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin

88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	–	–	IE2	P1IF	TF3
R/W	–	–	–	–	–	R/W	R/W	R/W
Reset	–	–	–	–	–	0	0	0

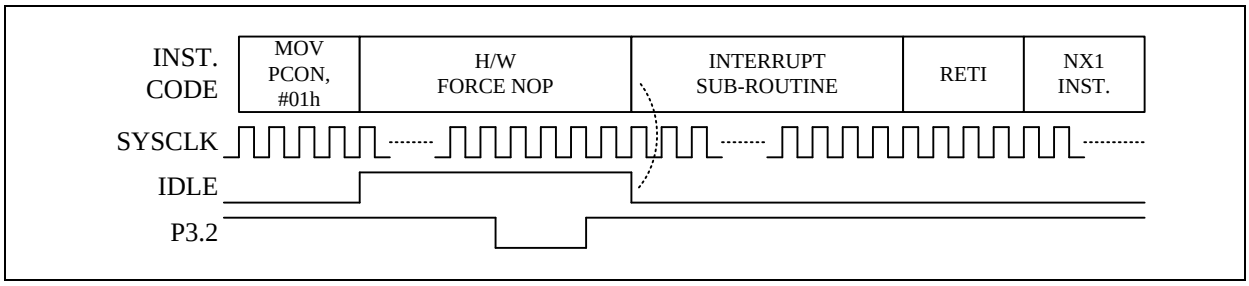
95h.2 **IE2:** External Interrupt 2 (INT2 pin) edge flag
Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FBh to INTFLG to clear this bit.

95h.1 **P1IF:** Port1 pin change interrupt flag
Set by H/W when a Port1 pin state change is detected and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FDh to INTFLG to clear this bit.

Note2: S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.

6.3 Idle mode Wake up and Interrupt

Idle mode is waked up by enabled Interrupts, which means individual interrupt enable bit (ex: EX0) and EA bit must be both set to 1 to establish Idle mode wake up capability. All enabled Interrupts (Pins, Timers and UART) can wake up CPU from Idle mode. Upon Idle wake-up, Interrupt service routine is entered immediately. "The first instruction behind IDL (PCON.0) setting" is executed after interrupt service routine return.



EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

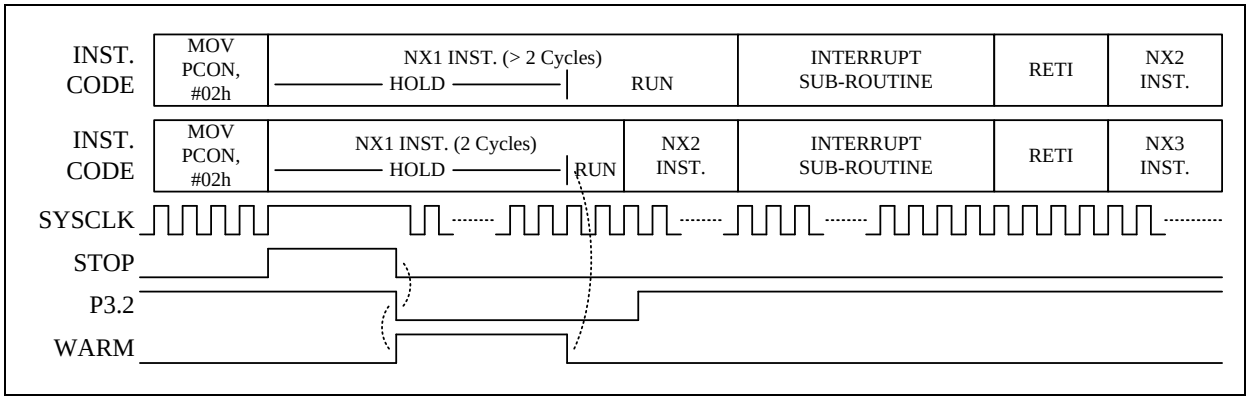
87h.1 **PD:** Power down control bit, set 1 to enter STOP mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter IDLE mode.

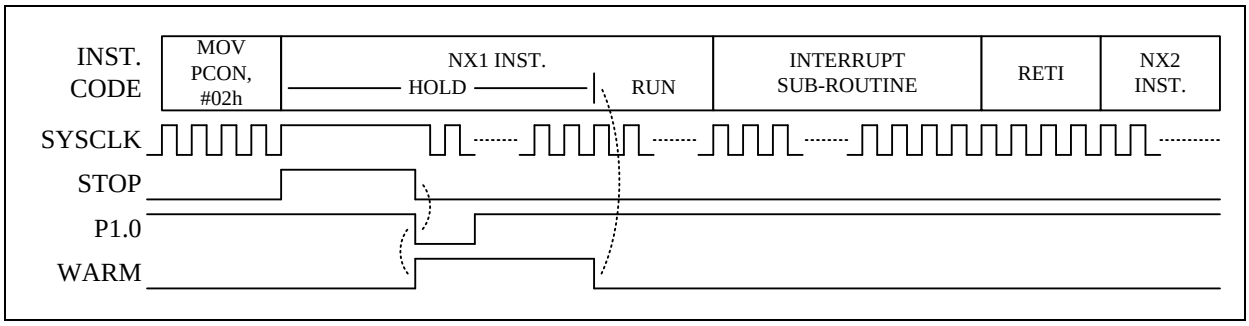
6.4 Stop mode Wake up and Interrupt

Stop mode wake up is simple, as long as the individual pin interrupt enable bit (ex: EX0) is set, the pin wake up capability is asserted. Set EX0/EX1/EX2 can enable INT0/INT1/INT2 pins' Stop mode wake up capability. Set P1WKUP bit 7~0 can enable P1.7~P1.0's Stop mode wake up capability. Upon Stop wake up, "the first instruction behind PD setting (PCON.1)" is executed immediately before Interrupt service. Interrupt entry requires EA=1 (P1WKUP also needs P1IE=1) and trigger state of the pin staying sufficiently long to be observed by the System clock. This feature allows CPU to enter or not enter Interrupt sub-routine after Stop mode wake up.

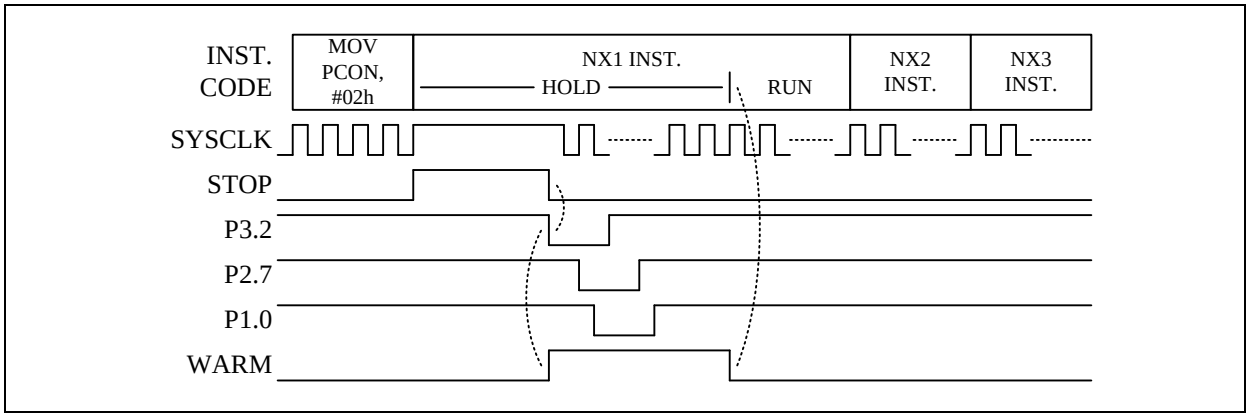
Note: Chip cannot enter Stop Mode if INTn pin is low and wakeup is enable. (INTn=0 and EXn=1, n=0,1,2)
Note: It is recommended to place the NX1/NX2 with NOP Instruction in figures below.



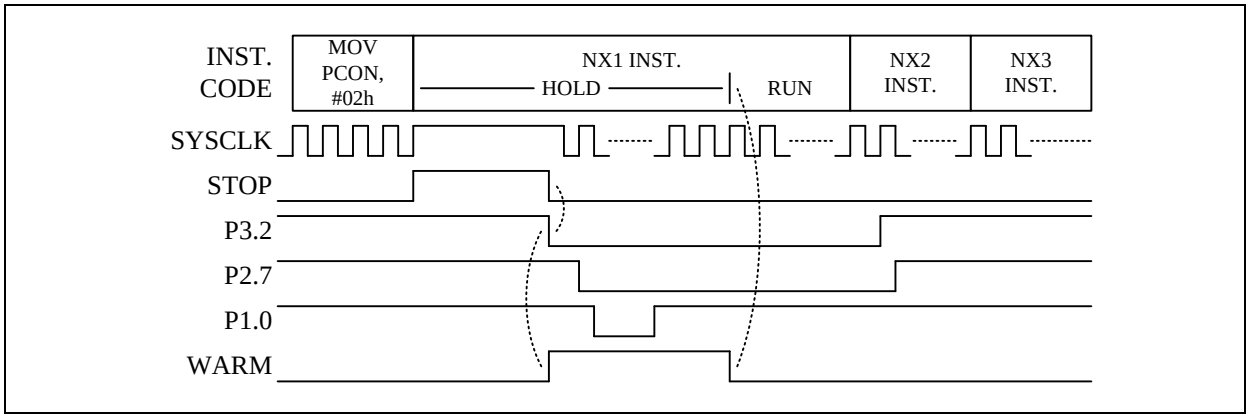
EA=EX0=1, P3.2 (INT0) is sampled after warm-up, Stop mode wake-up and Interrupt



EA=P1IE=P1WKUP=1, P1.0 change (not need clock sample), Stop mode wake-up and Interrupt



EA=EX0=EX2=P1WKUP=1, P1IE=0, Stop mode wake-up but not Interrupt. P3.2/P2.7 pulse too narrow



EX0=EX2=P1WKUP=P1IE=1, EA=0, Stop mode wake-up but not Interrupt

7. I/O Ports

The **F2260** has total 25 multi-function I/O pins. All I/O pins follow the standard 8051 "Read-Modify-Write" feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR. (ex: ANL P1, A; INC P0; CPL P3.0)

7.1 Port1 & Port3

These pins can operate in four different modes as below.

Mode	Port1, Port3 pin function		P1.n / P3.n SFR data	Pin State	Resistor Pull-up	Digital Input
	P3.0~P3.2	Others				
Mode 0	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Pull-up	Y	Y
Mode 1	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Hi-Z	N	Y
Mode 2	CMOS Output		0	Drive Low	N	N
			1	Drive High	N	N
Mode 3	Alternative Function, such as RFC and Clock output		X (don't care)	–	N	N

Port1, Port3 I/O Pin Function Table

If a Port1 or Port3 pin is used for Schmitt-trigger input, S/W must set the I/O pin to Mode0 or Mode1 and set the corresponding Port Data SFR to 1 to disable the pin's output driving circuitry.

Beside I/O port function, each Port1 and Port3 pin has one or more alternative functions, such as RFC and Clock output. Most of the functions are activated by setting the individual pin mode control SFR to Mode3. Port1/Port3 pins also have standard 8051 auxiliary definition such as INT0/1, T0/1/2, or RXD/TXD. These pin functions need to set the pin mode SFR to Mode0 or Mode1 and keep the P1.n / P3.n SFR at 1.

Pin Name	8051	Wake-up	CKO	RFC	Mode3
P1.0	T2	Y	T2O		T2O
P1.1	T2EX	Y			
P1.2		Y			
P1.3		Y			
P1.4		Y		RFC0R	RFC0R
P1.5		Y		RFC1R	RFC1R
P1.6		Y		RFC2R	RFC2R
P1.7		Y		RFCX	RFCX
P3.0	RXD				
P3.1	TXD				
P3.2	INT0	Y			
P3.3	INT1	Y			
P3.4	T0				
P3.5	T1		T1O		T1O
P3.6			T1B		T1B
P3.7			TCO		TCO

Port1, Port3 multi-function Table

The necessary SFR setting for Port1/Port3 pin's alternative functions is list below.

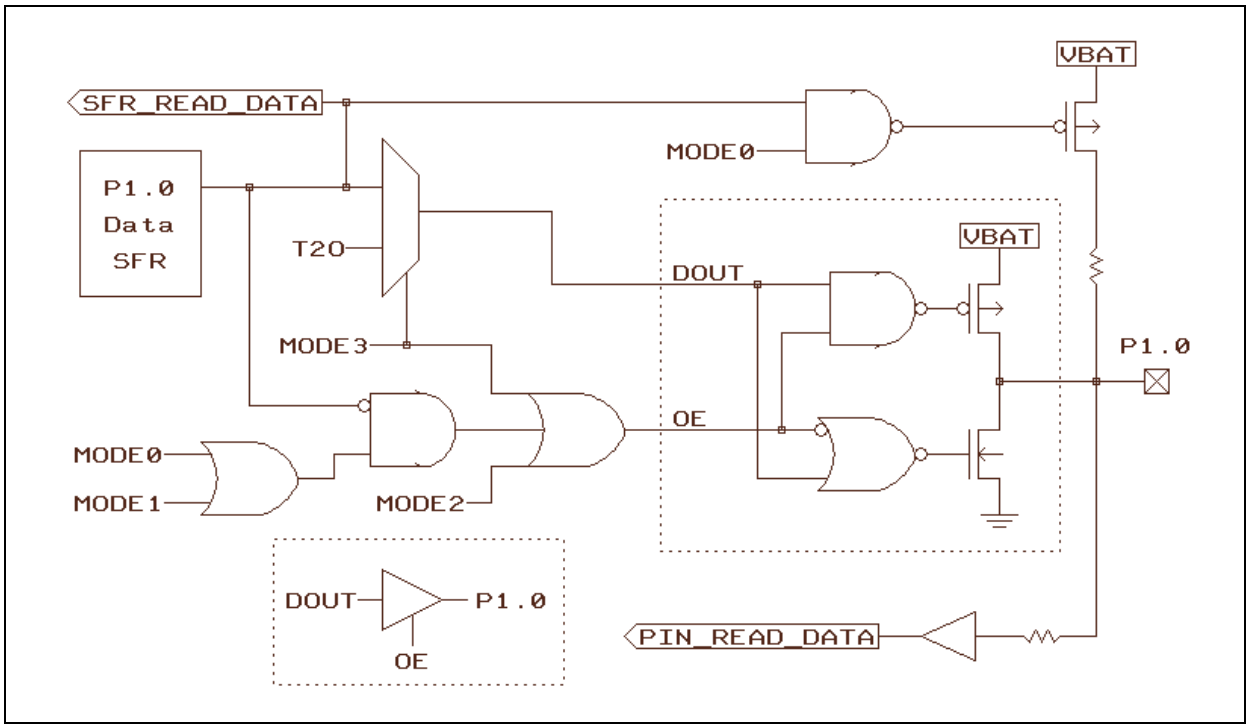
Alternative Function	Mode	P1.n / P3.n SFR data	Pin State
T0, T1, T2, T2EX, INT0, INT1	**0**	1	Input with Pull-up
	1	1	Input
RXD, TXD	**0**	1	Input with Pull-up / Pseudo Open Drain Output
	1	1	Input / Pseudo Open Drain Output
TCO, T1O, T1B, T2O	**3**	X	Clock Output (CMOS Push-Pull)
RFCX, RFC0R~RFC2R	**3**	X	RFC clock oscillating

Mode Setting for Port1, Port3 Alternative Function

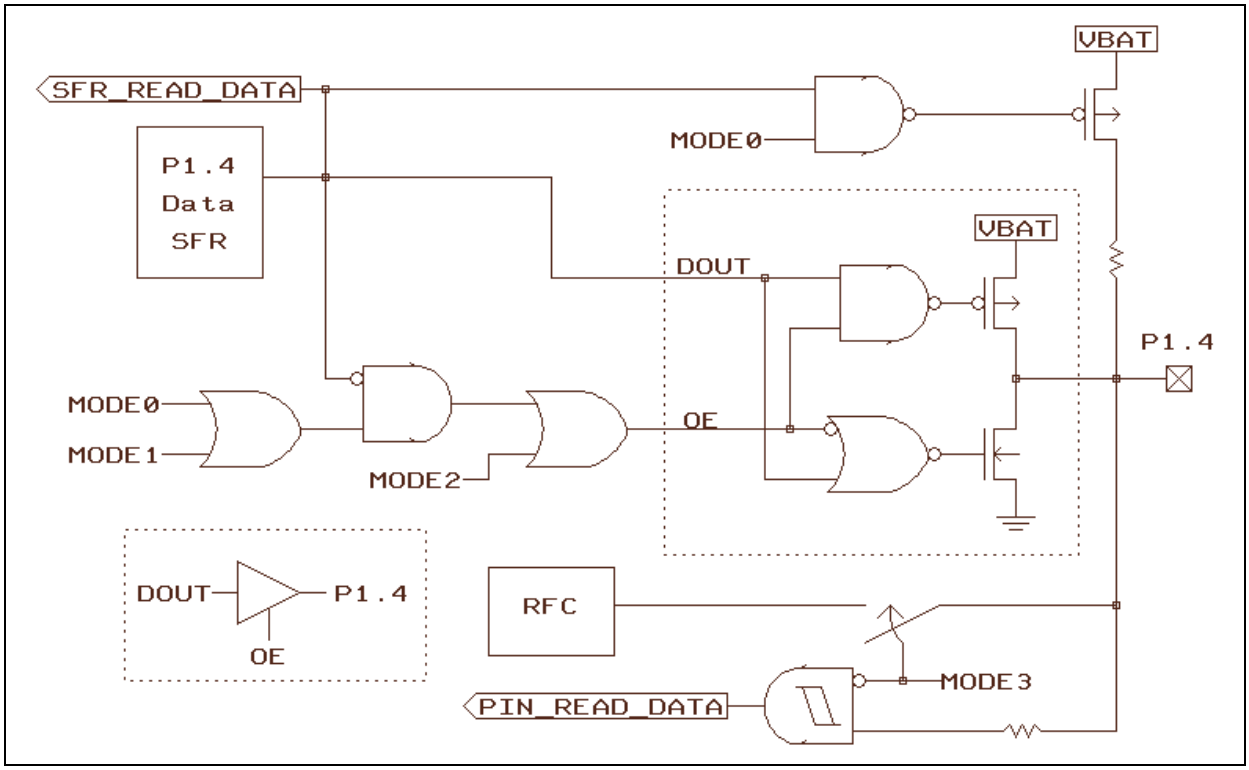
For tables above, a "**CMOS Output**" pin means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.

An "**Open Drain**" pin means it can sink at least 4mA current but only drive a small current (< 20uA). It can be used as input or output function and typically needs an external pull up resistor.

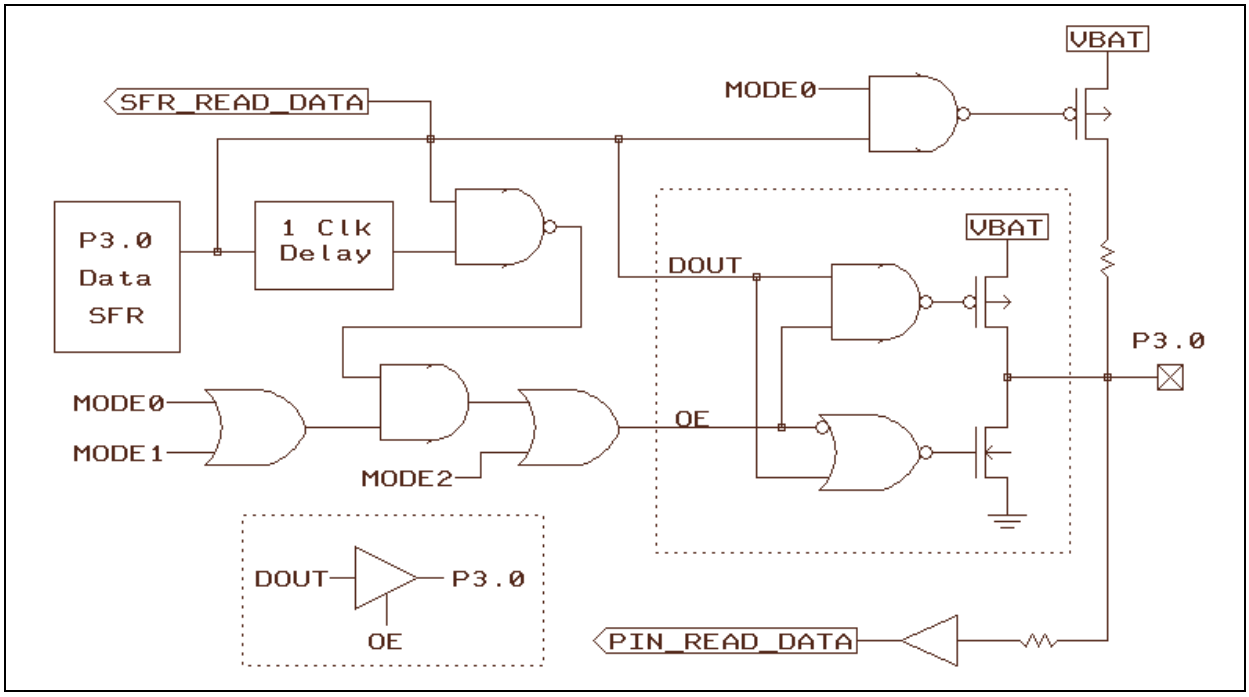
An 8051 standard pin is a "**Pseudo Open Drain**" pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 1~2 clock cycle when output transits from low to high, then keeps driving a small current (< 20uA) to maintain the pin at high level. It can be used as input or output function.



P1.0 Pin Structure



P1.4 Pin Structure



P3.0 Pin Structure

SFR **90h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

90h.7~0 **P1:** Port1 data

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.7~0 **P3:** Port3 data

SFR **A2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A2h.7~6 **P1MOD3:** P1.3 pin control.
00: Mode0
01: Mode1
10: Mode2
11: not used

A2h.5~4 **P1MOD2:** P1.2 pin control.
00: Mode0
01: Mode1
10: Mode2
11: not used

A2h.3~2 **P1MOD1:** P1.1 pin control.
00: Mode0
01: Mode1
10: Mode2
11: not used

A2h.1~0 **P1MOD0:** P1.0 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.0 is “Timer2 overflow divided by 2/3/4” (T2O) CMOS push pull output.

SFR **A3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A3h.7~6 **P1MOD7:** P1.7 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.7 is RFC clock input pin (RFCX)

A3h.5~4 **P1MOD6:** P1.6 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.6 is RFC resistor connection pin (RFC2R)

A3h.3~2 **P1MOD5:** P1.5 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.5 is RFC resistor connection pin (RFC1R)

A3h.1~0 **P1MOD4:** P1.4 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.4 is RFC resistor connection pin (RFC0R)

SFR **A4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A4h.7~6 **P3MOD3:** P3.3 pin control.
00: Mode0
01: Mode1
10: Mode2
11: not used

A4h.5~4 **P3MOD2:** P3.2 pin control.
00: Mode0
01: Mode1
10: Mode2
11: not used

A4h.3~2 **P3MOD1:** P3.1 pin control.
00: Mode0
01: Mode1
10: Mode2
11: not used

A4h.1~0 **P3MOD0:** P3.0 pin control.
00: Mode0
01: Mode1
10: Mode2
11: not used

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A5h.7~6 **P3MOD7:** P3.7 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.7 is “SYSCLK divided by 1/2/3/4” (TCO) CMOS push pull output.

A5h.5~4 **P3MOD6:** P3.6 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.6 is “Negative Timer1 overflow divided by 2/3/4” (T1B) CMOS push pull output.

A5h.3~2 **P3MOD5:** P3.5 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.5 is “Positive Timer1 overflow divided by 2/3/4” (T1O) CMOS push pull output.

A5h.1~0 **P3MOD4:** P3.4 pin control.
00: Mode0
01: Mode1
10: Mode2
11: not used

7.2 P2.7

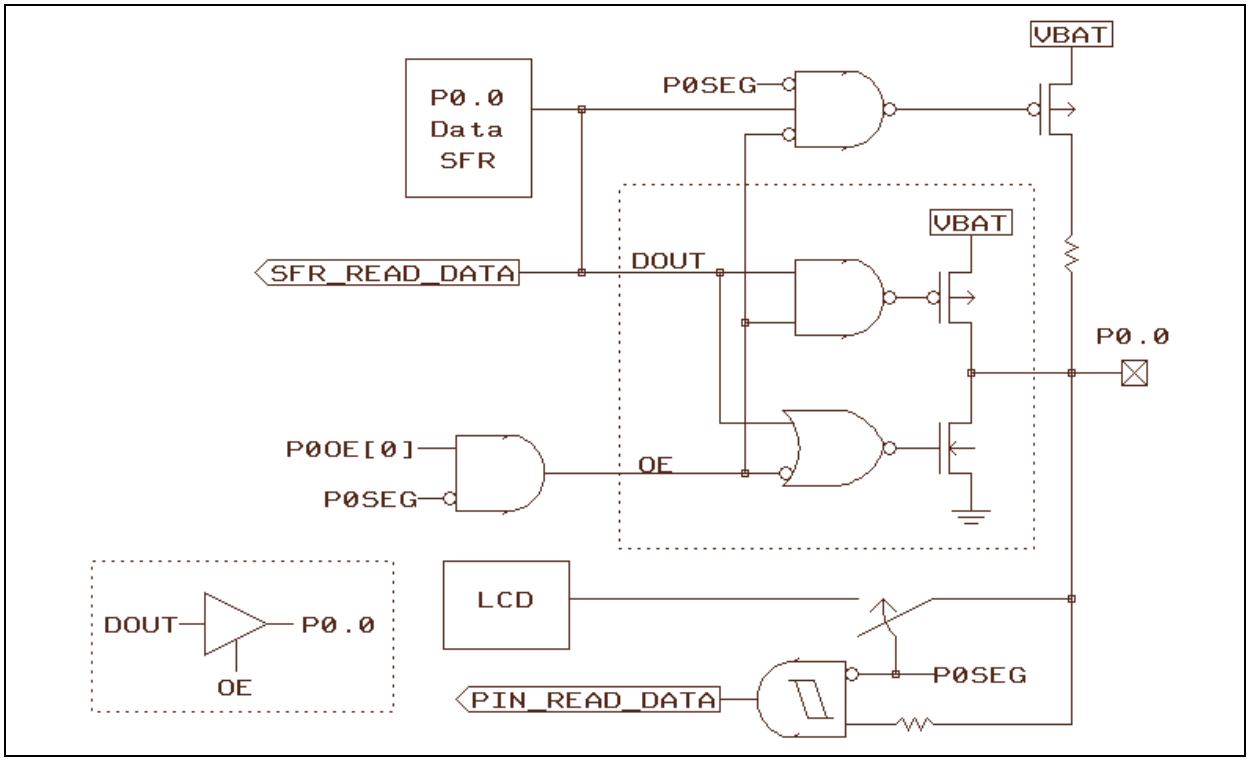
P2.7 can be only used as Schmitt-trigger input or open-drain output, with pull-up resistor always enable. P2.7 pin is shared with RSTn, INT2 and Flash VPP function.

7.3 Port0

Port0 pins are shared with LCD segment pins. The pin's LCD mode is controlled by P0SEG SFR. If a Port0 pin is defined as I/O pin, it can be used as CMOS push-pull output or Schmitt-trigger input. The pin's pull up function is enable while SFR bit P0OE.n=0 and P0.n=1.

Port0 pin function	P0OE.n	P0.n SFR data	Pin State	Resistor Pull-up	Digital Input
Input	0	0	Hi-Z	N	Y
	0	1	Pull-up	Y	Y
CMOS Output	1	0	Drive Low	N	N
	1	1	Drive High	N	N

Port0 I/O Pin Function Table



P0.0 Pin Structure

SFR **80h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

80h.7~0 **P0:** Port0 data, also controls the P0.n pin's pull-up function. If the P0.n SFR data is "1" and the corresponding P0OE.n=0 (input mode), the pull-up is enabled.

SFR **A0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.7 **P2.7:** P2.7 data, 0=Open Drain output low, 1=Schmitt-trigger input with pull up

A0h.6~0 **P2.6~P2.0:** General purpose register.

SFR **91h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0OE	P0OE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

91h.7~0 **P0OE:** Port0 CMOS Push-Pull output enable control, 1=Enable.

SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCON	DSPON	LCDCLK	LCDFMR		LCDUTY	P0SEG		
R/W	R/W	R/W	R/W		R/W	R/W		
Reset	0	0	1	0	1	1	1	1

B1h.2~0 **P0SEG:** Port0 LCD mode control.

000: P0.0~P0.7 are I/O pins
001: P0.0~P0.5 are I/O pins, P0.6~P0.7 are LCD Segment pins
010: P0.0~P0.4 are I/O pins, P0.5~P0.7 are LCD Segment pins
011: P0.0~P0.3 are I/O pins, P0.4~P0.7 are LCD Segment pins
100: P0.0~P0.2 are I/O pins, P0.3~P0.7 are LCD Segment pins
101: P0.0~P0.1 are I/O pins, P0.2~P0.7 are LCD Segment pins
110: P0.0 is I/O pin, P0.1~P0.7 are LCD Segment pins
111: P0.0~P0.7 are LCD Segment pins

8. Timers

Timer0, Timer1 and Timer2 are provided as standard 8051 compatible timer/counter. Timer3 is provided for a real-time clock count. Compare to the traditional 12T 8051, the chip's Timer0/1/2 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every "2 System clock" rate; in counter mode, T0/T1/T2 pin input pulse must be wider than 2 System clock to be seen by this device. In addition to the standard 8051 timers function, the T1O and T1B pin can output the positive and negative "Timer1 overflow divided by 2/3/4" signal, and the T2O pin can output the "Timer2 overflow divided by 2/3/4" signal. These outputs can be used for Buzzer application. Timer0's extra utility is to supports RFC. The RFC clock divided by 1/4/16/64 signal can replace T0 pin as the Timer0's event count input.

8.1 Timer0 / Timer1

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs

88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR **89h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set

89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin's negative edge

89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops

89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

89h.2 **CT0N:** Timer0 Counter/Timer select bit
0: Timer mode, Timer0 data increases at 2 System clock cycle rate
1: Counter mode, Timer0 data increases at T0 pin's negative edge

89h.1~0 **TMOD0:** Timer0 mode select
00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR **8Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR **8Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

SFR **8Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

SFR **8Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

SFR **AFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCON	–	–	–	T0RFC	RFCPSC		RFCS	
R/W	–	–	–	R/W	R/W		R/W	
Reset	–	–	–	0	1	1	0	0

AFh.4 **T0RFC:** Timer0 Counter mode (CT0N=1) input select
0: T0 (P3.4) pin
1: RFC Clock divided by 1/4/16/64

AFh.3~2 **RFCPSC:** RFC clock divider to Timer0
00: divided by 64
01: divided by 16
10: divided by 4
11: divided by 1

8.2 Timer2

Timer2 is controlled through the TCON2 register with the low and high bytes of Timer/Counter2 stored in TL2 and TH2 and the low and high bytes of the Timer2 reload/capture registers stored in RCAP2L and RCAP2H.

SFR **C8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

C8h.7 **TF2:** Timer2 overflow flag
Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.

C8h.6 **EXF2:** T2EX interrupt pin falling edge flag
Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.

C8h.5 **RCLK:** UART receive clock control bit
0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3
1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3

C8h.4 **TCLK:** UART transmit clock control bit
0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3
1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3

C8h.3 **EXEN2:** T2EX pin enable
0: T2EX pin disable
1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0

C8h.2 **TR2:** Timer2 run control
0: Timer2 stops
1: Timer2 runs

C8h.1 **CT2N:** Timer2 Counter/Timer select bit
0: Timer mode, Timer2 data increases at 2 System clock cycle rate
1: Counter mode, Timer2 data increases at T2 pin's negative edge

C8h.0 **CPRL2N:** Timer2 Capture/Reload control bit
0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1.
1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1.
If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.

SFR **CAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2L	RCP2L							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CAh.7~0 **RCP2L:** Timer2 reload/capture data low byte

SFR **CBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2H	RCP2H							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CBh.7~0 **RCP2H:** Timer2 reload/capture data high byte

SFR **CCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL2	TL2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CCh.7~0 **TL2:** Timer2 data low byte

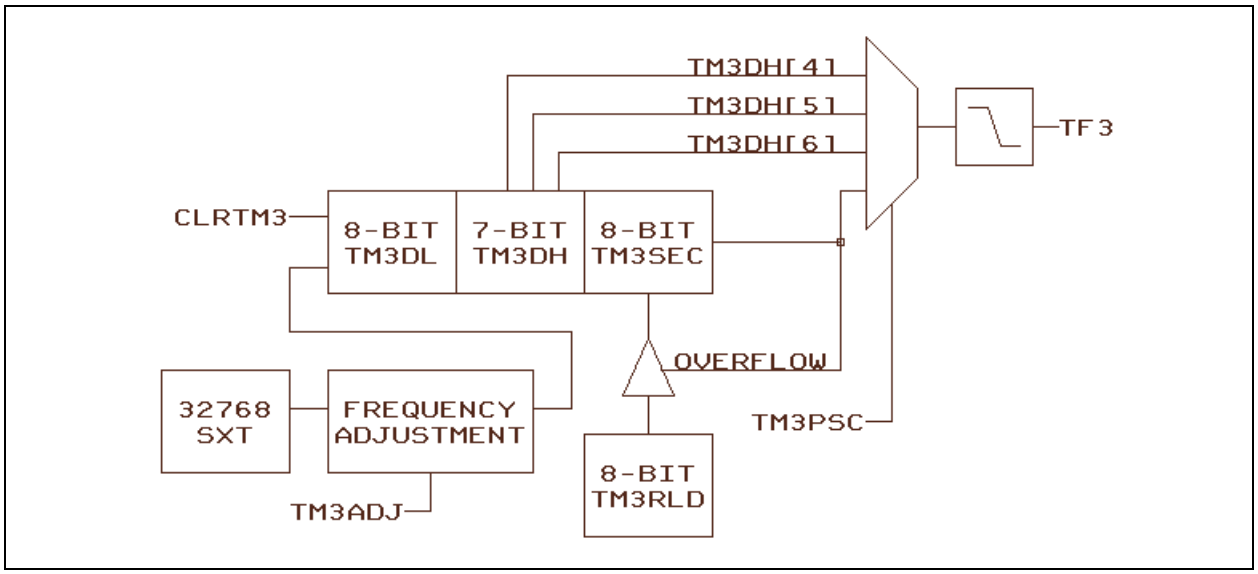
SFR **CDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH2	TH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CDh.7~0 **TH2:** Timer2 data high byte

8.3 Timer3

The 23-bit wide Timer3 is reloadable for its 8-bit MSB when overflow. Its time base is 32768Hz SXT clock. Timer3 can generate interrupt periodically at different rate, and its counting data can be read out by CPU. However, while CPU clock is switched to FRC or RFC, the clock source of CPU and Timer3 are different, CPU may read a "under changing Timer3 data". User F/W must have some filter mechanism to avoid such kind un-stability. On the contrast, Timer3 interrupt has no ambiguous behavior no matter what the CPU clock source is.

Timer3 can control its counting rate by the TM3ADJ SFR. This feature compensates the 32768 SXT crystal's in-accuracy. While TM3ADJ=0, Timer3 increase its data count normally at each SXT clock cycle. If TM3ADJ is set to positive adjustment, Timer3 increase its data count by 2 in particular SXT cycles, resulting a faster counting rate. If TM3ADJ is set to negative adjustment, Timer3 stop increase in particular SXT cycles, resulting a slower counting rate. The adjustment is 0.477ppm per step, and the total adjustable range is ± 61ppm.



Timer3 Structure

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	–	–	–	–	CLRWDT	CLRTM3	STPRFC	DPSEL
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

F8h.2 **CLRTM3:** Set 1 to Clear Timer3

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	CMPO	CMPVS			UART1W	WDTPSC	TM3PSC	
R/W	R	R/W			R/W	R/W	R/W	
Reset	–	0	0	0	0	0	0	1

94h.1~0 **TM3PSC:** Timer3 Interrupt rate

00: Timer3 interrupt occurs when 23 bit count data overflow

01: Timer3 interrupt is 1.0 second rate (32768 SXT cycles)

10: Timer3 interrupt is 0.5 second rate (16384 SXT cycles)

11: Timer3 interrupt is 0.25 second rate (8192 SXT cycles)

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	–	–	–	–	–	IE2	P1IF	TF3
R/W	–	–	–	–	–	R/W	R/W	R/W
Reset	–	–	–	–	–	0	0	0

95h.0 **TF3:** Timer3 Interrupt Flag

Set by H/W when Timer3 reaches TM3PSC setting cycles. Cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit. (***Note2***)

SFR **B3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3SEC	TM3SEC							
R/W	R							
Reset	–	–	–	–	–	–	–	–

B3h.7~0 **TM3SEC:** Timer3 count data bit 22~15

SFR **B4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3DL	TM3DL							
R/W	R							
Reset	–	–	–	–	–	–	–	–

B4h.7~0 **TM3DL:** Timer3 count data bit 7~0

SFR **B5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3DH	–	TM3DH						
R/W	–	R						
Reset	–	–	–	–	–	–	–	–

B5h.6~0 **TM3DH:** Timer3 count data bit 14~8

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3RLD	TM3RLD							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

B6h.7~0 **TM3RLD:** Timer3 overflow reload data for Timer3 bit 22~15 (TM3SEC)

SFR **B7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3ADJ	TM3ADJS	TM3ADJ						
R/W	R/W	R/W						
Reset	0	0	0	0	0	0	0	0

B7h.7 **TM3ADJS:** Timer3 adjustment sign

0: Timer3 positive adjust, to increase Timer3 counting rate

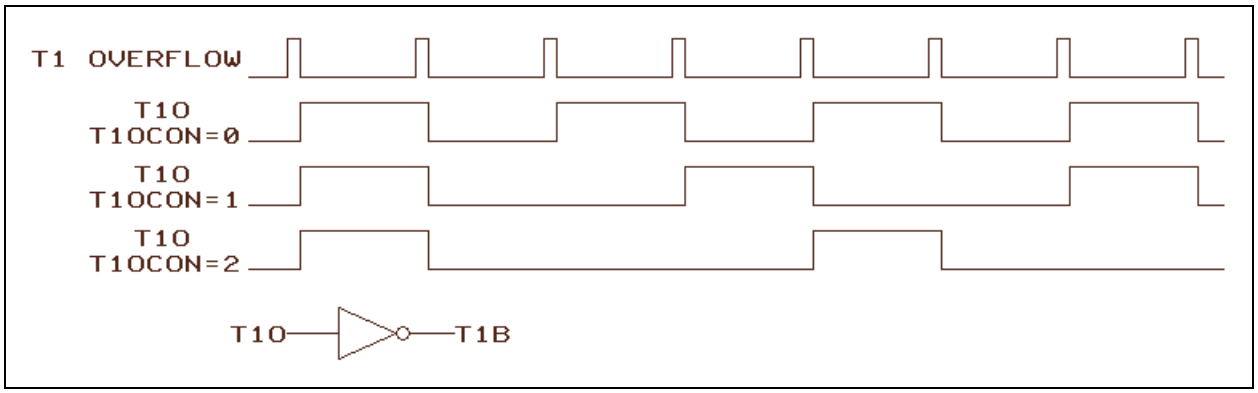
1: Timer3 negative adjust, to decrease Timer3 counting rate

B7h.6~0 **TM3ADJ:** Timer3 adjust magnitude, 0.477 ppm per LSB.

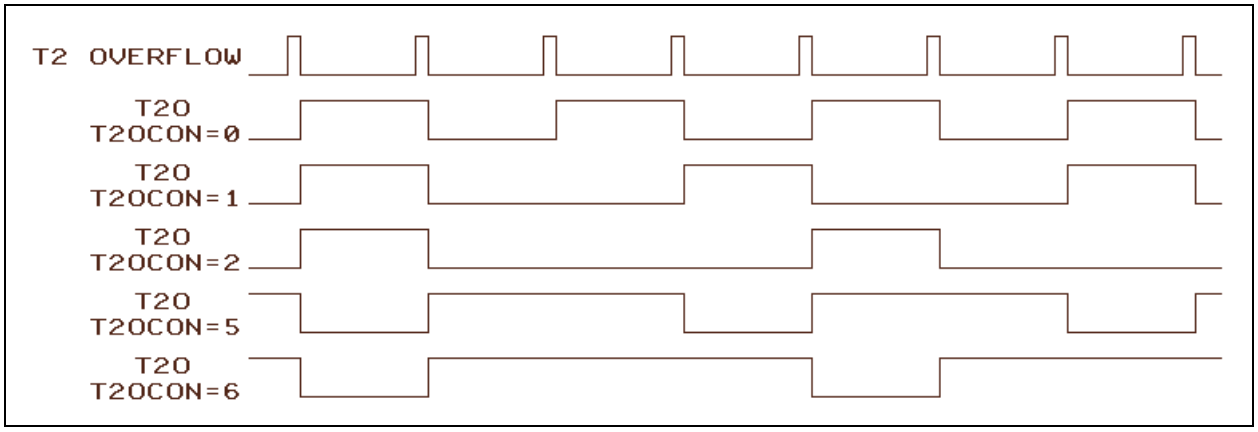
The adjustment is calculated as ±TM3ADJ*0.477ppm. The total adjustable range is ± 61ppm.

8.4 T1O, T1B and T2O output Control

This device can generate various frequency or duty cycle waveform output (in CMOS push pull format) for Buzzer or Remote IR control application. The T1O, T1B and T2O waveform is derived by Timer1 / Timer2 overflow signal. User can control their frequency by Timers auto reload value, as well as set their duty cycle by TOCON SFR. The pin output function is enabled by setting the P3MODH SFR to Mode3 for each pin (***see Section 7***).



T1O, T1B waveform with T1OCON



T2O waveform with T2OCON

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TOCON	T1OCON		T2OCON			TCOCON		
R/W	R/W		R/W			R/W		
Reset	0	0	0	0	0	0	0	0

A6h.7~6 **T1OCON:** T1O pin duty and frequency control
00: 1/2 duty, 1/2 Timer1 overflow frequency
01: 1/3 duty, 1/3 Timer1 overflow frequency
10: 1/4 duty, 1/4 Timer1 overflow frequency

A6h.5~3 **T2OCON:** T2O pin duty and frequency control
000: 1/2 duty, 1/2 Timer2 overflow frequency
001: 1/3 duty, 1/3 Timer2 overflow frequency
010: 1/4 duty, 1/4 Timer2 overflow frequency
101: 2/3 duty, 1/3 Timer2 overflow frequency
110: 3/4 duty, 1/4 Timer2 overflow frequency

Note6: also refer to Section 6 for more information about Timer0/1/2/3 Interrupt enable and priority.

9. UART

The UART uses SCON and SBUF SFRs. SCON is the control register, SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are completely independent. In addition to standard 8051's full duplex mode, this chip also provides one wire mode. If the UART1W bit is set, both transmit and receive data use P3.1 pin.

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.7 **SMOD:** UART double baud rate control bit
0: Disable UART double baud rate
1: Enable UART double baud rate

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	CMPO	CMPVS			UART1W	WDTPSC	TM3PSC	
R/W	R	R/W			R/W	R/W	R/W	
Reset	–	0	0	0	0	0	0	1

94h.3 **UART1W:** One wire UART mode enable, both TXD/RXD use P3.1 pin
0: Disable one wire UART mode
1: Enable one wire UART mode

SFR **98h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** Serial port mode select bit 0,1
00: Mode0: 8 bit shift register, Baud Rate = F_{SYSCLK} / 2
01: Mode1: 8 bit UART, Baud Rate is variable
10: Mode2: 9 bit UART, Baud Rate = F_{SYSCLK} / 32 or / 64
11: Mode3: 9 bit UART, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2
SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART reception enable
0: Disable reception
1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR **99h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

99h.7~0 **SBUF:** UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

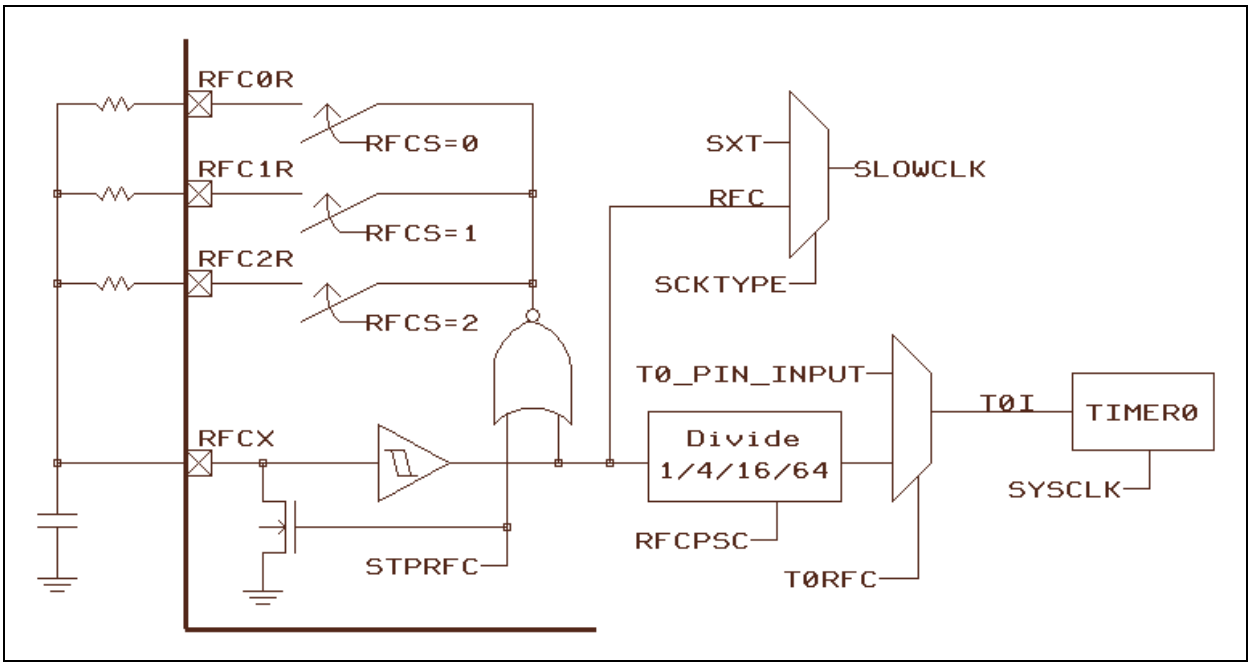
F_{SYSCLK} denotes System clock frequency, the UART baud rate is calculated as below.

- **Mode 0:**
  Baud Rate = F_{SYSCLK} / 2
- **Mode 1, 3:** if using Timer1 auto reload mode
  Baud Rate = (SMOD + 1) x F_{SYSCLK} / (32 x 2 x (256 – TH1))
- **Mode 1, 3:** if using Timer2
  Baud Rate = Timer2 overflow rate / 16 = F_{SYSCLK} / (32 x (65536 – RCP2H, RCP2L))
- **Mode 2:**
  Baud Rate = (SMOD + 1) x F_{SYSCLK} / 64

Note6: also refer to Section 6 for more information about UART Interrupt enable and priority.
Note8: also refer to Section 8 for more information about how Timer2 controls UART clock.

10. Resistance to Frequency Converter (RFC)

The RFC module can build the RC oscillation circuitry with RFCX pin and RFC0R, RFC1R or RFC2R pins. Only one RC oscillation circuitry is active at a time. There are 2 methods to measure the RFC clock frequency. One is to set the RFC as the Timer0 Counter mode input, the other one is to set RFC as the SYSCLK and assign Timer0, 1 or 2 running with timer mode. Since Timer3's clock source is the precise 32768 SXT, compare the Timer which running by RFC with Timer3's data/interrupt, user can derive the RFC frequency.



RFC Structure

SFR **AFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCON	–	–	–	T0RFC	RFCPSC		RFCS	
R/W	–	–	–	R/W	R/W		R/W	
Reset	–	–	–	0	1	1	0	0

AFh.4 **T0RFC:** Timer0 Counter mode (CT0N=1) input select
0: T0 (P3.4) pin
1: RFC Clock divided by 1/4/16/64

AFh.3~2 **RFCPSC:** RFC clock divider to Timer0
00: divided by 64
01: divided by 16
10: divided by 4
11: divided by 1

AFh.1~0 **RFCS:** Select RFC convert channel.
00: RFC0R (P1.4)
01: RFC1R (P1.5)
10: RFC2R (P1.6)

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	–	–	–	–	CLRWDT	CLRTM3	STPRFC	DPSEL
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

F8h.1 **STPRFC:** Set 1 to stop RFC clock oscillating

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	SXTGAIN		STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W		R/W	R/W	R/W	R/W	
Reset	0	1	1	0	0	1	1	1

D8h.7 **SCKTYPE:** Slow clock Type. This bit can be changed only in Fast mode (SELFCK=1).
0: SXT
1: RFC, Software must setup RFC oscillating circuitry before set this bit to 1.

SFR **A3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A3h.7~6 **P1MOD7:** P1.7 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.7 is RFC clock input pin (RFCX)

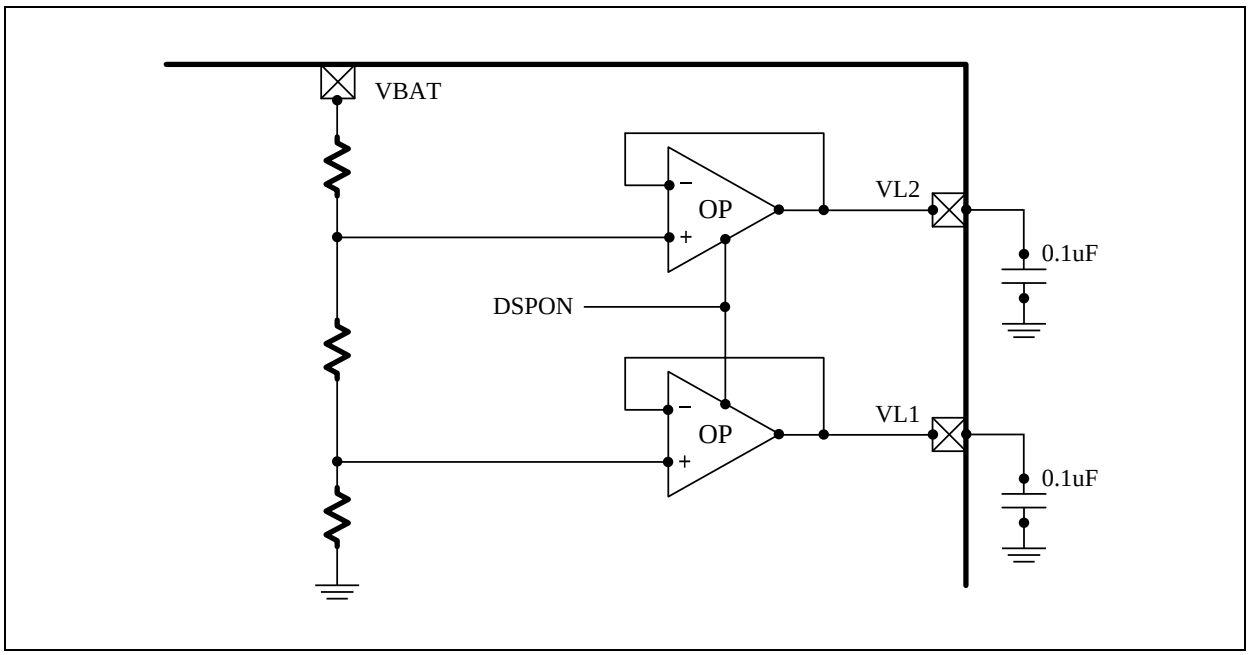
A3h.5~4 **P1MOD6:** P1.6 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.6 is RFC resistor connection pin (RFC2R)

A3h.3~2 **P1MOD5:** P1.5 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.5 is RFC resistor connection pin (RFC1R)

A3h.1~0 **P1MOD4:** P1.4 pin control.
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.4 is RFC resistor connection pin (RFC0R)

11. LCD Driver

The LCD Driver is capable of driving the LCD panel with maximum 144 dots by 4 Commons and 36 Segments. The VL1/VL2 LCD Bias voltage is divided from V_{BAT} by 3 identical resistors. Therefore, the VL1 and VL2 voltage level always equal to $V_{BAT}/3$ and $V_{BAT}*2/3$. The LCD Clock can be driven by SXT or FRC. If SXT is the clock source, the LCD Frame rate ranges from 43Hz to 98Hz depends on LCD Duty and LCDFRM. If FRC is the LCD clock source, the V_{DD} voltage level would affect the FRC frequency and LCD Frame rate. The LCDRAM is located in the 8051's External Data Memory space, addressing from F000h to F011h.



LCD Driver Structure

LCD Frame Rate (Hz)	LCDFMR (SFR B1h.5~4)			
	00	01	10	11
1/3 Duty	57	68	85	98
1/4 Duty	43	51	64	73

LCD Frame Rate when LCDCLK = SXT

SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCON	DSPON	LCDCLK	LCDFMR		LCDUTY	P0SEG		
R/W	R/W	R/W	R/W		R/W	R/W		
Reset	0	0	1	0	1	1	1	1

B1h.7 **DSPON:** LCD display enable control
0: LCD disable
1: LCD enable

B1h.6 **LCDCLK:** LCD clock source
0: SXT
1: FRC/64

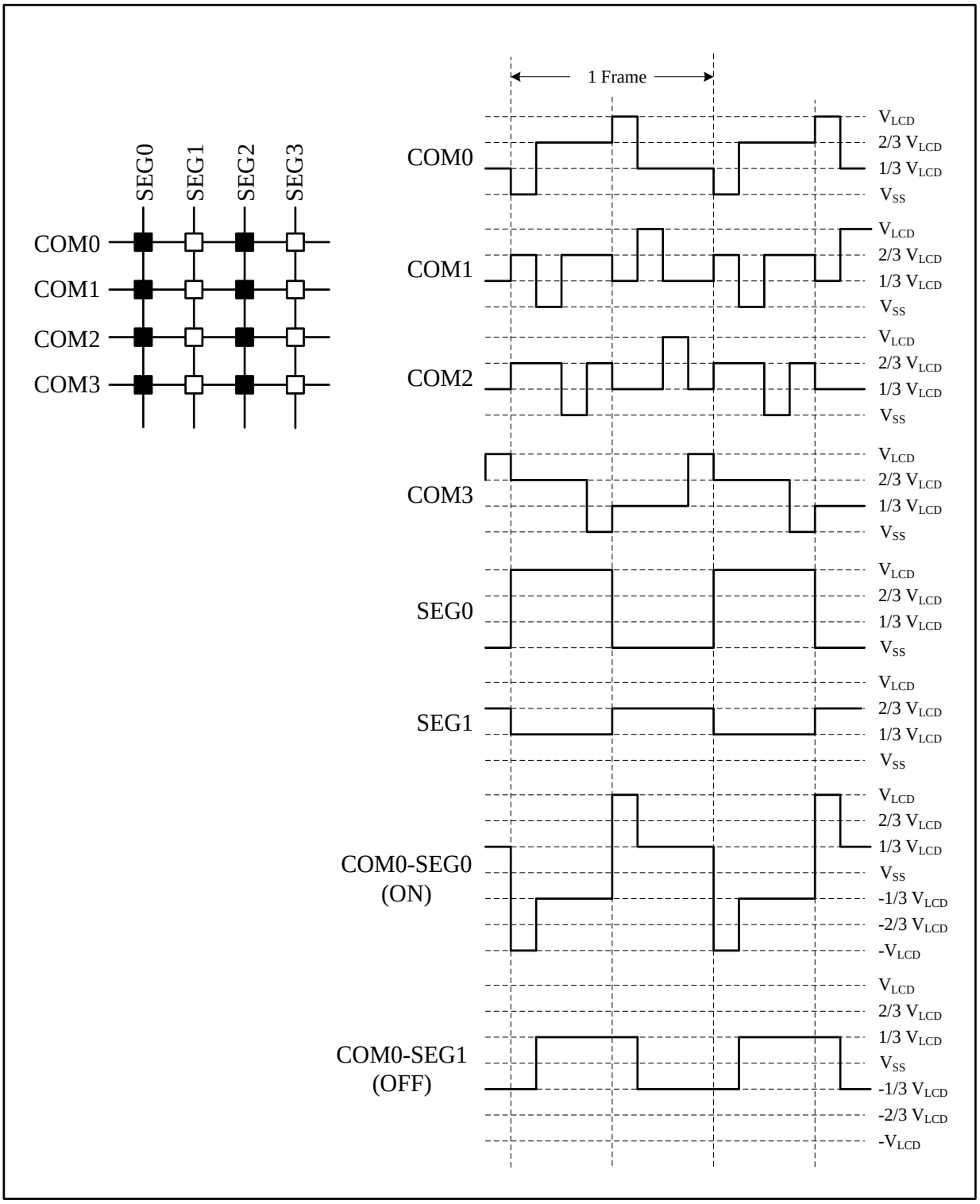
B1h.5~4 **LCDFMR:** LCD Frame rate control. If LCDCLK=0, SXT is the LCD clock source, the accurate LCD frame rate is listed in the table above. If LCDCLK=1, FRC provides LCD clock source, user should consider the FRC's frequency variation with V_{DD} voltage.

B1h.3 **LCDUTY:** LCD Duty control
0: 1/3 Duty
1: 1/4 Duty

B1h.2~0 **P0SEG:** Port0 LCD mode control.
000: P0.0~P0.7 are I/O pins
001: P0.0~P0.5 are I/O pins, P0.6~P0.7 are LCD Segment pins
010: P0.0~P0.4 are I/O pins, P0.5~P0.7 are LCD Segment pins
011: P0.0~P0.3 are I/O pins, P0.4~P0.7 are LCD Segment pins
100: P0.0~P0.2 are I/O pins, P0.3~P0.7 are LCD Segment pins
101: P0.0~P0.1 are I/O pins, P0.2~P0.7 are LCD Segment pins
110: P0.0 is I/O pin, P0.1~P0.7 are LCD Segment pins
111: P0.0~P0.7 are LCD Segment pins

	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
Adr	bit7	Bit6	Bit5	Bit4	Bit3	Bit2	bit1	bit0
F000	SEG1	SEG1	SEG1	SEG1	SEG0	SEG0	SEG0	SEG0
F001	SEG3	SEG3	SEG3	SEG3	SEG2	SEG2	SEG2	SEG2
F002	SEG5	SEG5	SEG5	SEG5	SEG4	SEG4	SEG4	SEG4
F003	SEG7	SEG7	SEG7	SEG7	SEG6	SEG6	SEG6	SEG6
F004	SEG9	SEG9	SEG9	SEG9	SEG8	SEG8	SEG8	SEG8
F005	SEG11	SEG11	SEG11	SEG11	SEG10	SEG10	SEG10	SEG10
F006	SEG13	SEG13	SEG13	SEG13	SEG12	SEG12	SEG12	SEG12
F007	SEG15	SEG15	SEG15	SEG15	SEG14	SEG14	SEG14	SEG14
F008	SEG17	SEG17	SEG17	SEG17	SEG16	SEG16	SEG16	SEG16
F009	SEG19	SEG19	SEG19	SEG19	SEG18	SEG18	SEG18	SEG18
F00A	SEG21	SEG21	SEG21	SEG21	SEG20	SEG20	SEG20	SEG20
F00B	SEG23	SEG23	SEG23	SEG23	SEG22	SEG22	SEG22	SEG22
F00C	SEG25	SEG25	SEG25	SEG25	SEG24	SEG24	SEG24	SEG24
F00D	SEG27	SEG27	SEG27	SEG27	SEG26	SEG26	SEG26	SEG26
F00E	SEG29	SEG29	SEG29	SEG29	SEG28	SEG28	SEG28	SEG28
F00F	SEG31	SEG31	SEG31	SEG31	SEG30	SEG30	SEG30	SEG30
F010	SEG33	SEG33	SEG33	SEG33	SEG32	SEG32	SEG32	SEG32
F011	SEG35	SEG35	SEG35	SEG35	SEG34	SEG34	SEG34	SEG34

LCD RAM (External Data Memory)

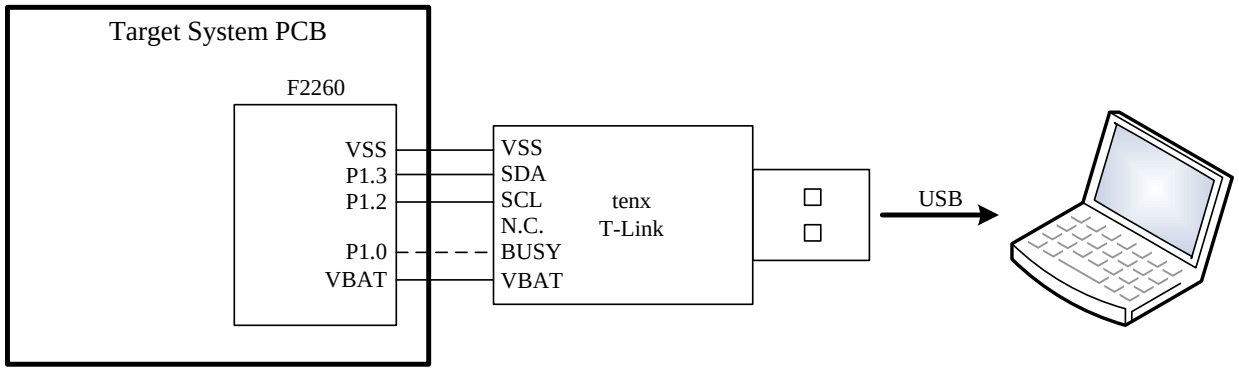


LCD Waveform, 1/3 Bias, 1/4 Duty, (VLCD = 3*VL1)

12. In Circuit Emulation (ICE) Mode

The **F2260** can support the In Circuit Emulation Mode. To use the ICE Mode, user just needs to connect P1.2 and P1.3 pin to the tenx proprietary EV Module. The benefit is that user can emulate the whole system without changing the on board target device. But there are some limits for the ICE mode as below.

1. The device must be un-protect.
2. The device's P1.2 and P1.3 pins must work in input Mode (P1MOD2=0/1 and P1MOD3=0/1).
3. During Program Code download, P1.0 sent acknowledge signal to T-Link unit. After download stage, P1.0 can be emulated as any other pins.
4. During Program Code download, P1.1 always output Low. After download stage, P1.1 can be emulated as any other pins.
5. The Program ROM's addressing space 1D00h~1FFFh and 0033h~003Ah are occupied by tenx EV Module. So user Program cannot access these spaces.
6. The P1.2 and P1.3 pin's function cannot be emulated.
7. The V_{DD} level and VCON SFR are controlled by EV module.



ICE Mode Connection

SFR & CFGW MAP

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	1111-1111	**P0**	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	**SP**	SP							
82h	0000-0000	**DPL**	DPL							
83h	0000-0000	**DPH**	DPH							
87h	0xxx-0000	**PCON**	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	**TMOD**	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	**TL0**	TL0							
8Bh	0000-0000	**TL1**	TL1							
8Ch	0000-0000	**TH0**	TH0							
8Dh	0000-0000	**TH1**	TH1							
90h	1111-1111	**P1**	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
91h	0000-0000	**P0OE**	P0OE							
94h	x000-0001	**OPTION**	CMPO	CMPVS			UART1W	WDTPSC	TM3PSC	
95h	xxxx-x000	**INTFLG**	–	–	–	–	–	IE2	P1IF	TF3
96h	0000-0000	**P1WKUP**	P1WKUP							
97h	xxxx-xxx0	**SWCMD**	IAPALL / SWRST							
98h	0000-0000	**SCON**	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	**SBUF**	SBUF							
A0h	1111-1111	**P2**	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
A2h	0000-0000	**P1MODL**	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
A3h	0000-0000	**P1MODH**	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
A4h	0000-0000	**P3MODL**	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
A5h	0000-0000	**P3MODH**	P3MOD7		P3MOD6		P3MOD5		P3MOD4	
A6h	0000-0000	**TOCON**	T1OCON		T2OCON			TCOCON		
A7h	x010-0010	**VCON**	–	PWRSAV	VSET2			VSET1		
A8h	0x00-0000	**IE**	EA	–	ET2	ES	ET1	EX1	ET0	EX0
A9h	xxxx-x000	**INTE1**	–	–	–	–	–	EX2	P1IE	TM3IE
AFh	xxx0-1100	**RFCON**	–	–	–	T0RFC	RFCPSC		RFCS	
B0h	1111-1111	**P3**	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
B1h	0010-1111	**LCON**	DSPON	LCDCLK	LCDFMR		LCDUTY	P0SEG		
B3h	xxxx-xxxx	**TM3SEC**	TM3SEC							
B4h	xxxx-xxxx	**TM3DL**	TM3DL							
B5h	xxxx-xxxx	**TM3DH**	–	TM3DH						
B6h	0000-0000	**TM3RLD**	TM3RLD							
B7h	0000-0000	**TM3ADJ**	TM3ADJS	TM3ADJ						
B8h	xx00-0000	**IP**	–	–	PT2	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	**IPH**	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
BAh	xxxx-x000	**IP1**	–	–	–	–	–	PX2	PP1	PT3
BBh	xxxx-x000	**IP1H**	–	–	–	–	–	PX2H	PP1H	PT3H
C8h	0000-0000	**T2CON**	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
CAh	0000-0000	**RCP2L**	RCP2L							
CBh	0000-0000	**RCP2H**	RCP2H							
CCh	0000-0000	**TL2**	TL2							
CDh	0000-0000	**TH2**	TH2							
D0h	0000-0000	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
D8h	0110-0111	**CLKCON**	SCKTYPE	SXTGAIN		STPPCK	STPFCK	SELFCK	CLKPSC	
E0h	0000-0000	**ACC**	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
F0h	0000-0000	**B**	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F8h	xxxx-0000	**AUX1**	–	–	–	–	CLRWDT	CLRTM3	STPRFC	DPSEL

Flash Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FFEh	**CFGWL**	–	–	–	–	–	–	–	–
3FFFh	**CFGWH**	PROT	XRSTE	MVCLOCK	WDTE	–	–	LVRE	–

SFR & CFGW DESCRIPTION

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
80h	**P0**	7~0	P0	R/W	FFh	Port0 data, also controls the P0.n pin's pull-up function. If the P0.n SFR data is "1" and the corresponding P0OE.n=0 (input mode), the pull-up is enabled.
81h	**SP**	7~0	SP	R/W	07h	Stack Point
82h	**DPL**	7~0	DPL	R/W	00h	Data Point low byte
83h	**DPH**	7~0	DPH	R/W	00h	Data Point high byte
87h	**PCON**	7	SMOD	R/W	0	Set 1 to enable UART double baud rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit
		1	PD	R/W	0	Power down control bit, set 1 to enter STOP mode
		0	IDL	R/W	0	Idle control bit, set 1 to enter IDLE mode
88h	**TCON**	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control. 1: timer runs; 0: timer stops
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control. 1:timer runs; 0:timer stops
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin
89h	**TMOD**	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin's negative edge
		5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	**TL0**	7~0	TL0	R/W	00h	Timer0 data low byte
8Bh	**TL1**	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	**TH0**	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	**TH1**	7~0	TH1	R/W	00h	Timer1 data high byte

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
90h	**P1**	7~0	P1	R/W	FFh	Port1 data
91h	**P0OE**	7~0	P0OE	R/W	00h	Port0 CMOS Push-Pull output enable control, 1=Enable.
94h	**OPTION**	7	CMPO	R	–	Compare result of BandGap voltage and V_{BAT} voltage divider. "1" means the V_{BAT} divider voltage is higher.
		6~4	CMPVS	R/W	000	Select V_{BAT} resistor divider to compare with the 1.2V BandGap reference. 000: Comparator Disable 001: the Comparator input is V_{BAT}*12/25 010: the Comparator input is V_{BAT}*12/26 011: the Comparator input is V_{BAT}*12/27 100: the Comparator input is V_{BAT}*12/28 101: the Comparator input is V_{BAT}*12/29 110: the Comparator input is V_{BAT}*12/30 111: the Comparator input is V_{BAT}*12/31
		3	UART1W	R/W	0	Set 1 to enable one wire UART mode, both TXD/RXD use P3.1 pin.
		2	WDTPSC	R/W	0	WDT Prescaler 0: WDT overflow at 65536 System clock count 1: WDT overflow at 32768 System clock count
		1~0	TM3PSC	R/W	01	Timer3 Interrupt rate 00: Timer3 interrupt occurs when 23 bit count data overflow 01: Timer3 interrupt is 1.0 second rate (32768 SXT cycles) 10: Timer3 interrupt is 0.5 second rate (16384 SXT cycles) 11: Timer3 interrupt is 0.25 second rate (8192 SXT cycles)
95h	**INTFLG**	2	IE2	R/W	0	External Interrupt 2 (INT2 pin) edge flag Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine. S/W can write FBh to INTFLG to clear this bit.
		1	P1IF	R/W	0	Port1 pin change Interrupt flag Set by H/W when a Port1 pin state change is detected and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting. It is cleared automatically when the program performs the interrupt service routine. S/W can write FDh to INTFLG to clear this bit.
		0	TF3	R/W	0	Timer3 Interrupt Flag Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.
96h	**P1WKUP**	7~0	P1WKUP	R/W	00h	P1.7~P1.0 pin individual Wake-up / Interrupt enable control 0: Disable 1: Enable
97h	**SWCMD**	7~0	SWRST	W	–	Write 56h to generate S/W Reset
		7~0	IAPALL	W	–	Write 65h to set IAPALL flag; Write other value to clear IAPALL flag.
		0	IAPALL	R	0	Flag indicates whole Flash can be access by IAP or not
98h	**SCON**	7	SM0	R/W	0	Serial port mode select bit 0, 1 (SM0, SM1)= 00: Mode0: 8 bit shift register, Baud Rate = F_{SYSCLK} / 2 01: Mode1: 8 bit UART, Baud Rate is variable 10: Mode2: 9 bit UART, Baud Rate = F_{SYSCLK} / 32 or / 64 11: Mode3: 9 bit UART, Baud Rate is variable
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 In Modes 2/3, if SM2 is set then the received interrupt will not be generated if the received ninth bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	Set 1 to enable UART Reception
		3	TB8	R/W	0	Transmitter bit 8, ninth bit to transmit in Modes 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0
		1	TI	R/W	0	Transmit Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W
		0	RI	R/W	0	Receive Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
99h	**SBUF**	7~0	SBUF	R/W	–	UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
A0h	**P2**	7	P2.7	R/W	1	P2.7 data 0: Open Drain output low 1: Schmitt-trigger input with pull up
		6~0	P2.6~P2.0	R/W	7Fh	General purpose register
A2h	**P1MODL**	7~6	P1MOD3	R/W	00	P1.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not used
		5~4	P1MOD2	R/W	00	P1.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not used
		3~2	P1MOD1	R/W	00	P1.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not used
		1~0	P1MOD0	R/W	00	P1.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P1.0 is T2O output
A3h	**P1MODH**	7~6	P1MOD7	R/W	00	P1.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.7 is RFC clock input pin (RFCX)
		5~4	P1MOD6	R/W	00	P1.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.6 is RFC resistor connection pin (RFC2R)
		3~2	P1MOD5	R/W	00	P1.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.5 is RFC resistor connection pin (RFC1R)
		1~0	P1MOD4	R/W	00	P1.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.4 is RFC resistor connection pin (RFC0R)
A4h	**P3MODL**	7~6	P3MOD3	R/W	00	P3.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not used
		5~4	P3MOD2	R/W	00	P3.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not used
		3~2	P3MOD1	R/W	00	P3.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not used
		1~0	P3MOD0	R/W	00	P3.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not used
A5h	**P3MODH**	7~6	P3MOD7	R/W	00	P3.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P3.7 is TCO output
		5~4	P3MOD6	R/W	00	P3.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P3.6 is T1B output
		3~2	P3MOD5	R/W	00	P3.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: Mode3, P3.5 is T1O output
		1~0	P3MOD4	R/W	00	P3.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2; 11: not used
A6h	**TOCON**	7~6	T1OCON	R/W	00	T1O pin duty and frequency control 00: 1/2 duty, 1/2 Timer1 overflow frequency 01: 1/3 duty, 1/3 Timer1 overflow frequency 10: 1/4 duty, 1/4 Timer1 overflow frequency
		5~3	T2OCON	R/W	000	T2O pin duty and frequency control 000: 1/2 duty, 1/2 Timer2 overflow frequency 001: 1/3 duty, 1/3 Timer2 overflow frequency 010: 1/4 duty, 1/4 Timer2 overflow frequency 101: 2/3 duty, 1/3 Timer2 overflow frequency 110: 3/4 duty, 1/4 Timer2 overflow frequency
		2~0	TCOCON	R/W	000	TCO pin duty and frequency control 000: 1/2 duty, 1/2 SYSCLK frequency 001: 1/3 duty, 1/3 SYSCLK frequency 010: 1/4 duty, 1/4 SYSCLK frequency 011: 1/4 duty, 1/2 SYSCLK frequency 100: 1/2 duty, 1/1 SYSCLK frequency 101: 2/3 duty, 1/3 SYSCLK frequency 110: 3/4 duty, 1/4 SYSCLK frequency 111: 3/4 duty, 1/2 SYSCLK frequency

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A7h	**VCON**	6	PWRSAV	R/W	0	V_{DD} voltage control. 0: $V_{DD}=V_{BAT}$ 1: $V_{DD}=V_{BAT}$*115/300~V_{BAT}*192/300
		5~3	VSET2	R/W	100	V_{DD} voltage setting in Fast/Slow mode while PWRSAV=1. 000: $V_{DD}=V_{BAT}$*115/300 in Fast/Slow mode 001: $V_{DD}=V_{BAT}$*126/300 in Fast/Slow mode 010: $V_{DD}=V_{BAT}$*137/300 in Fast/Slow mode 011: $V_{DD}=V_{BAT}$*148/300 in Fast/Slow mode 100: $V_{DD}=V_{BAT}$*159/300 in Fast/Slow mode 101: $V_{DD}=V_{BAT}$*170/300 in Fast/Slow mode 110: $V_{DD}=V_{BAT}$*181/300 in Fast/Slow mode 111: $V_{DD}=V_{BAT}$*192/300 in Fast/Slow mode
		2~0	VSET1	R/W	010	V_{DD} voltage setting in Idle/Stop mode while PWRSAV=1. Definition is the same as VSET2.
A8h	**IE**	7	EA	R/W	0	Global interrupt enable control. 0: Disable all Interrupts. 1: Each interrupt is enabled or disabled by its own interrupt control bit.
		5	ET2	R/W	0	Set 1 to enable Timer2 interrupt
		4	ES	R/W	0	Set 1 to enable Serial Port (UART) Interrupt
		3	ET1	R/W	0	Set 1 to enable Timer1 Interrupt
		2	EX1	R/W	0	Set 1 to enable external INT1 pin Interrupt & Stop mode wake up capability
		1	ET0	R/W	0	Set 1 to enable Timer0 Interrupt
		0	EX0	R/W	0	Set 1 to enable external INT0 pin Interrupt & Stop mode wake up capability
A9h	**INTE1**	2	EX2	R/W	0	Set 1 to enable external INT2 pin Interrupt & Stop mode wake up capability
		1	P1IE	R/W	0	Set 1 to enable Port1 Pin Change Interrupt
		0	TM3IE	R/W	0	Set 1 to enable Timer3 Interrupt
AFh	**RFCON**	4	T0RFC	R/W	0	Timer0 Counter mode (CT0N=1) input select 0: T0 (P3.4) pin 1: RFC Clock divided by 1/4/16/64
		3~2	RFCPSC	R/W	11	RFC clock divider to Timer0 00: divided by 64 01: divided by 16 10: divided by 4 11: divided by 1
		1~0	RFCS	R/W	00	Select RFC convert channel. 00: RFC0R (P1.4) 01: RFC1R (P1.5) 10: RFC2R (P1.6)
B0h	**P3**	7~0	P3	R/W	FFh	Port 3 data
B1h	**LCON**	7	DSPON	R/W	0	Set 1 to enable LCD Display
		6	LCDCLK	R/W	0	LCD clock source 0: SXT; 1: FRC/64
		5~4	LCDFMR	R/W	10	LCD Frame Rate, 3=Highest; 0=Lowest
		3	LCDUTY	R/W	1	LCD Duty control 0: 1/3 Duty 1: 1/4 Duty
		2~0	P0SEG	R/W	111	Port0 LCD mode control. 000: P0.0~P0.7 are I/O pins 001: P0.0~P0.5 are I/O pins, P0.6~P0.7 are LCD Segment pins 010: P0.0~P0.4 are I/O pins, P0.5~P0.7 are LCD Segment pins 011: P0.0~P0.3 are I/O pins, P0.4~P0.7 are LCD Segment pins 100: P0.0~P0.2 are I/O pins, P0.3~P0.7 are LCD Segment pins 101: P0.0~P0.1 are I/O pins, P0.2~P0.7 are LCD Segment pins 110: P0.0 is I/O pin, P0.1~P0.7 are LCD Segment pins 111: P0.0~P0.7 are LCD Segment pins

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
B3h	**TM3SEC**	7~0	TM3SEC	R	–	Timer3 count data bit 22~15
B4h	**TM3DL**	7~0	TM3DL	R	–	Timer3 count data bit 7~0
B5h	**TM3DH**	6~0	TM3DH	R	–	Timer3 count data bit 14~8
B6h	**TM3RLD**	7~0	TM3RLD	R/W	00h	Timer3 overflow reload data for Timer3 bit 22~15 (TM3SEC)
B7h	**TM3ADJ**	7	TM3ADJS	R/W	0	Timer3 adjustment sign 0: Timer3 positive adjust, to increase Timer3 counting rate 1: Timer3 negative adjust, to decrease Timer3 counting rate
		6~0	TM3ADJ	R/W	00h	Timer3 adjust magnitude, 0.477 ppm per LSB. The adjustment is calculated as ±TM3ADJ*0.477ppm. The total adjustable range is ± 61ppm.
B8h	**IP**	5	PT2	R/W	0	Timer2 Interrupt Priority Low bit
		4	PS	R/W	0	Serial Port (UART) Interrupt Priority Low bit
		3	PT1	R/W	0	Timer1 Interrupt Priority Low bit
		2	PX1	R/W	0	External INT1 Pin Interrupt Priority Low bit
		1	PT0	R/W	0	Timer0 Interrupt Priority Low bit
		0	PX0	R/W	0	External INT0 Pin Interrupt Priority Low bit
B9h	**IPH**	5	PT2H	R/W	0	Timer2 Interrupt Priority High bit
		4	PSH	R/W	0	Serial Port (UART) Interrupt Priority High bit
		3	PT1H	R/W	0	Timer1 Interrupt Priority High bit
		2	PX1H	R/W	0	External INT1 Pin Interrupt Priority High bit
		1	PT0H	R/W	0	Timer0 Interrupt Priority High bit
		0	PX0H	R/W	0	External INT0 Pin Interrupt Priority High bit
BAh	**IP1**	2	PX2	R/W	0	External INT2 Pin Interrupt Priority Low bit
		1	PP1	R/W	0	Port1 pin change Interrupt Priority Low bit
		0	PT3	R/W	0	Timer3 Interrupt Priority Low bit
BBh	**IP1H**	2	PX2H	R/W	0	External INT2 Pin Interrupt Priority High bit
		1	PP1H	R/W	0	Port1 Interrupt Priority High bit
		0	PT3H	R/W	0	Timer3 Interrupt Priority High bit
C8h	**T2CON**	7	TF2	R/W	0	Timer2 overflow flag Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
		6	EXF2	R/W	0	T2EX interrupt pin falling edge flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
		5	RCLK	R/W	0	UART receive clock control bit 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3
		4	TCLK	R/W	0	UART transmit clock control bit 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
		3	EXEN2	R/W	0	T2EX pin enable 0: T2EX pin disable 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0
		2	TR2	R/W	0	Timer2 run control. 1:timer runs; 0:timer stops
		1	CT2N	R/W	0	Timer2 Counter/Timer select bit 0: Timer mode, Timer2 data increases at 2 System clock cycle rate 1: Counter mode, Timer2 data increases at T2 pin's negative edge
		0	CPRL2N	R/W	0	Timer2 Capture/Reload control bit 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1. 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1. If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.
CAh	**RCP2L**	7~0	RCP2L	R/W	00h	Timer2 reload/capture data low byte
CBh	**RCP2H**	7~0	RCP2H	R/W	00h	Timer2 reload/capture data high byte
CCh	**TL2**	7~0	TL2	R/W	00h	Timer2 data low byte
CDh	**TH2**	7~0	TH2	R/W	00h	Timer2 data high byte

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
D0h	**PSW**	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	Register Bank Select bit 1
		3	RS0	R/W	0	Register Bank Select bit 0
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag
D8h	**CLKCON**	7	SCKTYPE	R/W	0	Slow clock Type. This bit can be changed only in Fast mode (SELFCK=1). 0: SXT 1: RFC, S/W must setup RFC oscillating circuitry before set this bit to 1
		6~5	SXTGAIN	R/W	11	32768 SXT oscillator gain, 3=Highest gain, 0=Lowest gain.
		4	STPPCK	R/W	0	Set 1 to stop UART/Timer0/1/2 clock in Idle mode for current reducing.
		3	STPFCK	R/W	0	Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
		2	SELFCK	R/W	1	System clock select. This bit can be changed only when STPFCK=0. 0: Slow clock; 1: Fast clock
		1~0	CLKPSC	R/W	11	System clock prescaler. 00: System clock is Fast/Slow clock divided by 64 01: System clock is Fast/Slow clock divided by 16 10: System clock is Fast/Slow clock divided by 4 11: System clock is Fast/Slow clock divided by 1
E0h	**ACC**	7~0	ACC	R/W	00h	Accumulator
F0h	**B**	7~0	B	R/W	00h	B register
F8h	**AUX1**	3	CLRWDT	R/W	0	Set to 1 to clear Watch Dog Timer
		2	CLRTM3	R/W	0	Set 1 to Clear Timer3
		1	STPRFC	R/W	0	Set 1 to stop RFC clock oscillating
		0	DPSEL	R/W	0	Active DPTR Select

Adr	Flash	Bit#	Bit Name	Description
3FFEh	**CFGWL**	7~0	–	–
3FFFh	**CFGWH**	7	PROT	Flash Code Protect, 1=Protect
		6	XRSTE	Pin Reset enable, 1=enable.
		5	MVCLOCK	If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.
		4	WDTE	WDT Reset enable, 1=enable.
		1	LVRE	Low Voltage Reset enable, 1=enable.

INSTRUCTION SET

Instructions are 1, 2 or 3 bytes long as listed in the 'byte' column below. Each instruction takes 1~8 System clock cycles to execute as listed in the 'cycle' column below.

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ADD A,Rn	Add register to A	1	2	28-2F
ADD A,dir	Add direct byte to A	2	2	25
ADD A,@Ri	Add indirect memory to A	1	2	26-27
ADD A,#data	Add immediate to A	2	2	24
ADDC A,Rn	Add register to A with carry	1	2	38-3F
ADDC A,dir	Add direct byte to A with carry	2	2	35
ADDC A,@Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A,#data	Add immediate to A with carry	2	2	34
SUBB A,Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	2	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8	A4
DIV AB	Divide A by B	1	8	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ANL A,Rn	AND register to A	1	2	58-5F
ANL A,dir	AND direct byte to A	2	2	55
ANL A,@Ri	AND indirect memory to A	1	2	56-57
ANL A,#data	AND immediate to A	2	2	54
ANL dir,A	AND A to direct byte	2	2	52
ANL dir,#data	AND immediate to direct byte	3	4	53
ORL A,Rn	OR register to A	1	2	48-4F
ORL A,dir	OR direct byte to A	2	2	45
ORL A,@Ri	OR indirect memory to A	1	2	46-47
ORL A,#data	OR immediate to A	2	2	44
ORL dir,A	OR A to direct byte	2	2	42
ORL dir,#data	OR immediate to direct byte	3	4	43
XRL A,Rn	Exclusive-OR register to A	1	2	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A,#data	Exclusive-OR immediate to A	2	2	64
XRL dir,A	Exclusive-OR A to direct byte	2	2	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
SWAP A	Swap Nibbles of A	1	2	C4
RL A	Rotate A left	1	2	23
RLC A	Rotate A left through carry	1	2	33
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MOV A,Rn	Move register to A	1	2	E8-EF
MOV A,dir	Move direct byte to A	2	2	E5
MOV A,@Ri	Move indirect memory to A	1	2	E6-E7
MOV A,#data	Move immediate to A	2	2	74
MOV Rn,A	Move A to register	1	2	F8-FF
MOV Rn,dir	Move direct byte to register	2	4	A8-AF
MOV Rn,#data	Move immediate to register	2	2	78-7F
MOV dir,A	Move A to direct byte	2	2	F5
MOV dir,Rn	Move register to direct byte	2	4	88-8F
MOV dir,dir	Move direct byte to direct byte	3	4	85
MOV dir,@Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir,#data	Move immediate to direct byte	3	4	75
MOV @Ri,A	Move A to indirect memory	1	2	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	2	76-77
MOV DPTR,#data	Move immediate to data pointer	3	4	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4	93
MOVC A,@A+PC	Move code byte relative PC to A	1	4	83
MOVX A,@Ri	Move external data(A8) to A	1	4	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	4	E0
MOVX @Ri,A	Move A to external data(A8)	1	4	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	4	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A,Rn	Exchange A and register	1	2	C8-CF
XCH A,dir	Exchange A and direct byte	2	2	C5
XCH A,@Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C,bit	AND direct bit to carry	2	4	82
ANL C,/bit	AND direct bit inverse to carry	2	4	B0
ORL C,bit	OR direct bit to carry	2	4	72
ORL C,/bit	OR direct bit inverse to carry	2	4	A0
MOV C,bit	Move direct bit to carry	2	2	A2
MOV bit,C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ACALL addr 11	Absolute jump to subroutine	2	4	11-F1
LCALL addr 16	Long jump to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	4	01-E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	4	80
JC rel	Jump on carry=1	2	4	40
JNC rel	Jump on carry=0	2	4	50
JB bit,rel	Jump on direct bit=1	3	4	20
JNB bit,rel	Jump on direct bit=0	3	4	30
JBC bit,rel	Jump on direct bit=1 and clear	3	4	10
JMP @A+DPTR	Jump indirect relative DPTR	1	4	73
JZ rel	Jump on accumulator=0	2	4	60
JNZ rel	Jump on accumulator … 0	2	4	70
CJNE A,dir,rel	Compare A,direct, jump not equal relative	3	4	B5
CJNE A,#data,rel	Compare A,immediate, jump not equal relative	3	4	B4
CJNE Rn,#data,rel	Compare register,immediate, jump not equal relative	3	4	B8-BF
CJNE @Ri,#data,rel	Compare indirect,immediate, jump not equal relative	3	4	B6-B7
DJNZ Rn,rel	Decrement register, jump not zero relative	2	4	D8-DF
DJNZ dir,rel	Decrement direct byte, jump not zero relative	3	4	D5

MISCELLANEOUS				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply voltage	V_{SS} – 0.3 ~ V_{SS} + 4.2	V
Input voltage	V_{SS} – 0.3 ~ V_{BAT} + 0.3	
Output voltage	V_{SS} – 0.3 ~ V_{BAT} + 0.3	
Output current high per 1 pin	–20	mA
Output current high per all pins	–50	
Output current low per 1 pin	+30	
Output current low per all pins	+100	
Maximum Operating Voltage	4.2	V
Operating temperature	–40 ~ +85	℃
Storage temperature	–65 ~ +150	

DC Characteristics (TA=25℃)

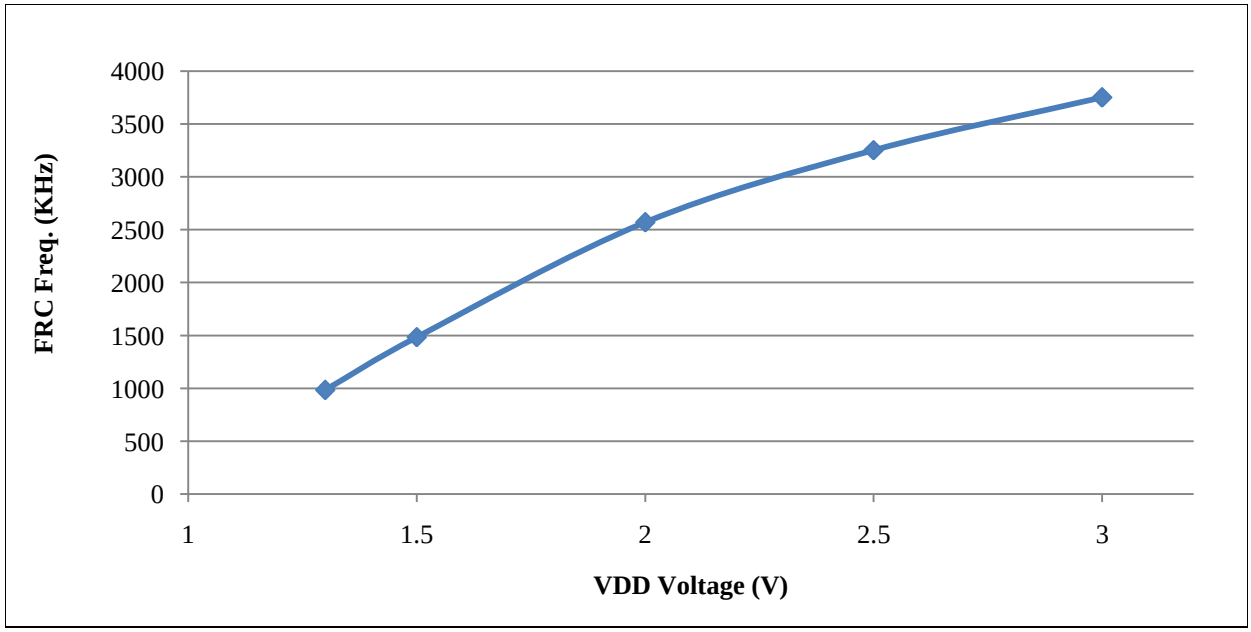
Parameter	Sym	Conditions		Min	Typ	Max	Unit
Input High Voltage	V_{IH}	all except P2.7	V_{BAT}=3V	0.6V_{BAT}	–	–	V
		P2.7	V_{BAT}=3V	0.8V_{BAT}	–	–	
Input Low Voltage	V_{IL}	all Input	V_{BAT}=3V	–	–	0.2V_{BAT}	V
I/O Port Source Current	I_{OH}	all except P2.7	V_{BAT}=3V V_{OH}=2.7V	2	4	–	mA
I/O Port Sink Current	I_{OL}	all except P2.7	V_{BAT}=3V V_{OL}=0.3V	6	12	–	mA
		P2.7		5	9	–	
Input Leakage Current (pin high)	I_{ILH}	all Input	V_{IN}=V_{BAT}	–	–	1	uA
Input Leakage Current (pin low)	I_{ILL}	all Input	Vin=0V	–	–	–1	
Power Supply Current	I_{BAT}	Fast, 3.7MHz	V_{BAT}=3V V_{DD}=3V	–	970	–	uA
		Fast, 1.5MHz	V_{BAT}=3V V_{DD}=1.5V LCD On	–	160	–	
		Slow, 32KHz		–	4.2	–	
		Slow, 2KHz		–	1.2	–	
		Idle, 2KHz		–	1	–	
		Stop	V_{BAT}=3V V_{DD}=1.5V	–	0.3	–	uA
Pull-Up Resistor	R_{PU}	all except P2.7	V_{BAT}=3V V_{IN}=0V	–	420	–	KΩ
		P2.7		–	270	–	KΩ

BandGap Reference Voltage

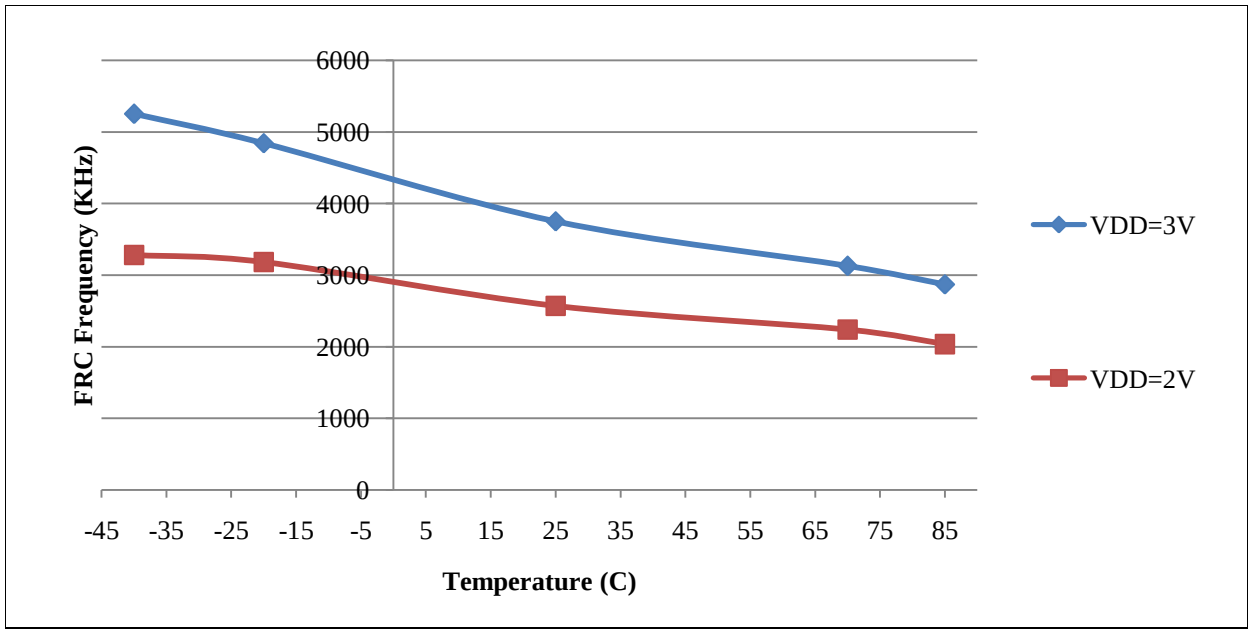
Parameter	Sym	Conditions	Min	Typ	Max	Unit
BandGap Voltage	V_{BG}	V_{BAT}=3V, 25℃	1.14	1.2	1.26	V
		V_{BAT}=2.2V~3.3V, –40℃~85℃	1.11	1.2	1.29	V

Clock Timing (TA=25℃)

Parameter	Sym	Conditions		Min	Typ	Max	Unit
FRC Clock Frequency	F_{FRC}	V_{DD}=3.0V	V_{BAT}=3V	–	3.75	–	MHz
		V_{DD}=1.8V		–	2.2	–	
		V_{DD}=1.5V		–	1.5	–	



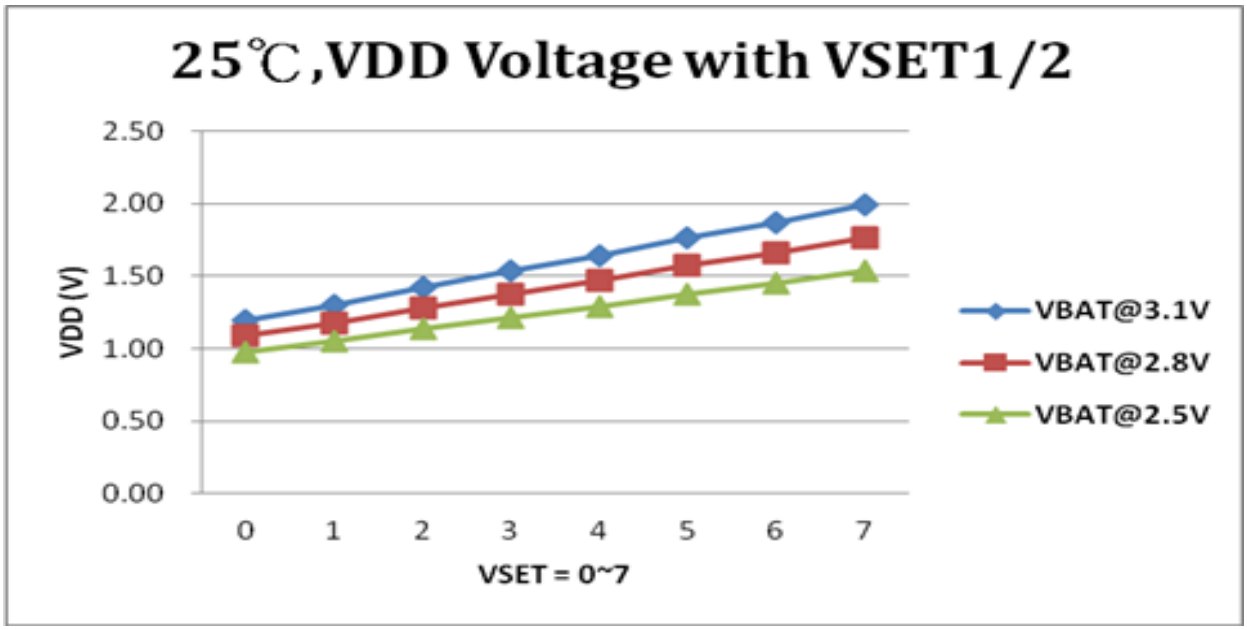
FRC Frequency with V_{DD}, T_A=25℃



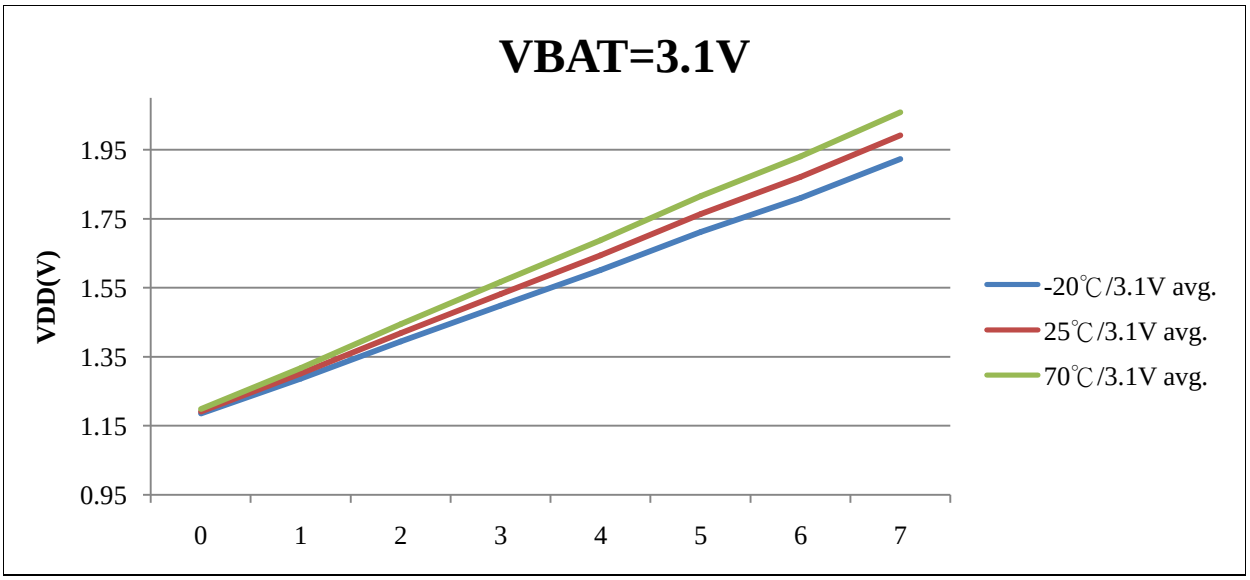
FRC Frequency with Temperature, VDD=3V & VDD=2V

V_{DD} Voltage Level

Parameter	Sym	Conditions		Min	Typ	Max
V_{DD} Voltage Level	V_{DD}	V_{BAT}=3.1V, VSET=3	25℃	–	1.53	–
		V_{BAT}=2.8V, VSET=4	25℃	–	1.47	–
		V_{BAT}=3.1V, VSET=3	70℃	–	1.57	–
		V_{BAT}=2.8V, VSET=4	70℃	–	1.51	–
		V_{BAT}=3.1V, VSET=3	–20℃	–	1.50	–
		V_{BAT}=2.8V, VSET=4	–20℃	–	1.43	–



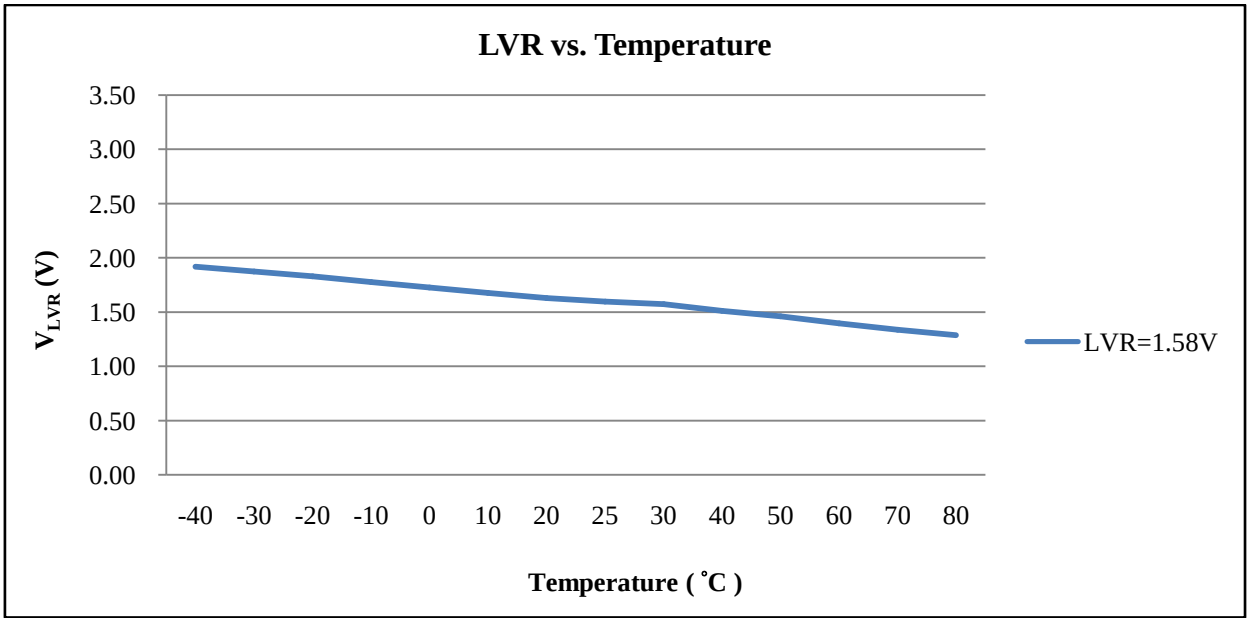
V_{DD} Voltage with VSET1/2, V_{BAT} = 2.5V~3.1V



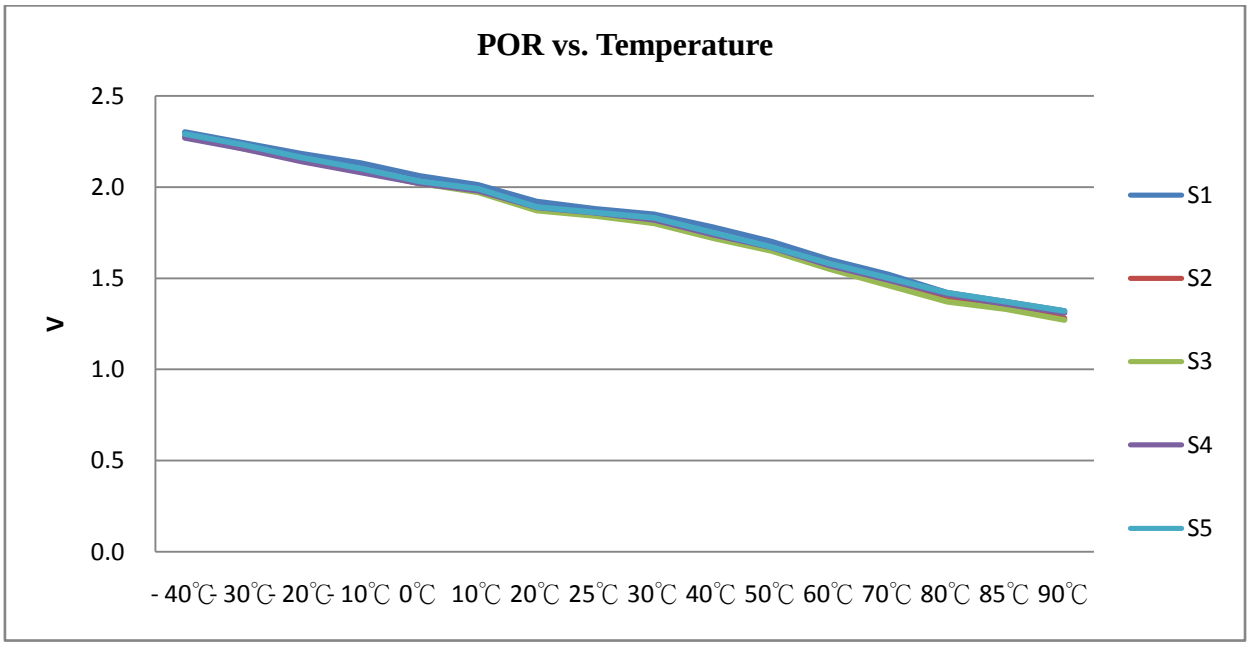
VDD Voltage with VSET1/2, TA = –20℃~70℃

LVR/POR Level

Parameter	Sym	Conditions	Min	Typ	Max	Unit
LVR Voltage Level	V_{LVR}	25℃	1.43	1.58	1.75	V
Power On Reset Voltage	V_{POR}	25℃	1.6	1.8	2.0	V



LVR with Temperature, T_A = –40°C~80°C



POR with Temperature (Power on Reset needs VBAT > VPOR)

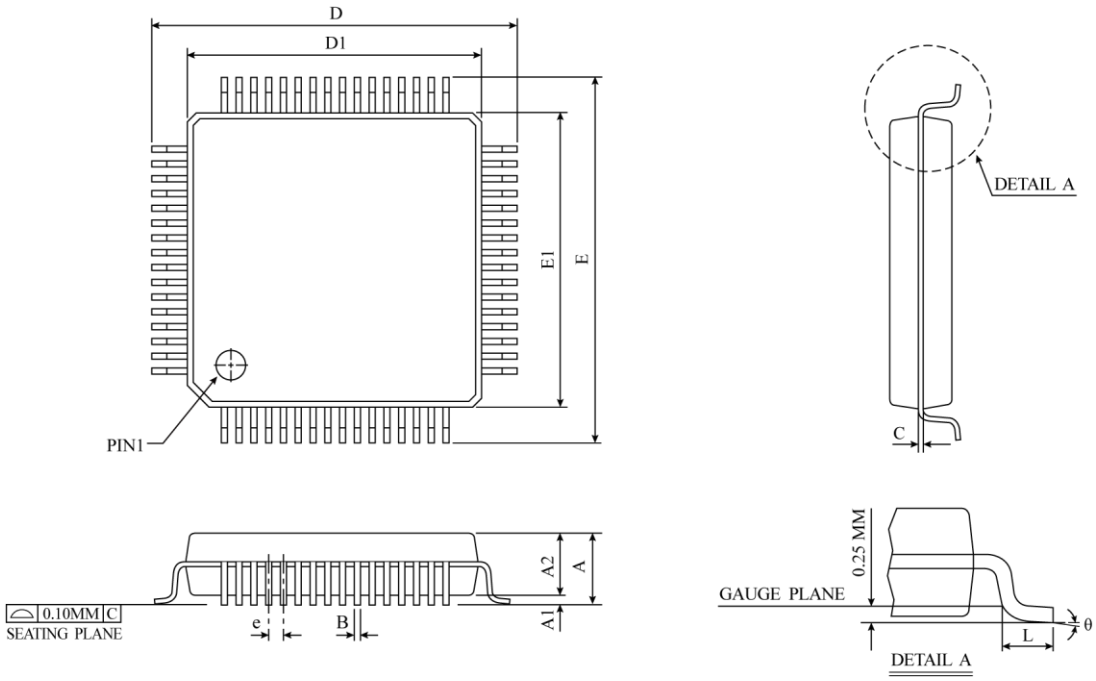
PACKAGE INFORMATION

Ordering Information

Ordering Number	Package
TM52F2260-COD	Wafer / Dice with code
TM52F2260-MTP	Wafer / Dice blank chip
TM52F2260-MTP-73	LQFP64 (7*7*1.4mm)
TM52F2260-MTP-76	LQFP64 (10*10*1.4mm)

Package Information

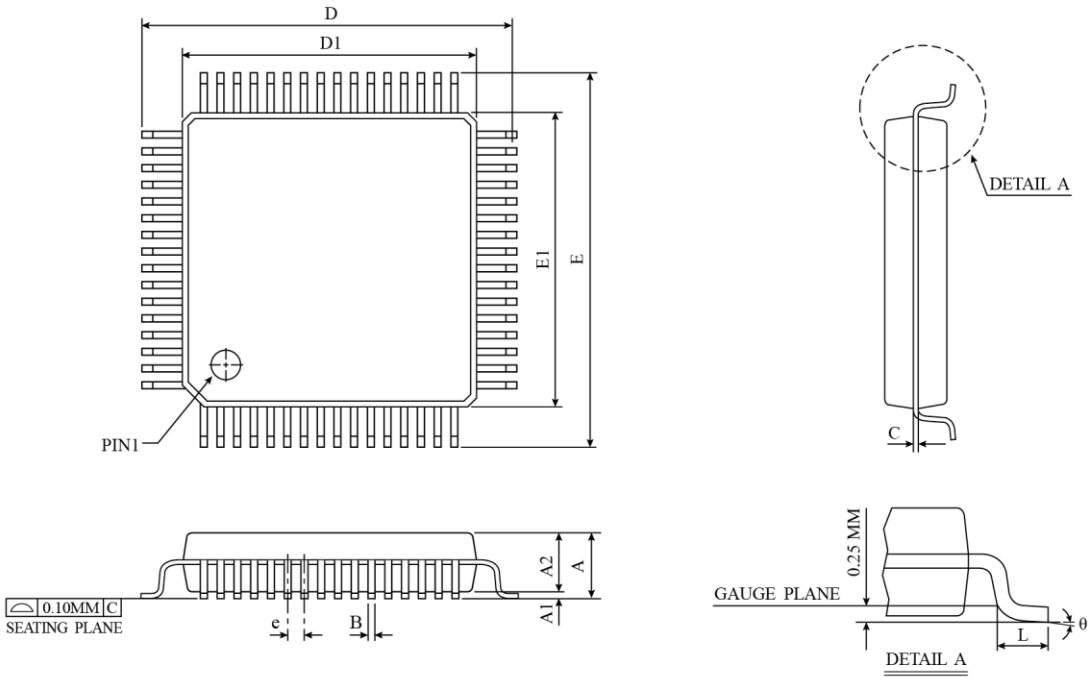
LQFP-64 (10×10mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.20	0.23	0.007	0.008	0.009
C	0.09	0.13	0.16	0.004	0.005	0.006
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
e	0.50 BASIC			0.020 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	3.5°	7°	0°	3.5°	7°
JEDEC	MS-026 (BCD)					

△ * NOTES：DIMENSION ″D1″ AND ″E1″ DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSIONS IS 0.25mm PER SIDE. ″D1″ AND ″E1″ ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMACH.

LQFP-64 (7×7mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.13	0.18	0.23	0.005	0.007	0.009
C	0.09	-	0.20	0.004	-	0.008
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
e	0.40 BASIC			0.016 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	3.5°	7°	0°	3.5°	7°
JEDEC	MS-026 (BBD)					

⚠ * NOTES : DIMENSION "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSIONS IS 0.25mm PER SIDE. "D1" AND "E1" ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMACH.