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TM52F5250

DATA SHEET

Rev 0.92

AMENDMENT HISTORY

Version	Date	Description
0.90	Feb, 2017	New release.
0.91	Aug, 2017	1. FRC accuracy & Temp. curve 2. Add Tiny current description 3. Other detail
0.92	May, 2018	1. Add package DIP-20, QFN-20 2. CFGW descript update

CONTENTS

TM52$_{Series}$ F52xx FAMILY

Common Features

CPU	MTP/Flash Program Memory	RAM Bytes	Dual Clock	Operation Mode	Timer0 Timer1 Timer2	UART	Real-time Timer3	LVD	LVR
Fast 8051 (2T)	4K~16K With IAP, ISP, ICP	256 ~ 768	SXT SRC FXT FRC	Fast Slow Idle Stop	8051 Standard		15-bit	2.3V	1.8V 2.3V 2.9V

Note: IAP, ISP only for Flash type program memory

Family Members Features

P/N	Program Memory	RAM Bytes	IO Pin	PWM	SAR ADC	Touch Key	LCD	LED	SPI	Others
TM52-M5254	MTP 4K Bytes	256	18	(8+2)-bit x2	12-bit 12-ch	–	–	–	–	–
TM52-M5258						14-ch				
TM52-M5250	Flash 4K Bytes	256	18	(8+2)-bit x2	12-bit 12-ch	–	–	–	–	–
TM52-F5264C	Flash 8K Bytes	256	22	(8+2)-bit x2	12-bit 12-ch	–	–	–	Yes	–
TM52-F5268C						14-ch				
TM52-F5274C	Flash 8K Bytes	512	30	(8+2)-bit x2	12-bit 12-ch	–	4x18	4x18	Yes	–
TM52-F5278C						14-ch				
TM52-F5273B	Flash 16K Bytes	768	30	(8+2)-bit x2	12-bit 12-ch	–	4x20	8x16	Yes	–
TM52-F5276B						16-ch				
TM52-F5288C	Flash 16K Bytes	512	42	(8+2)-bit x2	12-bit 12-ch	–	8x20	8x20	Yes	–
TM52-F5284C						12-ch				

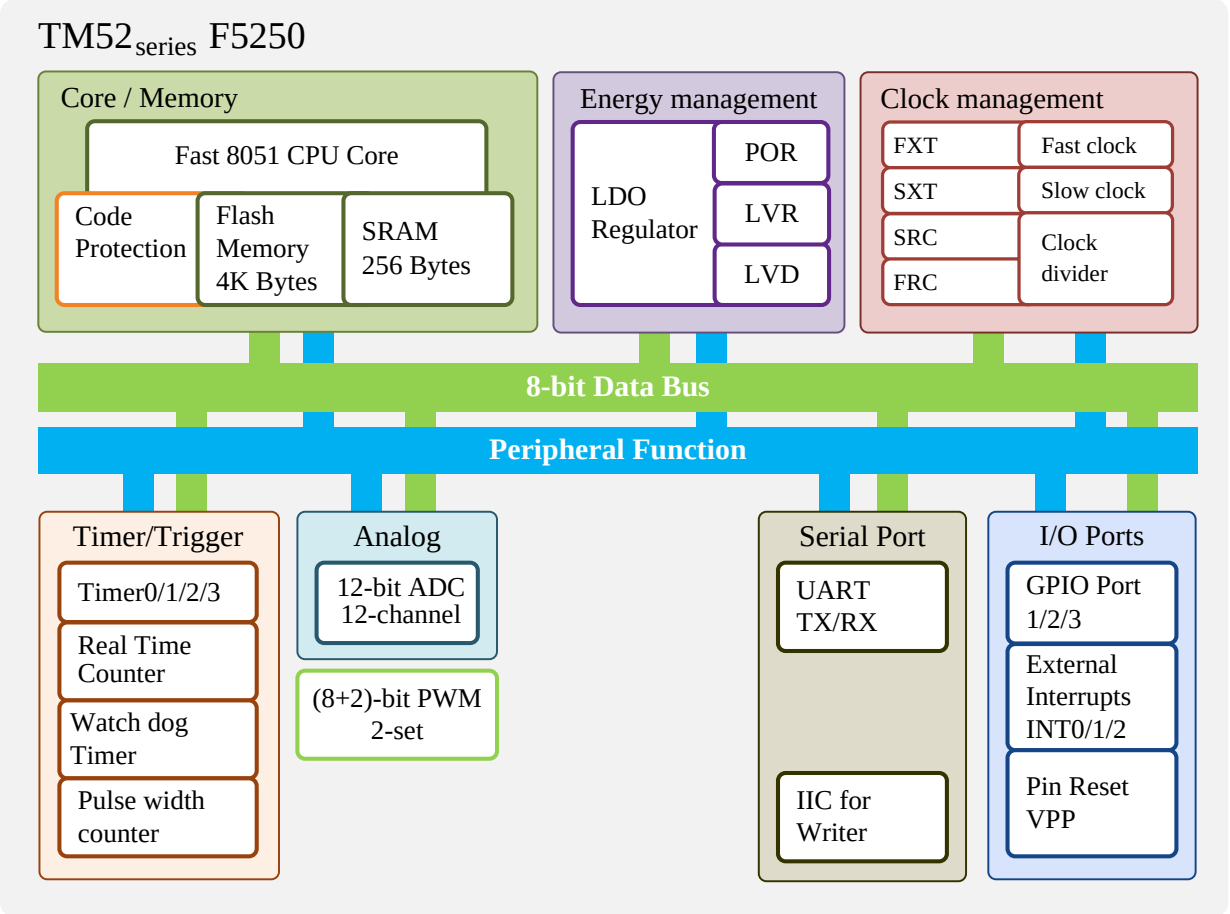
P/N	Operation Voltage	Operation Current (V_{CC}=3V) MODE3V=1, PWRSAV=1, LVR Disable				Max. System Clock (Hz)			
		Fast FRC	Slow SRC	Idle SRC	Stop	SXT	SRC	FXT	FRC
TM52-M5254	1.9~5.5V	2.0mA	21μA	5.2μA	<0.1μA	32K	80K	6M	7.37M
TM52-M5258									
TM52-F5250	2.0~5.5V	3mA	1mA	6μA	3μA	32K	24K	14.74M	9.83M
TM52-F5264C	2.0~5.5V	2.5mA	12μA	6μA	3μA	32K	24K	8M	7.37M
TM52-F5268C									
TM52-F5274C	2.0~5.5V	2.5mA	12μA	6μA	3μA	32K	24K	8M	7.37M
TM52-F5278C									
TM52-F5273B	1.8~5.5V	2.5mA	12μA	6μA	3μA	32K	24K	10M	9.83M
TM52-F5276B									
TM52-F5288C	1.9~5.5V	2.3mA	22μA	4.5μA	< 0.1μA	32K	80K	8M	7.37M
TM52-F5284C									

GENERAL DESCRPTION

TM52 $_{\text{Series}}$ **F5250** are versions of a new, fast 8051 architecture for an 8-bit microcontroller single chip with an instruction set fully compatible with industry standard 8051, C language development platform, and retains most 8051 peripheral function block. Typically, the **TM52** executes instructions six times faster than the traditional 8051 architecture.

The **TM52-F5250** provides improved performance, lower cost and fast time-to-market by integrating features on the chip, including 4K Bytes Flash program memory, 256 Bytes SRAM, Low Voltage Reset (LVR), Low Voltage Detector (LVD), dual clock power saving operation mode, 8051 standard UART and Timer0/1/2, real time Timer3, 2 set (8+2)-bit PWMs, 12 channels 12-bit A/D Convertor and Watchdog Timer. Its high reliability and low power consumption feature can be widely applied in consumer and home appliance products.

BLOCK DIAGRAM



FEATURES

1. **Standard 8051 Instruction set, fast machine cycle**
   - Executes instructions six times faster than the traditional 8051
2. **4K Bytes Flash Program Memory**
   - Support “In Circuit Programming” (ICP) or “In System Programming” (ISP) for the Flash code
   - Byte Write “In Application Programming” (IAP) mode is convenient as Data EEPROM access
   - Code Protection Capability
3. **Total 256 Bytes SRAM**
   - 256 Bytes IRAM in the 8051 internal data memory area
4. **Four System Clock type Selections**
   - Fast clock from 1~14.746 MHz Crystal
   - Fast clock from Internal RC (9.83 MHz)
   - Slow clock from 32768 Hz Crystal
   - Slow clock from Internal RC (24 KHz)
   - System clock can be divided by 1/2/4/16 option
5. **8051 Standard Timer – Timer0/1/2**
   - 16-bit Timer0, also supports T0O clock output for Buzzer application
   - 16-bit Timer1, also supports Slow clock/16 input counting
   - 16-bit Timer2, also supports Slow clock/16 input counting and T2O clock output
6. **15-bit Time3**
   - Clock source is Slow clock
   - Interrupt period can be clock divided by 32768/16384/8192/128 option
7. **8051 Standard UART**
   - One Wire UART option can be used for ISP or other application
8. **Two independent "8+2" bits PWMs with prescaler/period-adjustment**
9. **12-bit ADC with 10 Channels External Pin Input and 2 Channels Internal Reference Voltage**

10. 10 Sources, 4-level Priority Interrupt

- Timer0/Timer1/Timer2/Timer3 Interrupt
- INT0/INT1 Falling-Edge/Low-Level Interrupt
- Port1 Pin Change Interrupt
- UART TX/RX Interrupt
- P3.7 (INT2) Interrupt
- ADC Interrupt

11. Pin Interrupt can Wake up CPU from Power-Down (Stop) mode

- P3.2/P3.3 (INT0/INT1) Interrupt & Wake-up
- P3.7 (INT2) Interrupt & Wake-up
- Each Port1 pin can be defined as Interrupt & Wake-up pin (by pin change)

12. Max. 18 Programmable I/O pins

- CMOS Output
- Pseudo-Open-Drain, or Open-Drain Output
- Schmitt Trigger Input
- Pin Pull-up can be Enable or Disable

13. Independent RC Oscillating Watchdog Timer

- 360ms/180ms/90ms/45ms Selectable WDT Timeout options

14. Five types Reset

- Power on Reset
- Selectable External Pin Reset
- Software Command Reset
- Selectable Watchdog Timer Reset
- Selectable Low Voltage Reset

15. 4-level Low Voltage Reset

- 2.0V/2.3V/2.9V/3.5V

16. 1-level Low Voltage Detect

- 2.3V (can be disabled)

17. Four Operation Modes

- Fast/Slow/Idle/Stop Mode

18. Operating Voltage and Current

- V_{CC}=3.5V ~ 5.5V @ F_{SYSCLK}=14.746 MHz
- V_{CC}=2.9V ~ 5.5V @ F_{SYSCLK}=9.8 MHz
- V_{CC}=2.3V ~ 5.5V @F_{SYSCLK}=5 MHz
- V_{CC}=2.0V ~ 5.5V @F_{SYSCLK}=2.5 MHz
- I_{CC}=4mA @Fast mode, F_{SYSCLK}=9.8 MHz, V_{CC}=5V
- I_{CC}=1mA @Slow mode, F_{SYSCLK}=32 KHz, V_{CC}=3V
- I_{CC}=6μA @Idle mode, F_{SYSCLK}=32 KHz, V_{CC}=3V
- I_{CC}=3μA @Stop mode, V_{CC}=3V

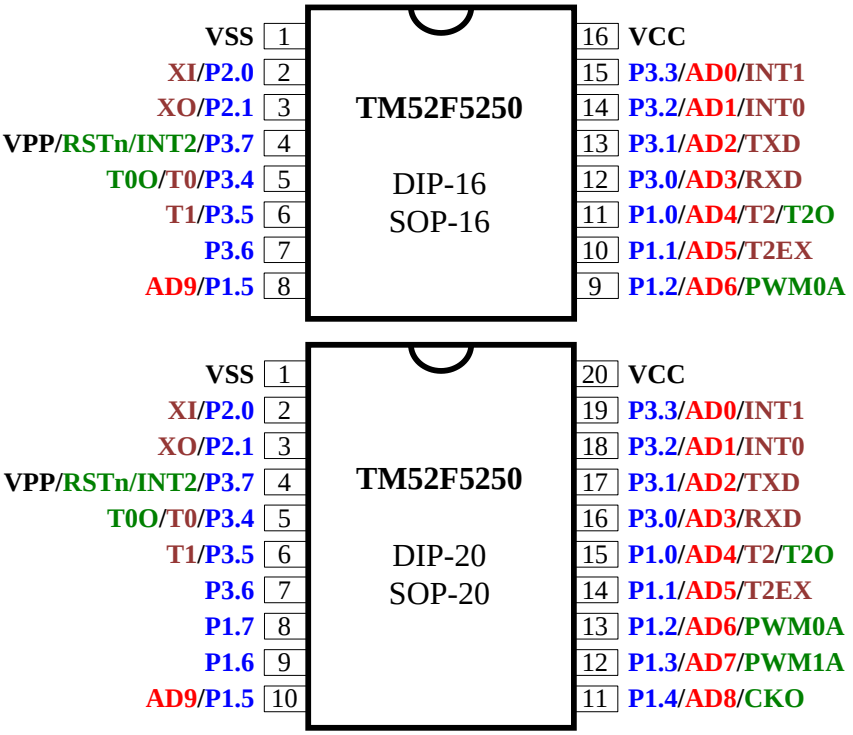
19. Operating Temperature Range

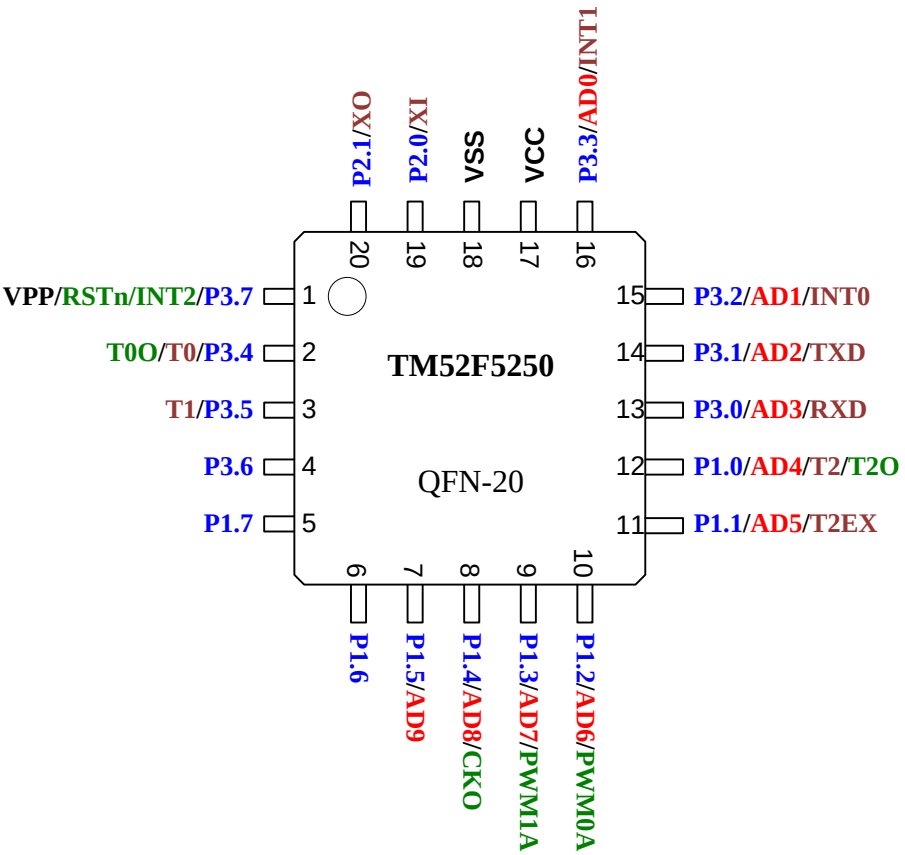
- –40°C ~ +85°C

20. Package Types

- DIP 16-pin (300 mil)
- SOP 16-pin (150 mil)
- DIP 20-pin (300 mil)
- SOP 20-pin (300 mil)
- QFN-20 (4*4*0.75-0.5mm)

PIN ASSIGNMENT





PIN DESCRIPTION

Name	In/Out	Pin Description
P1.0~P1.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software. These pin's level change can wake up CPU from Idle/Stop mode.
P2.0~P2.1	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
P3.0~P3.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "pseudo open drain" output. Pull-up resistors are assignable by software.
P3.3~P3.6	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or "open-drain" output. Pull-up resistor is fix enable.
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Stop mode wake up input.
INT2	I	External falling edge Interrupt input, Idle/Stop mode wake up input.
RXD	I/O	UART Mode0 transmit & receive data, Mode1/2/3 receive data
TXD	I/O	UART Mode0 transmit clock, Mode1/2/3 transmit data. In One Wire UART mode, this pin transmits and receives serial data.
T0, T1, T2	I	Timer0, Timer1, Timer2 event count pin input
T0O	O	Timer0 overflow divided by 64 output
T2O	O	Timer2 overflow divided by 2 output
CKO	O	System Clock divided by 2 output
T2EX	I	Timer2 external trigger input
PWM0 PWM1	O	8+2 bit PWM output
AD0~AD9	I	ADC input
RSTn	I	External active low reset input, Pull-up resistor is fixed enable
XI, XO	–	Crystal/Resonator oscillator connection for system clock
VPP	I	Flash programming high voltage input
VCC, VSS	P	Power input pin and ground

PIN SUMMARY

TM52F5250

Pin Number			Pin Name	Type	Input			Output			Alternate Function				Misc
SOP/DIP-20	DIP/SOP-16	QFN-20			Pull-up Control	Wake up	Ext. Interrupt	P.P.	P.O.D.	O.D.	ADC	UART	PWM	Timer	
1	1	18	VSS	P											
2	2	19	XI/P2.0	I/O	O			●		●					Crystal
3	3	20	XO/P2.1	I/O	O			●		●					Crystal
4	4	1	VPP/RSTn/INT2/P3.7	I/O	⊙	●	●			●					Reset
5	5	2	T0/T0O P3.4	I/O	O			●		●				●	
6	6	3	T1/P3.5	I/O	O			●		●				●	
7	7	4	P3.6	I/O	O			●		●					
8	–	5	P1.7	I/O	O	●		●		●					
9	–	6	P1.6	I/O	O	●		●		●					
10	8	7	AD9/P1.5	I/O	O	●		●		●	●				
11	–	8	CKO/AD8/P1.4	I/O	O	●		●		●	●				
12	–	9	PWM1/AD7/P1.3	I/O	O	●		●		●	●		●		
13	9	10	PWM0/AD6/P1.2	I/O	O	●		●		●	●		●		
14	10	11	T2EX/AD5/P1.1	I/O	O	●		●		●	●			●	
15	11	12	T2/T2O/AD4/P1.0	I/O	O	●		●		●	●			●	
16	12	13	RXD/AD3/P3.0	I/O	O			●	●		●	●			
17	13	14	TXD/AD2/P3.1	I/O	O			●	●		●	●			
18	14	15	INT0/AD1/P3.2	I/O	O	●	●	●	●		●				
19	15	16	INT1/AD0/P3.3	I/O	O	●	●	●		●	●				
20	16	17	VCC	P											

Symbol:

P.P. = Push-Pull Output
O.D. = Open Drain
P.O.D. = Pseudo Open Drain

PS:

1. ⊙ 3.7 Pull up resistor is fix enable
2. O Port1, P2.0, P2.1, Port3 these pins control Pull up resistor by operation modes

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The TM52 device features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a programming counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as “A” or “ACC,” including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR **E0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC:** Accumulator

1.2 B Register (B)

The “B” register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands are in A and B.

ex: DIV AB

When this instruction is executed, data inside A and B are divided, and the answer is stored in A.

SFR **F0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B:** B register

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer. The Stack Pointer points to the top location of the stack.

SFR **81h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP:** Stack Point

1.4 Dual Data Pointer (DPTRs)

TM52 device has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs.

SFR **82h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL:** Data Point low byte

SFR **83h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH:** Data Point high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W
Reset	0	0	–	0	0	0	0	0

F8h.0 **DPSEL:** Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The PSW affected by instructions is listed below.

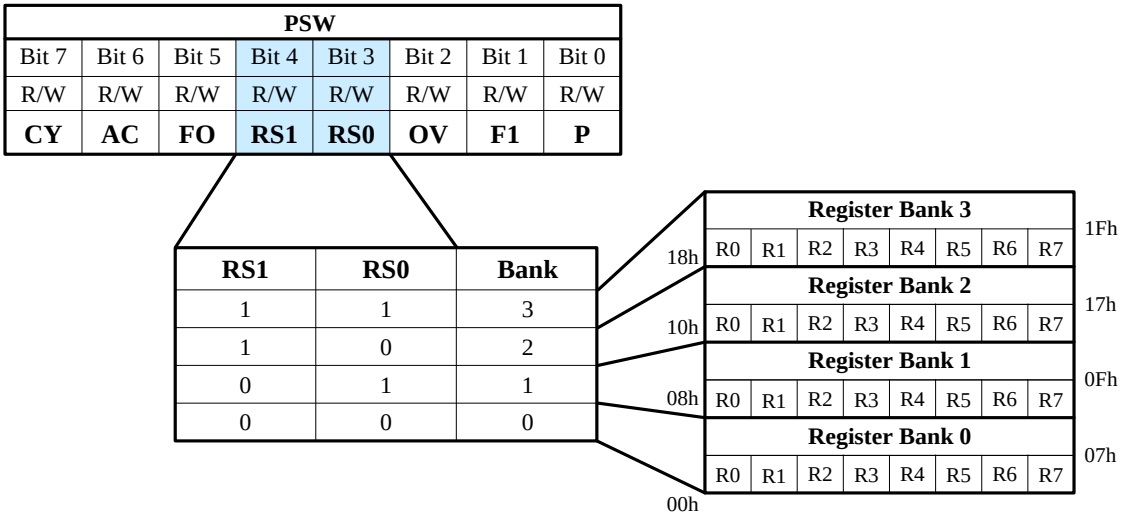
Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR **D0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY:** ALU carry flag
D0h.6 **AC:** ALU auxiliary carry flag
D0h.5 **F0:** General purpose user-definable flag
D0h.4~3 **RS1, RS0:** The contents of (RS1, RS0) enable the working register banks as:
00: Bank 0 (00h~07h)
01: Bank 1 (08h~0Fh)
10: Bank 2 (10h~17h)
11: Bank 3 (18h~1Fh)
D0h.2 **OV:** ALU overflow flag
D0h.1 **F1:** General purpose user-definable flag
D0h.0 **P:** Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.



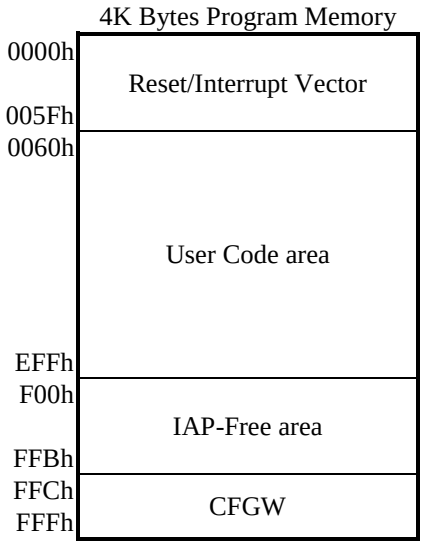
2. Memory

2.1 Program Memory

The **F5250** has a 4K Bytes Flash program memory, which can support in-circuit program (ICP), in-application program (IAP) and in-system program (ISP) function modes. The Flash write endurance is at least 50K cycles. The program memory address continuous space (0000h~FFFh) is partitioned to several sectors for device operation.

2.1.1 Program Memory Functional Partition

The last 4 bytes (FFCh~FFFh) of program memory is defined as chip Configuration Word (CFGW). Two of them are loaded into the device control registers upon power on reset (POR). The address space F00h~FFBh is the IAP free area, while the 0000h~005Fh is occupied by Reset/Interrupt vectors as standard 8051 definition.



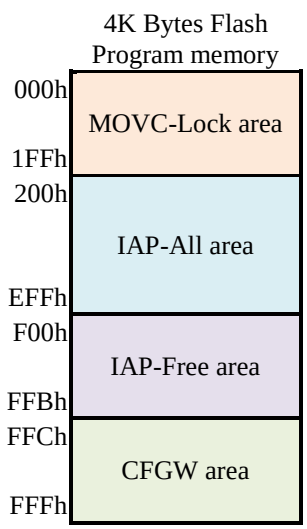
2.1.2 Flash ICP Mode

The Flash memory can be programmed by the tenx proprietary writer **(TWR98/TWR99)**, which needs at least four wires (VCC, VSS, P3.0 and P3.1 pins) to connect to this chip. To shorten the programming time, it is recommended to connect Writer with an additional fifth wire, which is the VPP (P3.7) pin. If the user wants to program the Flash memory on the target circuit board (In Circuit Program, ICP), these pins must be reserved sufficient freedom to be connected to the Writer. More pins connected to Writer ensure more writing efficiency and speed.

Writer wire number	Pin connection
4-Wire	VCC, VSS, P3.0, P3.1
5-Wire	VCC, VSS, P3.0, P3.1, VPP
7-Wire	VCC, VSS, P3.0, P3.1, VPP, P3.3, P1.2 ***Note:*** P3.2 output FRC/4 and P3.5 always output Low in this mode

2.1.3 Flash IAP Mode

The **F5250** has "In Application Program" (IAP) capability, which allows software to read/write data from/to the Flash memory during CPU run time as conveniently as data EEPROM access. The IAP function is byte writable, meaning that the **F5250** does not need to erase one Flash page before write. The available IAP data space is 252 Bytes after chip reset, and can be re-defined by the "MVCLOCK" and "IAPALL" control register as shown below.



Flash memory	MVCLOCK	IAPALL	MOVC Accessible	MOVX (IAP) Accessible
000h~1FFh	1	X	No	No
	0	0	Yes	No
	0	1	Yes	Yes
200h~EFFh	X	0	Yes	No
	X	1	Yes	Yes
F00h~FFBh	X	X	Yes	Yes
FFCh~FFEh	X	0	Yes	No
	X	1	Yes	Yes
FFFh	X	X	Yes	No

In IAP mode, the program Flash memory is separated into four sectors: MOVC-Lock area, IAP-All area, IAP-Free area, and CFGW area. These four sectors are regulated differently.

In the **MOVC-Lock area,** IAP read/write is limited by MVCLOCK bit, which can be set to control the accessibility of the MOVC and MOVX instructions to this area. The size of this area is 512 Bytes. The lock function is made to protect the main program code against unconsciously writing Flash memory in IAP mode. Locking or unlocking the function should be performed by the tenx TWR98/99 writing to the CFGW in Flash memory.

The **IAP-All area** is protected by the IAPALL register to prevent IAP mode from writing application data to the program area, resulting in a program code error that cannot be repaired. The size of this area is 3328 Bytes. Enabling IAPALL requires writing 65h to SFR SWCMD 97h to set the IAPALL control flag. Then, software can use MOVX instructions to write application data to flash memory from 0200h to EFFh. If user wants to disable IAPALL function, user can write other values to SFR SWCMD 97h to clear the IAPALL control flag. User must be careful not to overwrite program code which is already resided on the same Flash memory area.

The **IAP-Free area** has no control bit to protect. It can be used to reliably store system application data that needs to be programmed once or periodically during system operation. Other areas of Flash memory can be used to store data, but this area is usually the best. The size of this area is 252 Bytes, equivalent to an EEPROM, and Flash memory can provide byte access to read and write commands. In the past, storage of configuration data required an additional EEPROM or the other storage device. However, this functionality can now be provided by on-chip Flash, reducing the chip count of embedded applications. An external EEPROM or SRAM may not be needed.

The **CFGW area** has 4 data bytes (CFGWH, CFGWL and CFGWRx), which is located at the last 4 addresses of Flash memory. The CFGWH is not accessible to IAP, while the CFGWL and CFGWR can be read or written by IAP in case the IAPALL flag is set. CFGWL is copied to the SFR F7h after power on reset, software then take over CFGWL's control capability by modifying the SFR F7h.

2.1.4 IAP Mode Access Routines

Flash IAP Write is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target Flash address (0000h~FFEh), and the ACC contains the data being written. The F5250 accepts IAP write command only when IAPWE=1. Flash IAP writing requires approximately 200~500µs. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers and others) continue running during the writing time. The software must handle the pending interrupts after an IAP write. Flash IAP writing needs higher V_{CC} voltage, V_{CC} > 2.8V.

Because the Program memory and the IAP data space share the same entity, a **Flash IAP Read** can be performed by the "MOVX A, @DPTR" or "MOVC" instruction as long as the target address points to the 0000h~FFEh area. A Flash IAP read does not require extra CPU wait time.

```
; IAP example code
; need   2.8V < VDD < 3.6V
MOV     DPTR, #F00h         ; DPTR=F00h=target IAP address
MOV     A, #5Ah             ; A=5Ah=target IAP write data
MOV     C9h, #47h           ; IAPWE=1
MOVX    @DPTR, A            ; Flash[F00h]=5Ah, after IAP write
                            ; 200µs~500µs H/W writing time, CPU wait
MOV     C9h, #00h           ; IAPWE=0 immediately after IAP write
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=5Ah
CLR     A                   ; A=0
MOVC    A, @A+DPTR          ; A=5Ah
```

Flash **FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		VCCFLT	PWRSAV	MVCLOCK	–

FFFh.1 **MVCLOCK:** If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL/SWRST							
R/W	W							R/W
Reset	–							0

97h.7~0 **IAPALL (W):** Write 65h to set IAPALL control flag; Write other value to clear IAPALL flag. It is recommended to clear it immediately after IAP access.

97h.0 **IAPALL (R):** Flag indicates Flash memory sectors can be accessed by IAP or not. This bit combines with MVCLOCK to define the accessible IAP area.

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPWE	IAPWE							
R/W	R/W	W						
Reset	0	–						

C9h.7~0 **IAPWE (W):** Write 47h to set IAPWE control flag; Write other value to clear IAPWE flag. It is recommended to clear it immediately after IAP write.

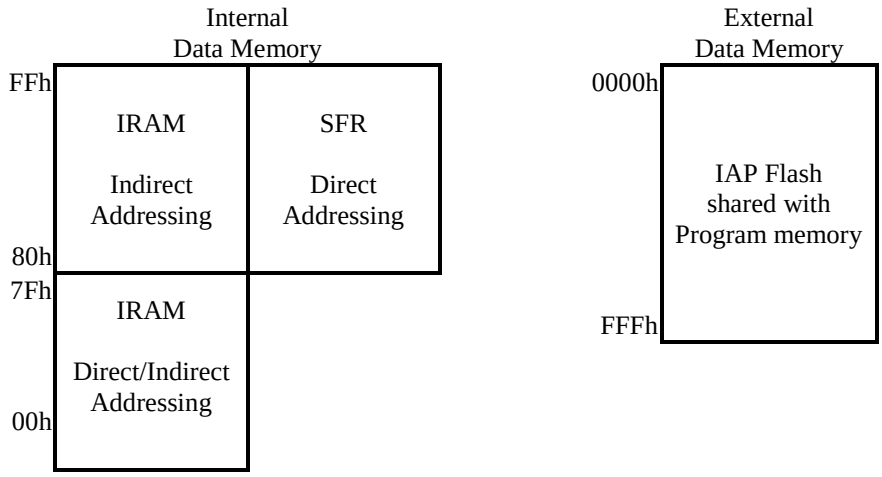
C9h.7 **IAPWE (R):** Flag indicates Flash memory can be written by IAP or not, 1=IAP Write enable.

2.1.5 Flash ISP Mode

The "In System Program" (ISP) usage is similar to IAP, except the purpose is to refresh the Program code. User can use UART or other method to get new Program code from external host, then writes code as the same way as IAP. ISP operation is complicated; basically it needs to assign a Boot code area to the Flash which does not change during the ISP process.

2.2 Data Memory

As the standard 8051, the **F5250** has both Internal and External Data Memory space. The Internal Data Memory space consists of 256 Bytes IRAM and 52 SFRs, which are accessible through a rich instruction set.

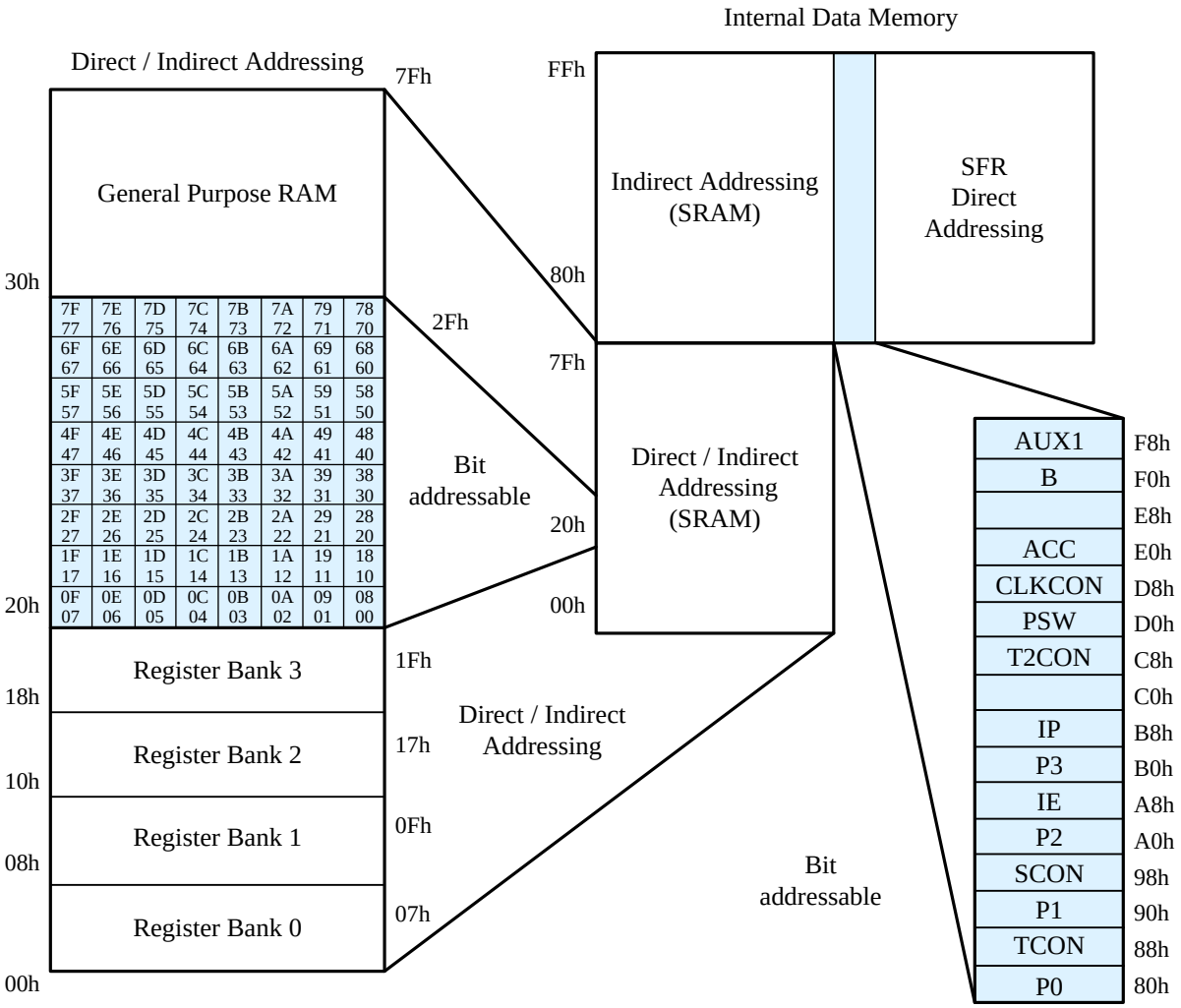


2.2.1 IRAM

IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

2.2.2 SFRs

All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with the resources and peripherals of the **F5250**. The TM52 series of microcontrollers provides complete binary code with standard 8051 instruction set compatibility. Beside the standard 8051 SFRs, the **F5250** implements additional SFRs used to configure and access subsystems such as the ADC, which are unique to the **F5250**.



	7	6	5	4	3	2	1	0
7Fh	7F	7E	7D	7C	7B	7A	79	78
77h	77	76	75	74	73	72	71	70
6Fh	6F	6E	6D	6C	6B	6A	69	68
67h	67	66	65	64	63	62	61	60
5Fh	5F	5E	5D	5C	5B	5A	59	58
57h	57	56	55	54	53	52	51	50
4Fh	4F	4E	4D	4C	4B	4A	49	48
47h	47	46	45	44	43	42	41	40
3Fh	3F	3E	3D	3C	3B	3A	39	38
37h	37	36	35	34	33	32	31	30
2Fh	2F	2E	2D	2C	2B	2A	29	28
27h	27	26	25	24	23	22	21	20
1Fh	1F	1E	1D	1C	1B	1A	19	18
17h	17	16	15	14	13	12	11	10
0Fh	0F	0E	0D	0C	0B	0A	09	08
07h	07	06	05	04	03	02	01	00

	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B							CFGWL
E8h								
E0h	ACC							
D8h	CLKCON							
D0h	PSW							
C8h	T2CON	IAPWE	RCP2L	RCP2H	TL2	TH2		
C0h								
B8h	IP	IPH	IP1	IP1H				
B0h	P3							
A8h	IE	INTE1	ADTKDT	ADCDH			CHSEL	
A0h	P2	PWMCON	P1MODL	P1MODH	P3MODL	P3MODH	PINMOD	
98h	SCON	SBUF	PWM0PRD	PWM0DH	PWM1PRD	PWM1DH		
90h	P1			P2MOD	OPTION	INTFLG	P1WKUP	SWCMD
88h	TCON	TMOD	TL0	TL1	TH0	TH1		
80h	P0	SP	DPL	DPH				PCON

3. Power

The **F5250** has a built-in internal low dropout regulator. When MODE3V=0, the voltage regulator outputs 3.3V power to the internal chip circuit. When MODE3V=1, the LDO is turned off, and the internal circuit receives a power supply directly from the VCC pin. Because the LDO consumes 150μA for operation, turning off LDO by setting MODE3V=1 can reduce the chip current consumption. However, setting MODE3V=1 is only valid for an operating condition of V_{CC} <3.6V. The PWRSAV also control the LDO. When MODE3V=0 and PWRSAV=1, the LDO is turned off in Stop mode for saving power consumption. In addition, set PWRSAV will affect the LVR/LVD setting.

MODE3V=0

Operation Mode	CFGW		Tiny Current	LDO	LVR	LVD	Function
	PWRSAV	LVRE					
Fast Slow Idle	X	00	–	ON	ON	–	LV Reset 2.9V
	X	01	–	ON	ON	–	LV Reset 2.3V
	X	10	–	ON	ON	–	LV Reset 3.5V
	X	11	–	ON	ON	ON	LV Reset 2.0V
Stop	0	00	–	ON	ON	–	LV Reset 2.9V
	0	01	–	ON	ON	–	LV Reset 2.3V
	0	10	–	ON	ON	–	LV Reset 3.5V
	0	11	–	ON	ON	–	LV Reset 2.0V
	1	00	Y	OFF	ON	–	LV Reset 2.0V
	1	01	Y	OFF	ON	–	LV Reset 2.0V
	1	10	Y	OFF	ON	–	LV Reset 2.0V
	1	11	Y	OFF	ON	–	LV Reset 2.0V

MODE3V=1

Operation Mode	CFGW		Tiny Current	LDO	LVR	LVD	Function
	PWRSAV	LVRE					
Fast Slow Idle	0	00	–	OFF	ON	–	LV Reset 2.9V
	0	01	–	OFF	ON	–	LV Reset 2.3V
	0	10	–	OFF	ON	–	LV Reset 3.5V
	0	11	–	OFF	ON	ON	LV Reset 2.0V
	1	00	Idle	OFF	ON	–	LV Reset 2.0V
	1	01	Idle	OFF	ON	–	LV Reset 2.0V
	1	10	Idle	OFF	ON	–	LV Reset 2.0V
	1	11	Idle	OFF	ON	–	LV Reset 2.0V
Stop	0	00	–	OFF	ON	–	LV Reset 2.9V
	0	01	–	OFF	ON	–	LV Reset 2.3V
	0	10	–	OFF	ON	–	LV Reset 3.5V
	0	11	Y	OFF	ON	–	LV Reset 2.0V
	1	00	Y	OFF	ON	–	LV Reset 2.0V
	1	01	Y	OFF	ON	–	LV Reset 2.0V
	1	10	Y	OFF	ON	–	LV Reset 2.0V
	1	11	Y	OFF	ON	–	LV Reset 2.0V

Note: Typical Tiny current of F5250 are Idle=5uA and Stop=3uA @VCC=3V, 32KHz
Note: FW must turn off Bandgap to obtain Tiny Current (ADCHS≠0b1011)

Flash **FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		VCCFLT	PWRSAV	MVCLOCK	–

FFFh.3 **VCCFLT:** Set 1 to enhance the chip's power noise immunity

FFFh.2 **PWRSAV:** Power save function control bit

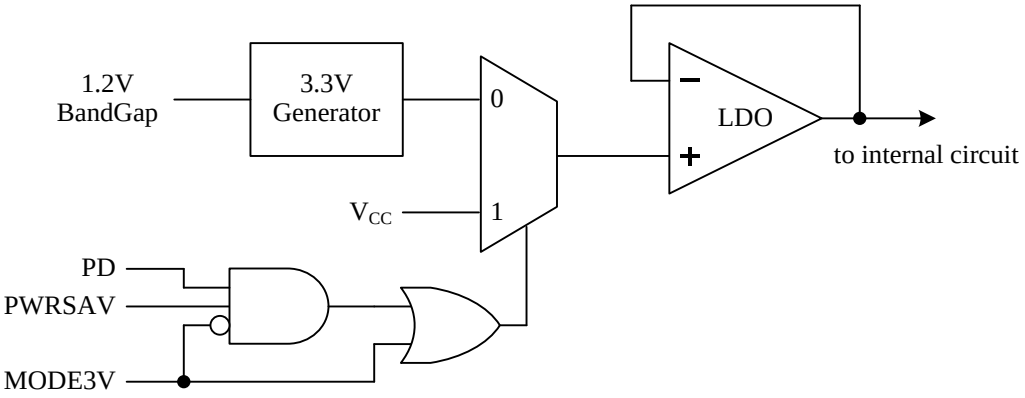
0: Disable Power save function

1: Enable Power save function

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.6 **MODE3V:** 3V mode selection control bit

If this bit is set, the chip can be only operated in the condition of V_{CC} < 3.6V, and LDO is turned off to save current



4. Reset

The **F5250** has five types of reset methods. Resets can be caused by Power on Reset (POR), External Pin Reset (XRST), Software Command Reset (SWRST), Watchdog Timer Reset (WDTR), or Low Voltage Reset (LVR). The CFGW controls the Reset functionality. The SFRs are returned to their default value after Reset.

4.1 Power on Reset

After Power on Reset, the device stays on Reset state for 40 ms as chip warm up time, then downloads the CFGW register from Flash‘s last two bytes (Other Reset will not reload the CFGW). The Power on Reset needs VCC pin’s voltage first discharge to near VSS level, then rise beyond 2.1V.

4.2 External Pin Reset

External Pin Reset is active low. It needs to keep at least 2 SRC clock cycle long to be seen by the chip. External Pin Reset can be disabled or enabled by CFGW.

4.3 Software Command Reset

Software Reset is activated by writing the SFR 97h with data 56h.

4.4 Watchdog Timer Reset

WDT overflow Reset is disabled or enabled by SFR F7h. The WDT uses SRC as its counting time base. It runs in Fast/Slow mode and runs or stops in Idle/Stop mode. WDT overflow speed can be defined by WDTPSC SFR. WDT is cleared by device Reset or CLRWDT SFR bit.

4.5 Low Voltage Reset

The **F5250** offers four options for LVR and Low Voltage Detection (LVD) functions. The user can make a selection by CFGW, let LVR voltages of 3.5V, 2.9V, 2.3V, and 2.0V be selected separately, and let LVD be 2.3V only. If the LVR is selected as 2.0V, the 2.3V LVD flag is available for LVD. If LVR is selected as 2.3V, 2.9V or 3.5V, the LVD flag cannot be used.

System Clock frequency	14.74MHz	9.8MHz	5MHz	2.5MHz
Minimum LVR level	LVR=3.5V	LVR=2.9V	LVR=2.3V	LVR=2.0V

LVR setting table

Note: LVR must be enable, also refer to AP-TM52XXXXX_02S for LVR setting information

Flash **FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		VCCFLT	PWRSAV	MVCLOCK	–

FFFh.6 **XRSTE:** External Pin Reset control
0: Disable External Pin Reset
1: Enable External Pin Reset

FFFh.5~4 **LVRE:** Low Voltage Reset function select
00: Set LVR at 2.9V
01: Set LVR at 2.3V
10: Set LVR at 3.5V
11: Set LVR at 2.0V and LVD at 2.3V

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	WDTE		–	FRCF				
R/W	R/W		–	R/W				
Reset	–	–	–	–	–	–	–	–

F7h.7~6 **WDTE:** Watchdog Timer Reset control. It is automatically loaded with Flash's FFEh data at power on reset and can be read/written as any other SFR register in normal mode. So the WDT can be changed on CPU run time by S/W.
0x: Watchdog Timer Reset disable
10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Stop mode
11: Watchdog Timer Reset always enable

Note: FW should not change FRCF while writing WDTE

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.5~4 **WDTPSC:** Watchdog Timer pre-scalar time select
00: 360ms WDT overflow rate
01: 180ms WDT overflow rate
10: 90ms WDT overflow rate
11: 45ms WDT overflow rate

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	–	ADIF	–	IE2	P1IF	TF3
R/W	R	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

95h.7 **LVD:** Low Voltage Detect flag
Set by H/W when a low voltage occurs. The flag is valid when LVR is 2.0V. This flag is disabled if MODE3V=1 and PWRSAV=1.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL/SWRST							
R/W	W							R/W
Reset	–							0

97h.7~0 **SWRST:** Write 56h to generate S/W Reset

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W
Reset	0	0	–	0	0	0	0	0

F8h.7 **CLRWDT:** Set to clear WDT, H/W auto clear it at next clock cycle

5. Clock Circuitry and Operation Mode

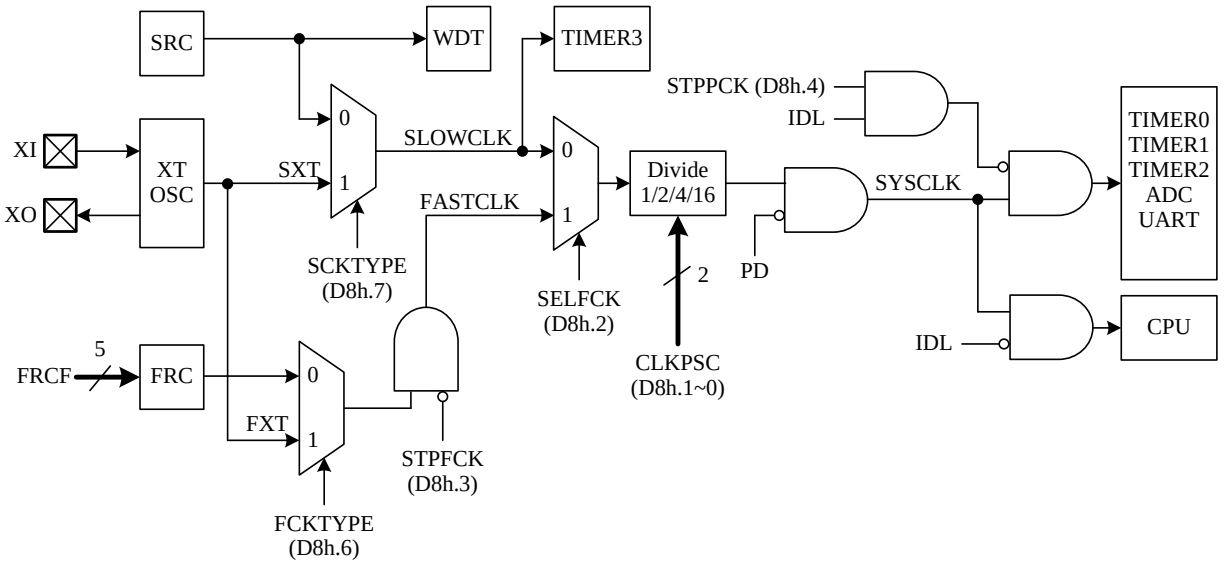
5.1 System Clock

The **F5250** is designed with dual-clock system. During runtime, user can directly switch the System clock from fast to slow or from slow to fast. It also can directly select a clock divider of 1, 2, 4 or 16. The Fast clock can be selected as FXT (Fast Crystal, 1~14.746 MHz) or FRC (Fast Internal RC, 9.83 MHz). The Slow clock can be selected as SXT (Slow Crystal, 32 KHz) or SRC (Slow Internal RC, 24 KHz). Fast mode and Slow mode are defined as the CPU running at Fast and Slow clock speeds.

After Reset, the device is running at Slow mode with 24 KHz SRC. S/W should select the proper clock rate for chip operation safety. The higher V_{CC} allows the chip to run at a higher System clock frequency. In a typical condition, a 9.8 MHz System clock rate requires V_{CC} >2.9V.

The **F5250** has an external oscillators connected to the XI/XO pins. It relies on external circuitry for the clock signal and frequency stabilization, such as a stand-alone oscillator, quartz crystal, or ceramic resonator. In Fast mode, the fast oscillator can be used in the range from 1~14.746 MHz. In Slow mode, the slow oscillator can only use a clock frequency of 32.768 KHz.

The **CLKCON** SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow clock type in Fast mode and change the Fast clock type in Slow mode. Never to write both STPFCK=1 & SELFCK=1. It is recommended to write this SFR bit by bit.



Flash **FFEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	–	–	–	FRCF				

FFEh.4~0 **FRCF:** FRC frequency adjustment.
FRC is trimmed to 9.83 MHz in chip manufacturing. FRCF records the adjustment data.

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	WDTE		–	FRCF				
R/W	R/W		–	R/W				
Reset	–	–	–	–	–	–	–	–

F7h.4~0 **FRCF:** FRC frequency adjustment. It is automatically loaded with Flash's FFEh data at power on reset and can be read/written as any other SFR register in normal mode. So the FRC clock speed can be changed on CPU run time by S/W.
00h=central frequency, 0Fh=highest frequency, 10h=lowest frequency.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	–	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	
Reset	0	0	–	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC
1: SXT

D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC
1: FXT

D8h.4 **STPPCK:** Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode.
This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

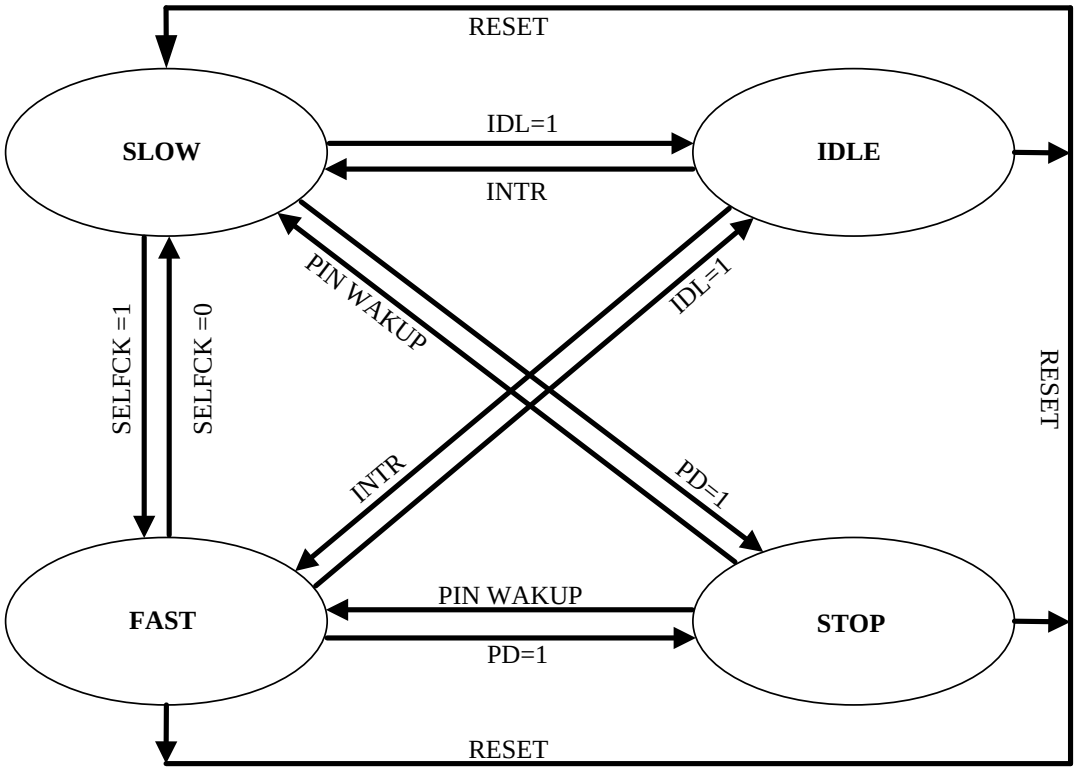
Note: also refer to AP-TM52XXXXX_01S and AP-TM52XXXXX_02S about System Clock Application Note.

5.2 Operation Mode

There are four operation modes for this device. **Fast Mode** is defined as the CPU running at Fast clock speed. **Slow Mode** is defined as the CPU running at Slow clock speed. When the System clock speed is lower, the power consumption is lower.

Idle Mode is entered by setting the IDL bit in PCON SFR. Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The "STPPCK" bit in CLKCON SFR can be set to furthermore reduce Idle mode current. If STPPCK=1, Timer0/1/2, ADC and UART are stopped in Idle mode. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Stop Mode is entered by setting the PD bit in PCON SFR. This mode is the so-called "Power Down" mode in standard 8051. In Stop mode, all clocks stop except the WDT is alive if it is enabled. Stop mode can be terminated by Reset or pin wake up.



Operation Mode Transition

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Stop bit. If 1 Stop mode is entered.
87h.0 **IDL:** Idle bit. If 1, Idle mode is entered.

6. Interrupt and Wake-up

This **F5250** has a 10-source four-level priority interrupt structure. All enabled Interrupts can wake up CPU from Idle mode, but only the Pin Interrupts can wake up CPU from Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter whether its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	Flag	Description
0003	IE0	INT0 external pin Interrupt (can wake up Stop mode)
000B	TF0	Timer0 Interrupt
0013	IE1	INT1 external pin Interrupt (can wake up Stop mode)
001B	TF1	Timer1 Interrupt
0023	RI+TI	Serial Port (UART) Interrupt
002B	TF2+EXF2	Timer2 Interrupt
0033	–	Reserved
003B	TF3	Timer3 Interrupt
0043	P1IF	Port1 external pin change Interrupt (can wake up Stop mode)
004B	IE2	INT2 external pin Interrupt (can wake up Stop mode)
0053	ADIF	ADC Interrupt

Interrupt Vector & Flag

6.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

SFR **96h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1WKUP	P1WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

96h.7~0 **P1WKUP:** P1.7~P1.0 pin individual Wake up/Interrupt enable control
0: Disable
1: Enable

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable
0: Disable all interrupts
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.5 **ET2:** Timer2 interrupt enable
0: Disable Timer2 interrupt
1: Enable Timer2 interrupt

A8h.4 **ES:** Serial Port (UART) interrupt enable
0: Disable Serial Port (UART) interrupt
1: Enable Serial Port (UART) interrupt

A8h.3 **ET1:** Timer1 interrupt enable
0: Disable Timer1 interrupt
1: Enable Timer1 interrupt

A8h.2 **EX1:** INT1 pin Interrupt enable and Stop mode wake up enable
0: Disable INT1 pin Interrupt and Stop mode wake up
1: Enable INT1 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A8h.1 **ET0:** Timer0 interrupt enable
0: Disable Timer0 interrupt
1: Enable Timer0 interrupt

A8h.0 **EX0:** INT0 pin Interrupt enable and Stop mode wake up enable
0: Disable INT0 pin Interrupt and Stop mode wake up
1: Enable INT0 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	–	–	–	–	ADIE	EX2	P1IE	TM3IE
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

A9h.3 **ADIE:** ADC interrupt enable
0: Disable ADC interrupt
1: Enable ADC interrupt

A9h.2 **EX2:** INT2 pin Interrupt enable and Stop mode wake up enable
0: Disable INT2 pin Interrupt and Stop mode wake up
1: Enable INT2 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A9h.1 **P1IE:** Port1 pin change interrupt enable
0: Disable Port1 pin change interrupt
1: Enable Port1 pin change interrupt

A9h.0 **TM3IE:** Timer3 interrupt enable
0: Disable Timer3 interrupt
1: Enable Timer3 interrupt

SFR **B9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

SFR **B8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

B9h.5, B8h.5 **PT2H, PT2:** Timer2 interrupt priority control. (PT2H, PT2) =
00: Level 0 (lowest priority)
01: Level 1
10: Level 2
11: Level 3 (highest priority)

B9h.4, B8h.4 **PSH, PS:** Serial Port (UART) interrupt priority control. Definition as above.
B9h.3, B8h.3 **PT1H, PT1:** Timer1 interrupt priority control. Definition as above.
B9h.2, B8h.2 **PX1H, PX1:** INT1 pin interrupt priority control. Definition as above.
B9h.1, B8h.1 **PT0H, PT0:** Timer0 interrupt priority control. Definition as above.
B9h.0, B8h.0 **PX0H, PX0:** INT0 pin interrupt priority control. Definition as above.

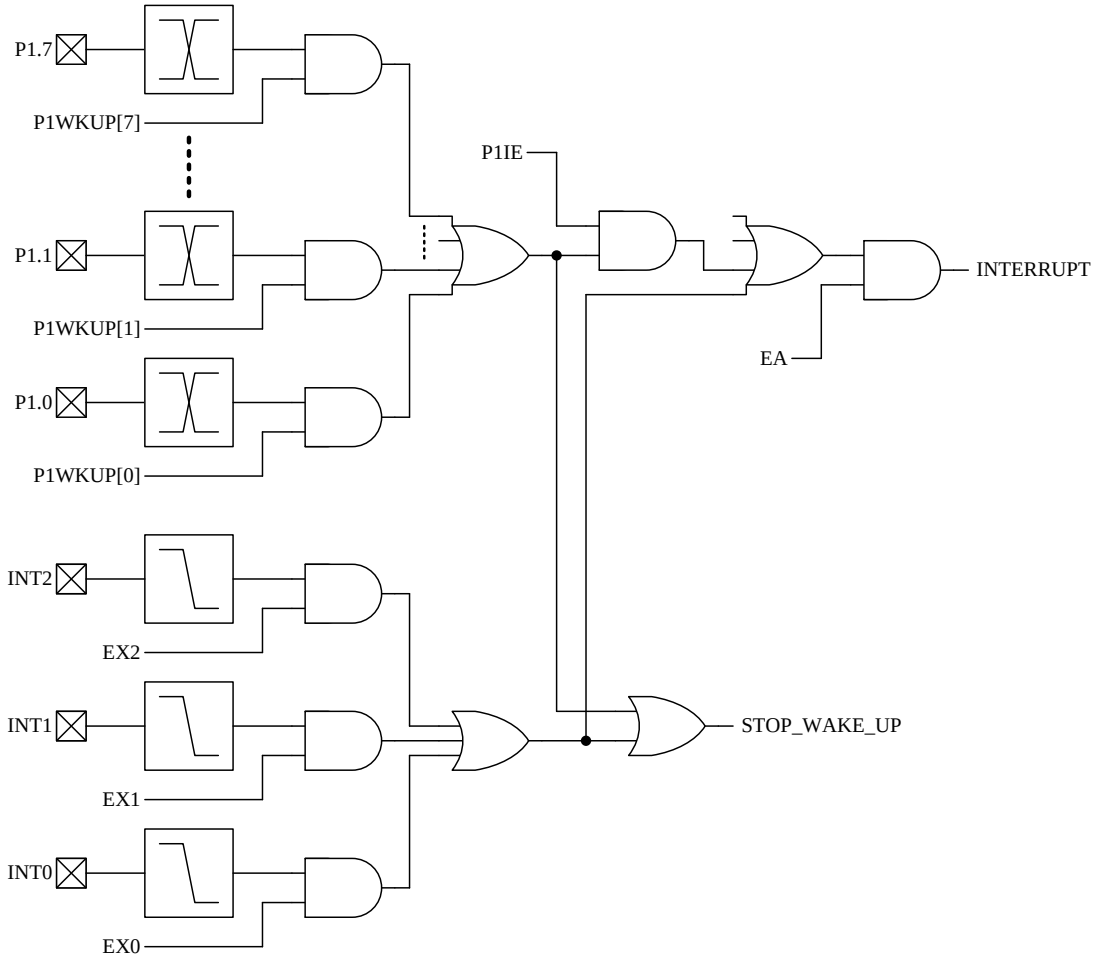
SFR **BBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	–	–	–	–	PADIH	PX2H	PP1H	PT3H
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

SFR **BAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	–	–	–	–	PADI	PX2	PP1	PT3
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

BBh.3, BAh.3 **PADIH, PADI:** ADC interrupt priority control. Definition as above.
BBh.2, BAh.2 **PX2H, PX2:** INT2 pin interrupt priority control. Definition as above.
BBh.1, BAh.1 **PP1H, PP1:** Port1 pin change interrupt priority control. Definition as above.
BBh.0, BAh.0 **PT3, PT3:** Timer3 interrupt priority control. Definition as above.

6.2 Pin Interrupt

Pin Interrupts include INT0 (P3.2), INT1 (P3.3), INT2 (P3.7) and Port1 Change Interrupt. These pins also have the Stop mode wake up capability. INT0 and INT1 are falling edge or low level triggered as the 8051 standard. INT2 is falling edge triggered, while Port1 Change Interrupt is triggered by any Port1 pin state change.



Pin Interrupt & Wake up

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin

88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	–	ADIF	–	IE2	P1IF	TF3
R/W	R	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

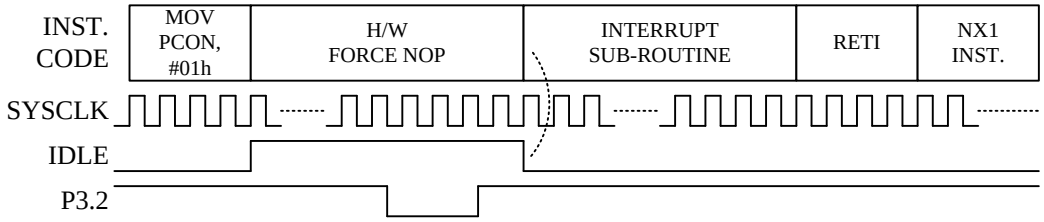
95h.2 **IE2:** External Interrupt 2 (INT2 pin) edge flag
Set by H/W when a falling edge is detected on the INT2 pin state, no matter the EX2 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FBh to INTFLG to clear this bit. (Note2)

95h.1 **P1IF:** Port1 pin change interrupt flag
Set by H/W when a P1 pin state change is detected, and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FDh to INTFLG to clear this bit. (Note2)

Note2: S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.

6.3 Idle Mode Wake up and Interrupt

Idle mode is waked up by enabled Interrupts, which means individual interrupt enable bit (ex: EX0) and EA bit must be both set to 1 to establish Idle mode wake up capability. All enabled Interrupts (Pins, Timers, ADC and UART) can wake up CPU from Idle mode. Upon Idle wake-up, Interrupt service routine is entered immediately. "The first instruction behind IDL (PCON.0) setting" is executed after interrupt service routine return.



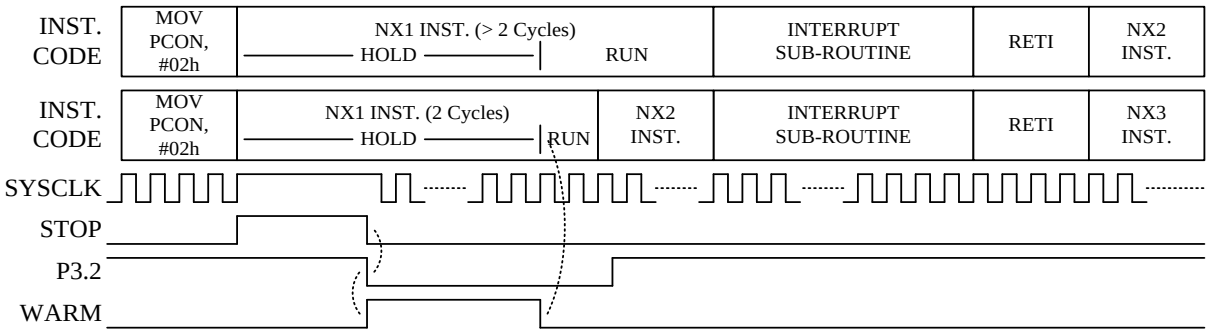
EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

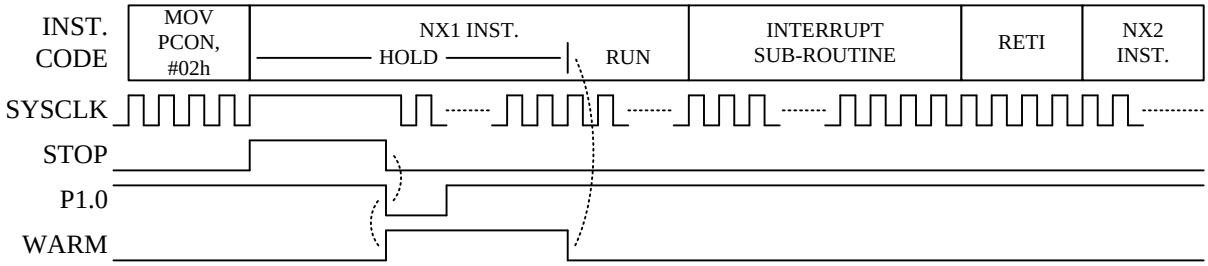
87h.1 **PD:** Stop bit. If 1, Stop mode is entered.
87h.0 **IDL:** Idle bit. If 1, Idle mode is entered.

6.4 Stop Mode Wake up and Interrupt

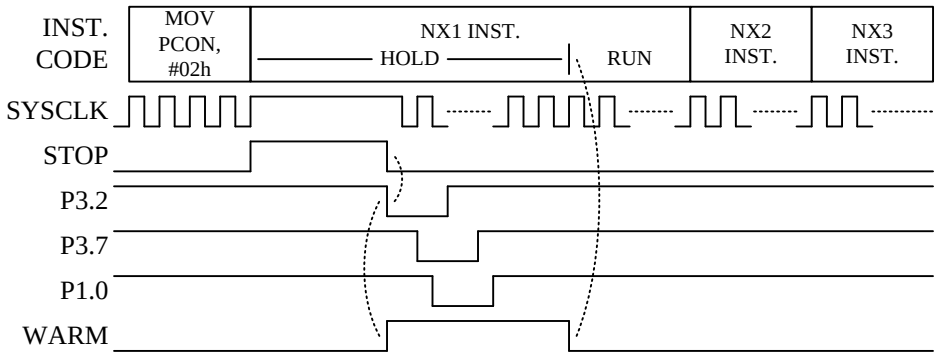
Stop mode wake up is simple, as long as the individual pin interrupt enable bit (ex: EX0) is set, the pin wake up capability is asserted. Set EX0/EX1/EX2 can enable INT0/INT1/INT2 pins' Stop mode wake up capability. Set P1WKUP bit 7~0 can enable P1.7~P1.0's Stop mode wake up capability. Upon Stop wake up, "the first instruction behind PD (PCON.1) setting" is executed immediately before Interrupt service. Interrupt entry needs EA=1 (P1WKUP also needs P1IE=1) and the trigger state of the pin staying sufficiently long to be observed by the System clock. This feature allows CPU to enter or not enter Interrupt sub-routine after Stop mode wake up.



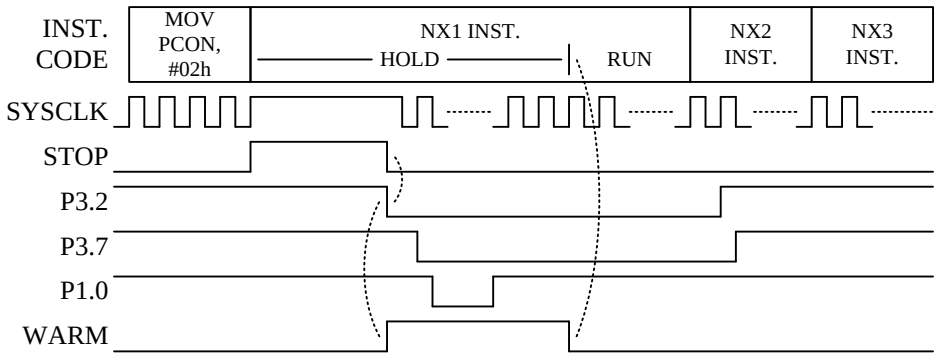
EA=EX0=1
P3.2 (INT0) is sampled after warm-up, Stop mode wake-up and Interrupt.



EA=P1IE=P1WKUP=1
P1.0 change (not need clock sample), Stop mode wake-up and Interrupt.



EA=EX0=EX2=P1WKUP=1, P1IE=0
Stop mode wake-up but not Interrupt, P3.2/P3.7 pulse too narrow.



EX0=EX2=P1WKUP=1=P1IE=1, EA=0
Stop mode wake-up but not Interrupt.

7. I/O Ports

The **F5250** has total 18 multi-function I/O pins. All I/O pins follow the standard 8051 "Read-Modify-Write" feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR. (ex: ANL P1, A; INC P2; CPL P3.0)

7.1 Port1 & P2.1~P2.0 & P3.6~P3.0

These pins can operate in four different modes as below.

Mode	Port1, P2.1~P2.0, P3.6~P3.0 pin function		Px.n SFR data	Pin State	Resistor Pull-up	Digital Input
	P3.2~P3.0	Others				
Mode 0	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Pull-up	Y	Y
Mode 1	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Hi-Z	N	Y
Mode 2	CMOS Output		0	Drive Low	N	N
			1	Drive High	N	N
Mode 3	Alternative Function, such as ADC		X (don't care)	–	N	N

Port1, P2.1~P2.0, P3.6~P3.0 I/O Pin Function Table

If a Port1, P2.1~P2.0 or P3.6~P3.0 pin is used for Schmitt-trigger input, S/W must set the I/O pin to Mode0 or Mode1 and set the corresponding Port Data SFR to 1 to disable the pin's output driving circuitry.

Beside I/O port function, each Port1, P2.1~P2.0 and P3.6~P3.0 pin has one or more alternative functions, such as ADC. Most of the functions are activated by setting the individual pin mode control SFR to Mode3. Port1/Port3 pins have standard 8051 auxiliary definition such as INT0/1, T0/1/2, or RXD/TXD. These pin functions need to set the pin mode SFR to Mode0 or Mode1 and keep the P1.n/P3.n SFR at 1.

Pin Name	8051	Wake-up	CKO	ADC	others	Mode3
P1.0	T2	Y	T2O	AD4		AD4
P1.1	T2EX	Y		AD5		AD5
P1.2		Y		AD6	PWM0	AD6
P1.3		Y		AD7	PWM1	AD7
P1.4		Y	CKO	AD8		AD8
P1.5		Y		AD9		AD9
P1.6		Y				
P1.7		Y				
P3.0	RXD			AD3		AD3
P3.1	TXD			AD2		AD2
P3.2	INT0	Y		AD1		AD1
P3.3	INT1	Y		AD0		AD0
P3.4	T0		T0O			
P3.5	T1					
P3.6						
P2.0					XI	
P2.1					XO	

Port1, P2.1~P2.0, P3.6~P3.0 multi-function Table

The necessary SFR setting for Port1/P2.1~P2.0/P3.6~P3.0 pin's alternative function is list below.

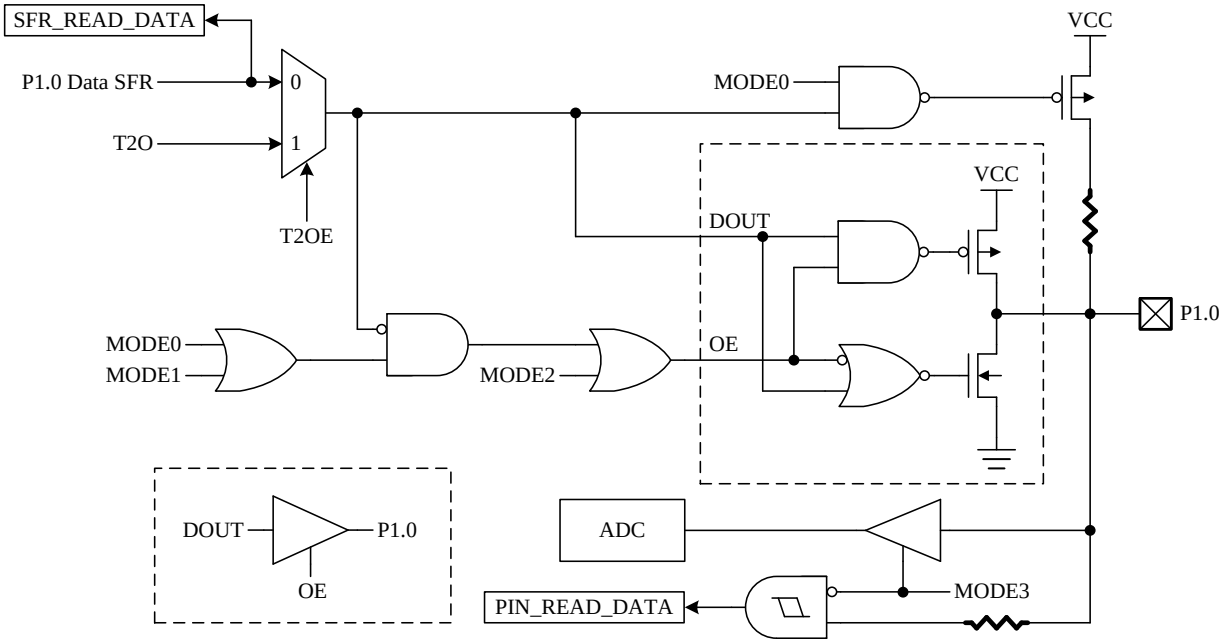
Alternative Function	Mode	Px.n SFR data	Pin State	Other necessary SFR setting
T0, T1, T2, T2EX, INT0, INT1	**0**	1	Input with Pull-up	
	1	1	Input	
RXD, TXD	**0**	1	Input with Pull-up/Pseudo Open Drain Output	
	1	1	Input/Pseudo Open Drain Output	
T0O, T2O, CKO	**0**	X	Clock Open Drain Output with Pull-up	PINMOD P3MODH
	1	X	Clock Open Drain Output	
	2	X	Clock Output (CMOS Push-Pull)	
AD0~AD9	**3**	X	ADC Channel	
PWM0, PWM1	**0**	X	PWM Open Drain Output with Pull-up	PINMOD
	1	X	PWM Open Drain Output	
	2	X	PWM Output (CMOS Push-Pull)	
XI, XO	**0**	1	Crystal oscillation	CLKCON

Mode Setting for Port1, P2.1~P2.0, P3.6~P3.0 Alternative Function

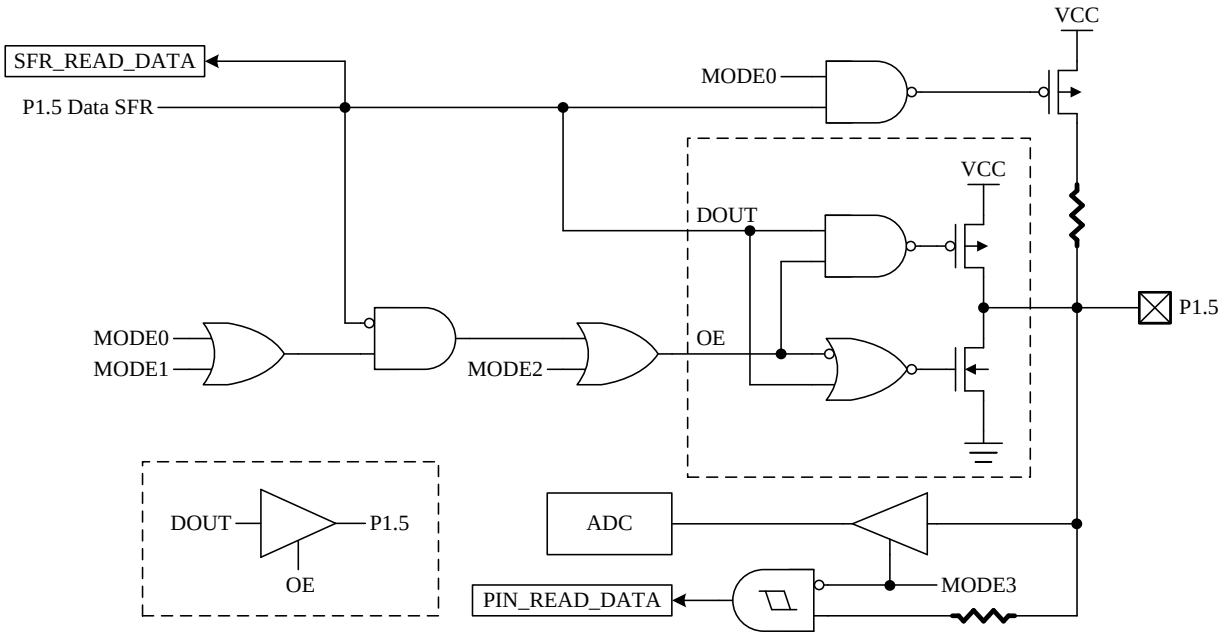
For tables above, a **"COMS Output"** pin means it can sink and drive at least 4 mA current. It is not recommended to use such pin as input function.

An **"Open Drain"** pin means it can sink at least 4 mA current but only drive a small current (<20μA). It can be used as input or output function and typically needs an external pull up resistor.

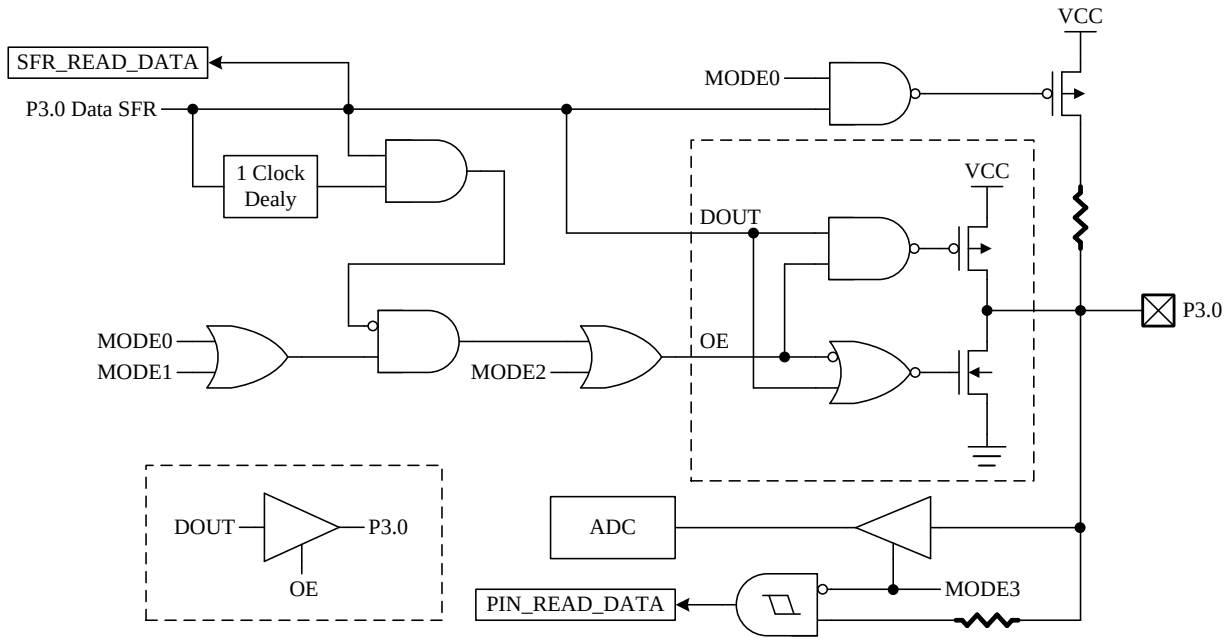
An 8051 standard pin is a **"Pseudo Open Drain"** pin. It can sink at least 4 mA current when output is at low level, and drives at least 4 mA current for 1~2 clock cycle when output transits from low to high, then keeps driving a small current (<20μA) to maintain the pin at high level. It can be used as input or output function.



P1.0 Pin Structure



P1.5 Pin Structure



P3.0 Pin Structure

SFR **90h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

90h.7~0 **P1:** Port1 data

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.6~0 **P3.6~P3.0:** P3.6~P3.0 data

SFR **A0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.1~0 **P2.1~P2.0:** P2.1~P2.0 data

SFR **A2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A2h.7~6 **P1MOD3:** P1.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.3 is ADC input

A2h.5~4 **P1MOD2:** P1.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.2 is ADC input

A2h.3~2 **P1MOD1:** P1.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.1 is ADC input

A2h.1~0 **P1MOD0:** P1.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.0 is ADC input

SFR **A3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A3h.7~6 **P1MOD7:** P1.7 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

A3h.5~4 **P1MOD6:** P1.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

A3h.3~2 **P1MOD5:** P1.5 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.5 is ADC input

A3h.1~0 **P1MOD4:** P1.4 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.4 is ADC input

SFR **A4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A4h.7~6 **P3MOD3:** P3.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.3 is ADC input

A4h.5~4 **P3MOD2:** P3.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.2 is ADC input

A4h.3~2 **P3MOD1:** P3.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.1 is ADC input

A4h.1~0 **P3MOD0:** P3.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.0 is ADC input

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	T0OE	–	P3MOD6		P3MOD5		P3MOD4	
R/W	R/W	–	R/W		R/W		R/W	
Reset	0	–	0	0	0	0	0	0

A5h.7 **T0OE:** Timer0 signal output (T0O) control
0: Disable Timer0 overflow divided by 64 output to P3.4
1: Enable Timer0 overflow divided by 64 output to P3.4

A5h.5~4 **P3MOD6:** P3.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

A5h.3~2 **P3MOD5:** P3.5 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

A5h.1~0 **P3MOD4:** P3.4 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2MOD	P2OE				P2MOD1		P2MOD0	
R/W	R/W				R/W		R/W	
Reset	0	0	0	0	0	1	0	1

93h.3~2 **P2MOD1:** P2.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

93h.1~0 **P2MOD0:** P2.0 pin control
00: Mode0 01: Mode1 10: Mode2 11: not defined

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1AOE	–	PWM0AOE	–	TCOE	T2OE	–	–
R/W	R/W	–	R/W	–	R/W	R/W	–	–
Reset	0	–	0	–	0	0	–	–

A6h.7 **PWM1AOE:** PWM1 signal output enable
0: Disable PWM1 signal output to P1.3
1: Enable PWM1 signal output to P1.3

A6h.5 **PWM0AOE:** PWM0 signal output enable
0: Disable PWM0 signal output to P1.2
1: Enable PWM0 signal output to P1.2

A6h.3 **TCOE:** System clock signal output (CKO) control
0: Disable System clock divided by 2 output to P1.4
1: Enable System clock divided by 2 output to P1.4

A6h.2 **T2OE:** Timer2 signal output (T2O) control
0: Disable Timer2 overflow divided by 2 output to P1.0
1: Enable Timer2 overflow divided by 2 output to P1.0

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	–	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	
Reset	0	0	–	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC, P2.1~P2.0 are I/O pins
1: SXT, P2.1~P2.0 are crystal pins

D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC, P2.1~P2.0 are I/O pins
1: FXT, P2.1~P2.0 are crystal pins

7.2 P3.7

P3.7 can be only used as Schmitt-trigger input or open-drain output, with pull-up resistor always enable. P3.7 pin is shared with RSTn, INT2 and Flash VPP function.

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

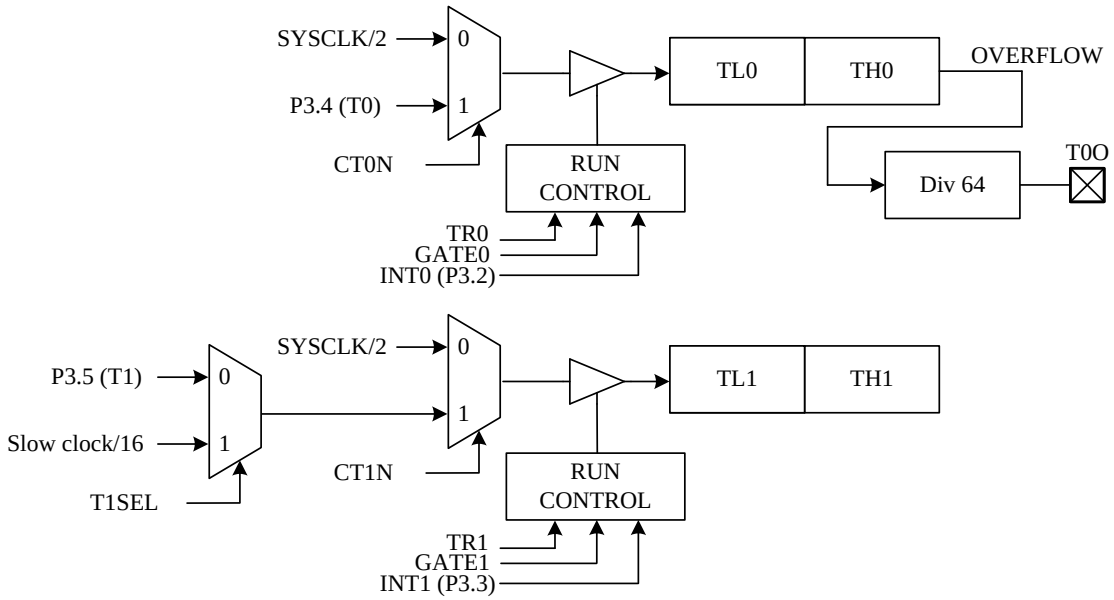
B0h.7 **P3.7:** P3.7 data, also controls the P3.7 pin's I/O mode. If the P3.7 SFR data is "1", the P3.7 is assigned as Schmitt-trigger input mode; otherwise, it is assigned as open-drain output mode.

8. Timers

Timer0, Timer1 and Timer2 are provided as standard 8051 compatible timer/counter. Timer3 is provided for a real-time clock count, when its time base is SXT.

8.1 Timer0/Timer1/Timer2

Compare to the traditional 12T 8051, the chip's Timer0/1/2 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every "2 System clock" rate; in counter mode, T0/T1/T2 pin input pulse must be wider than 2 System clock to be seen by this device. In addition to the standard 8051 timers function, SLOWCLK/16 can replace P3.5 (T1) and P1.0 (T2) pins as the Timer1 and Timer2 counter mode input. The T0O pin can output the "Timer0 overflow divided by 64" signal, and the T2O pin can output the "Timer2 overflow divided by 2" signal.



Timer0 and Timer1 Structure

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows.
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs

88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows.
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR **89h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set

89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin or SLOWCLK/16 falling edge

89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops

89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

89h.2 **CT0N:** Timer0 Counter/Timer select bit
0: Timer mode, Timer0 data increases at 2 System clock cycle rate
1: Counter mode, Timer0 data increases at T0 pin's negative edge

89h.1~0 **TMOD0:** Timer0 mode select
00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR **8Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR **8Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

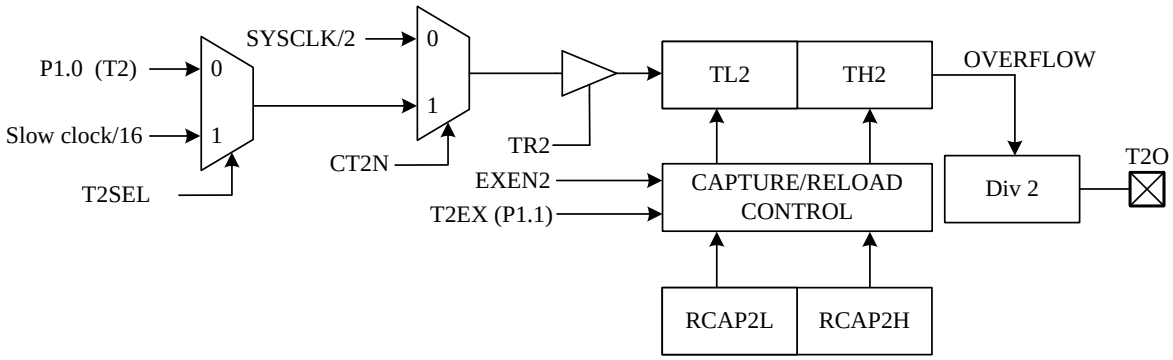
SFR **8Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

SFR **8Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

Timer2 is controlled through the TCON2 register with the low and high bytes of Timer/Counter 2 stored in TL2 and TH2 and the low and high bytes of the Timer2 reload/capture registers stored in RCAP2L and RCAP2H.



Timer2 Structure

SFR **C8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

C8h.7 **TF2:** Timer2 overflow flag
Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.

C8h.6 **EXF2:** T2EX interrupt pin falling edge flag
Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.

C8h.5 **RCLK:** UART receive clock control bit
0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3
1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3

C8h.4 **TCLK:** UART transmit clock control bit
0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3
1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3

C8h.3 **EXEN2:** T2EX pin enable
0: T2EX pin disable
1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0

C8h.2 **TR2:** Timer2 run control
0: Timer2 stops
1: Timer2 runs

C8h.1 **CT2N:** Timer2 Counter/Timer select bit
0: Timer mode, Timer2 data increases at 2 System clock cycle rate
1: Counter mode, Timer2 data increases at T2 pin or SLOWCLK/16 falling edge

C8h.0 **CPRL2N:** Timer2 Capture/Reload control bit
0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1
1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1
If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow

SFR **CAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2L	RCP2L							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CAh.7~0 **RCP2L:** Timer2 reload/capture data low byte

SFR **CBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2H	RCP2H							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CBh.7~0 **RCP2H:** Timer2 reload/capture data high byte

SFR **CCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL2	TL2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CCh.7~0 **TL2:** Timer2 data low byte

SFR **CDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH2	TH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CDh.7~0 **TH2:** Timer2 data high byte

This device can generate various frequency waveform pin output (in CMOS or Open-Drain format) for Buzzer. The T0O waveform is Timer0 overflow divided by 64, and T2O waveform is Timer2 overflow divided by 2. User can control their frequency by Timers auto reload speed. Set T0OE and T2OE SFRs can output these waveforms.

The Time1 and Timer2's SLOWCLK/16 counter mode input makes the Timer usage more flexible. Set T1SEL and T2SEL SFRs can enable this function.

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1AOE	–	PWM0AOE	–	TCOE	T2OE	–	–
R/W	R/W	–	R/W	–	R/W	R/W	–	–
Reset	0	–	0	–	0	0	–	–

A6h.2 **T2OE:** Timer2 signal output (T2O) control
0: Disable Timer2 overflow divided by 2 output to P1.0
1: Enable Timer2 overflow divided by 2 output to P1.0

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	T0OE	–	P3MOD6		P3MOD5		P3MOD4	
R/W	R/W	–	R/W		R/W		R/W	
Reset	0	–	0	0	0	0	0	0

A5h.7 **T0OE:** Timer0 signal output (T0O) control
0: Disable Timer0 overflow divided by 64 output to P3.4
1: Enable Timer0 overflow divided by 64 output to P3.4

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W
Reset	0	0	–	0	0	0	0	0

F8h.2 **T2SEL:** Timer2 counter mode (CT2N=1) input select
0: P1.0 (T2) pin (8051standard)
1:Slow clock divide by 16 (SLOWCLK/16)

F8h.1 **T1SEL:** Timer1 counter mode (CT1N=1) input select
0: P3.5 (T1) pin (8051 standard)
1: Slow clock divide by 16 (SLOWCLK/16)

8.2 Timer3

Timer3 of **F5250** works as a time-base counter, which generates interrupts periodically. It generates an interrupt flag (TF3) with the clock divided by 32768, 16384, 8192, or 128 depending on the TM3PSC bits. The Timer3 clock source is Slow clock (SRC or SXT). This is ideal for real-time-clock (RTC) functionality when the clock source SXT.

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.1~0 **TM3PSC:** Timer3 interrupt rate control select
00: Interrupt rate is 32768 Slow clock cycle
01: Interrupt rate is 16384 Slow clock cycle
10: Interrupt rate is 8192 Slow clock cycle
11: Interrupt rate is 128 Slow clock cycle

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	–	ADIF	–	IE2	P1IF	TF3
R/W	R	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

95h.0 **TF3:** Timer 3 interrupt flag
Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit. (***Note2***)

Note2: S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W
Reset	0	0	–	0	0	0	0	0

F8h.6 **CLRTM3:** Set to clear Timer3, H/W auto clear it at next clock cycle

Note: also refer to Section 6 for more information about Timer0/1/2/3 Interrupt enable and priority.

9. UART

The UART uses SCON and SBUF SFRs. SCON is the control register, SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are completely independent. In addition to standard 8051's full duplex mode, this chip also provides one wire mode. If the UART1W bit is set, both transmit and receive data use P3.1 pin.

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.7 **SMOD:** UART double baud rate control bit
0: Disable UART double baud rate
1: Enable UART double baud rate

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.7 **UART1W:** One wire UART mode enable, both TXD/RXD use P3.1 pin
0: Disable one wire UART mode
1: Enable one wire UART mode

SFR **98h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** Serial port mode select bit 0,1
00: Mode0: 8 bit shift register, Baud Rate=$F_{SYSCLK}/2$
01: Mode1: 8 bit UART, Baud Rate is variable
10: Mode2: 9 bit UART, Baud Rate=$F_{SYSCLK}/32$ or /64
11: Mode3: 9 bit UART, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2
SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART reception enable
0: Disable reception
1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR **99h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

99h.7~0 **SBUF:** UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

F_{SYSCLK} denotes System clock frequency.

- Mode 0:

  Baud Rate=$F_{SYSCLK}/2$

- Mode 1, 3: if using Timer1 auto reload mode

  Baud Rate= (SMOD+1) xF_{SYSCLK}/ (32x2x (256–TH1))

- Mode 1, 3: if using Timer2

  Baud Rate=Timer2 overflow rate/16=F_{SYSCLK}/ (32 x (65536–RCP2H, RCP2L))

- Mode 2:

  Baud Rate= (SMOD+1) x $F_{SYSCLK}/64$

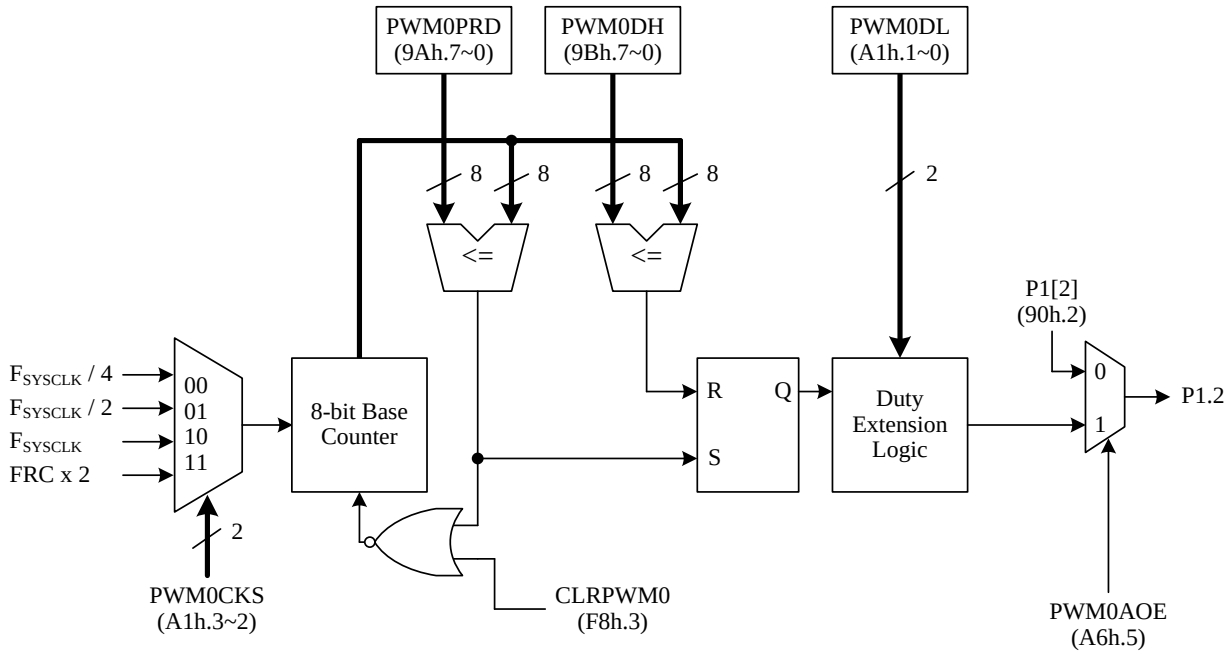
Note: also refer to Section 6 for more information about UART Interrupt enable and priority.
Note: also refer to Section 8 for more information about how Timer2 controls UART clock.

10. PWMs

The **F5250** has two independent PWM modules, PWM0 and PWM1. The PWM can generate a fixed frequency waveform with 1024 duty resolution on the basis of the PWM clock. The PWM clock can select FRC double frequency (FRCx2) or F_{SYSCLK} divided by 1, 2, or 4 as its clock source. A spread LSB technique allows PWM to run its frequency at the "PWM clock divided by 256" instead of at the "PWM clock divided by 1024", which means the PWM is four times faster than normal. The advantage of a higher PWM frequency is that the post RC filter can transform the PWM signal to a more stable DC voltage level.

The PWM output signal resets to a low level whenever the 8-bit base counter matches the 8-bit MSB of the PWM duty register. When the base counter rolls over, the 2-bit LSB of the PWM duty register decides whether to set the PWM output signal high immediately or set it high after one clock cycle delay. The PWM period can be set by writing the period value to the 8-bit PWM period register.

The pin mode SFR controls the PWM output waveform format. Mode1 makes the PWM open drain output and Mode2 makes the PWM CMOS push-pull output. (***see section 7***)



PWM Structure

SFR **9Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRD	PWM0PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Ah.7~0 **PWM0PRD:** PWM0 8-bit period register

SFR **9Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DH	PWM0DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

9Bh.7~0 **PWM0DH:** bits 9~2 of the PWM0 10-bit duty register

SFR **9Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRD	PWM1PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Ch.7~0 **PWM1PRD:** PWM1 8-bit period register

SFR **9Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DH	PWM1DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

9Dh.7~0 **PWM1DH:** bits 9~2 of the PWM1 10-bit duty register

SFR **A1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON	PWM1CKS		PWM1DL		PWM0CKS		PWM0DL	
R/W	R/W		R/W		R/W		R/W	
Reset	1	0	0	0	1	0	0	0

A1h.7~6 **PWM1CKS:** PWM1 clock source
00: $F_{SYSCLK}/4$
01: $F_{SYSCLK}/2$
10: F_{SYSCLK}
11: FRCx2

A1h.5~4 **PWM1DL:** bits 1~0 of the PWM1 10-bit duty register

A1h.3~2 **PWM0CKS:** PWM0 clock source
00: $F_{SYSCLK}/4$
01: $F_{SYSCLK}/2$
10: F_{SYSCLK}
11: FRCx2

A1h.1~0 **PWM0DL:** bits 1~0 of the PWM0 10-bit duty register

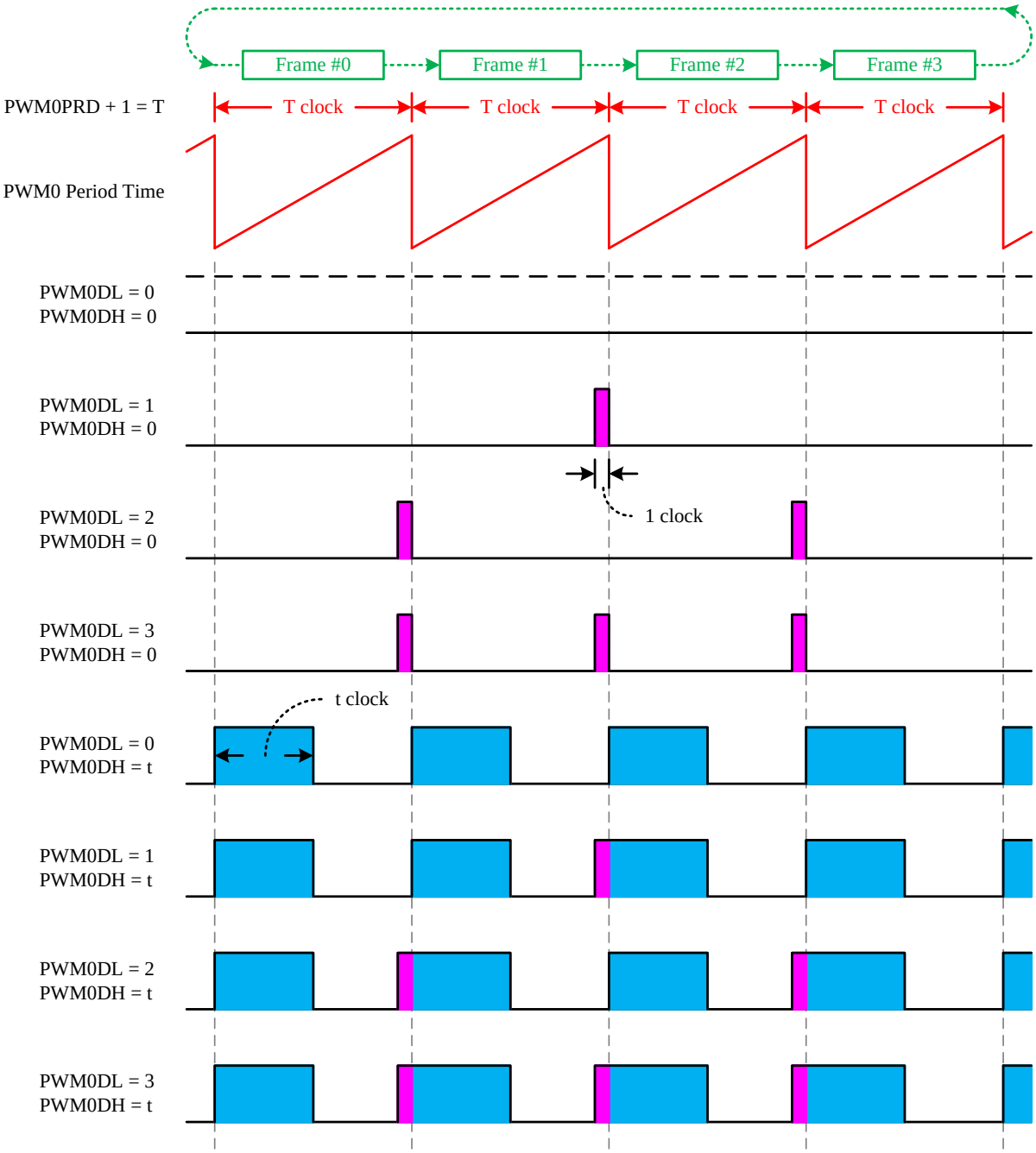
SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1AOE	–	PWM0AOE	–	TCOE	T2OE	–	–
R/W	R/W	–	R/W	–	R/W	R/W	–	–
Reset	0	–	0	–	0	0	–	–

A6h.7 **PWM1AOE:** PWM1 signal output enable
0: Disable PWM1 signal output to P1.3
1: Enable PWM1 signal output to P1.3

A6h.5 **PWM0AOE:** PWM0 signal output enable
0: Disable PWM0 signal output to P1.2
1: Enable PWM0 signal output to P1.2

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W
Reset	0	0	–	0	0	0	0	0

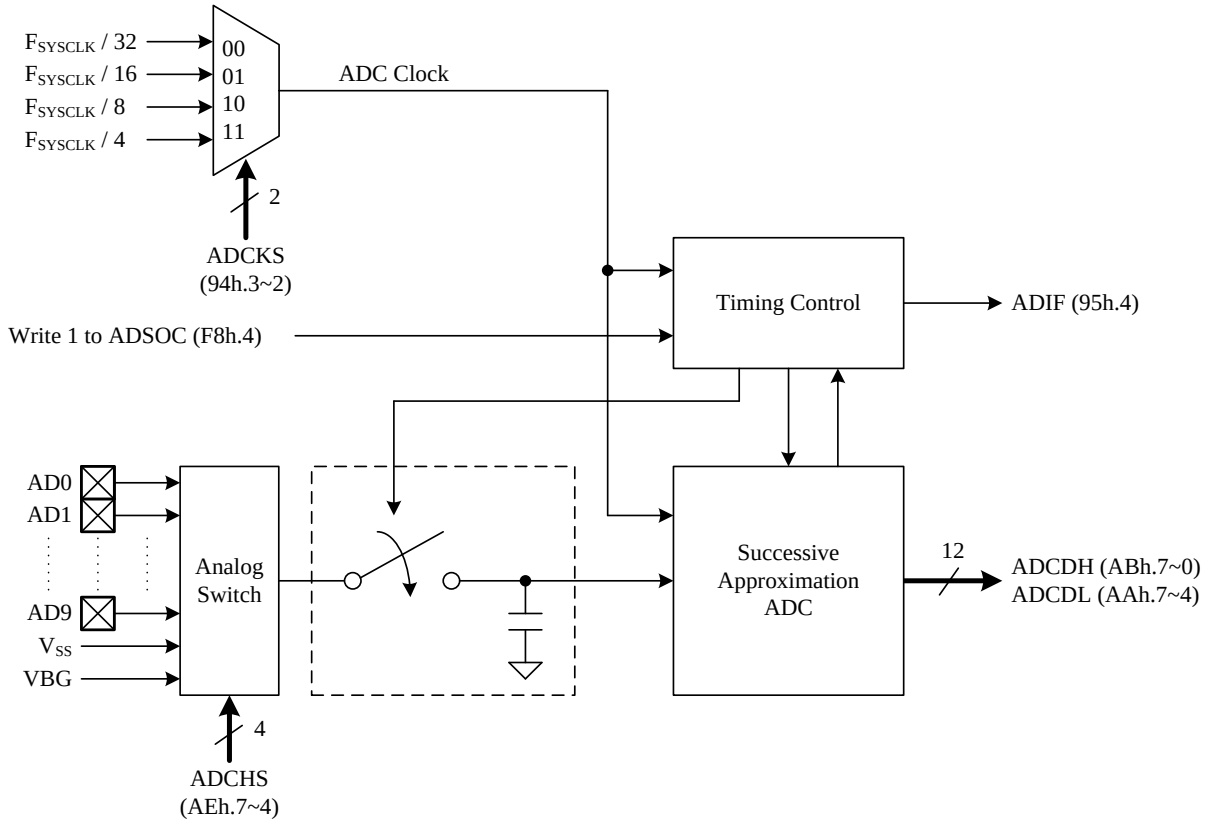
F8h.3 **CLRPWM0:** PWM0 clear enable
0: PWM0 is running
1: PWM0 is cleared and held



PWM Waveform

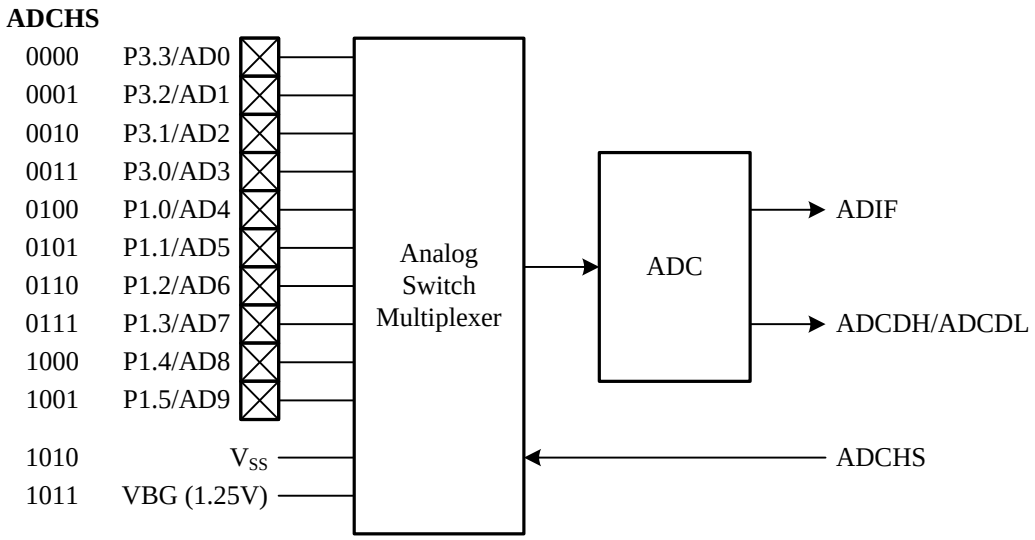
11. ADC

The **F5250** offers a 12-bit ADC consisting of a 12-channel analog input multiplexer, control register, clock generator, 12-bit successive approximation register, and output data register. To use the ADC, set the ADCKS bit first to choose a proper ADC clock frequency, which must be less than 1 MHz. Then, launch the ADC conversion by setting the ADSOC bit, and H/W will automatic clear it at the end of the conversion. After the end of the conversion, H/W will set the ADIF bit and generate an interrupt if an ADC interrupt is enabled. The ADIF bit can be cleared by writing 0 to this bit or 1 to the ADSOC bit. The analog input level must remain within the range from V_{SS} to V_{CC}.



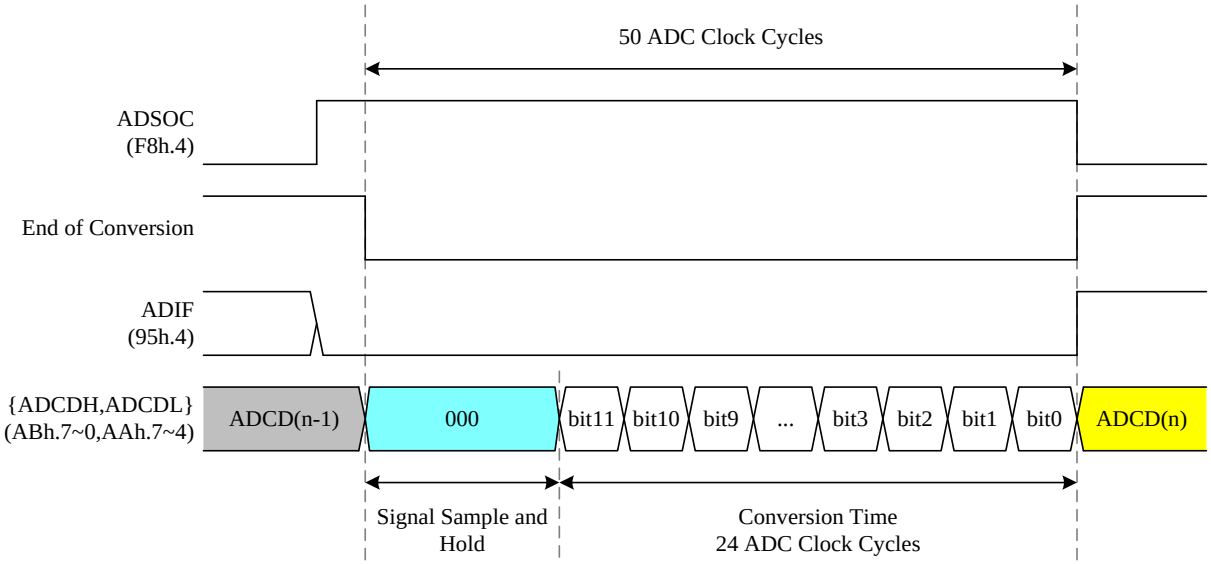
11.1 ADC Channels

The 12-bit ADC has a total of 12 channels, designated AD0~AD9, V_{SS}, and VBG. The ADC channels are connected to the analog input pins via the analog switch multiplexer. The analog switch multiplexer is controlled by the ADCHS register. **F5250** offers up to 10 analog input pins, designated AD0~AD9. In addition, there are two analog input pins for voltage reference connections. When ADCHS is set to 1010b, the analog input will connect to V_{SS}, and when ADCHS is set to 1011b, the analog input will connect to VBG. VBG is an internal voltage reference at 1.25V.



11.2 ADC Conversion Time

The conversion time is the time required for the ADC to convert the voltage. The ADC requires two ADC clock cycles to convert each bit and several clock cycles to sample and hold the input voltage. A total of 50 ADC clock cycles are required to perform the complete conversion. When the conversion time is complete, the ADIF interrupt flag is set by H/W, and the result is loaded into the ADCDH and ADCDL registers of the 12-bit A/D result.



11.3 VBG Voltage Conversion

The VBG voltage is measured by ADC and the convert result (ADC data bit 7~0, @VCC=5V) is stored to Flash FFCh in chip manufacturing. User can refer the data to obtain the actual Bandgap voltage.

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.3~2 **ADCKS:** ADC clock rate select
00: $F_{SYSCLK}/32$
01: $F_{SYSCLK}/16$
10: $F_{SYSCLK}/8$
11: $F_{SYSCLK}/4$

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	–	ADIF	–	IE2	P1IF	TF3
R/W	R	–	–	R/W	–	R/W	R/W	R/W
Reset	–	–	–	0	–	0	0	0

95h.4 **ADIF:** ADC interrupt flag
Set by H/W at the end of conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.

SFR **AAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTKDT	ADCDL				–	–	–	–
R/W	R				–	–	–	–
Reset	–	–	–	–	–	–	–	–

AAh.7~4 **ADCDL:** ADC data bit 3~0

SFR **ABh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDH	ADCDH							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ABh.7~0 **ADCDH:** ADC data bit 11~4

SFR **AEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHSEL	ADCHS				–	–	–	–
R/W	R/W				–	–	–	–
Reset	1	1	1	1	–	–	–	–

AEh.7~4 **ADCHS:** ADC channel select
0000: ADC0 (P3.3)
0001: ADC1 (P3.2)
0010: ADC2 (P3.1)
0011: ADC3 (P3.0)
0100: ADC4 (P1.0)
0101: ADC5 (P1.1)
0110: ADC6 (P1.2)
0111: ADC7 (P1.3)
1000: ADC8 (P1.4)
1001: ADC9 (P1.5)
1010: V_{SS}
1011: VBG (internal Bandgap reference voltage)
11xx: Undefined

Note: FW must turn off Bandgap to obtain Tiny Current (ADCHS≠0b1011)

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W
Reset	0	0	–	0	0	0	0	0

F8h.4 **ADSOC:** Start ADC conversion

Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

Flash **FFCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWR1	VBG							

FFCh.7~0 **VBG:** Bandgap voltage.

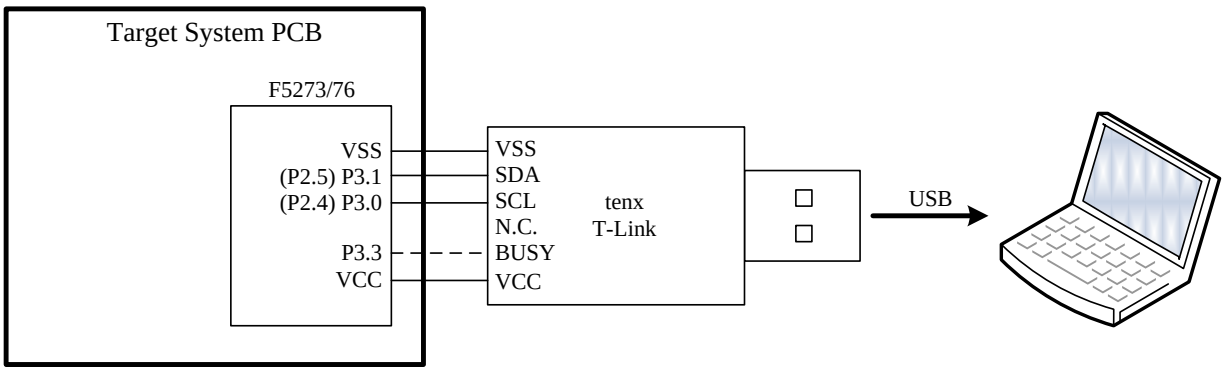
ADC convert data bit 7~0 for VBG, @VCC=5V and ADCHS=1011b

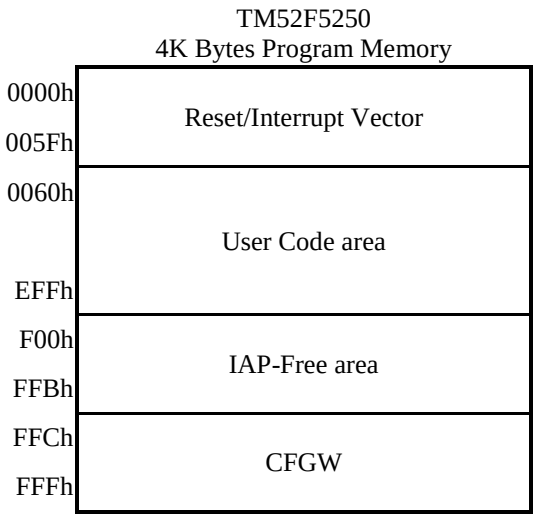
Note: also refer to Section 6 for more information about ADC Interrupt enable and priority.
Note: also refer to Section 7 for more information about ADC pin input setting.

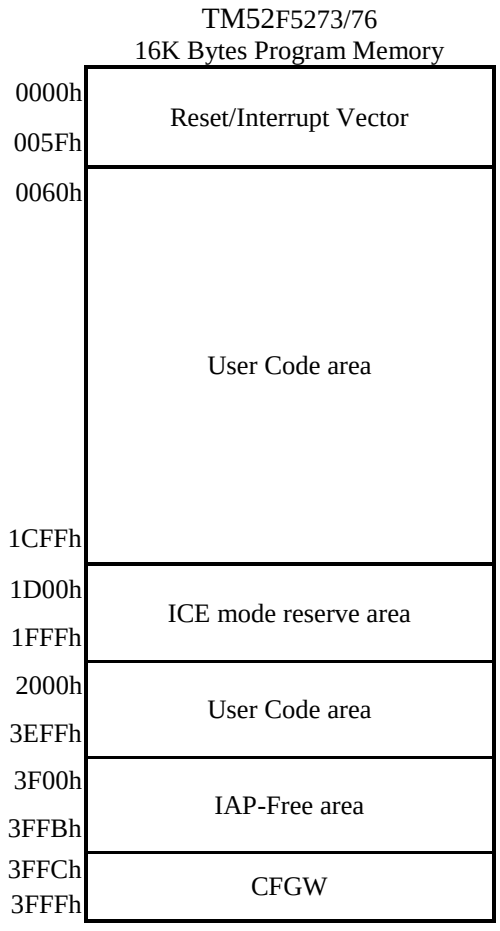
12. In Circuit Emulation (ICE) Mode

This device is not support ICE mode but it can use F5273/76 to simulate F5250. When using F5273/67 to simulate F5250, there are some different from F5250 should be notice such as program memory area, CFGW area and IAP area. Please see DS-TM52F5273_76 for more F5273/76 ICE mode detail.

Note: When using F5273/67 to simulate F5250, User should take care about different from the **program memory**, **CFGW area** and **IAP area** arrangement. For example Using F5273/67 to simulate F5250, Programming IAP area F00h~FFbh have to set SFR IAPALL, but F5250 real chip doesn't need to set SFR IAPALL.







SFR & CFGW MAP

Adr	Rst	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	1111-1111	**P0**	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	**SP**	SP							
82h	0000-0000	**DPL**	DPL							
83h	0000-0000	**DPH**	DPH							
87h	0xxx-0000	**PCON**	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	**TMOD**	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	**TL0**	TL0							
8Bh	0000-0000	**TL1**	TL1							
8Ch	0000-0000	**TH0**	TH0							
8Dh	0000-0000	**TH1**	TH1							
90h	1111-1111	**P1**	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
93h	0000-0101	**P2MOD**	–	–	–	–	P2MOD1		P2MOD0	
94h	0000-0000	**OPTION**	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
95h	xx00-x000	**INTFLG**	LVDO	–	–	ADIF	–	IE2	P1IF	TF3
96h	0000-0000	**P1WKUP**	P1WKUP							
97h	xxxx-xxx0	**SWCMD**	IAPALL / SWRST							
98h	0000-0000	**SCON**	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	**SBUF**	SBUF							
9Ah	1111-1111	**PWM0PRD**	PWM0PRD							
9Bh	1000-0000	**PWM0DH**	PWM0DH							
9Ch	1111-1111	**PWM1PRD**	PWM1PRD							
9Dh	1000-0000	**PWM1DH**	PWM1DH							
A0h	1111-1111	**P2**	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
A1h	1000-1000	**PWMCON**	PWM1CKS		PWM1DL		PWM0CKS		PWM0DL	
A2h	0000-0000	**P1MODL**	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
A3h	0000-0000	**P1MODH**	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
A4h	0101-0101	**P3MODL**	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
A5h	0x00-0000	**P3MODH**	T0OE	–	P3MOD6		P3MOD5		P3MOD4	
A6h	0000-0000	**PINMOD**	PWM1AOE	–	PWM0AOE	–	TCOE	T2OE	–	–
A8h	0x00-0000	**IE**	EA	–	ET2	ES	ET1	EX1	ET0	EX0
A9h	xxx0-0000	**INTE1**	–	–	–	–	ADIE	EX2	P1IE	TM3IE
AAh	xxxx-xxxx	**ADTKDT**	ADCDL				–	–	–	–
ABh	xxxx-xxxx	**ADCDH**	ADCDH							
AEh	1111-1111	**CHSEL**	ADCHS				–	–	–	–
B0h	1111-1111	**P3**	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
B8h	xx00-0000	**IP**	–	–	PT2	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	**IPH**	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
BAh	xxx0-0000	**IP1**	–	–	–	–	PADI	PX2	PP1	PT3
BBh	xxx0-0000	**IP1H**	–	–	–	–	PADIH	PX2H	PP1H	PT3H
C8h	0000-0000	**T2CON**	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
C9h	0xxx-xxxx	**IAPWE**	IAPWE							
CAh	0000-0000	**RCP2L**	RCP2L							
CBh	0000-0000	**RCP2H**	RCP2H							
CCh	0000-0000	**TL2**	TL2							
CDh	0000-0000	**TH2**	TH2							
D0h	0000-0000	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
D8h	00x0-0011	**CLKCON**	SCKTYPE	FCKTYPE	–	STPPCK	STPFCK	SELFCK	CLKPSC	
E0h	0000-0000	**ACC**	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Adr	Rst	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F0h	0000-0000	**B**	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F7h	xxxx-xxxx	**CFGWL**	WDTE		–	FRCF				
F8h	0000-0000	**AUX1**	CLRWDT	CLRTM3	–	ADSOC	CLRPWM0	T2SEL	T1SEL	DPSEL

Flash Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FFCh	**CFGWR1**	VBG@5.0v							
FFDh	**CFGWR2**	–							
FFEh	**CFGWL**	–	–	–	FRCF				
FFFh	**CFGWH**	PROT	XRSTE	LVRE		VCCFLT	PWRSAV	MVCLOCK	–

SFR & CFGW DESCRIPTION

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
80h	P0	7~0	P0	R/W	FFh	Port0 data, also controls the P0.n pin's pull-up function. If the P0.n SFR data is "1" and the corresponding P0OE.n=0 (input mode), the pull-up is enabled.
81h	SP	7~0	SP	R/W	07h	Stack Point
82h	DPL	7~0	DPL	R/W	00h	Data Point low byte
83h	DPH	7~0	DPH	R/W	00h	Data Point high byte
87h	PCON	7	SMOD	R/W	0	UART double baud rate control bit 0: Disable UART double baud rate 1: Enable UART double baud rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit
		1	PD	R/W	0	Stop bit. If 1 Stop mode is entered.
		0	IDL	R/W	0	Idle bit. If 1, Idle mode is entered.
88h	TCON	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control 0: Timer1 stops 1: Timer1 runs
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control 0: Timer0 stops 1: Timer0 runs
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine.
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin
89h	TMOD	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin or SLOWCLK/16 falling edge

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
89h	TMOD	5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	TL0	7~0	TL0	R/W	00h	Timer0 data low byte
8Bh	TL1	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	TH0	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	TH1	7~0	TH1	R/W	00h	Timer1 data high byte
90h	P1	7~0	P1	R/W	FFh	Port1 data
93h	P2MOD	3~2	P2MOD1	R/W	01h	P2.1 pin control
		1~0	P2MOD0	R/W	01h	P2.0 pin control
94h	OPTION	7	UART1W	R/W	0	One wire UART mode enable, both TXD/RXD use P3.1 pin 0: Disable one wire UART mode 1: Enable one wire UART mode
		6	MODE3V	R/W	0	3V mode selection control bit If this bit is set, the chip can be only operated in the condition of V_{CC} <3.6V, and LDO is turned off to save current
		5~4	WDTPSC	R/W	00	Watchdog Timer pre-scalar time select 00: 360ms WDT overflow rate 01: 180ms WDT overflow rate 10: 90ms WDT overflow rate 11: 45ms WDT overflow rate
		3~2	ADCKS	R/W	00	ADC clock rate select 00: F_{SYSCLK}/32 01: F_{SYSCLK}/16 10: F_{SYSCLK}/8 11: F_{SYSCLK}/4
		1~0	TM3PSC	R/W	00	Timer3 interrupt rate control select 00: Interrupt rate is 32768 Slow clock cycle 01: Interrupt rate is 16384 Slow clock cycle 10: Interrupt rate is 8192 Slow clock cycle 11: Interrupt rate is 128 Slow clock cycle

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
95h	INTFLG	7	LVDO	R		Low Voltage Detect flag Set by H/W when a low voltage occurs. The flag is valid when LVR is 2.0V. This flag is disabled if MODE3V=1 and PWRSAV=1.
		4	ADIF	R/W	0	ADC interrupt flag Set by H/W at the end of conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.
		2	IE2	R/W	0	External Interrupt 2 (INT2 pin) edge flag Set by H/W when a falling edge is detected on the INT2 pin state, no matter the EX2 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine. S/W can write FBh to INTFLG to clear this bit.
		1	P1IF	R/W	0	Port1 pin change interrupt flag Set by H/W when a P1 pin state change is detected, and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting. It is cleared automatically when the program performs the interrupt service routine. S/W can write FDh to INTFLG to clear this bit.
		0	TF3	R/W	0	Timer 3 interrupt flag Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.
96h	P1WKUP	7~0	P1WKUP	R/W	00h	P1.7~P1.0 pin individual Wake up/Interrupt enable control 0: Disable 1: Enable
97h	SWCMD	7~0	SWRST	W		Write 56h to generate S/W Reset
		7~0	IAPALL	W		Write 65h to set IAPALL control flag; Write other value to clear IAPALL flag. It is recommended to clear it immediately after IAP access.
		0	IAPALL	R	0	Flag indicates Flash memory sectors can be accessed by IAP or not. This bit combines with MVCLOCK to define the accessible IAP area.

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
98h	SCON	7	SM0	R/W	0	Serial port mode select bit 0,1 00: Mode0: 8 bit shift register, Baud Rate=F_{SYSCLK}/2 01: Mode1: 8 bit UART, Baud Rate is variable 10: Mode2: 9 bit UART, Baud Rate=F_{SYSCLK}/32 or /64 11: Mode3: 9 bit UART, Baud Rate is variable
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	UART reception enable 0: Disable reception 1: Enable reception
		3	TB8	R/W	0	Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0
		1	TI	R/W	0	Transmit interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.
		0	RI	R/W	0	Receive interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.
99h	SBUF	7~0	SBUF	R/W		UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
9Ah	PWM0PRD	7~0	PWM0PRD	R/W	FFh	PWM0 8-bit period register
9Bh	PWM0DH	7~0	PWM0DH	R/W	80h	bits 9~2 of the PWM0 10-bit duty register
9Ch	PWM1PRD	7~0	PWM1PRD	R/W	FFh	PWM1 8-bit period register
9Dh	PWM1DH	7~0	PWM1DH	R/W	80h	bits 9~2 of the PWM1 10-bit duty register
A0h	P2	7~0	P2	R/W	FFh	Port2 data
A1h	PWMCON	7~6	PWM1CKS	R/W	10	PWM1 clock source 00: F_{SYSCLK}/4 01: F_{SYSCLK}/2 10: F_{SYSCLK} 11: FRCx2
		5~4	PWM1DL	R/W	00	bits 1~0 of the PWM1 10-bit duty register
		3~2	PWM0CKS	R/W	10	PWM0 clock source 00: F_{SYSCLK}/4 01: F_{SYSCLK}/2 10: F_{SYSCLK} 11: FRCx2
		1~0	PWM0DL	R/W	00	bits 1~0 of the PWM0 10-bit duty register
A2h	P1MODL	7~6	P1MOD3	R/W	00	P1.3 pin control
		5~4	P1MOD2	R/W	00	P1.2 pin control
		3~2	P1MOD1	R/W	00	P1.1 pin control
		1~0	P1MOD0	R/W	00	P1.0 pin control

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
A3h	P1MODH	7~6	P1MOD7	R/W	00	P1.7 pin control
		5~4	P1MOD6	R/W	00	P1.6 pin control
		3~2	P1MOD5	R/W	00	P1.5 pin control
		1~0	P1MOD4	R/W	00	P1.4 pin control
A4h	P3MODL	7~6	P3MOD3	R/W	01h	P3.3 pin control
		5~4	P3MOD2	R/W	01h	P3.2 pin control
		3~2	P3MOD1	R/W	01h	P3.1 pin control
		1~0	P3MOD0	R/W	01h	P3.0 pin control
A5h	P3MODH	7	T0OE	R/W	0	Timer0 signal output (T0O) control 0: Disable Timer0 overflow divided by 64 output to P3.4 1: Enable Timer0 overflow divided by 64 output to P3.4
		5~4	P3MOD6	R/W	00	P3.6 pin control
		3~2	P3MOD5	R/W	00	P3.5 pin control
		1~0	P3MOD4	R/W	00	P3.4 pin control
A6h	PINMOD	7	PWM1AOE	R/W	0	PWM1 signal output enable 0: Disable PWM1 signal output to P1.3 1: Enable PWM1 signal output to P1.3
		5	PWM0AOE	R/W	0	PWM0 signal output enable 0: Disable PWM0 signal output to P1.2 1: Enable PWM0 signal output to P1.2
		3	TCOE	R/W	0	TCOE: System clock signal output (CKO) control 0: Disable System clock divided by 2 output to P1.4 1: Enable System clock divided by 2 output to P1.4
		2	T2OE	R/W	0	Timer2 signal output (T2O) enable 0: Disable Timer2 overflow divided by 2 output to P1.0 1: Enable Timer2 overflow divided by 2 output to P1.0
A8h	IE	7	EA	R/W	0	Global interrupt enable 0: Disable all interrupts 1: Each interrupt is enabled or disabled by its individual interrupt control bit
		5	ET2	R/W	0	Timer2 interrupt enable 0: Disable Timer2 interrupt 1: Enable Timer2 interrupt
		4	ES	R/W	0	Serial Port (UART) interrupt enable 0: Disable Serial Port (UART) interrupt 1: Enable Serial Port (UART) interrupt
		3	ET1	R/W	0	Timer1 interrupt enable 0: Disable Timer1 interrupt 1: Enable Timer1 interrupt
		2	EX1	R/W	0	INT1 pin Interrupt enable and Stop mode wake up enable 0: Disable INT1 pin Interrupt and Stop mode wake up 1: Enable INT1 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.
		1	ET0	R/W	0	Timer0 interrupt enable 0: Disable Timer0 interrupt 1: Enable Timer0 interrupt
		0	EX0	R/W	0	INT0 pin Interrupt enable and Stop mode wake up enable 0: Disable INT0 pin Interrupt and Stop mode wake up 1: Enable INT0 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
A9h	INTE1	3	ADIE	R/W	0	ADC interrupt enable 0: Disable ADC interrupt 1: Enable ADC interrupt
		2	EX2	R/W	0	INT2 pin Interrupt enable and Stop mode wake up enable 0: Disable INT2 pin Interrupt and Stop mode wake up 1: Enable INT2 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.
		1	P1IE	R/W	0	Port1 pin change interrupt enable 0: Disable Port1 pin change interrupt 1: Enable Port1 pin change interrupt
		0	TM3IE	R/W	0	Timer3 interrupt enable 0: Disable Timer3 interrupt 1: Enable Timer3 interrupt
AAh	ADTKDT	7~4	ADCDL	R		ADC data bit 3~0
ABh	ADCDH	7~0	ADCDH	R		ADC data bit 11~4
AEh	CHSEL	7~4	ADCHS	R/W	1111	ADC channel select 0000: ADC0 (P3.3) 0001: ADC1 (P3.2) 0010: ADC2 (P3.1) 0011: ADC3 (P3.0) 0100: ADC4 (P1.0) 0101: ADC5 (P1.1) 0110: ADC6 (P1.2) 0111: ADC7 (P1.3) 1000: ADC8 (P1.4) 1001: ADC9 (P1.5) 1010: V_{SS} 1011: VBG (internal Bandgap reference voltage) 11xx: Undefined
B0h	P3	7~0	P3	R/W	FFh	Port3 data
B8h	IP	5	PT2	R/W	0	Timer2 interrupt priority low bit
		4	PS	R/W	0	Serial Port interrupt priority low bit
		3	PT1	R/W	0	Timer1 interrupt priority low bit
		2	PX1	R/W	0	INT1 interrupt priority low bit
		1	PT0	R/W	0	Timer0 interrupt priority low bit
		0	PX0	R/W	0	INT0 interrupt priority low bit
B9h	IPH	5	PT2H	R/W	0	Timer2 interrupt priority high bit
		4	PSH	R/W	0	Serial Port interrupt priority high bit
		3	PT1H	R/W	0	Timer1 interrupt priority high bit
		2	PX1H	R/W	0	INT1 interrupt priority high bit
		1	PT0H	R/W	0	Timer0 interrupt priority high bit
		0	PX0H	R/W	0	INT0 interrupt priority high bit
BAh	IP1	3	PADI	R/W	0	ADC interrupt priority low bit
		2	PX2	R/W	0	INT2 interrupt priority low bit
		1	PP1	R/W	0	Port1 pin change interrupt priority low bit
		0	PT3	R/W	0	Timer3 interrupt priority low bit
BBh	IP1H	3	PADIH	R/W	0	ADC interrupt priority high bit
		2	PX2H	R/W	0	INT2 interrupt priority high bit
		1	PP1H	R/W	0	Port1 interrupt priority high bit
		0	PT3H	R/W	0	Timer3 interrupt priority high bit

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
C8h	T2CON	7	TF2	R/W	0	Timer2 overflow flag Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
		6	EXF2	R/W	0	T2EX interrupt pin falling edge flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
		5	RCLK	R/W	0	UART receive clock control bit 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3
		4	TCLK	R/W	0	UART transmit clock control bit 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
		3	EXEN2	R/W	0	T2EX pin enable 0: T2EX pin disable 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0
		2	TR2	R/W	0	Timer2 run control 0: Timer2 stops 1: Timer2 runs
		1	CT2N	R/W	0	Timer2 Counter/Timer select bit 0: Timer mode, Timer2 data increases at 2 System clock cycle rate 1: Counter mode, Timer2 data increases at T2 pin or SLOWCLK/16 falling edge
		0	CPRL2N	R/W	0	Timer2 Capture/Reload control bit 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1 If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow
C9h	IAPWE	7~0	IAPWE	W		Write 47h to set IAPWE control flag; Write other value to clear IAPWE flag. It is recommended to clear it immediately after IAP write.
		7	IAPWE	R	0	Flag indicates Flash memory can be written by IAP or not, 1=IAP Write enable.
CAh	RCP2L	7~0	RCP2L	R/W	00h	Timer2 reload/capture data low byte
CBh	RCP2H	7~0	RCP2H	R/W	00h	Timer2 reload/capture data high byte
CCh	TL2	7~0	TL2	R/W	00h	Timer2 data low byte
CDh	TH2	7~0	TH2	R/W	00h	Timer2 data high byte

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
D0h	PSW	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	The contents of (RS1, RS0) enable the working register banks as: 00: Bank 0 (00h~07h) 01: Bank 1 (08h~0Fh) 10: Bank 2 (10h~17h) 11: Bank 3 (18h~1Fh)
		3	RS0	R/W	0	
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.
D8h	CLKCON	7	SCKTYPE	R/W	0	Slow clock type. This bit can be changed only in Fast mode (SELFCK=1). 0: SRC 1: SXT
		6	FCKTYPE	R/W	0	Fast clock type. This bit can be changed only in Slow mode (SELFCK=0). 0: FRC 1: FXT
		4	STPPCK	R/W	0	Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode
		3	STPFCK	R/W	0	Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
		2	SELFCK	R/W	0	System clock source selection. This bit can be changed only when STPFCK=0. 0: Slow clock 1: Fast clock
		1~0	CLKPSC	R/W	11	System clock prescaler. 00: System clock is Fast/Slow clock divided by 16 01: System clock is Fast/Slow clock divided by 4 10: System clock is Fast/Slow clock divided by 2 11: System clock is Fast/Slow clock divided by 1
E0h	ACC	7~0	ACC	R/W	00h	Accumulator
F0h	B	7~0	B	R/W	00h	B register
F7h	CFGWL	7~6	WDTE	R/W		Watchdog Timer Reset control 0x: Watchdog Timer Reset disable 10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Stop mode 11: Watchdog Timer Reset always enable
		4~0	FRCF	R/W		FRC frequency adjustment 00h=central frequency, 0Fh=highest frequency, 10h=lowest frequency.

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
F8h	AUX1	7	CLRWDT	R/W	0	Set to clear WDT, H/W auto clear it at next clock cycle
		6	CLRTM3	R/W	0	Set to clear Timer3, H/W auto clear it at next clock cycle
		4	ADSOC	R/W	0	Start ADC conversion Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		3	CLRPWM0	R/W	0	PWM0 clear enable 0: PWM0 is running 1: PWM0 is cleared and held
		2	T2SEL	R/W	0	Timer2 counter mode (CT2N=1) input select 0: P1.0 (T2) pin (8051standard) 1:Slow clock divide by 16 (SLOWCLK/16)
		1	T1SEL	R/W	0	Timer1 counter mode (CT1N=1) input select 0: P3.5 (T1) pin (8051 standard) 1: Slow clock divide by 16 (SLOWCLK/16)
		0	DPSEL	R/W	0	Active DPTR Select

Flash Adr	Bit #	Name	Description
FFCh	7~0	CFGWR1	ADC convert data bit 7~0 for VBG, @VCC=5.0V and ADCHS=1011b If Bit 7~0 in 00H~3FH, ADC convert data is 400H~43FH If Bit 7~0 in C0H~FFH, ADC convert data is 3C0H~3FFH
FFDh	7~0	CFGWR2	Reserved
FFEh	4~0	FRCF	FRC frequency adjustment. FRC is trimmed to 9.83 MHz in chip manufacturing. FRCF records the adjustment data.
FFFh	7	PROT	Flash Memory Code Protect 0: Disable protect 1: Enable protect
	6	XRSTE	External Pin Reset control 0: Disable External Pin Reset 1: Enable External Pin Reset
	5~4	LVRE	Low Voltage Reset function select 00: Set LVR at 2.9V 01: Set LVR at 2.3V 10: Set LVR at 3.5V 11: Set LVR at 2.0V and LVD at 2.3V
	3	VCCFLT	Set 1 to enhance the chip's power noise immunity
	2	PWRSAV	Power save function control bit 0: Disable Power save function 1: Enable Power save function
	1	MVCLOCK	If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.

INSTRUCTION SET

Instructions are 1, 2 or 3 Bytes long as listed in the 'byte' column below. Each instruction takes 2~8 System clock cycles to execute as listed in the 'cycle' column below.

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ADD A,Rn	Add register to A	1	2	28-2F
ADD A,dir	Add direct byte to A	2	2	25
ADD A,@Ri	Add indirect memory to A	1	2	26-27
ADD A,#data	Add immediate to A	2	2	24
ADDC A,Rn	Add register to A with carry	1	2	38-3F
ADDC A,dir	Add direct byte to A with carry	2	2	35
ADDC A,@Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A,#data	Add immediate to A with carry	2	2	34
SUBB A,Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	2	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8	A4
DIV AB	Divide A by B	1	8	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ANL A,Rn	AND register to A	1	2	58-5F
ANL A,dir	AND direct byte to A	2	2	55
ANL A,@Ri	AND indirect memory to A	1	2	56-57
ANL A,#data	AND immediate to A	2	2	54
ANL dir,A	AND A to direct byte	2	2	52
ANL dir,#data	AND immediate to direct byte	3	4	53
ORL A,Rn	OR register to A	1	2	48-4F
ORL A,dir	OR direct byte to A	2	2	45
ORL A,@Ri	OR indirect memory to A	1	2	46-47
ORL A,#data	OR immediate to A	2	2	44
ORL dir,A	OR A to direct byte	2	2	42
ORL dir,#data	OR immediate to direct byte	3	4	43
XRL A,Rn	Exclusive-OR register to A	1	2	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A,#data	Exclusive-OR immediate to A	2	2	64
XRL dir,A	Exclusive-OR A to direct byte	2	2	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4
SWAP A	Swap Nibbles of A	1	2	C4
RL A	Rotate A left	1	2	23

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
RLC A	Rotate A left through carry	1	2	33
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MOV A,Rn	Move register to A	1	2	E8-EF
MOV A,dir	Move direct byte to A	2	2	E5
MOV A,@Ri	Move indirect memory to A	1	2	E6-E7
MOV A,#data	Move immediate to A	2	2	74
MOV Rn,A	Move A to register	1	2	F8-FF
MOV Rn,dir	Move direct byte to register	2	4	A8-AF
MOV Rn,#data	Move immediate to register	2	2	78-7F
MOV dir,A	Move A to direct byte	2	2	F5
MOV dir,Rn	Move register to direct byte	2	4	88-8F
MOV dir,dir	Move direct byte to direct byte	3	4	85
MOV dir,@Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir,#data	Move immediate to direct byte	3	4	75
MOV @Ri,A	Move A to indirect memory	1	2	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	2	76-77
MOV DPTR,#data	Move immediate to data pointer	3	4	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4	93
MOVC A,@A+PC	Move code byte relative PC to A	1	4	83
MOVX A,@Ri	Move external data(A8) to A	1	4	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	4	E0
MOVX @Ri,A	Move A to external data(A8)	1	4	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	4	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A,Rn	Exchange A and register	1	2	C8-CF
XCH A,dir	Exchange A and direct byte	2	2	C5
XCH A,@Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C,bit	AND direct bit to carry	2	4	82
ANL C,/bit	AND direct bit inverse to carry	2	4	B0
ORL C,bit	OR direct bit to carry	2	4	72
ORL C,/bit	OR direct bit inverse to carry	2	4	A0
MOV C,bit	Move direct bit to carry	2	2	A2
MOV bit,C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ACALL addr 11	Absolute jump to subroutine	2	4	11-F1
LCALL addr 16	Long jump to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	4	01-E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	4	80
JC rel	Jump on carry=1	2	4	40
JNC rel	Jump on carry=0	2	4	50
JB bit,rel	Jump on direct bit=1	3	4	20
JNB bit,rel	Jump on direct bit=0	3	4	30
JBC bit,rel	Jump on direct bit=1 and clear	3	4	10
JMP @A+DPTR	Jump indirect relative DPTR	1	4	73
JZ rel	Jump on accumulator=0	2	4	60
JNZ rel	Jump on accumulator … 0	2	4	70
CJNE A,dir,rel	Compare A,direct, jump not equal relative	3	4	B5
CJNE A,#data,rel	Compare A,immediate, jump not equal relative	3	4	B4
CJNE Rn,#data,rel	Compare register,immediate, jump not equal relative	3	4	B8-BF
CJNE @Ri,#data,rel	Compare indirect,immediate, jump not equal relative	3	4	B6-B7
DJNZ Rn,rel	Decrement register, jump not zero relative	2	4	D8-DF
DJNZ dir,rel	Decrement direct byte, jump not zero relative	3	4	D5

MISCELLANEOUS				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A=25°C)

Parameter	Rating	Unit
Supply voltage	V_{SS} –0.3 ~ V_{SS} +5.5	V
Input voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output current high per 1 PIN	–25	mA
Output current high per all PIN	–80	
Output current low per 1 PIN	+30	
Output current low per all PIN	+150	
Maximum Operating Voltage	5.5	V
Operating temperature	–40 ~ +85	°C
Storage temperature	–65 ~ +150	

2. DC Characteristics (T_A=25°C, V_{CC}=2.0V ~ 5.5V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Operating Voltage	V_{CC}	Fast mode, F_{SYSCLK}=14.74 MHz		3.5	–	5.5	V
		Fast mode, F_{SYSCLK}=9.8 MHz		2.9	–	5.5	
		Fast mode, F_{SYSCLK}=5 MHz		2.3	–	5.5	
		Fast mode, F_{SYSCLK}=2.5 MHz		2.0	–	5.5	
		Slow mode, SRC		2.0	–	5.5	
Input High Voltage	V_{IH}	All Input, except P3.7, P2.1	V_{CC}=5V	0.6V_{CC}	–	–	V
			V_{CC}=3V	0.6V_{CC}	–	–	
		P3.7, P2.1	V_{CC}=5V	0.8V_{CC}	–	–	
			V_{CC}=3V	0.8V_{CC}	–	–	
Input Low Voltage	V_{IL}	All Input	V_{CC}=5V	–	–	0.2V_{CC}	V
			V_{CC}=3V	–	–	0.2V_{CC}	
I/O Port Source Current	I_{OH}	All Output, except P3.7	V_{CC}=5V V_{OH}=0.9V_{CC}	5	10	–	mA
			V_{CC}=3V V_{OH}=0.9V_{CC}	2.5	5	–	
I/O Port Sink Current	I_{OL}	All Output	V_{CC}=5V V_{OL}=0.1V_{CC}	9	18	–	mA
			V_{CC}=3V V_{OL}=0.1V_{CC}	5	10	–	
Input Leakage Current (pin high)	I_{ILH}	All Input	V_{in}=V_{CC}	–	–	1	µA
Input Leakage Current (pin low)	I_{IILL}	All Input	V_{in}=0V	–	–	–1	

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply Current	I_{CC}	Fast, V_{CC}=5V MODE3V=0	FXT=8 MHz	–	4	–	mA
			FRC=9.83 MHz	–	4	–	
			FRC=4.92 MHz	–	3	–	
		Slow, V_{CC}=5V MODE3V=0	SXT=32 KHz	–	2	–	
			SRC=24 KHz	–	2	–	
		Slow, V_{CC}=3V MODE3V=1 PWRSAV=1	SXT=32 KHz	–	1.3	–	
			SRC=24 KHz	–	1.3	–	
		Idle, V_{CC}=3V MODE3V=1 PWRSAV=1	SXT=32 KHz	–	5	–	µA
			SRC=24 KHz	–	4	–	
		Stop, V_{CC}=3V MODE3V=1	PWRSAV=0	–	40	–	
			PWRSAV=1	–	3	–	
System Clock Frequency	F_{SYSCLK}	V_{CC} >LVR_{th} T_A=25°C	V_{CC}=3.5V	–	–	14.74	MHz
			V_{CC}=2.9V	–	–	9.8	
			V_{CC}=2.3V			5	
			V_{CC}=2.0V	–	–	2.5	
LVR Reference Voltage	V_{LVR}	T_A=25°C		–	3.5	–	V
				–	2.9	–	
				–	2.3	–	
				–	2.0	–	
LVR Hysteresis Voltage	V_{HYST}	T_A=25°C		–	±0.1	–	V
LVD Reference Voltage	V_{LVD}	T_A=25°C		–	2.3	–	V
Low Voltage Detection time	t_{LVR}	T_A=25°C		100	–	–	µs
Pull-Up Resistor	R_P	V_{IN}=0V All except P3.7	V_{CC}=5V	–	120	–	KΩ
			V_{CC}=3V		240		
		V_{IN}=0V P3.7	V_{CC}=5V	–	160	–	
			V_{CC}=3V		160		

3. Clock Timing (T_A= –40°C ~ +85°C, V_{CC}=3.0 ~ 5.5V)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Internal RC Frequency	25°C, V_{CC}=5.0V	–1.2%	9.83	+1.2%	MHz
	0°C ~ 70°C, V_{CC}=3.0 ~ 5.5V	–2.5%	9.83	+2.5%	
	–40°C ~ 85°C, V_{CC}=3.0 ~ 5.5V	–7.0%	9.83	+2.5%	

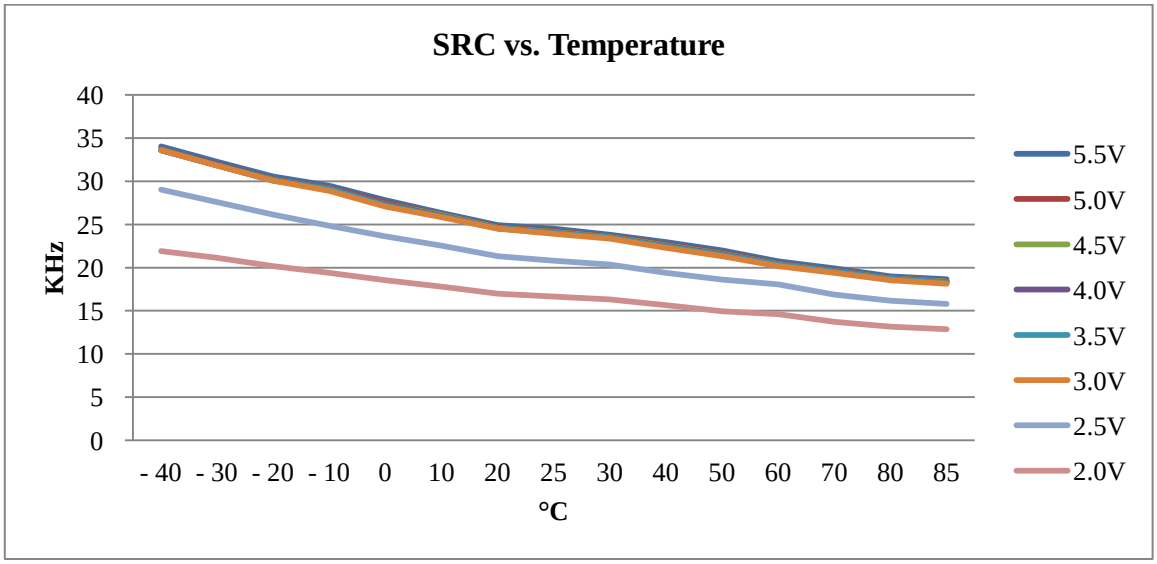
4. Reset Timing Characteristics (T_A= –40°C ~ +85°C, V_{CC}=3.0V ~ 5.0V)

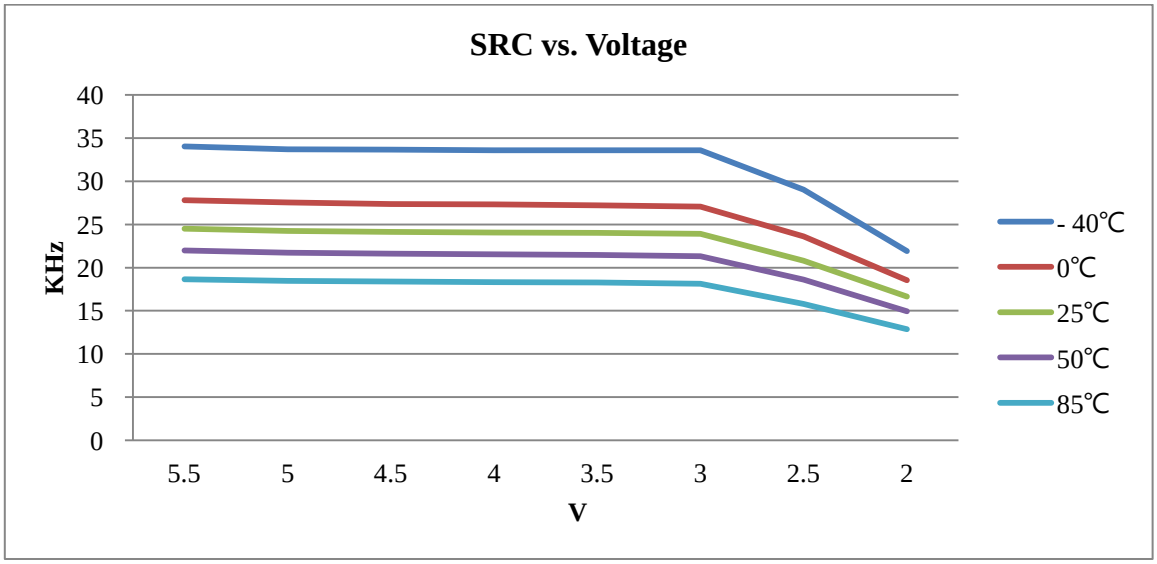
Parameter	Conditions	Min.	Typ.	Max.	Unit
RESET Input Low width	Input V_{CC}=5.0V ±10%	90	–	–	µs
WDT wakeup time	V_{CC}=5.0V, WDTPSC=11	–	40	–	ms
	V_{CC}=3.0V, WDTPSC=11	–	40	–	

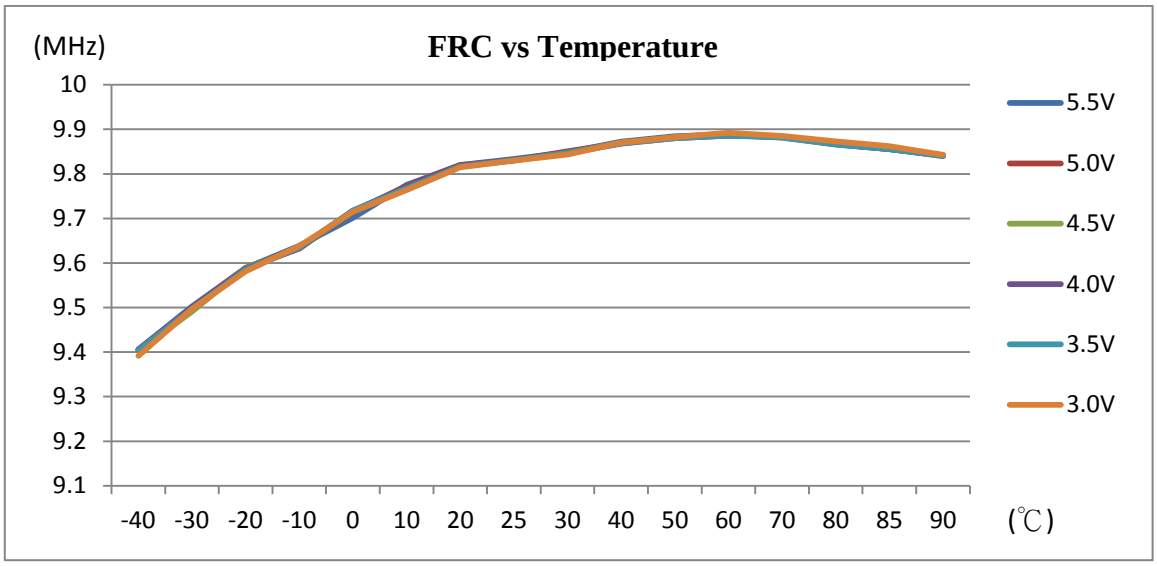
5. ADC Electrical Characteristics (T_A=25°C, V_{CC}=3.0V ~ 5.5V, V_{SS}=0V)

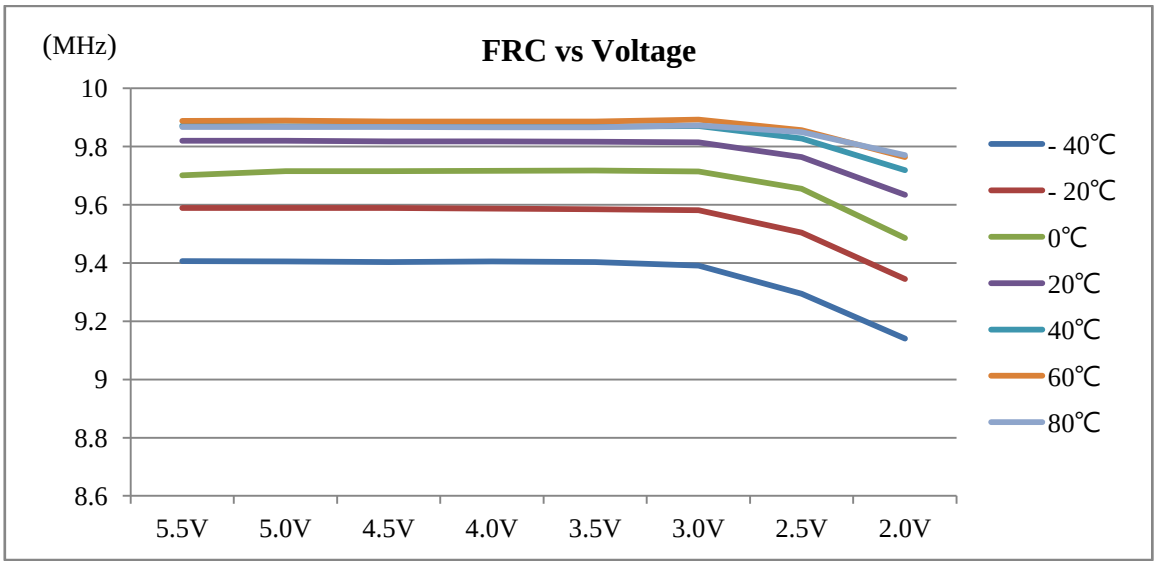
Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Accuracy	V_{CC}=5.12V, V_{SS}=0V	–	±2.5	±4	LSB
Integral Non-Linearity		–	±3.2	±5	
Max Input Clock (f_{ADC})	–	–	–	1	MHz
Conversion Time	f_{ADC}=1 MHz	–	50	–	μs
BandGap Voltage	V_{CC}=5V	-8%	1.25	+8%	V
Input Voltage	–	V_{SS}	–	V_{CC}	V

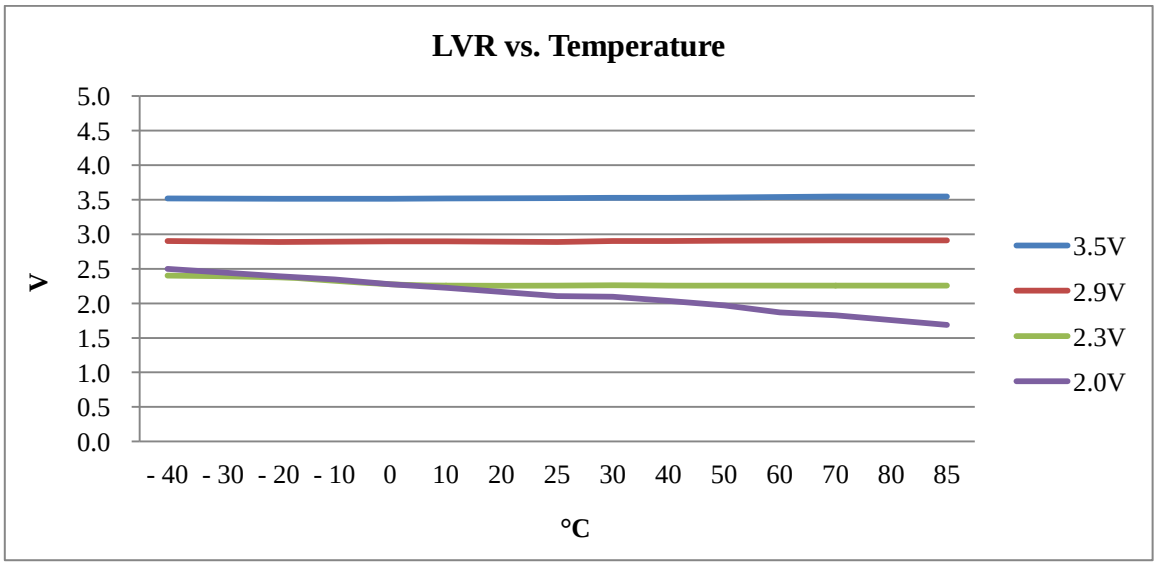
6. Characteristics Graphs

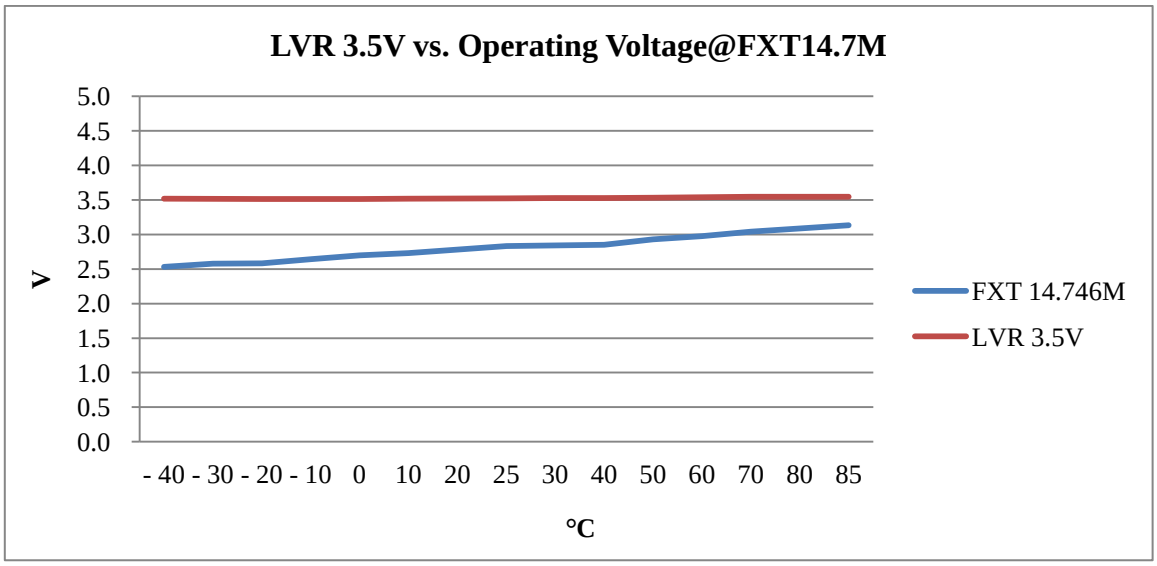


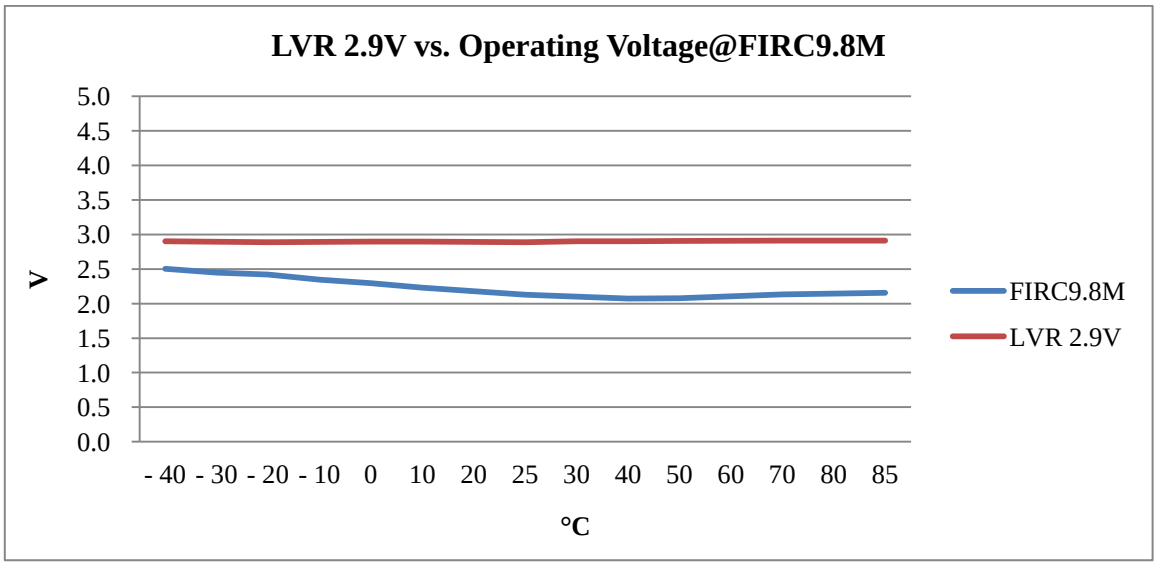



FRC vs Temperature
(MHz)
10
9.9
9.8
9.7
9.6
9.5
9.4
9.3
9.2
9.1
-40 -30 -20 -10 0 10 20 25 30 40 50 60 70 80 85 90
(℃)
5.5V
5.0V
4.5V
4.0V
3.5V
3.0V


FRC vs Voltage
(MHz)
10
9.8
9.6
9.4
9.2
9
8.8
8.6
5.5V 5.0V 4.5V 4.0V 3.5V 3.0V 2.5V 2.0V
- 40℃
- 20℃
0℃
20℃
40℃
60℃
80℃


LVR vs. Temperature
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
V
- 40 - 30 - 20 - 10 0 10 20 25 30 40 50 60 70 80 85
°C
3.5V
2.9V
2.3V
2.0V


LVR 3.5V vs. Operating Voltage@FXT14.7M
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
V
- 40 - 30 - 20 - 10 0 10 20 25 30 40 50 60 70 80 85
°C
FXT 14.746M
LVR 3.5V


LVR 2.9V vs. Operating Voltage@FIRC9.8M
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
V
- 40 - 30 - 20 - 10 0 10 20 25 30 40 50 60 70 80 85
°C
FIRC9.8M
LVR 2.9V

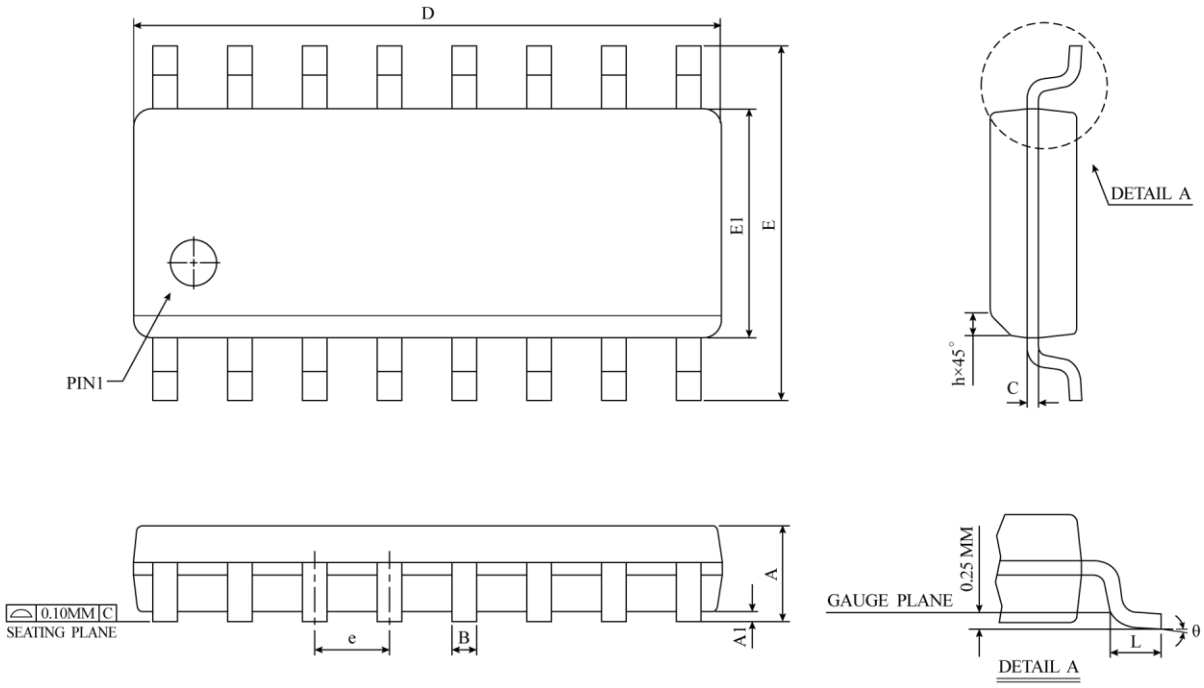
PACKAGE INFORMATION

Ordering Information

Ordering Number	Package
TM52F5250-OTP	Wafer/Dice blank chip
TM52F5250COD	Wafer/Dice blank chip
TM52F5250-MTP-16	SOP 16-pin (150mil)
TM52F5250-MTP-03	DIP 16-pin (300mil)
TM52F5250-MTP-21	SOP 20-pin (300mil)
TM52F5250-MTP-05	DIP 20-pin (300mil)
TM52F5250-MTP-97	QFN 20-pin (4*4*0.75 - 0.5mm)

Package Information

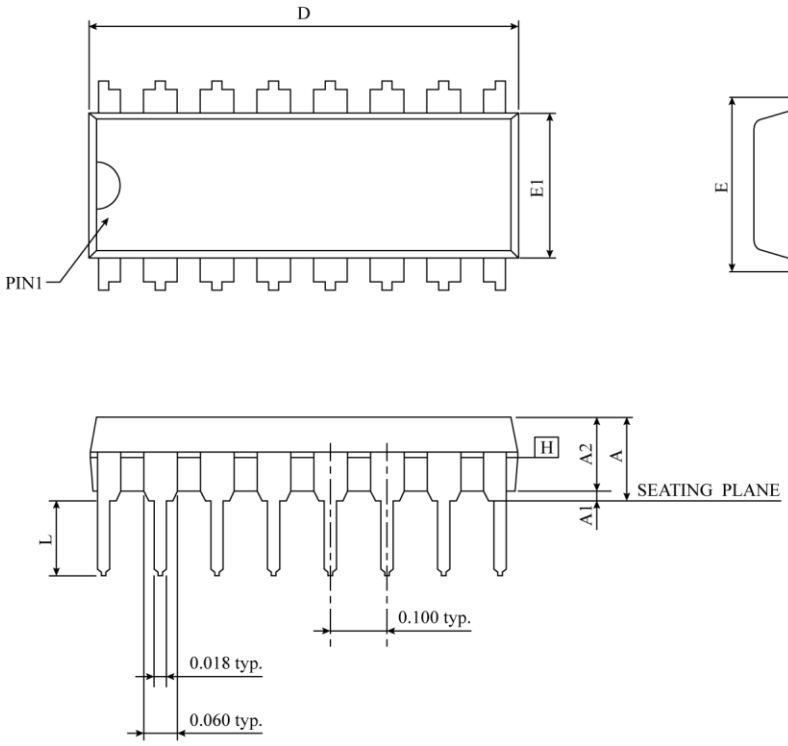
SOP-16 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	9.80	9.90	10.00	0.3859	0.3898	0.3937
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AC)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

DIP-16 (300mil) Package Dimension

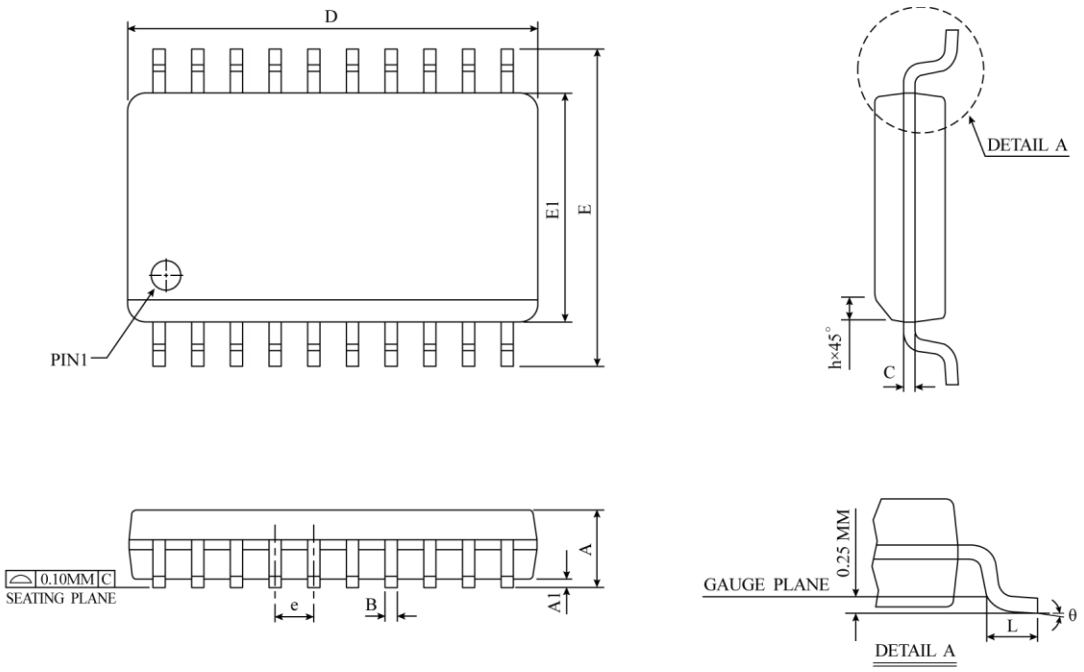


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	4.369	-	-	0.172
A1	0.381	0.673	0.965	0.015	0.027	0.038
A2	3.175	3.302	3.429	0.125	0.130	0.135
D	18.669	19.177	19.685	0.735	0.755	0.775
E		7.620 BSC			0.300 BSC	
E1	6.223	6.350	6.477	0.245	0.250	0.255
L	2.921	3.366	3.810	0.115	0.133	0.150
^{e}B	8.509	9.017	9.525	0.335	0.355	0.375
θ	0°	7.5°	15°	0°	7.5°	15°
JEDEC	MS-001 (BB)					

NOTES：

1. "D" , "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOTEXCEED .010 INCH.
2. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
3. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
4. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
5. DATUM PLANE H COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

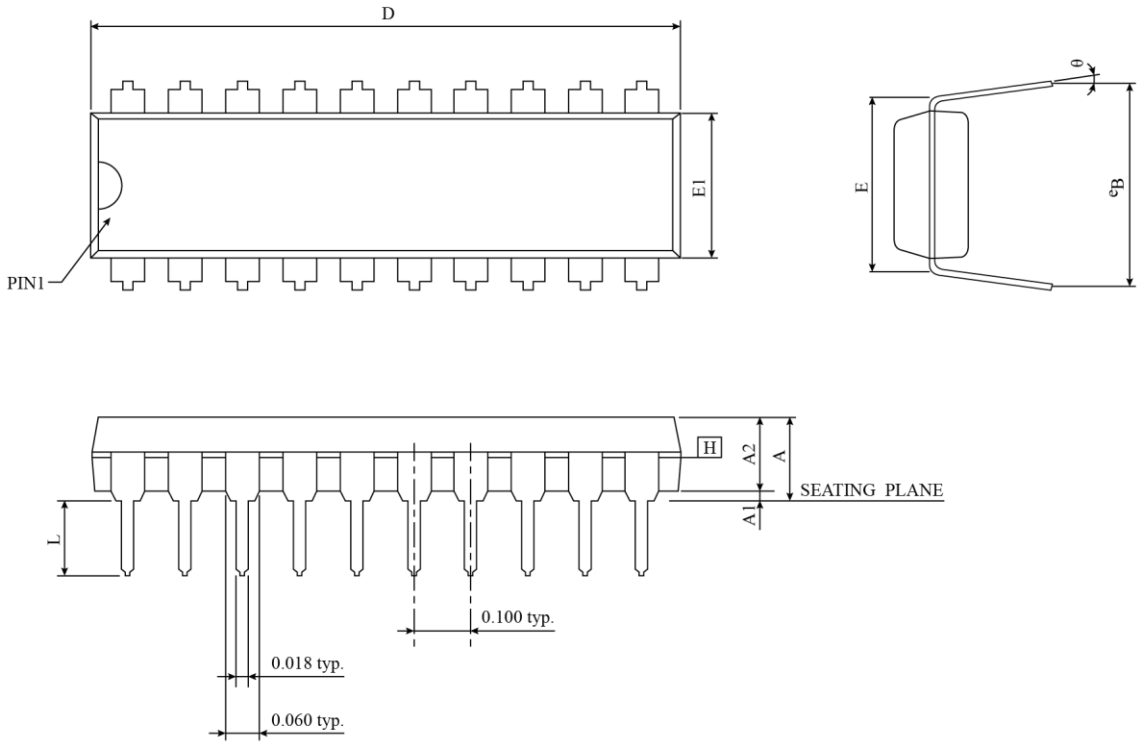
SOP-20 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	12.60	12.80	13.00	0.4961	0.5040	0.5118
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AC)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

DIP-20 (300mil) Package Dimension

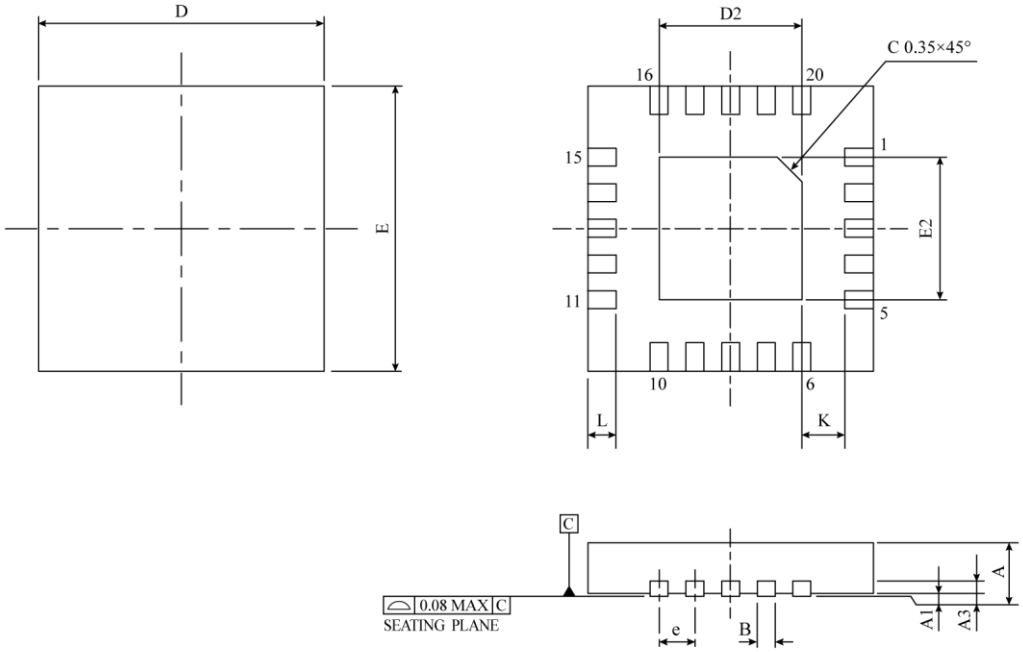


SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN	MAX	MIN	MAX
A	-	4.445	-	0.175
A1	0.381	-	0.015	-
A2	3.175	3.429	0.125	0.135
D	25.705	26.416	1.012	1.040
E	7.620	7.874	0.300	0.310
E1	6.223	6.477	0.245	0.255
L	3.048	3.556	0.120	0.140
^{e}B	8.509	9.525	0.335	0.375
θ	0°	15°	0°	15°
JEDEC	MS-001 (AD)			

NOTES：

1. "D" , "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOTEXCEED .010 INCH.
2. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
3. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
4. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
5. DATUM PLANE H COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

QFN 20 (4*4*0.75-0.5mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.03	0.05	0.000	0.001	0.002
A3		0.20 REF.			0.008 REF.	
B	0.20	0.25	0.30	0.008	0.001	0.012
D		4.00 BSC			0.157 BSC	
E		4.00 BSC			0.157 BSC	
e		0.50 BSC			0.020 BSC	
K	0.20	-	-	0.008	-	-
E2	2.40	2.48	2.55	0.094	0.097	0.100
D2	2.40	2.48	2.55	0.094	0.097	0.100
L	0.35	0.45	0.55	0.014	0.018	0.022
JEDEC	W(V) GGD-11					

⚠ * NOTES : DIMENSION B APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.