I. Overview

TM7707/8 Is used for low frequency measurement 2/3 The analog front end of the channel. The device can accept low-level input signals directly from the sensor, and then generate a serial digital output. use Σ-Δ Conversion technology Technique achieved twenty four No missing code performance. The selected input signal is sent to an analog modulator based Dedicated front end with programmable gain. The on-chip digital filter processes the output signal of the modulator. Send via on-chip control The register can adjust the cut-off point of the filter and the output update rate, thereby entering the first notch of the digital filter Line programming.

TM7707/8 Just 2.7~3.3V or 4.75~5.25V Single power supply. TM7707 Is dual channel fully differential Analog input, while TM7708 Yes 3 Channel pseudo differential analog input, both have a differential reference input. When the power supply voltage is 5V , The reference voltage is 2.5V When these two devices can change the input signal range from 0~+20mV To 0~+2.5V The signal is processed. Can also handle ±20mV~±2.5V Bipolar input signal, for TM7707 So AIN (-) The input terminal is the reference point, and TM7708 Yes COMMON Input terminal. When the power supply voltage is 3V , The reference voltage is 1.225V Can be processed 0~+10mV To 0~+1.225V Unipolar input signal, its bipolar input signal range is ±10mV To ±1.225V . therefore, TM7707/8 can be realised 2/3 The conditioning and conversion of all signals in the channel system.

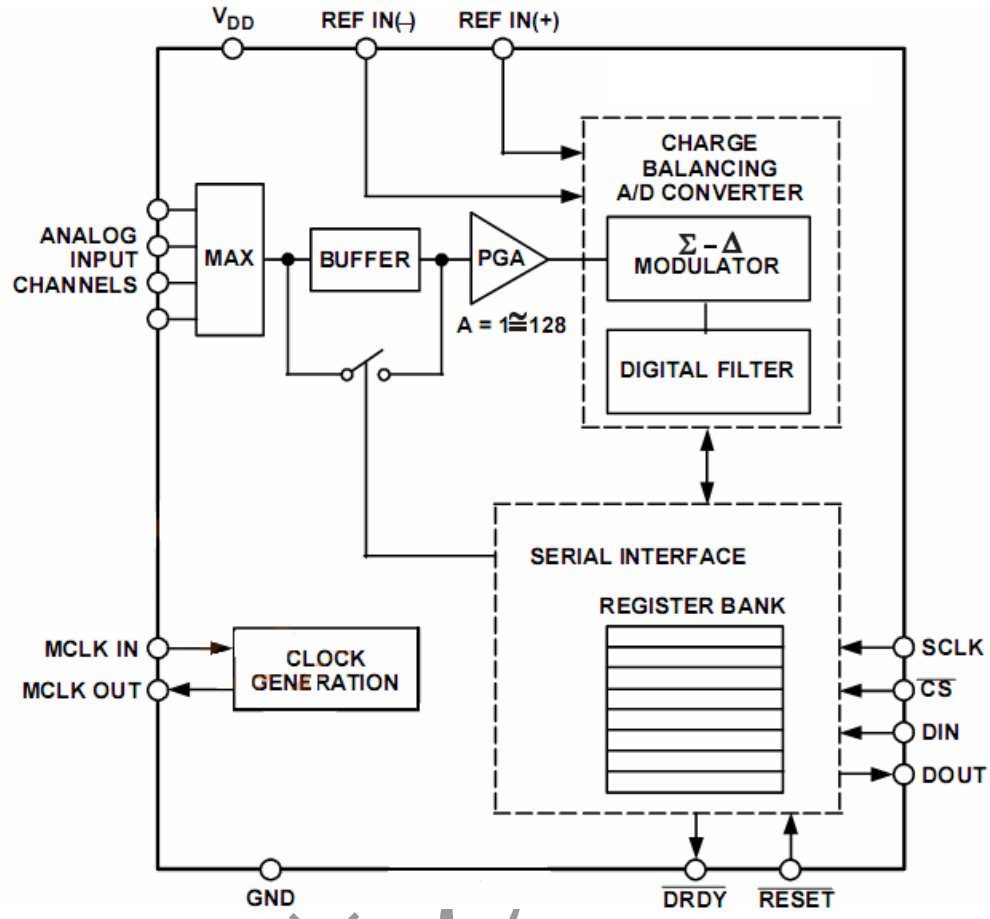
TM7707/7708 Is used in intelligent systems, microcontroller systems and based on DSP The ideal product of the system. The serial interface can be configured as a three-wire interface. The selection of gain value, signal polarity and update rate can be serial The input port is configured by software. The device also includes self-calibration and system calibration options to eliminate the device itself or The gain and offset error of the system.

CMOS The structure ensures that the device has extremely low power consumption, and the power-down mode reduces the power consumption during (Typical value). TM7707/8 use 16 foot SOPL Package.

2. Features

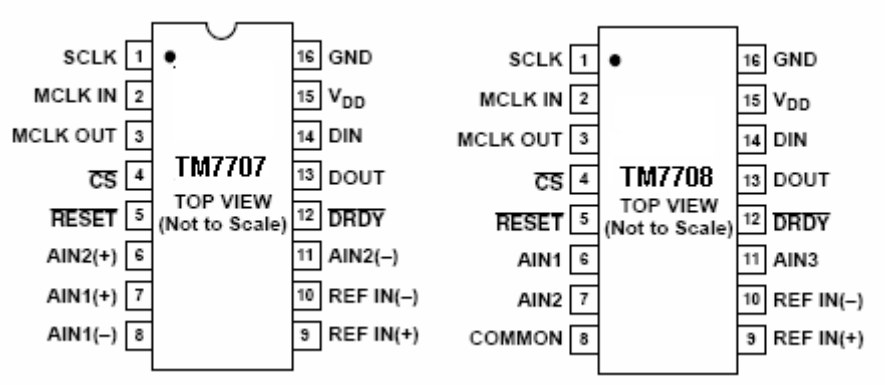
- TM7707 : 2 Fully differential input channels ADC
- TM7708 : 3 Pseudo-differential input channels ADC
  twenty four No missing code
  0.003% Non-linear
- Programmable gain front end
  Gain: 1 ~ 128
- Three-wire serial interface
- Ability to buffer analog input
- 2.7 ~ 3.3V or 4.75 ~ 5.25V Operating Voltage
- 3V At voltage, the maximum power consumption is 1mW
- The maximum waiting current is 8μA
- 16 foot SOP16L Package

Three, functional block diagram



Fourth, pin arrangement and function

TM7707 with TM7708 Pinout



Five, pin function

Numbering	name Weigh	Work can
1	**SCLK**	Serial clock, Schmitt logic input. Add an external serial clock to this Enter the port to access TM7707/TM7708 Serial data. The serial clock It can be a continuous clock that transmits all data in continuous bursts. Conversely, it also It can be a non-continuous clock, and the information is sent to TM7707/TM7708
2	**MCLK IN**	Provide the master clock signal for the converter. Can be in the form of crystal/resonator or external clock provide. The crystal/resonator can be connected to MCLK IN with MCLK OUT Between two pins. In addition, MCLK IN Also available CMOS Compatible clock driver, and MCLK OUT Not connected. The range of clock frequency is 500kHz~5MHz
3	**MCLK OUT**	When the main clock is a crystal/resonator, the crystal/resonator is connected to MCLK IN with MCLK OUT between. If in MCLK IN An external clock is connected to the pin, MCLK OUT An inverted clock signal will be provided. This clock can be used for external The circuit provides a clock source and can drive one CMOS load. If the user No need, MCLK OUT Can be passed in the clock register CLK DIS Bit off. In this way, the device will not be MCLK OUT Drive capacitive load on the pin and consume Unnecessary power
4	**$\overline{CS}$**	Chip select, active low logic input, select TM7707/TM7708 . Put The pin is connected to low level, TM7707/8 Can operate in three-wire interface mode (in SCLK , DIN with DOUT Interface with the device). Multiple devices on the serial bus In the software system, $\overline{CS}$ Make a choice for these devices, or TM7707/TM7708 When communicating, $\overline{CS}$ Can be used as a frame synchronization signal
5	**$\overline{RESET}$**	Reset input. The low-level input is effective to combine the control logic, interface logic, Calibration coefficients, digital filters and analog modulators are reset to the power-on state
6	**AIN2(+)[AIN1]**	for TM7707 , Differential analog input channel 2 The positive input terminal. for TM7708 , Analog input channel 1 Input
7	**AIN1(+)[AIN2]**	for TM7707 , Differential analog input channel 1 The positive input terminal. for TM7708 , Analog input channel 2 Input
8	**AIN1(-)[COMMON]** COMMON Input terminal, analog channel 1 , 2 , 3 The input is based on this input quasi-	for TM7707 , Differential analog input channel 1 Negative input terminal; for TM7708 ,
9	**REF IN (+)**	Reference input. TM7707/TM7708 The positive input terminal of the differential reference input. base Quasi-input is differential and stipulates REF IN (+) Must be greater than REF IN (-). REF IN (+) Can take V_{DD} with GND Any value between the reference input. TM7707/TM7708 The negative
10	**REF IN (-)**	input terminal of the differential reference input. REF IN (-) can take V_{DD} with GND Any value between and satisfy REF IN (+) more than the REF IN (-)
11	**AIN2 (-)[AIN3]**	for TM7707 , Differential analog input channel 2 The negative input terminal. for TM7708 , Analog input channel 3 Input
12		Logic output. A logic low level on this output indicates that TM7707 with

	$\overline{DRDY}$	TM7708 Get the new output word in the data register. Complete to a complete loss After reading the word, $\overline{DRDY}$ The pin immediately returns to high level. If you lose twice No data reading occurs between updates, $\overline{DRDY}$ Will be before the next output update 500 X t_{CLKIN} The time returns to high level. when $\overline{DRDY}$ When in the high level, the read operation cannot be performed, so as to avoid the read operation when the data in the data register is being updated Made. When the data is updated, $\overline{DRDY}$ It will return to low again. $\overline{DRDY}$ Also use To indicate when TM7707/ TM7708 The on-chip calibration sequence serial data output terminal has been
13	**DOUT**	completed. The serial data read from the on-chip output shift register is This end is output. According to the register selection bit in the communication register, the shift register can be Contains information from communication registers, clock registers or data registers
14	**DIN**	Serial data input terminal. The serial data written to the on-chip input shift register is determined by This input. Enter the shift register according to the register selection bit in the communication register The data in is transferred to the setting register, clock register or communication register
15	**V_{DD}**	Power supply voltage, + 2.7V~+5.25V
16	**GND**	Ground potential reference point of internal circuit

Six, limit parameters (TA = +25 ℃, unless otherwise specified)

V_{DD} Correct GND	**-0.3V ~+ 7V**
Analog input voltage pair GND	**-0.3V ~ V_{DD} + 0.3V**
Reference input voltage pair GND	**-0.3V ~ V_{DD} + 0.3V**
Digital input voltage pair GND	**-0.3V ~ V_{DD} + 0.3V**
Digital output voltage pair GND	**-0.3V ~ V_{DD} + 0.3V**
Operating temperature range (commercial grade, B)	**-40 ℃ ~ + 85 °C**
Storage temperature range	**-65 ℃ ~ + 150 °C**
Junction temperature	**+ 150 °C**
Power consumption (plastic DIP Package)	**450mW**
θ_{JA} Thermal resistance	**105 ℃/ W**
Pin temperature (soldering, 10 second)	**+ 260 °C**
Power consumption (plastic SOIC Package)	**450mW**
θ_{JA} Thermal resistance	**75 ℃/ W**
Pin temperature (soldering)	
Vapor phase (60 second)	**+ 215 °C**
infrared(15 second)	**+ 220 °C**
Power consumption (SSOP Package)	**450mW**
θ_{JA} Thermal resistance	**139 ℃/ W**
Pin temperature (soldering)	
Vapor phase (60 second)	**+ 215 °C**
infrared(15 second)	**+ 220 °C**
anti- ESD	**> 4000V**

Note: Strength exceeding the listed limit parameters may cause permanent damage to the device. These are just limit parameters,

It does not mean that the device is under extreme conditions or in any other conditions that exceed the parameters shown in the recommended operating condi

Pieces can work effectively. Extending the working time under extreme parameter conditions will affect the reliability of the device.

Seven, electrical characteristics

($V_{DD=+}$ 3V Or + 5V , REF IN (+)=+ 1.225V ; REF IN (-)= GND , MCLK IN =2.4576MHz , T_A= T_{MIN} ~ T_{MAX} ,unless Otherwise stated).

Parameter	B Version [1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	16	Bits min	Guaranteed by Design. Filter Notch <60 Hz
Output Noise	See Tables I and III		Dependson Filter Cutoffs and Selected Gain
Integral Nonlinearity [2]	±0.003	%of FSR	Filter Notch <60 Hz. Typically max 0.0003%
Unipolar Offset Error	See Note3		
Unipolar Offset Drift [4]	0.5	μV/ °C typ	
Bipolar Zero Error	See Note 3		
Bipolar Zero Drift [4]	0.5	μV/ °C typ	For Gains1,2and4 μV/ °C typ For
	0.1		Gains8,16,32,64and128
Positive Full-Scale Error [5]	See Note3		
Full-Scale Drift [4.6]	0.5	μV/ °C typ	
Gain Error [7]	See Note3		
Gain Drift [4.8]	0.5	ppm of FSR/ °C typ	
Bipolar Negative Full -Scale Error [2]	±0.003	%of FSR/ °C typ	Typically±0.001%
Bipolar Negative Full -Scale Drift [4]	1	μV/ °C typ	For Gains of 1 to 4
	0.6	μV/ °C typ	For Gains of 8 to 128
ANALOG INPUTS/REFERENCE INPUTS			Specifications for AIN and REF IN UnlessNoted
Input Common-Mode Rejection(CMR) [2]			
$V_{DD=}$ 5V			
Gain=1	96	dB typ	
Gain=2	105	dB typ	
Gain=4	110	dB typ	
Gain=8 → 128	130	dB typ	
$V_{DD=}$ 3V			
Gain=1	105	dB typ	
Gain=2	110	dB typ	
Gain=4	120	dB typ	

Gain=8 → 128	130	dB typ	
Normal-Mode50Hz Rejection [2]	98	dB typ	For Filter Notches of 25Hz, 50Hz, ±0.02×f_{NOTCH}
Normal-Mode60Hz Rejection [2]	98	dB typ	For Filter Notches of 20Hz, 60Hz, ±0.02×f_{NOTCH}
Common-Mode 50Hz Rejection [2]	150	dB typ	For Filter Notches of 25Hz, 50Hz, ±0.02×f_{NOTCH}
Common-Mode 60Hz Rejection [2]	150	dB typ	For Filter Notches of 20Hz, 60Hz, ±0.02×f_{NOTCH}
Absolute/Common-Mode REF IN Voltage [2]	GND to V_{DD}	Vmin to V mas	
Absolute/Common-Mode AIN Voltage [2,9]	GND—30mV	Vmin	BUF Bit of Setup Register=0
	V_{DD}+ 30mV	Vmax	
Absolute/Common-Mode AIN Voltage [2,9]	GND+50mV	Vmin	BUF Bit of Setup Register=1
	V_{DD} -1.5V	Vmax	
AIN DC Input Current [2]	1	nAmax	
AIN SamplingCapacitance [2]	10	pF max	
AIN Differential Voltage Range [10]	0to+V_{REF}/ GAIN [11]	nom	Unipolar Input Range(B/U Bit of Setup Register=1)
	±V_{REF}/ GAIN	nom	Bipolar Input Range(B/U Bit of Setup Register=0)
AIN Input Sampling Rate,fs	GAIN×f_{CLKIN}/ 64		For Gains of 1 to 4
	f_{CLKIN}/ 8		For Gains of 8 to 128
ReferenceInput Range			
REFIN(+)—REFIN(-) Voltage	1/1.75	Vmin/max = 2.7V to 3.3V.V_{REF}= 1.225±1 % for Specifled Performance	V_{DD}
REFIN(+)—REFIN(-) Voltage	1/3.5	Vmin/max = 4.75V to 5.25V.V_{REF}= 2.5±1 % for Specifled Performance	V_{DD}
REF IN Input SamplingRate, fs	f_{CLKIN}/ 64		
LOGIC INPUTS			
Input Current			
All Inputs Except MCLK IN	±1	μAmax	Typically±20nA
MCLK	±10	μAmax	Typically±20μA
All Inputs Except			

SCLK and MCLK IN			
V_{INL}, Input Low Voltage	0.8	Vmax	$V_{DD=}$ 5V
	0.4	Vmax	$V_{DD=}$ 3V
V_{INL}, Input High Voltage	2.0	Vmin	$V_{DD=}$ 3V and 5V
SCLK Only(Schmitt Triggered Input)			$V_{DD=}$ 5V NOMINAL
V_{T+}	1.4/3	Vmin/V max	
$V_{T\_}$	0.8/1.4	Vmin/V max	
V_{T+} -$V_{T\_}$	0.4/0.8	Vmin/V max	
SCLK Only(Schmitt Triggered Input)			
V_{T+}	1/2.5	Vmin/Vm ax	
$V_{T\_}$	0.4/1.1	Vmin/Vm ax	
V_{T+} $V_{T\_}$	0.375/0.8	Vmin/Vm ax	
MCLK IN Only			$V_{DD=}$ 5V NOMINAL
V_{INL}, Input Low Voltage	0.8	V max	
V_{INL}, Input High Voltage	3.5	V min	
MCLK IN Only			$V_{DD=}$ 3V NOMINAL
V_{INL}, Input Low Voltage	0.4	V max	
V_{INL}, Input High Voltage	2.5	V min	
LOGIC OUTPUTS(Including MCLK OUT)			
V_{OL}, Output Low Voltage	0.4	V max	$I_{SINK=}$ 800μA Exceptfor MCLK OUT. $_{12}$ $V_{DD=}$ 5V.
V_{OL}, Output Low Voltage	0.4	V max	$I_{SINK=}$ 100μA Exceptfor MCLK OUT. $_{12}$ $V_{DD=}$ 3V.
V_{OH}, Output High Voltage	4	V min	$I_{SOURCE=}$ 200μA Exceptfor MCLK OUT. $_{12}$ $V_{DD=}$ 5V.
V_{OH}, Output High Voltage	V_{DD} —0.6	V min	$I_{SOURCE=}$ 100μA Exceptfor MCLK OUT. $_{12}$ $V_{DD=}$ 3V.
Floating StateLeakage	± 10	μAmax	

Current			
Floating StateOutput 9 Capacitance 13		pF typ	
Data Output Coding	Binary		Unipolar Mode
	OffsetBinary		Bipolar Mode
SYSTEM CALIBRATION			
Positive Full—Scale Calibration Limit 14	(1.0 5× V_{REF}) GAIN	V max	GAIN Is the Selected PGA Gain(1 to 128)
Negative Full—Scale Calibration Limit 14	— (1.0 5× V_{REF}) GAIN	V max	GAIN Is the Selected PGA Gain(1 to 128)
Offset Calibration Limit 14	— (1.0 5× V_{REF}) GAIN	V max	GAIN Is the Selected PGA Gain(1 to 128)
Input Span 15	(0. 8× V_{REF})/ GAIN V min		GAIN Is the Selected PGA Gain(1 to 128)
	(2.1 X V_{REF})/ GAIN V max		GAIN Is the Selected PGA Gain(1 to 128)
POWER REQUIREMENTS			
V_{DD} Voltage	+ 2.7 to +3.3	Vmin to Vmax	For Specified Performance
Power Supply Currents 16			Digital I/Ps=0V or V_{DD}. External MCLK IN and CLK DIS=1
	0.32	mAmax	BUF Bit=O. f_{CLKIN}= 1MHz.Gains of 1 to 128
	0.6	mAmax	BUF Bit=1. f_{CLKIN}= 1MHz.Gains of 1 to 128
	0.4	mAmax	BUF Bit=Of $_{CLKIN}$= 2.4576MHz. Gains of 1 to 4
	0.6	mAmax	BUF Bit=O. f_{CLKIN}= 2.4576MHz. Gains of 8 to 128
	0.7	mAmax	BUF Bit=O. f_{CLKIN}= 2.4576MHz. Gains of 1 to 4
	1.1	mAmax	BUF Bit=1. f_{CLKIN}= 2.4576MHz. Gains of 8 to 128
V_{DD} Voltage	+ 4.75 to +5.25	Vmin toVmax	For Specified Performance
Power Supply Currents 16	0.45		Digital I/Ps=0V or V_{DD}. External MCLK IN and CLK DIS=1.
		mAmax	BUF Bit=0. f_{CLKIN}= 1MHz.Gains of 1 to 128
	0.7	mAmax	BUF Bit=1. f_{CLKIN}= 1MHz.Gains of 1 to 128
	0.6	mAmax	BUF Bit=0. f_{CLKIN}= 2.4576MHz. Gains of 1 to 4

	0.85	mAmax	BUF Bit=0. f_{CLKIN}= 2.4576MHz. Gains of 8 to 128
	0.9	mAmax	BUF Bit=1. f_{CLKIN}= 2.4576MHz. Gains of 1 to 4
	1.3	mAmax	BUF Bit=1. f_{CLKIN}= 2.4576MHz. Gains of 8 to 128
Standby(Power-Down)Current [17]	16	μAmax	External MCLK IN=0V or V_{DD}. V_{DD}= 5V.See Figure 9
	8	μAmax	External MCLK IN=0V or V_{DD}. V_{DD}= 3V
Power Supply Rejection [18]	See Note 19	dB typ	

Notes:

1. B Grade temperature range is- 40 ℃~+ 85 ℃.
2. These data are released according to the originally designed product.
3. A calibration is actually a conversion, so these errors are the table 1 And table 3 The order of the switching noise shown. This applies after calibration at the desired temperature.
4. Recalibration under any temperature conditions will remove these drift errors.
5. Positive full-scale error includes zero-scale error (Zero-Scale Error) (Unipolar offset error or bipolar zero error), and it is suitable for both unipolar input range and bipolar input range.
6. Full-scale drift includes zero-scale drift (unipolar offset drift or bipolar zero drift) and is suitable for unipolar and Bipolar input range.
7. Gain error does not include zero-scale error, it is calculated as full-scale error-unipolar offset for unipolar range Error, and for bipolar range is full-scale error-bipolar zero error.
8. Gain error drift does not include unipolar offset drift and unipolar zero drift. When only the zero-scale calibration is completed, add The gain error is actually the amount of drift of the device.
9. Common mode voltage range: analog input voltage does not exceed V_{DD+} 30mV ,not lower than GND-30mV . Voltage is lower than GND-200mV When the device function is effective, the leakage current will increase at high temperature.
10. Given here AIN (+) terminal analog input voltage range, right TM7707 In terms of AIN (-) Terminal voltage Correct TM7708 In terms of COMMON Input terminal. The input analog voltage should not exceed V_{DD+} 30mV, Should not be lower than GND-30mV . GND-200mV The input voltage can also be used, but the leakage current will increase at high temperatures.
11. VREF=REF IN (+)- REF IN (-).
12. Only when loading one CMOS Load, these logic output levels are only suitable for MCLK OUT .
13. +25 Test samples at ℃ to ensure consistency.
14. After calibration, if the analog input exceeds the positive full scale, the converter will output full 1, If the analog input is below the negative full scale, Will output all 0 .
15. The limit of the calibration voltage applied to the analog input terminal should not exceed V_{DD+} 30mV Or less than GND - 30mV .
16. When using a crystal or ceramic resonator as the clock source of the device (by MCLK Pin), V_{DD} Current and power consumption Varies with the type of crystal and resonator (see the "Clock and Oscillator Circuit" section).
17. In wait mode, the external main clock continues to run, 5V Wait for the current to increase to 150 μ A , 3V Electricity Increase to 75 μ A . When a crystal or ceramic resonator is used as the clock source of the device, the internal oscillator continues to run in the wait mode, and the power consumption of the power supply varies with the type of crystal and resonator (see "Wait Mode" one period)
18. Measured in the DC state, applicable to the selected passband. 50Hz Time, PSRR exceed 120dB (Filter notch

for 25Hz or 50Hz). 60Hz Time, PSRR exceed 120dB (The filter notch is 20Hz or 60Hz).

19. PSRR By gain and V_{DD} Decide as follows:

Gain	1	2	4	8~128
V_{DD}= 3V	86	78	85	93
V_{DD}= 5V	90	78	84	91

8. Timing parameters

(V_{DD} = + 2.7V~+5.2V ; GND=0V ; f_{CLKIN} = 2.4567MHz ; Input Logic 0=0 V , Logic 1 = V_{DD} Unless otherwise Description)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
f_{CLKIN} [3,4]	400	kHzmin	Master Clock Frequency: Crystal Oscillator or Externally Supplied for Specified
	2.5	MHz max	Performance
$t_{CLKIN\ LO}$	0.4×t_{CLKIN}	ns min	Master Clock Input Low Time. t_{CLKIN}= 1/ f_{CLKIN}
$t_{CLKIN\ HI}$	0.4×t_{CLKIN}	ns min	Master Clock Input High Time. DRDY
t_1	500×t_{CLKIN}	ns mon	High Time
t_2	100	ns min	RESETPulsewidth
Read Operation			
t_3	0	ns min	DRDY to CS Setup Time
t_4	120	ns min	CS Falling Edge to SCLK Rising Edge Setup Time
t_5	0	ns min	SCLK Falling Edge to Data Valid Delay
	80	ns max	V_{DD}=+ 5V
	100	ns max	V_{DD}=+ 3.0V
t_6	100	ns min	SCLK High Pulsewidth
t_7	100	ns min	SCLK Low Pulsewidth
t_8	0	ns min	CS Rising Edge to SCLK Rising Edge Hold Time
t_9	10	ns min	Bus RelinguishTimeafter SCLK Rising Edge
	60	ns max	V_{DD}=+ 5V
	100	ns max	V_{DD}=+ 3.0V
t_{10}	100	ns max	SCLK Falling Edge to DRDY High [7]
Write Operation			
t_{11}	120	ns min	CS Falling Edge to SCLK Rising Edge Setup Time
t_{12}	30	ns min	Data Valid to SCLK Rising Edge

			Setup Time
t_{13}	**20**	**ns min**	**Data Valid to SCLK Rising Edge Hold Time**
t_{14}	**100**	**ns min**	**SCLK High Pulsewidth**
t_{15}	**100**	**ns min**	**SCLK High Pulsewidth**
t_{16}	**0**	**ns min**	**$\overline{CS}$ Rising Edge to SCLK Rising Edge Hold Time**

Notes:

1. The sample test temperature is + 25 ℃ to ensure consistency. All input signals meet: $t_r = t_f = 5ns$ (V_{DD} of 10%~90%), and from 1.6V Level timing.

2. See picture 16 And figure 17 .

3. f_{CLKIN} The duty cycle is 45%~55% . as long as TM7707/8 Not in wait mode, must provide f_{CLKIN} . At this In this case, if there is no clock, the device will draw more current than specified and may become uncalibrated.

4. $f_{CLKIN} = 2.4567MHz$ Carry out production test from time to time to ensure the device works 400kHz .

5. These numbers are in the figure 1 Measured under the load circuit. They are defined as output through V_{OL} or V_{OH}

6. The value is in the data output as 0.5V Measured at the time (the load situation is shown in the figure 1 Shown)Then the measured value is pushed Play back to eliminate 50pF The effect of capacitor charging or discharging. This means that all mentioned in the timing parameter table The time values are the real bus withdrawal time (relinquish time), and therefore there is no connection with the external bus load capacitance turn off.

7. After the output is updated, DRDY Return to high level after reading from the device for the first time. when DRDY When it is high, if If necessary, the same data can be read again. But it must be noted that after the next output update, random randomness will not happen soon. After reading.

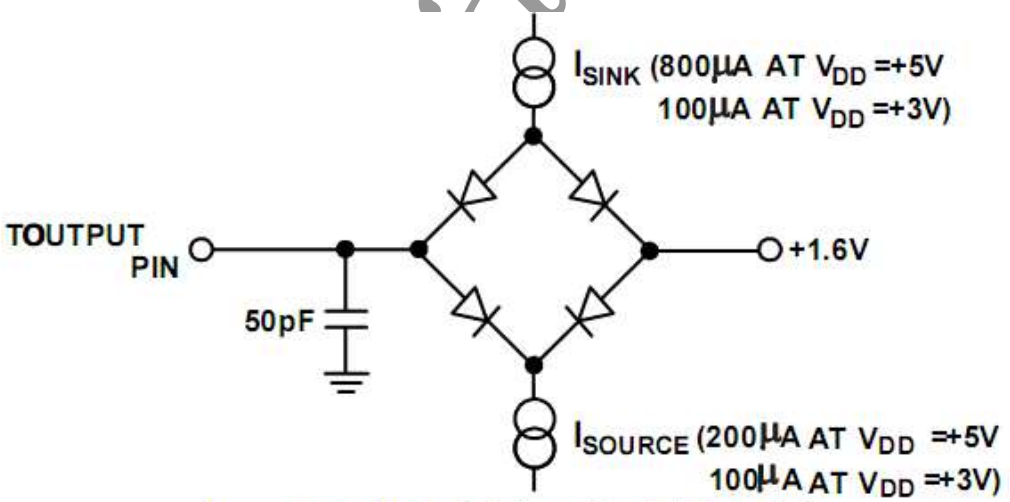


图1 访问时间和总线撤回时间的负载电路图

Nine, typical characteristic curve

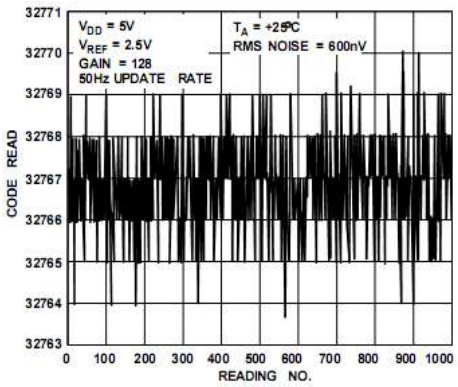


图2 典型噪声曲线（增益=128，更新速率=50Hz）

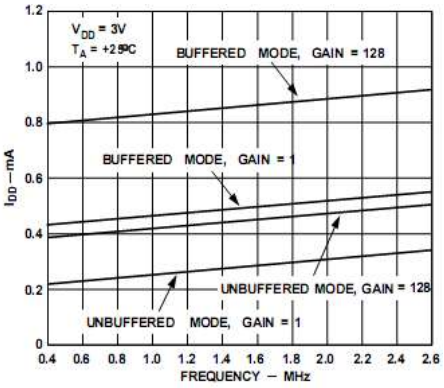


图3 I_{DD}与MCLKIN 频率的关系（3V电源电压）

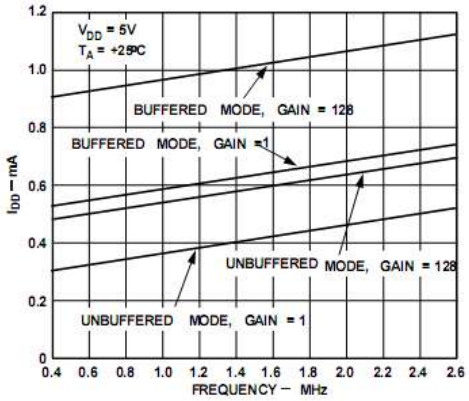


图6 I_{DD}与MCLKIN 频率的关系（5V电源电压）

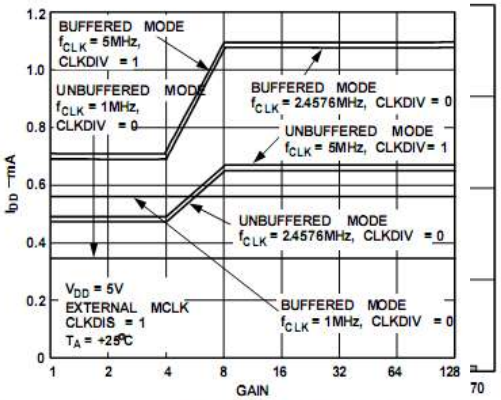


图7 I_{DD}与增益和时钟频率的关系（5V电源电压

10. Output noise

10.1TM7707/8 5V Output noise

table 1a Means when f_{CLKIN}= 2.4576MH z When, for some typical notches and- 3dB frequency, TM7707/8 The output rms noise and effective resolution; table 1b Gives f_{CLKIN}= 1MHZ Time data. The data given applies to V_{REF}

As + 2.5V And BUFFER=0 The bipolar input range. These data are typical values and the analog input voltage is 0V Under the circumstances. The data in parentheses in each table is the effective resolution of the period (rounded to the nearest 0.5LSB) .

The effective resolution of the device is defined as the output rms noise and the input full scale (ie, 2 X V_{REF}/ GAIN)Ratio. should

Note that it is not calculated using peak-to-peak output noise data. Peak-to-peak noise data can be as high as the root mean square data 6.6 Times,

At the same time, the effective resolution data based on peak-to-peak noise can be compared with the effective resolution based on rms noise shown in the slogan in the table.

Low resolution 2.5 Bit.

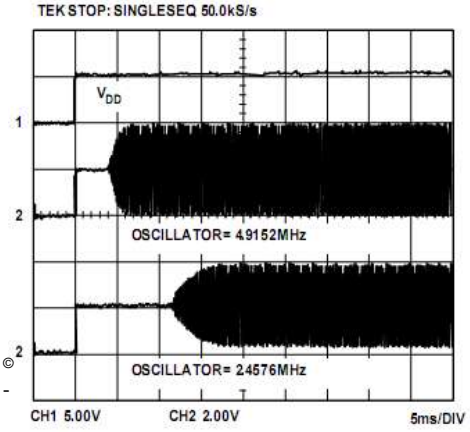


图8 典型晶体振荡器上电时间

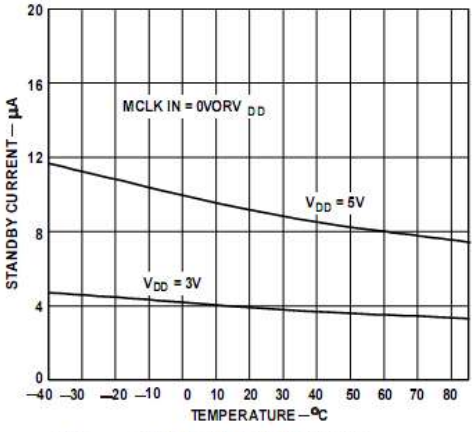


图9 等待电流与温度的关系

The output noise of the device comes from two sources. The first source is the electrical noise of the semiconductor devices used in the implementation of the modulator. Piece noise) . Second, when the analog input signal is converted to the digital domain, quantization noise is added. Device noise is low level And basically has nothing to do with frequency. The quantization noise starts at a fairly low level, but rises rapidly as the frequency increases to become The main noise source. Therefore, the lower filter notch setting (for f_{CLKIN}= 2.4576MHz , About below 100MHZ , for f_{CLKIN}= 1MHz , About below 40Hz) Is controlled by the device noise, and the setting of the higher notch is controlled by the quantization noise system. As table I As shown, the change of the filter notch and cutoff frequency in the quantization noise control domain will be greater than that in the device noise control domain The change in is independent of the gain in noise performance. At the same time, device noise is added to PGA Medium, therefore, high frequency at lower notches In the case of gain, the effective resolution will decrease. In addition, in the device noise control area, the output noise (with μ V meter) Basically it has nothing to do with the reference voltage; in the quantization noise control area, the noise ratio is based on the value of the reference. Adopted on the device Post-filtering may improve the output data rate for a given -3dB frequency, and further reduce the output Out of noise.

Set at the lower filter notch (f_{CLKIN}= 2.4576MHz Time below 60Hz , f_{CLKIN}= 1MHz) Case, The error-free performance of the device is at twenty four Bit level. In the case of a higher setting, more errors will be generated until the f_{CLKIN}= 2.4576MHz When the notch is set to 1kHz (f_{CLKIN}= 1MHz Set as 400Hz)until. Only for 12 Bits guarantee error-free performance.

table 1a fCLKIN=2.4576MHZ , BUFFER=0 Time

TM7707/8 Output noise/resolution and gain 1 The relationship of a notch (5V Voltage)

Filter First	Typical Output RMS Noise in μ V(Effective Resolution in bits)							
Notch and O/P — 3 dB	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of
Data Rate Frequency	1	2	4	8	16	32	64	128
5Hz 1.31Hz	0.87 (22.5)	0.48 (22.5)	0.24 (22.5)	0.2 (21.5)	0.18 (20.5)	0.17 (20)	0.17 (19)	0.17 (18)
10Hz 2.62Hz	1.0 (22.5)	0.78 (21.5)	0.48 (21.5)	0.33 (twenty one)	0.25 (20.5)	0.25 (19.5)	0.25 (18.5)	0.25 (17.5)
25Hz 6.55Hz	1.8 (21.5)	1.1 (twenty one)	0.63 (twenty one)	0.5 (20)	0.44 (19.5)	0.41 (18.5)	0.38 (17.5)	0.38 (16.5)
30Hz 7.86Hz	2.5 (twenty one)	1.31 (twenty one)	0.84 (20.5)	0.57 (20)	0.46 (19.5)	0.43 (18.5)	0.4 (17.5)	0.4 (16.5)
50Hz 13.1Hz	4.33 (20)	2.06 (20)	1.2 (20)	0.64 (20)	0.54 (19)	0.46 (18.5)	0.46 (17.5)	0.46 (16.5)
60Hz 15.72Hz	5.28 (20)	2.36 (20)	1.33 (20)	0.87 (19.5)	0.63 (19)	0.62 (18)	0.6 (17)	0.56 (16)
100 Hz 26.2 Hz	12.1 (18.5)	5.9 (18.5)	2.86 (19)	1.91 (18.5)	1.06 (18)	0.83 (17.5)	0.82 (16.5)	0.76 (15.5)
250Hz 65.5Hz	127 (15.5)	58 (15.5)	29 (15.5)	15.9 (15.5)	6.7 (15.5)	3.72 (15.5)	1.96 (15.5)	1.5 (14.5)
500Hz 131Hz	533 (13)	267 (13)	137 (13)	66 (13)	38 (13)	20 (13)	8.6 (13)	4.4 (13)

1Hz 262Hz	2850 (11)	1258 (11)	680 (11)	297 (11)	131 (11)	99 (10.5)	53 (10.5)	28 (10.5)

table 1b fCLKIN=1MHZ , BUFFER=0 Time

TM7707/8 Output noise/resolution and gain 1 The relationship of a notch (5V Voltage)

Filter First	Typical Output RMS Noise in μ V(Effective Resolution in bits)							
Notch and O/P — 3 dB	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of
Data Rate Frequency	1	2	4	8	16	32	64	128
2Hz 0.52Hz	0.75 (22.5)	0.56 (twenty two)	0.31 (twenty two)	0.19 (21.5)	0.17 (twenty one)	0.14 (20)	0.14 (19)	0.14 (18)
4Hz 1.05Hz	1.04 (twenty two)	0.88 (21.5)	0.45 (21.5)	0.28 (twenty one)	0.21 (20.5)	0.21 (19.5)	0.21 (18.5)	0.21 (17.5)
10Hz 2.62Hz	1.66 (21.5)	1.01 (21.5)	0.77 (20.5)	0.41 (20.5)	0.27 (19.5)	0.35 (1 9)	0.35 (18)	0.35 (17)
25Hz 6.55Hz	5.2 (20)	2.06 (20)	1.4 (20)	0.86 (19.5)	0.63 (19)	0.61 (18)	0.59 (17)	0.59 (16)
30Hz 7.86Hz	7.1 (19.5)	3.28 (19.5)	1.42 (19.5)	1.07 (19)	0.78 (18.5)	0.64 (18)	0.61 (17)	0.61 (16)
50Hz 13.1Hz	19.4 (18)	9.11 (18)	4.2 (18)	2.45 (18)	1.56 (17.5)	1.1 (17)	0.82 (16.5)	0.8 (15.5)
60Hz 15.72Hz	25 (17.5)	16 (17.5)	6.5 (17.5)	2.9 (17.5)	1.93 (17.5)	1.4 (17)	1.1 (16)	0.98 (15.5)
100Hz 26.2Hz	102 (15.5)	58 (15.5)	25 (15.5)	13.5 (15.5)	5.7 (15.5)	3.9 (15.5)	2.1 (15)	1.3 (15)
200Hz 52.4Hz	637 (13)	259 (13)	130 (13)	76 (13)	33 (13)	16 (13)	11 (13)	6 (12.5)
400Hz 104.8Hz	2830 (11)	1430 (11)	720 (11)	334 (11)	220 (10.5)	94 (10.5)	54 (10.5)	25 (10.5)

10.2 TM7707/8 3V Output noise

table 2a Means when f CLKIN= 2.4576MH Z When, for some typical notches and- 3dB frequency, TM7707/8 The output rms noise and effective resolution; table 2b Gives f CLKIN= 1MHZ Time data. The data given applies to V REF

As + 1.25V And BUFFER=0 The bipolar input range. These data are typical values and the analog input voltage is 0V Under the circumstances. The data in parentheses in each table is the effective resolution of the device (rounded to the nearest 0.5LSB) .

The effective resolution of the device is defined as the output rms noise and the input full scale (ie, 2 X V REF/ GAIN)Ratio. should

Note that it is not calculated using peak-to-peak output noise data. Peak-to-peak noise data can be as high as the root mean square data 6.6 Times,

At the same time, the effective resolution data based on peak-to-peak noise can be compared with the effective resolution based on rms noise shown in the slogan in the table. Low resolution 2.5 Bit.

The output noise of the device comes from two sources. The first source is the electrical noise of the semiconductor devices used in the implementation of the modulator.

Piece noise) . Second, when the analog input signal is converted to the digital domain, quantization noise is added. Device noise is low level

And basically has nothing to do with frequency. The quantization noise starts at a fairly low level, but rises rapidly as the frequency increases to become

The main noise source. Therefore, the lower filter notch setting (for f_{CLKIN}= 2.4576MHz , About below 100HZ ,

for f_{CLKIN}= 1MHz , About below 40Hz) Is controlled by the device noise, and the setting of the higher notch is controlled by the quantization noise

system. As table I As shown, the change of the filter notch and cutoff frequency in the quantization noise control domain will be greater than that in the device noise control domain

The change in is independent of the gain in noise performance. At the same time, device noise is added to PGA Medium, therefore, high frequency at lower notches

In the case of gain, the effective resolution will decrease. In addition, in the device noise control area, the output noise (with μ V meter)

Basically it has nothing to do with the reference voltage; in the quantization noise control area, the noise ratio is based on the value of the reference. Adopted on the device

Post-filtering may improve the output data rate for a given -3dB frequency, and further reduce the output

Out of noise.

Set at the lower filter notch (f_{CLKIN}= 2.4576MHz Time below 60Hz , f_{CLKIN}= 1MHz) Case,

The error-free performance of the device is at twenty four Bit level. In the case of a higher setting, more errors will be generated until the

f_{CLKIN}= 2.4576MHz When the notch is set to 1kHz (f_{CLKIN}= 1MHz Set as 400Hz)until. Only for 12 Bits guarantee error-free performance.

table 2a fCLKIN=2.4576MHZ , BUFFER=0 Time

TM7707/8 Output noise/resolution and gain 1 Notch relationship (3V Voltage)

Filter First	Typical Output RMS Noise in μ V(Effective Resolution in bits)							
Notch and O/P — 3 dB	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of
Data Rate Frequency	1	2	4	8	16	32	64	128
5Hz 1.31Hz	1.07 (twenty one)	0.68 (twenty one)	0.29 (twenty one)	0.24 (20)	0.22 (19.5)	0.17 (20)	0.17 (19)	0.17 (18)
10Hz 2.62Hz	1.69 (20.5)	1.1 (20)	0.56 (20)	0.35 (19.5)	0.33 (19)	0.33 (18)	0.33 (17)	0.33 (16)
25Hz 6.55Hz	3.03 (19.5)	1.7 (19.5)	0.89 (19.5)	0.55 (19)	0.49 (18.5)	0.46 (17.5)	0.46 (16.5)	0.45 (15.5)
30Hz 7.86Hz	3.55 (19.5)	2.1 (19)	1.1 (19)	0.61 (18.5)	0.58 (18)	0.57 (17)	0.55 (16)	0.55 (15)
50Hz 13.1Hz	4.72 (19)	2.3 (19)	1.5 (18.5)	0.84 (18.5)	0.7 (18)	0.68 (17)	0.67 (16)	0.66 (15)
60Hz 15.72Hz	5.12 (19)	3.1 (18.5)	1.6 (18)	0.98 (18)	0.9 (17.5)	0.7 (17)	0.69 (16)	0.68 (18)
100 Hz 26.2 Hz	9.68 (18)	5.6 (18)	2.4 (18)	1.3 (18)	1.1 (17)	0.95 (16.5)	0.88 (15.5)	0.9 (14.5)
250Hz 65.5Hz	44 (16)	31 (15.5)	15 (15.5)	5.8 (15.5)	3.7 (15.5)	2.4 (15)	1.8 (14.5)	1.5 (14.5)
500Hz 131Hz	304 (13)	129 (13)	76 (13)	33 (13)	20 (13)	11 (13)	6.3 (12.5)	3 (12.5)
1Hz 262Hz	1410 (11)	715 (11)	350 (11)	177 (11)	101 (10.5)	51 (10.5)	31 (10.5)	12 (10.5)

table 2b fCLKIN=1MHZ , BUFFER=0 Time

TM7707/8 Output noise/resolution and gain 1 Notch relationship (3V Voltage)

Filter First	Typical Output RMS Noise in μ V(Effective Resolution in bits)							
Notch and O/P — 3 dB	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of
Data Rate Frequency	1	2	4	8	16	32	64	128
2Hz 0.52Hz	0.86 (21.5)	0.58 (twenty one)	0.32 (twenty one)	0.21 (20.5)	0.2 (19.5)	0.2 (18.5)	0.2 (17.5)	0.2 (16.5)
4Hz 1.05Hz	1.26 (twenty one)	0.74 (20.5)	0.44 (20.5)	0.35 (20)	0.3 (19)	0.3 (18)	0.3 (17)	0.3 (16)
10Hz 2.62Hz	1.68 (20.5)	1.33 (20)	0.73 (20)	0.5 (19)	0.49 (18.5)	0.49 (17.5)	0.48 (16.5)	0.47 (15.5)
25Hz 6.55Hz	3.82 (19.5)	2.0 (19.5)	1.2 (19)	0.88 (18.5)	0.66 (18)	0.57 (17)	0.55 (16)	0.55 (15)
30Hz 7.86Hz	4.88 (19)	2.1 (19)	1.3 (19)	0.93 (18.5)	0.82 (17.5)	0.69 (17)	0.68 (16)	0.66 (15)
50Hz 13.1Hz	61 (15.5)	30 (15.5)	12 (15.5)	6.1 (15.5)	2.9 (15.5)	2.4 (15)	1.8 (14.5)	1.8 (13.5)
60Hz 15.72Hz	25 (17.5)	16 (17.5)	6.5 (17.5)	2.9 (17.5)	1.93 (17.5)	1.4 (17)	1.1 (16)	0.98 (15.5)
100Hz 26.2Hz	102 (15.5)	58 (15.5)	25 (15.5)	13.5 (15.5)	5.7 (15.5)	3.9 (15.5)	2.1 (15)	1.3 (15)
200Hz 52.4Hz	275 (13)	130 (13)	65 (13)	33 (13)	17 (13)	11 (13)	6.3 (12.5)	3 (12.5)
400Hz 104.8Hz	1435 (11)	720 (11)	362 (11)	175 (11)	110 (10.5)	51 (10.5)	31 (10.5)	12 (10.5)

10.3 Buffer mode output noise

table 3 Means when f CLKIN= 2.4576MH Z with BUFFER=+5V When, for some typical notches and- 3dB frequency,

TM7707/8 The output rms noise and effective resolution; table 4 Gives f CLKIN= 2.4576MHz with BUFFER=+5V

Time TM7707/8 The data. The data given applies to the bipolar input range and has 0V Differential analog input voltage generation.

for TM7707/8 , VDD=5V Time V REF Voltage is + 2.5V ;for TM7707/8 , VDD=3V Time V REF Voltage

As + 1.25V . The effective resolution of the data device in the brackets in each table (rounded to the nearest 0.5LSB). Device

The effective resolution of the device is defined as the output rms noise and the input full scale (ie, 2 X V REF/ GAIN)Ratio. It should be noted

It is not calculated using peak-to-peak output noise data. Peak-to-peak noise data can be as high as the root mean square data 6.6 Times, the same

The effective resolution data based on peak-to-peak noise can be compared with the effective resolution based on root mean square noise shown in the slogan in the table.

Low rate 2.5 Bit.

table 3 fCLKIN=2.4576MHZ Time TM7707/8 Output noise in buffer mode/resolution (5V Voltage)

Filter First	Typical Output RMS Noise in μ V(Effective Resolution in bits)							
Notch and O/P — 3 dB	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of
Data Rate Frequency	1	2	4	8	16	32	64	128
5Hz 1.31Hz	0.99 (22.5)	0.68 (twenty two)	0.46 (21.5)	0.26 (twenty one)	0.26 (20)	0.26 (19)	0.26 (18)	0.260 (17)
10Hz 2.62Hz	1.5 (21.5)	0.95 (21.5)	0.63 (twenty one)	0.41 (20.5)	0.39 (19.5)	0.36 (18.5)	0.36 (17.5)	0.36 (16.5)
25Hz 6.55Hz	2.5 (twenty one)	1.7 (20.5)	0.88 (20.5)	0.75 (19.5)	0.57 (19)	0.57 (18)	0.57 (17)	0.56 (16)
30Hz 7.86Hz	2.9 (20.5)	1.8 (20.5)	1 (20)	0.87 (19.5)	0.75 (18.5)	0.72 (17.5)	0.72 (16.5)	0.71 (15.5)
50Hz 13.1Hz	4.2 (20)	2.5 (20)	1.5 (19.5)	1.1 (19)	0.94 (18.5)	0.94 (17.5)	0.94 (17.5)	0.87 (15.5)
60Hz 15.72Hz	6.1 (19.5)	2.9 (19.5)	2 (19.5)	1.2 (19)	1 (18.5)	0.97 (17.5)	0.95 (16.5)	0.94 (15.5)
100 Hz 26.2 Hz	13.8 (18.5)	6.5 (18.5)	3.5 (18.5)	2.2 (18)	1.3 (18)	1.2 (17)	1.3 (16)	1.1 (15)
250Hz 65.5Hz	87 (16)	56 (15.5)	25 (15.5)	11 (15.5)	5.7 (15.5)	3.6	2.4 (15)	2.1 (14)
500Hz 131Hz	508 (13.5)	241 (13.5)	117 (13.5)	73 (13)	34 (13)	16 (13)	8.5 (13)	5.2 (13)
1Hz 262Hz	2860 (11)	1700 (10.5)	745 (10.5)	480 (10.5)	197 (10.5)	94 (10.5)	53 (10.5)	twenty three (10.5)

table 4 fCLKIN=2.4576MHZ Time TM7707/8 Output noise in buffer mode/resolution (3V Voltage)

Filter First	Typical Output RMS Noise in μ V(Effective Resolution in bits)							
Notch and O/P — 3 dB	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of	Gain of
Data Rate Frequency	1	2	4	8	16	32	64	128
5Hz 1.31Hz	1.16 (twenty one)	0.76 (20.5)	0.34 (20)	0.29 (20)	0.29 (19)	0.28 (18)	0.26 (17)	0.26 (16)
10Hz 2.62Hz	1.5 (21.5)	0.95 (21.5)	0.63 (twenty one)	0.41 (20.5)	0.39 (19.5)	0.36 (18.5)	0.36 (17.5)	0.36 (16.5)
25Hz 6.55Hz	2.5 (twenty one)	1.7 (20.5)	0.88 (20.5)	0.75 (19.5)	0.57 (19)	0.57 (18)	0.57 (17)	0.56 (16)
30Hz	3.7	2.2	1.3	0.76	0.68	0.66	0.66	0.66

7.86Hz	(19.5)	(19)	(19)	(18.5)	(18)	(17)	(16)	(15)
50Hz	4.5	3	1.7	1.0	0.92	0.9	0.89	0.89
13.1Hz	(19)	(18.5)	(18.5)	(18)	(17.5)	(16.5)	(15.5)	(14.5)
60Hz	5.3	3.3	1.8	1.1	1	0.96	0.96	0.96
15.72Hz	(19)	(18.5)	(18.5)	(18)	(17)	(16.5)	(15.5)	(14.5)
100Hz	10	4.9	3.1	1.5	1.2	1.2	1.2	1.2
26.2Hz	(18)	(18)	(17.5)	(17.5)	(17)	(16)	(15)	(14)
250Hz	47	29	15	7.5	4.7	2.6	2.5	1.5
65.5Hz	(15.5)	(15.5)	(15.5)	(15.5)	(15)	(15)	(14)	(13.5)
500Hz	300	171	74	25	twenty one	8.6	5.6	3.1
131Hz	(13.5)	(13)	(13)	(13)	(13)	(13)	(13)	(12.5)
1 Hz	1722	723	380	230	93	55	30	12
262 Hz	(10.5) (10.5) (10.5) (10.5) (10.5) (10.5) (10.5) (10.5)							

11. On-chip registers

TM7707/8 Includes 8 These registers are accessed through the serial port of the device.

The first is the communication register, which manages the channel selection, determines whether the next operation is a read operation or a write operation, and the next Which register to read or write at a time. All communication with the device must start with writing to the communication register. After power-on or reset, The device is waiting for a write operation on the communication register. The data written to the communication register determines that the next operation is to read Or write, and at the same time determine which register the read operation or write operation occurs on. So, write any other registers first It is necessary to write the communication register before writing the selected register. All registers (including the communication register itself and output Data register) Before reading, the communication register must be written first, and then the selected register can be read. In addition, through The signal register also controls the wait mode and channel selection, in addition DRDY The status can also be read from the communication register.

First 2 One register is the setting register, which determines the calibration mode, gain setting, single/bipolar input and buffer mode.

First 3 Two registers are filter high registers, including filter high 4 Bit selection bit and clock control bit. First 4 This register is a data register, and the data output by the device is read from this register.

First 6 Each register is the filter low register, including the low filter selection word 8 Bit. The last register is the calibration register, which stores channel calibration data.

Detailed descriptions are given below.

1. Communication register (RS2 , RS1 , RS0 = 0 , 0 , 0)

The communication register is a 8 Bit register, you can either read data or write data into it. All communication with the device The letter must start from writing to this register. The data written up determines which register the next read or write operation will take place. Once the next read or write operation is completed on the selected register, the interface returns to the communication register to receive a write operation The state of work. This is the default state of the interface. After power-on or reset, TM7707/8 In this default state waiting for The communication register is written once. If the interface sequence is lost, if DIN The high-level write operation lasted for enough Long enough (at least 32 Serial clock cycles) , TM7707/8 Will return to the default state.

The following table 5 It is the description of each communication register.

table 5 Communication register

0/DRDY (0)	RS2 (0)	RS1 (0)	RSO (0)	R/W (0)	STBY	(0)	CHI (0) CH0 (0)

* The default value of power-on reset in brackets

0/ DRDY For write operations, there must be a " 0 "Is written to this bit so that the write operation on the communication register can Finished accurately. in case" 1 "Is written to this register, and subsequent people will not be able to write to this register. It will stay in This bit until there is a " 0 "Is written into this bit. Once there is" 0 "Write to 0/ DRDY Bits below 7 The bit will be loaded into the communication register. For read operations, this bit provides the device DRDY Sign. The position State and DRDY The state of the output pins is the same.

RS2-RS0 Register selection bit. This 3 The ones place selects the next read/write operation 8 Which one of the on-chip registers is sent Health, see table 6 (Attach register size). When the selected register has completed the read/write operation, the device returns to The status of waiting for the next write operation of the communication register. It will not remain in the state of continuing to access the original register.

table 6 Register selection select

RS2	RS1	RS0	register	Register bits
0	0	0	Communication register	8 Bit
0	0	1	Set register	8 Bit
0	1	0	Filter high register	8 Bit
0	1	1	Data register	twenty four Bit
1	0	0	Test register	8 Bit
1	0	1	Filter low register	8 Bit
1	1	0	Zero-scale calibration register	twenty four Bit
1	1	1	Full-scale calibration register	twenty four Bit

R/ W Read/write selection. This bit selects whether the next operation is to read or write to the selected register. " 0 "Means next fuck To write, " 1 "Indicates that the next operation is to read.

STBY Waiting mode. Write " 1 "Is in wait or power-down mode. In this mode, the device consumes The power supply current is only 10 μ A . In the standby mode, the device will maintain its calibration coefficients and control word information. write" 0 ", the device is in normal operating mode.

CHI-CH0 Channel selection. This 2 One place selects a channel for data conversion or access to calibration coefficients, as shown in the table 7 Shown. In-device 3 The calibration register is used to store calibration coefficients. As table 7 with 8 The display indicates which channel combinations have independent calibration coefficients. when CH1 For logic 1 and CH0 For logic 0 Time, it can be seen from the table TM7707 Yes AIN 1 (-) The input pin is short-circuited internally, and TM7708 Yes COMMON foot Short-circuit itself internally. This can be used as a test method for evaluating noise performance (no external noise source). In this mode, AIN 1 (-)/ COMMON The input must be connected to an external voltage within the common-mode voltage range allowed by the device.

table 7 TM7707 Channel selection

CH1	CH0	AIN (+)	AIN (-)	Calibration register pair
0	0	AIN1 (+)	AIN1 (-)	Register pair 0
0	1	AIN2 (+)	AIN2 (-)	Register pair 1
1	0	AIN1 (-)	AIN1 (-)	Register pair 0
1	1	AIN1 (-)	AIN2 (-)	Register pair 2

table 8 TM7708 Channel selection

CH1	CH0	AIN	Benchmark	Calibration register pair
0	0	AIN 1	COMMON	Register pair 0
0	1	AIN 2	COMMON	Register pair 1
1	0	COMMON	COMMON	Register pair 0
1	1	AIN 3	COMMON	Register pair 2

12. Set the register

(RS2 , RS1 , RS0 = 0 , 0 , 1); Power-on/Reset state: 01Hex

The setting register is a 8 Bit register, it can both read data and write data. table 9 Instructions for setting each bit of the register.

table 9 Set the bits of the register

MD1 (0) MD0 (0) G2 (0) G1 (0) G0 (0) B/U (0) BUF (0) FSYNC (1)							

MD1	MD0	Working mode formula
0	0	Normal mode, in this mode, the converter performs normal analog-to-digital conversion
0	1	Self-calibration. In the communication register CH1 with CH2 The self-calibration is activated on the selected channel. This is one step Calibration, after completing this task, return to normal mode, namely MD1 with MD0 All 0 . When starting calibration DRDY Output pin or DRDY Bit is high level and returns to low level after self-calibration. According to the register, a new valid word is generated. Zero-scale calibration is a short circuit inside the input terminal (zero input) And the selected gain is completed; the full-scale calibration is internally generated under the selected gain V_{REF} Completed under selected gain conditions
1	0	Zero-scale system calibration. In the communication register CH1 with CH2 Activate the zero-scale system on the selected channel System calibration. During this calibration sequence, the input voltage on the analog input is completed at the selected gain calibration. During calibration, the input voltage should remain stable. When starting calibration DRDY Output or DRDY The bit is high level, and returns to low level after the zero-scale system calibration is completed. At this time, in the data register Generate a new valid word. At the end of the calibration, the device returns to the normal mode, that is MD1 with MD0 All 0
1	1	Full-scale system calibration: Activate full-scale system calibration on the selected input channel. When this calibration sequence When column, the input voltage on the analog input terminal is calibrated under the selected gain. During calibration, input The input voltage should remain stable. When starting calibration DRDY Output or DRDY The bit is high, and the full-scale system returns to low after the calibration is completed. At this time, a new valid data register is generated. word. At the end of the calibration, the device returns to the normal mode, that is MD1 with MD0 All 0

G2-G0 Gain selection bit. These bits are responsible for the on-chip PGA Gain setting, as table 10 .

table 10 Gain selection

G2	G1	G0	Gain setting
0	0	0	1
0	0	1	2

0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

B/U Unipolar/bipolar operation. " 0 "Indicates that bipolar operation is selected, " 1 "Indicates that unipolar operation is selected.

BUF Buffer control. " 0 "Means that the on-chip buffer is short-circuited. After the buffer is short-circuited, the power supply current decreases. This position At high level, the buffer is connected in series with the analog input, and the input allows processing of high impedance sources.

FSYNC Filter synchronization. When this bit is high, the node of the digital filter, filter control logic and calibration control The control logic is in the reset state, and at the same time, the analog modulator is also controlled in the reset state. When in low power Usually, the modulator and filter begin to process data, and 3 ×(1/ Output update rate) within (also Is the settling time of the filter) to produce a valid word. FSYNC Does not affect the digital interface, nor does DRDY The output is reset (if it is low).

13. Filter high register

(RS2 , RS1 , RS0 = 0 , 1 , 0); Power-on/Reset state: 05Hex

The filter high register is one that can read/write data 8 Bit register. table 11 The description of each bit of the filter high register.

table 11 filter Koyo Register

ZERO	ZERO	BST	CLKDIS	FS11	FS10	FS9	FS8

ZERO You must write zeros on these bits to ensure TM7707/8 Operate correctly. Otherwise, it will cause the device Non-specified operation.

BST The current is increased. This bit is 0 Will reduce the current drawn by the analog front end. Although this bit is 1 The device also works, but in order to reduce the AVDD The current drawn when the device is f_{CLKIN}= 1MHz or f_{CLKIN}= 2.4576MHz , Gain is 1 to 4 When working under circumstances, this bit should be 0. when TM7714 Working at gain 8 to 128 , f_{CLKIN}= 2.4576MHz Case, this bit must be 1 , To ensure the normal operation of the device. The power-on or reset state of this bit is 0 .

CLKDIS Main clock disable bit. logic" 1 "Means to prevent the master clock from MCLK OUT Output on the pin. When prohibited, MCLK OUT The output pin is at low level. This feature allows users to flexibly use MCLK OUT Pins, for example MCLK OUT As the clock source of other devices in the system, it can also be turned off MCLK OUT , So that the device has power saving performance. When MCLK IN Connect an external master clock, TM7707 /TM7708 Continue to maintain the internal clock, and in CLKDIS Normal conversion can still be performed when the bit is valid. When MCLK IN with MCLK OUT Connect a crystal oscillator or a ceramic resonator in between, when CLKDIS When the bit is valid, TM7707/8 The clock will stop and no analog-to-digital conversion will be performed.

13. Filter low register

(RS2 , RS1 , RS0 = 1 , 0 , 1) Power-on/reset state: 00Hex

The filter low register is one that can read/write data 8 Bit register. table 12 The description of each bit of the filter low register.

table 12 filter Low wave register

FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

Filter selection. On-chip digital filter provides Sinc 3 (or (Sinx/x) 3) filter response. Programming to these The 12-bit data determines the cutoff frequency of the filter and the data rate of the first-level device at the position of the first notch of the filter. Plus

On the gain selection, it can also determine the output noise (and effective resolution) of the device

The frequency at which the first notch of the filter occurs is determined by the following relationship:

Frequency of the first notch of the filter=(f_{CLKIN}/128)/code

Where code is the decimal equivalent of the code in bits FSO to FS11, and its range is 19 to 4000. Rated frequency at 2.4576MHz f_{CLKIN} Below, the frequency of the first notch ranges from 4.8 Hz to 1.01 kHz. To ensure the normal operation of TM7714, the code value loaded into these bits must be within this range. Failure to do so will result in uncertain device operation. Change filter

The gain selected for the notch frequency stage will affect the resolution (or effective conversion time) equal to the one selected for the first notch of the filter Frequency of. For example, if the first notch frequency of the filter is selected to be 50Hz, then new words can be used at a rate of 50Hz or new words are available every 20ms. If the frequency of the first notch is 1kHz, then a new word is available every 1ms.

For the full-scale step input change, the worst of the filter settling time is 4×1/(output data rate). For example, in When the first filter notch is 50Hz, the maximum settling time of the variable filter for the full-scale step input is 80ms. By synchronizing the step input change with the reset of the digital filter, the settling time can be reduced to 3×1/(output Data rate) . In other words, if the step output occurs with the SYNC input being low or the FSYNC bit is high, the settling time will be 3×1/ (output data rate) from the SYNC input being low or FSYNC returning low . If it happens If the channel changes, the device sends an internal SYNC command when requesting to change the channel, so regardless of the SYNC or FSYNC state, the settling time is 3×1/(output data rate)-3dB. The frequency is the first programmed according to the following relationship concave Frequency decision:

Filter -3dB frequency=0.262 × filter first notch frequency

14. Data register (RS2 , RS1 , RS0 = 0 , 1 , 1)

The data register is a twenty four Bit read-only register, it contains data from TM7707/8 The latest conversion result. If the communication register sets the device to write to this register, a write operation must actually occur to make the device Return to the write operation to the communication register, but write to the device twenty four Digits will be TM7707/8 ignore.

15. Test register

(RS2 , RS1 , RS0 = 1 , 0 , 0); Power-on/Reset state: 00 Hex

The test register is used when testing the device. It is recommended that users do not change the default value of any bit of the test register (power on Or automatically set the full 0) Otherwise, when the device is in the test mode, it will not operate correctly.

16. Zero-scale calibration register

(RS2 , RS1 , RS0 = 1 , 1 , 0); Power-on/Reset state: 1F4000 Hex

TM7707/8 Contains several groups of independent zero-scale registers, and each zero-scale register is responsible for one input channel. it We are all twenty four Bit read/write register, twenty four The bit data must be written before it can be transferred to the zero-scale calibration register. The zero-scale register and the full-scale register are connected together to form a register pair. Each register pair corresponds to a pair of channels, see table 7 . When the device is set to allow access to these registers through the digital interface, the device itself no longer accesses the register coefficients So that the output data has the correct scale. As a result, after accessing the calibration register (whether it is a read/write operation), the slave device The first output data read may contain incorrect data. In addition, during data calibration, the calibration register cannot be Write operation. This kind of event can be avoided by the following method: Before the calibration register starts to work, set the mode register FSYNC The position is high, after the task is over, set it to low again.

17. Full-scale calibration register

(RS2 , RS1 , RS0 = 1 , 1 , 1); Power-on/Reset state: 5761AB Hex

TM7707/8 Contains several independent full-scale registers, each full-scale register is responsible for one input channel. it We are all twenty four Bit read/write register, twenty four The bit data must be written before it can be transferred to the full-scale calibration register. The full-scale register and the zero-scale register are connected together to form a register pair. Each register pair corresponds to a pair of channels, see table 7 . When the device is set to allow access to these registers through the digital interface, the device itself no longer accesses the register coefficients So that the output data has the correct scale. As a result, after accessing the calibration register (whether it is a read/write operation), the slave device The first output data read may contain incorrect data. In addition, during data calibration, the calibration register cannot be Write operation. This kind of event can be avoided by the following method: Before the calibration register starts to work, set the mode register FSYNC The position is high, after the task is over, set it to low again.

18. Calibration process

As mentioned earlier, TM7707/8 Includes many types of calibration, table 13 Summarized these calibration types, operation content and operation time. There are two ways to judge whether the calibration is over. The first method is: monitoring DRDY If DRDY Return to low level, indicating that the calibration process has ended, and it also indicates that there is a new valid data in the data register. The new data is a normal conversion result after calibration. The second method is: monitor the setting register MD1 , MD0 Bit if MD1 , MD0 Back to " 0 " (After calibration, MD1 , MD0 return" 0 ") , It means calibration The process has ended, this method cannot prompt whether there is a new conversion result in the data register, but it is better than the first judgment method To be early in time, that is, to know faster whether the calibration is over. Mode Bit (ie MD1 , MD0)return" 0 The duration before "is shown in the table 13 As shown, DRDY The process of returning to low level includes a normal conversion time and **One** Delay time with correct scale for second conversion result t_P, t_P No more than 2000 X t_{CLKIN} . The time required for these two judgment methods is as follows.

table 13 Calibration process

Calibration type	MD1, MD0	Calibration sequence	Time to set mode	Set DRDY of time
Self-calibration	0 , 1	Internal zero-scale calibration@选 Constant gain+ Internal full scale calibration@选 Constant gain	6 X 1/ Output frequency	9 X 1/ Output frequency Rate+ t_P
Zero-scale system calibration	1 , 0	use AIN Zero scale Calibration @ selected gain	3 X 1/ Output frequency	4 X 1/ Output frequency Rate+ t_P
Full-scale system calibration	1 , 1	use AIN Full scale Calibration @ selected gain	3 X 1/ Output frequency	4 X 1/ Output frequency Rate+ t_P

19. Circuit description

TM7707/8 Is an on-chip digital filter Σ- ΔA/D The converter is designed for the conversion of low-frequency signals in wide dynamic range measurement, industrial control or process control. It includes a Σ- Δ (Or charge balance) ADC , Static on-chip RAM The calibrated microcontroller, clock oscillator, digital filter and a two-way serial communication port. The device The supply current of the device is only 320 μ A , Making it ideal for battery-powered instruments. The device has two optional electrical The source voltage ranges are 2.7 ~ 3.3V or 4.75 ~ 5.25V .

TM7707 include 2 A programmable gain fully differential analog input channel, TM7708 include 3 A pseudo-differential analog input channel. The selectable gain of the input channel is 1 , 2 , 4 , 8 , 16 , 32 , 64 with 128 , When the reference input voltage is 2.5V

Allow the device to accept 0mV~+20mV with 0V~+2.5V Unipolar signal between or ±20mV to ±2.5V Within range Bipolar signal. The reference voltage is 1.225V When, in unipolar mode, the input range is 0mV~+10 mV to 0V~±1.225V , In bipolar mode, the input range is ±10mV~±1.225V . Description: Yes TM7707 Bipolar The sexual input range is relative to AIN (-), yes TM7708 Relative to COMMON Instead of right GND of.

The signal input to the analog input terminal is continuously sampled, and the sampling frequency is determined by the main clock MCLK IN Frequency and selected increase Benefit decision. Charge balance A/D Conversion (Σ- Δ Modulator) converts the sampled signal into a digital with a duty cycle containing digital information Pulse chain. Programmable gain function coordination of analog input Σ- Δ Modulator, modify the input sampling frequency to obtain higher gain. $Sinc^3$ Low-pass digital filter processing Σ- Δ The output of the modulator updates the output register at a certain rate, which is determined by the frequency of the first notch of the filter. Output data can be read randomly or periodically from the serial port

The read rate can be any value that does not exceed the update rate of the output register. The first notch frequency of the digital filter (in and- 3dB Frequency) can be set by the register FS0 with FS1 Programming. When the frequency of the main clock is 2.4576MHz Time, The programmable range of the first notch frequency is 50Hz~500Hz ,- 3dB The frequency range is 13.1Hz~131Hz . Master clock Frequency is 1 MHz , The programmable range of the first notch frequency is 20Hz~200Hz ,- 3dB The frequency range is 5.24Hz~52.4Hz .

Figure 10 Yes TM7707 The basic connection circuit diagram, as shown in the figure, the analog voltage is + 5V ; Precision+ 2.5V The reference voltage AD780 Provide a reference source for the device. On the digital signal side, the device is configured for three-wire operation, CS Ground. Quartz crystal or ceramic resonator provides the main clock source. In most cases, it is necessary to connect an electric The container ensures that there is no oscillation at the overtone of the basic operating frequency. The capacitance value of the capacitor varies with the manufacturer's requirements. This configuration also applies to TM7708 .

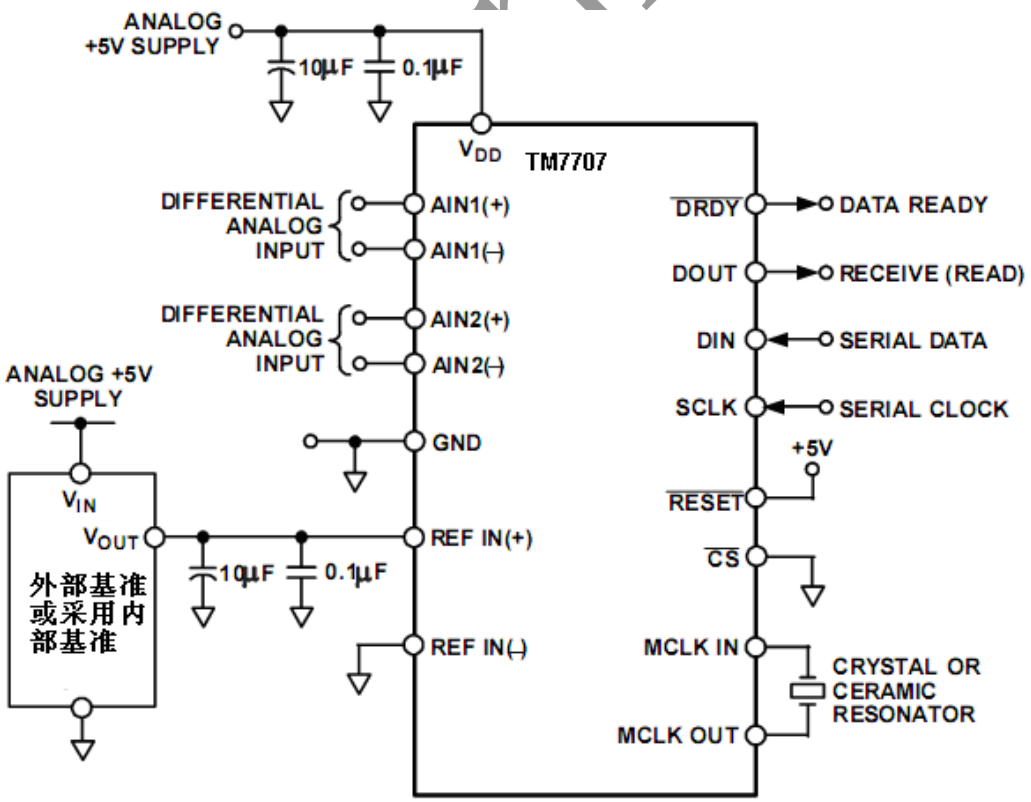


Figure 10 TM7707 The basic connection circuit diagram

Twenty, analog input

TM7707 include 2 Analog input pairs, namely AIN (+), AIN (-)with AIN2 (+), AIN2 (-). lose

The input pair provides a differential input channel with programmable gain and can handle unipolar and bipolar input signals. It should be noted that the bipolar input signal With their respective AIN The (-) end is for reference. TM7707 include 3 Two pseudo-differential analog input pairs, AIN 1 , AIN2 with

AIN3 , These inputs are COMMON The input is for reference.

In unbuffered mode, the common mode input range is from GND To V_{DD} . The absolute value of the analog input voltage is at GND-30mV with V_{DD+} 30mV between. This shows that the device can handle unipolar and bipolar input signals of all gains. 25 At ℃, the analog input can reach absolute voltage without degrading performance GND-200mV , But leakage current (leakage -current) Increases significantly with temperature rise. In buffer mode, the analog input can handle more power Source impedance, but the absolute input voltage range is limited to GND+50 mV To V_{DD+} 30mV Between, it also limits the common mode output 入range. This means that in buffer mode, the allowable gain of the bipolar input range is limited. Must be carefully set Mode voltage and input voltage range to ensure that they do not exceed the above limits, otherwise, the linear performance of the device will be degraded.

In unbuffered mode, the analog input is directly connected 7pF Sampling capacitor, C_{SAMP} . The maximum value of DC input leakage current is 1nA . As a result, a dynamic load converted at the input sampling rate is connected to the analog input (see figure 11). The sampling rate depends on the master clock frequency and the selected gain value. In each input loop, C_{SAMP} by AIN (+) Charge and then AIN (-) Discharge. Effective on-resistance of the switch (R_{SW}) Is typically 7kΩ .

Every input sampling period, C_{SAMP} Must pass R_{SW} And external power supply impedance for charging. So in unbuffered mode Next, the source impedance means the C_{SAMP} Longer charging time, which may cause gain errors of the device. table 14 Non-Allowable external resistance/capacitance value in buffer mode. Note: The capacitance value in the table is the external capacitance value plus the device pin and Pin holder 10 pF The sum of capacitance.

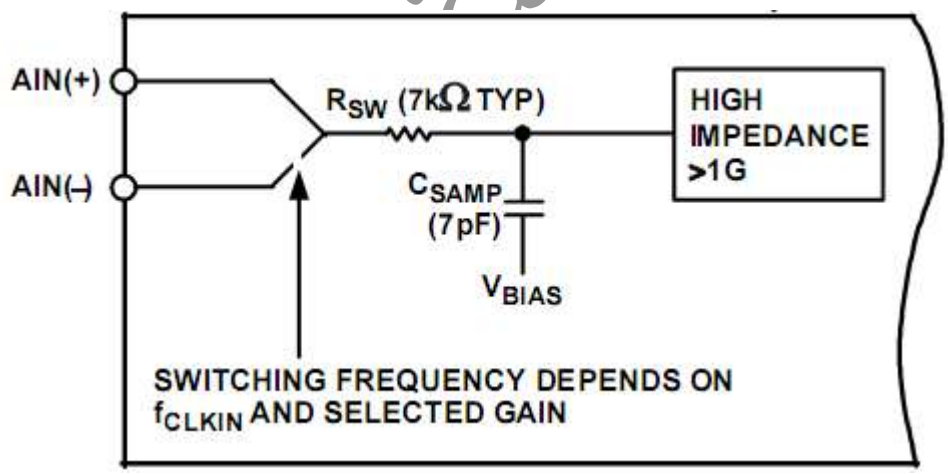


Figure 11 Unbuffered analog input structure

table 14 no 16 External resistance and capacitance value for bit gain error (unbuffered mode)

增益	外部电容（pF）					
	0	50	100	500	1000	5000
1	368kΩ	90.6kΩ	54.2kΩ	14.6kΩ	8.2kΩ	2.2kΩ
2	177.2kΩ	44.2kΩ	26.4kΩ	7.2kΩ	4kΩ	1.12kΩ
4	82.8kΩ	21.2kΩ	12.6kΩ	3.4kΩ	1.94kΩ	540kΩ
8-128	35.2kΩ	9.6kΩ	5.8kΩ	1.58kΩ	880kΩ	240kΩ

In the buffer mode, the high-impedance input stage of the on-chip buffer amplifier is seen from the analog input terminal. C_{SAMP} Pass buffer

The amplifier is charged so that the power supply impedance does not affect C_{SAMP} Charging. Buffer amplifier has 1nA The offset leakage current. In this buffer

mode, a large power supply impedance will cause a small DC offset voltage, but will not cause gain errors.

21. Input sampling rate

TM7707/8 The sampling frequency of the modulator is maintained at f_{CLKIN}/ 128(19.2kHz Time, f_{CLKIN}= 2.4576MHz) ,and

It has nothing to do with gain selection. However, greater than 1 The gain is achieved by multiple input sampling and reference in each modulator cycle

The multiple of the ratio of the capacitance to the input capacitance, which is a combination of the two. As a result of multiple sampling, the input sampling rate varies with the selected

Gain changes (see table 15). In buffer mode, the input terminal has been buffered before it is connected to the input sampling capacitor.

In unbuffered mode, the analog input terminal is directly connected to the sampling capacitor, and the effective input impedance is $1/C_{SAMP}$ X f_S. C_{SAMP}

Is the input sampling capacitor, f_S Is the input sampling rate.

table 15 The relationship between input sampling frequency and gain

增益	输入采样频率
1	$f_{CLKIN}/64$(38.4kHz @ f_{CLKIN}=2.4576MHz)
2	2 × $f_{CLKIN}/64$(76.8kHz @ f_{CLKIN}=2.4576MHz)
4	4 × $f_{CLKIN}/64$(76.8kHz @ f_{CLKIN}=2.4576MHz)
8-128	8 × $f_{CLKIN}/64$(307.2kHz @ f_{CLKIN}=2.4576MHz)

22. Unipolar/bipolar input

Whether it is unipolar or bipolar voltage, TM7707/7708 All analog inputs are acceptable. Bipolar input and

It does not mean that the device can handle the negative voltage at the analog input terminal, because the analog input voltage cannot be less than- 30mV To ensure that the device

Works normally. The input channel is fully differential. Therefore, for TM7707 , AIN(+) The input voltage is AIN 1(-)

As a benchmark; for TM7708 , The voltage applied to the analog input channel is COMMON As a benchmark. For example, if AIN

1(-)=2.5V , Unipolar input, gain is 2 , $V_{REF=+}$ 2.5V, Then AIN 1(+) The input voltage range of the terminal is

+ 2.5~+3.75V If AIN 1 (-)=+2.5V , TM7707 Configured as bipolar input, the gain is 2 , $V_{REF=+}$ 2.5V , Then AIN 1(+) The analog input voltage range of the terminal is + 1.25~+3.75V (That is 2.5V ± 1.25V). Selection list

Polarity or bipolar input is determined by the setting register B /U To decide. Whether in unipolar or bipolar output

It does not change the state of any input signal, it only changes the code of the output data and the calibration on the conversion function.

on time.

Twenty-three, reference input

REFIN (+) and REFIN (-)for TM7707/8 Provide differential reference input function, common mode range of differential input

Surrounding is GND~V_{DD} . when TM7707/8 To 5V When the power supply voltage is working, the reference voltage is + 2.5V ; The power supply voltage is 3V , The reference voltage is + 1.225V . when V_{REF} Down to 1V Time, TM7707/8 It can still work, but as the performance decreases, the output noise will become larger. In order to ensure that the device can work accurately, it must be used REFIN (+) greater than REFIN (-).

Similar to the analog input in unbuffered mode, both reference inputs provide high impedance and dynamic loads. Throughout Within the temperature range, the maximum value of the DC input current is ±1nA At this time, the power supply resistance may cause the gain error of the device. In this case, the sampling switch resistance is typically 5kΩ , And the reference capacitor (C_{REF}) Varies with gain. Benchmark The incoming sampling rate f_{CLKIN}/ 64 And does not change with the gain. Gain is 1 with 2 Time, C_{REF} for 8pF ; Gain is 16 Time, C_{REF} for 5.5 pF ; When the gain is 32 Time, C_{REF} Yes 4.25pF ; Gain is 64 Time, C_{REF} for 3.625pF ; And when the gain reaches 128 Time, C_{REF} for 3.3125 pF .

table 1 To 4 The analog input signal listed is 0V The output noise characteristics at the time, it effectively eliminates the reference noise Impact. In the entire input range, in order to obtain the noise characteristics as shown in the noise table, TM7707/ TM7708 Configure a low noise reference source. If the reference noise in the bandwidth is too large, TM7707/8 The performance will be reduced. When the power supply voltage is 5V 时，为 TM7707 Recommended reference voltage sources include AD780 , REF43 , REF192 ; When the electricity The source voltage is 3V When the recommended reference voltage source includes AD589 with AD1580 . To further reduce noise, it is usually recommended to decouple these reference voltage outputs.

twenty four, TM7707/8 Use of internal benchmarks

TM7707/8 series ADC You can choose to use an external reference voltage or an internal reference voltage.

(1) When using an external reference voltage, just press the pin REFIN(+) with REFIN(-) Connect the rules A fixed voltage will do.

(2) When using the internal reference voltage, the pin REFIN(+) Access to internal benchmarks, plus 104p The capacitor is grounded, REFIN(-) It needs to be grounded externally, and it is done by software writing instructions.

in TM7707/8 , Just write to the test register 01H Command, the internal reference will work, the typical value of the internal reference 2.48V .

Precautions for using internal reference voltage:

To make the internal benchmark work, you must write instructions first.

When the following three situations occur, the command becomes invalid, and the command needs to be rewritten before the internal reference will work again.

a. A power-on reset occurred.

b. Reset pin (pin 5)effective.

c. at least 32 Write logic to the serial port continuously within one serial clock cycle " 1 "To reset the serial interface.

Twenty-five, digital filtering

TM7707/8 Contains an on-chip low-pass digital filter to process the device's Σ- Δ The output signal of the modulator. Therefore, the device not only provides analog-to-digital conversion functions, but also has certain filtering capabilities. Digital filter and analog filter memory In many system differences, users must pay attention.

On the one hand, digital filtering occurs after the analog-to-digital conversion, which can eliminate the noise generated during the analog-to-digital conversion process. Quasi-filtering cannot do this. In addition, digital filtering is easier to achieve programmability than analog filtering. Rely on digital filters Design, the user can program the cutoff frequency and output update rate.

On the other hand, when the analog signal enters ADC Previously, analog filtering was able to eliminate noise superimposed on analog signals, Digital filtering cannot do this, and when the peak of noise parasitic on the signal is close to full scale, even the average signal Values in the limit range may also cause the analog modulator and digital filter to reach saturation. In order to solve this problem, TM7707/8 of Σ- Δ Inside the modulator and digital filter, a peak reserve is established, which allows to exceed the analog input range

Surround 5% . If the noise signal is larger than this, then you have to consider analog filtering at the input end, or reduce the input channel voltage,

Make the input voltage range half of the full-scale range of the analog input channel voltage. In this way, the dynamic range is reduced 50% ,will

Increase over-range performance 1 Times.

26. Filter characteristics

TM7707/8 The digital filter is a low pass (sinx/x)$_3$ Filter (also called sinc$_3$),Its Z The conversion function of the domain can be described as:

$$H(z)=\left|\frac{1}{N}\times\frac{1-Z^{-N}}{1-Z^{-1}}\right|^3$$

在频域可描述为:

$$H(f)=\left|\frac{1}{N}\times\frac{SIN(N\times\pi\times f/f_S)}{SIN(\pi\times f/f_S)}\right|^3$$

Here, N It is the ratio of modulation rate to output rate.

Phase response:

$$\angle H=-3\pi(N-2)\times f/f_S \text{ Rad}$$

Figure 4 Is the cutoff frequency 15.72Hz The frequency response of the filter at time, this frequency and the first notch frequency of the filter (60Hz)correspond.

This curve shows from DC to 390Hz . This frequency is on both sides of the sampling frequency of the digital filter

The curves repeat each time. This filter response is similar to that of an average filter. The output rate of the digital filter and the first

The positions of the two notches correspond. Therefore, in the figure 12 The output rate in is 60Hz , The frequency of the first notch of the filter is 60Hz . This (sinx/x

)$_3$ The notch position of the filter is repeated many times at the multiple of the first notch. The filter provides greater than 100dB The attenuation. The cutoff

frequency of the digital filter is determined by the clock register FS0 with FS1

Bit decision. by FS0 with FS1 Programming different cutoff frequencies does not change the shape of the filter response, it only changes the notch

Frequency of. The output update rate of the device corresponds to the frequency of the first notch.

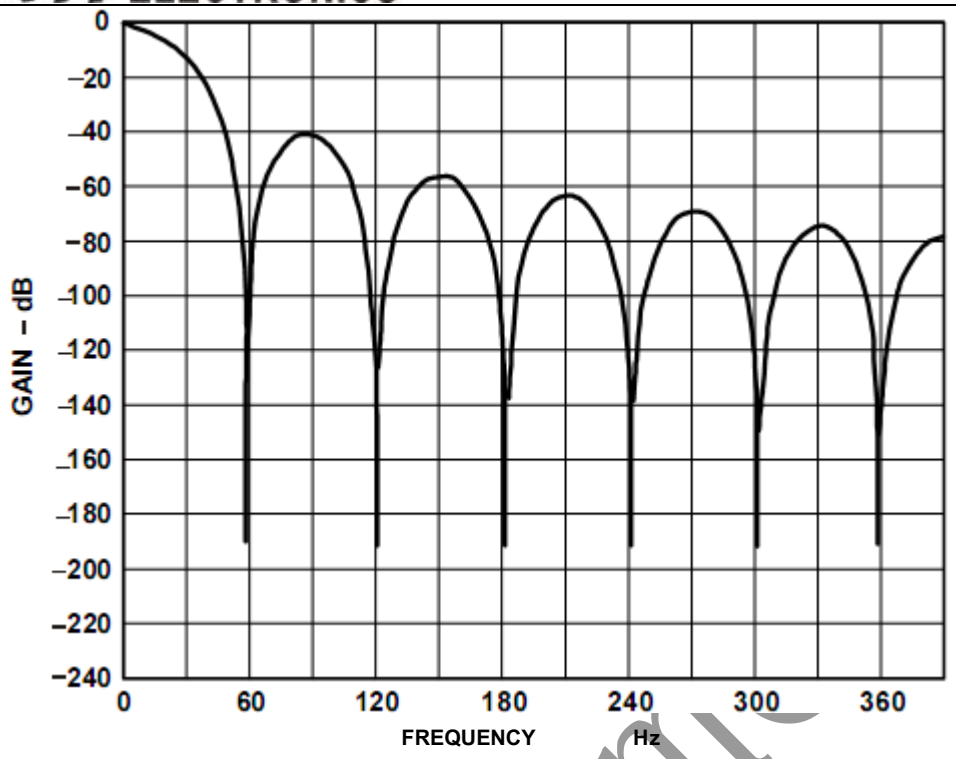


Figure 12 TM7707 The frequency response of the filter

due to TM7707/8 Including this on-chip low-pass filter, its settling time is related to the input step function, and the output The data is not valid until the stabilization time has elapsed. The settling time depends on the output rate selected for the filter. Full scale step The settling time of the filter at input can be as high as four times the output data period. For synchronous step input (use FSYC Function) Settling time is the period of output data 3 Times.

27. Post filtering (post-filtering)

when f_{clkin} for 2.4576 MHz When the on-chip modulator provides 19.2kHz The sampling output rate. Then, the on-chip digital filter samples these samples to provide data at a certain output rate. Because the output rate is better than Nyguist The standard is high, so for applications with a given bandwidth and noise performance, this output rate can meet most application requirements. begging. But for some special applications that require a higher output rate for a given bandwidth and noise performance, TM7707/8 Configure the post-filtering function after the digital filter. For example, if the bandwidth requirement is 7.86Hz , And the required update rate is 100Hz ; Then because when the data output rate is 100Hz Given when- 3dB Bandwidth is 26.2Hz . Post filtering can be applied to this occasion, it can reduce the bandwidth to 7.86Hz , While reducing the output noise, while maintaining The output rate is still 100Hz . Post filtering can also be used to reduce bandwidth less than 13.1Hz The output noise generated by the device, the gain is 128 , The bandwidth is 13.1Hz When, the root mean square value of the output noise is 450nV . This is the main noise of the device, that is, white noise, and because the input is clipped, the noise has a flat frequency response. By reducing the bandwidth to below 13.1Hz , The noise in the final passband will be reduced. Bandwidth 2 A reduction in multiples of will result in output noise (rms) To be close to 1.25 The multiple decreases. This additional post-filtering makes the settling time longer.

Twenty-eight, analog filtering

As mentioned earlier, the digital filter cannot suppress the integral multiple of the modulator sampling frequency. But because TM7707/8 Oversampling rate (oversampling ratio), these bands only occupy a small part of the entire frequency spectrum, and most of the broadband noise is filtered out. This means that compared to traditional converters without on-chip filtering, TM7707/8 Front end Analog filtering requirements have been greatly reduced. In addition, due to the device's 100dB The common mode rejection has reached the number kHz , This frequency

The noise within the range will be greatly reduced. However, in specific applications, it may be necessary to eliminate the frequency band that the digital filter can pass. In addition to unnecessary frequencies, TM7707/8 Add attenuation function to the front end; in other applications, it may be TM7707/8 The front end of the device performs analog filtering to prevent the differential noise signal outside the useful frequency band from saturating the analog modulator.

In non-buffered mode, if TM7707/8 Passive components are installed in the front end of the device, and the power supply impedance must be sufficiently low, So as not to introduce gain error in the system. This greatly limits TM7707/8 Front end passive anti-aliasing filtering (passive antialiasing filtering) Use in non-buffered mode. But when the device works in buffer mode, the large power supply The resistance will only produce a small DC offset error (10kΩ Power supply resistance cannot cause 10 μ V Offset error) . therefore, If the system needs to be TM7707/8 The front end uses passive analog filtering, and it is recommended to make the device work in buffer mode.

Twenty-nine, calibration

TM7707/8 Provides a variety of calibration options, which calibration can be selected by setting the register MD1 with MD0 Bit to program. Once given MD1 with MD0 Bit write data, a calibration cycle begins. Eliminate offset and gain errors generated on the device through calibration. When the working environment temperature and voltage change, the device should be calibrated routinely, If the selected gain, filter notch or unipolar/bipolar input range changes. Calibration should also be performed.

Calibration is divided into self-calibration and system calibration. When performing global calibration on the selected channel, the on-chip microcontroller must be Record the output of the modulator under different input states, that is " Zero scale " with " Full scale " point. These points are calibrated During the process, after inputting different voltage values at the input of the modulator, the device performs a conversion and the result is obtained. Of course, school The quasi-accuracy can only be comparable to the noise level provided in the normal mode. The result of the zero-scale calibration conversion is stored in the zero-scale calibration The full-scale calibration conversion result is stored in the full-scale calibration register. Relying on these data, the microcontroller The offset and gain slope of the converter's input-output transfer function can be calculated. The device is 33 Bit resolution to determine 16 Bit conversion result.

Thirty, self-calibration

By setting the register MD1 with MD0 Write the corresponding value (0 , 1), the device starts self-calibration. In the range of unipolar input signal, the zero-scale point used to determine the calibration coefficient is short-circuited inside the device with the input terminals of the differential input pair (Ie, for TM7707 , AIN (+)= AIN (-) = internal bias voltage; for TM7708 , AIN = COMMON = Internal bias voltage). Gain programmable amplifier (PGA) Set to the gain selected for zero-scale calibration conversion (From the communication register G1 with G0 Bit setting). Full scale standard conversion is generated internally V_{REF} Completed under the conditions of voltage and selected gain. The calibration duration is 6 X 1/ Output rate. It is calibrated by zero scale and full scale of 3 X 1/ The sum of output rate time. After the calibration is complete, MD1 with MD0 Automatically return to the initial value (0 , 0), this is the earliest indication of the end of the calibration process. When the calibration starts, DRDY At high level until there is a new Valid data, DRDY Before returning to low level, DRDY The duration of this process from high level to low level is 9 X 1/ Output rate, where the zero-scale calibration time, the full-scale calibration time and the time for setting the calibration coefficient are each 3 X 1/ Output rate. So, in terms of time, MD1 with MD0 The calibration completion prompt given is more than DRDY Bit early 3 X 1/ Output rate. in case DRDY It is at a low level before the calibration command is written into the setting register, it may take an extra modulation cycle time, DRDY Can be changed to high level, which shows that the calibration has started, therefore, in the most After the next byte is written into the setting register, you can DRDY Ignore it.

For the self-calibration of the bipolar input range, the whole process is similar to the above process. The zero-scale and full-scale points are almost the same as single-scale points. The polarity input is the same, but because TM7707/8 It is configured to work with bipolar input, the input point range is shortened, and the actual The above is in the middle area of the conversion function.

31. System calibration

Through system calibration, TM7707/8 It can compensate for system gain, offset error and internal error of the device itself

Compensation. System calibration performs the same slope coefficient calculation as self-calibration, but the voltage value used is the system AIN Input for The voltage value for zero and full scale calibration.

The whole process of system calibration is carried out in two steps, the first is ZS System calibration, then proceed FS System calibration. For a whole system calibration, the zero-scale point must be sent to the converter first at the beginning of the calibration, and it must be kept stable and straight. To the end of calibration.

ZS System calibration

Once the zero-scale voltage value of the system is set, pass to the setting register MD1 with MD0 Write (1 , 0) ,on Start ZS System calibration. The zero-scale system calibration is performed at the selected gain. The duration of zero-scale calibration is 3 X 1/ Output rate. During the calibration process, MDO with MD1 as well as DRDY The change in the self-calibration is the same like. However, from the calibration command to DRDY The time required to become low is 4 X 1/ Output rate

FS System calibration

After zero-scale point calibration, apply the full-scale voltage value to AIN End, then to MD1 with MD0 Write separately (1 , 1), FS The system calibration begins. Similarly, before the calibration starts, the full-scale voltage value must be set, and Keep it stable during the calibration process. During the calibration process, MDO with MD1 as well as DRDY The process of change is the same as ZS System calibration process.

In unipolar mode, the system calibration is completed between the two endpoints of the transfer function; in bipolar mode, it is It is done between mid-scale (zero differential voltage) and positive full-scale.

The system calibration is carried out in two steps. After the calibration sequence of the whole system has been completed, the offset and gain calibration can be automatic Execute to adjust the system zero reference point or system gain. Calibrate any one of the two parameters of the system offset or gain, without Affect another.

When the device is used in unbuffered mode, system calibration can also be used to eliminate the analog input terminal introduced by the power impedance Any errors. A simple analog front end R , C The anti-overlap filter may introduce gain errors in the analog input voltage, But system calibration can eliminate this error.

32. Limitation of input range and offset

Whenever the system calibration mode is applied, the offset and input voltage range are always limited. And determine the offset and adjustable The main requirement for the gain range of the section is: the maximum value of the positive full-scale input voltage < 1.05 ×$V_{DEF/}$ GAIN , Which can make the input voltage limit value higher than the rated value 5% . TM7707/8 The maximum tolerance of the analog modulator (headroom) Ensurer The voltage exceeds the rated voltage 5% It can still work normally.

In unipolar/bipolar mode, the minimum value of the input range is 0.8 X $V_{REF/}$ GAIN , The maximum value is 2.1 X $V_{REF/}$ GAIN , But this range has to consider the limit value of positive full scale. The adjustable offset depends on whether the device uses a single Polar mode is still bipolar mode. Similarly, the offset must consider the limit value of the positive full scale. In unipolar mode, negative bias There is considerable flexibility in moving. When selecting the limit values of the zero-scale and full-scale of the system, you must ensure that the offset and the input range The sum of the surroundings does not exceed 1.05 X $V_{REF/}$ GAIN . The best illustration on this point is to look at the following examples.

If the device is used in unipolar mode, the required input range is 0.8 X $V_{REF/}$ GAIN , The offset range that can be set for system calibration is from- 1.05 X $V_{REF/}$ GAIN To + 0.25 X $V_{REF/}$ GAIN . If the device is used in unipolar mode, the required input range is 1 X $V_{REF/}$ GAIN , The offset range that can be set for system calibration is- 1.05 X $V_{REF/}$ GAIN to 0.05 X $V_{REF/}$ GAIN . Similarly, if the device is used in unipolar mode and requires removal of 0.2 X VREF/GAIN , The system calibration can set the input range to 0.85 X $V_{REF/}$ GAIN .

If the device is used in bipolar mode, the required input range is ±0.4 ×$V_{REF/}$ GAIN , The system calibration can be set The offset range is from- 0.65 ×$V_{REF/}$ GAIN To + 0.65 ×$V_{REF/}$ GAIN . If the device is used in bipolar mode, you need The input range is 鑫 $_{REF/}$ GAIN , The offset range that can be set for system calibration is from- 0.05 ×$V_{REF/}$ GAIN To + 0.05 ×$V_{REF/}$ GAIN . Similarly, if the device is used in bipolar mode, it is required to remove ±0.2 ×$V_{REF/}$ GAIN Offset,

Then the system calibration can set the input range to ±0.85 ×V_{REF} / GAIN .

Thirty-three, power on and calibration

When powering up, TM7707/8 Reset internally, that is, set the internal register to a known state. After power-on or reset, All registers return to the default value state. The default value includes the nominal calibration coefficient of the calibration register. To ensure TM7707/ TM7708 The correct calibration should be performed routinely after power-on.

TM7707/8 The power consumption and temperature drift are very low, and there is no need to warm up before the initial calibration. But if you use The external reference must be stabilized before the calibration starts. Similarly, if TM7707/8 The clock signal is composed of two MCLK If it is generated by a crystal or ceramic resonator between the pins, the oscillator should be started before the calibration starts.

See picture 14 .

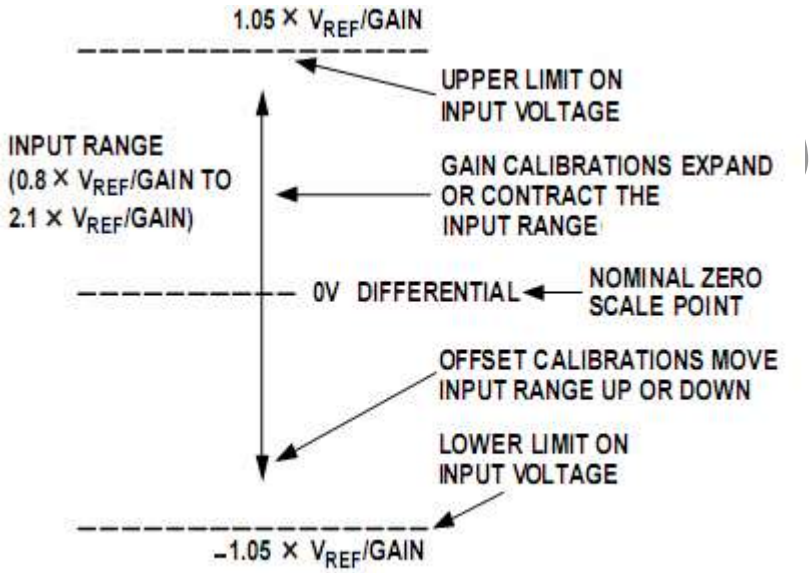


图13　　输入范围和偏移的限制

Thirty-four, TM7707/8 usage of

Clock and oscillator circuit

TM7707/8 Requires external main clock input, this main clock input can be MCLK OUT When the feet are not connected, add in MCLK IN An external on the pin CMOS Compatible with clock signals, or, in MCLK IN with MCLK OUT Connect a crystal or ceramic resonator with a suitable frequency between the two pins. In this case, the clock circuit works as an oscillator For TM7707/8 Provide the master clock signal. Master clock frequency f_{CLKIN} Directly affect the input sampling frequency, modulator sampling frequency,- 3dB Frequency, output update rate and calibration time. If the main clock frequency is reduced by half, input the sampling frequency, modulation Sampling frequency,- 3dB The frequency and output update rate will be reduced by half, and the calibration time will be doubled. In addition, the power supply Flow also with f_{CLKIN} Related, the main clock frequency is reduced by half, and the power supply current of the digital part will be reduced by half, but it will not affect the communication. The current through the analog circuit.

in MCLK IN with MCLK OUT Configure a crystal or ceramic resonator between two pins MCLK IN The working current of the driving clock signal introduced at the pin is large. This is because the on-chip oscillator circuit is using crystal or ceramic resonance Is more active in the case of the device. Thus, in MCLK IN An external clock is applied to the pin, and the MCLK OUT When the pin is vacant and no load is applied, the TM7707/8 Reach the smallest possible current value.

The amount of extra current consumed by the oscillator depends on many factors. MCLK IN with MCLK OUT Capacitor between two pins (C1 with C2) The larger the capacitance, the larger the current consumption. Be careful not to exceed the crystal or ceramic resonance The capacitor value recommended by the device manufacturer, these values are generally 30pF to 50pF Within range. Another influencing factor is crystalline ESR

Value, general, ESR The lower the value, the lower the current consumption.

The main clock frequency is 2.4576MHz, The power supply voltage is 3V When using a crystal or ceramic resonator as the oscillation circuit, the current required is larger than when using an external clock 50μ A ; The main clock frequency remains unchanged, and the power supply voltage is 5V Time, the former required typical current value increased 250μ A . At this frequency, the crystal/ceramic resonator ESR The value is small, and the difference between different crystals and resonators is small.

When 1MHz When working at the clock frequency, different crystal types correspond to ESR The values vary greatly. Therefore, no The current consumed by the same crystal type is different. V_{DD} = 3V When, use ESR for 700Ω Crystal/ceramic resonator ratio The clock consumes a lot of current 20 μ A , V_{DD} = 5V Time, more 200 μ A ; When using crystal ESR=3000Ω Time, V_{DD} = 3V Time and V_{DD} = 5V When the corresponding current increase value is 100 μ A with 400μ A .

Before the oscillation circuit starts to oscillate, it needs a start-up process. V_{DD} = 5V , The frequency of the crystal oscillator is 4.9512 MHz , 2.4576MHz with 1MHz The corresponding start times are 6ms , 16 ms with 20 ms . V_{DD} Reduced to 3V At the same frequency, the start-up time is shortened 20% .

The power supply voltage is 3V When, according to MCLK IN The load capacitance at the pin can be connected across the crystal or resonator One 1MΩ Resistance to keep the start-up time at approximately 20ms about.

TM7707/8 The master clock can be from MCLK OUT Pin leads, the maximum recommended load on this pin is one CMOS load. When a crystal or ceramic resonator is used to generate a clock signal, it may be necessary to use this clock as the system time Zhong Yuan. In this case, it is recommended to use CMOS Buffer pair MCLK OUT The signal is buffered before being added to the system circuit.

35. System synchronization

Set the register FSYNC Allow users to not affect TM7707/8 In the setting state, reset the modulator and digital filter. This allows the user to collect samples of the analog input from a known point in time, that is when FSYNC Position slave 1 Changed to 0 Time.

FSYNC Set 1 When the digital filter and analog modulator are in a known reset state, at this time TM7707/8 No input samples are processed. When will 0 Write in FSYNC , The modulator and filter are no longer in the reset state, TM7707/8 Start collecting samples from the next clock edge again.

FSYNC The input can also be used as a software-initiated conversion command that allows the device to work in normal conversion mode. In this kind of In mode, data write FSYNC , The conversion starts, DRDY The falling edge indicates that the conversion is complete. The disadvantage of this scheme is that, The data update of each data register must consider the settling time of the filter, therefore, the update rate of the data register must slow 3 Times.

due to FSYNC Reset the digital filter, so before a new word is written into the output register, the entire stabilization time It must end. in case FSYNC for 0 Time, DRDY At low level, FSYNC Command will be wrong DRDY Reset to make it high. This is because there is an unread word in the data register. Before the data register is updated, DRDY The line will remain low. DRDY The line will stay low until the data register is updated, at which time it will Becomes high 500 X t_{CLKIN} Then go back to low level. Reading data from the data register will make DRDY The signal goes high until the settling time of the filter has elapsed (from FSYNC After the command) and there is a valid word in the data register, DRDY Just return to low. If FSYNC When the command has been issued DRDY Line is high, then DRDY The line cannot return to the low level until the settling time of the filter has elapsed.

36. Reset input

The reset input circuit resets all logic, digital filters and analog modulators, and sets all on-chip registers To its default state. when RESET When the input signal is at low level, DRDY At high level, TM7707/8 Ignore any communication data sent to the register. when RESET After returning to high level, the device starts to process data. after 3 ×1/ lose

After the rate of time, DRDY Return low to indicate that there is a new valid word in the data register. After reset,

The device works in the default state, generally, once RESET After the command, you need to set all the registers and perform a

Calibration.

even if RESET When the input is at low level, the on-chip oscillator circuit continues to work, MCLK OUT The main clock signal of the pin continues to be valid. Therefore, by TM7707/8 In the application that provides the system clock, TM7707/8 During the reset process, an uninterrupted master clock signal is generated.

37. Waiting mode

Without the need to provide conversion results, the communication register STBY Bit allows the user to set the device

Work in electrical mode. In waiting mode, TM7707/8 Keep all on-chip registers (including data registers)

There is content. After leaving the wait mode, the device begins to process data, STBY Bit write 0 of 3 ×1/ After the output rate time, there may be new valid data in the data register.

STBY Bit does not affect the digital interface, nor does it affect DRDY The state of the bit. in case DRDY Is high, and

STBY At low level, it will remain high until there is a new valid word in the data register. in case DRDY At low level, STBY Also at low level, it will remain low until the data register is updated. If in DRDY When it is low, the device enters wait mode (indicating that there are unread valid words in the data register) , Can be read in wait mode

Data in the data register. After the read operation, DRDY Will return to high level.

The device works in wait mode, reduces the total current, uses an external clock and the external main clock stops, V_{DD} = 5V Time,

Typical value of current 9 μ A , V_{DD}= 3V , The typical value of the current is 4 μ A . The external clock continues to work, waiting for the current to increase to 150 μ A , 75 μ A . If a crystal or ceramic resonator is used as the clock source, then

5V with 3.3V The total current under the supply voltage is 400 μ A with 90 μ A . This is because in the wait mode, the on-chip oscillator circuit continues to work. This is caused by TM7707/8 It is very important to provide system clock applications, so that even while waiting

Mode, TM7707/ TM7708 Can still generate uninterrupted master clock signal.

38. Precision

Σ-ΔADC , Like VFC And other ADC Similarly, it does not contain any non-monotonic sources, and provides no missing codes.

Due to the use of high-quality on-chip capacitors, TM7707/8 Can obtain excellent linearity, the capacitance/voltage system of this capacitor

The number is very low. By applying clipping stabilization technology at the input stage, TM7707/8 It also has low input drift. To ensure the working temperature

Good performance in the range of TM7707/8 Use digital calibration techniques to obtain the smallest offset and gain errors.

Thirty-nine, drift

TM7707/8 Use clipping stabilization technology to minimize the drift of the input offset. The electricity injected into the analog switch

The DC leakage current of the charge and sampling nodes is the main source of offset voltage drift. The DC input leakage current is essentially

Benefit has nothing to do. The gain drift of the converter mainly depends on the temperature of the internal capacitor, which is not affected by the leakage current.

The measurement error caused by offset drift or gain drift can be eliminated by the next calibration. Use system calibration also

It can minimize the offset and gain errors in the signal conditioning circuit. Integral or differential linearity errors are not affected by temperature changes.

Forty. Power

TM7707/8 The power supply voltage range is 2.7V~5.25V . In order to avoid excessive current, REF IN ,

AIN Or logic input pins, you should give TM7707/8 powered by. If this is not possible, you must restrict the flow

The current of these pins. in case TM7707/8 And the digital circuit of the system use their own power supply, you should give TM7707/8 powered by. If this cannot be guaranteed, the current-limiting resistor should be connected in series with the logic input to limit the current. Locking current of the device

(Latch-up current)more than the 100mA .

41. Power supply current

TM7707/8 The current consumption varies with the supply voltage (2.7V~5.25V) And change. There is a current increase inside the device High bit, it makes the current set according to working conditions. This affects the current in the analog circuit. Figure 15 Gives f_{CLKIN} = 1MHz with f_{CLKIN}= 2.4576MHz Time I_{DD} Follow V_{DD} And the typical graph of change (+ 25 ℃). From the picture 15 It can be seen that IDD Follow VDD Decrease and decrease. By using an external master clock or when using the on-chip oscillator circuit, by optimizing external components The power supply current can be reduced. Figure 3 , 4 , 6 with 7 shown I_{DD} With gain, V_{DD} And the curve of the clock frequency.

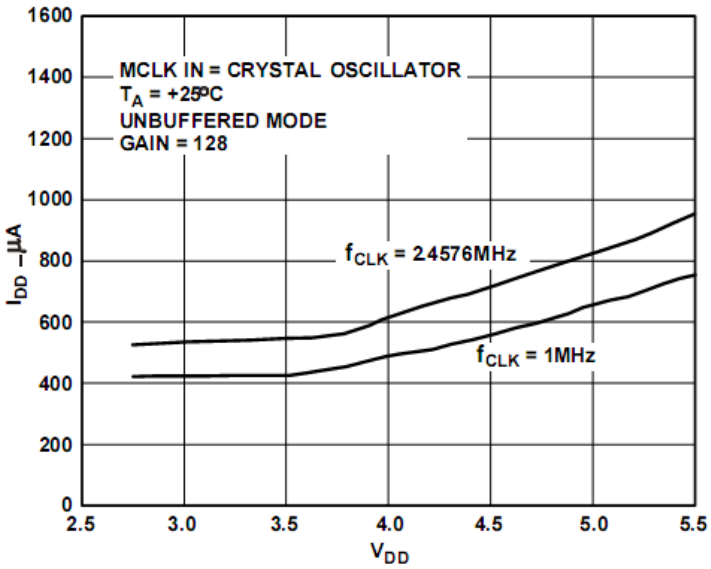


图15 I_{DD}和V_{DD}的关系

42. Grounding and wiring

Since the analog input and reference input are differential, most of the voltage of the analog modulator is a common-mode voltage. TM7707/8 The good common-mode rejection performance can eliminate the common-mode noise in these common-mode input signals. Digital filter can suppress power supply Broadband noise generated in addition to frequencies that are integer multiples of the modulator sampling frequency. In addition, digital filters can eliminate analog And the noise in the reference input signal does not saturate the analog modulator. In short, TM7707/8 Conversion of higher resolution than traditional The device is more immune to noise interference. However, because its resolution is too high and the noise level is too small, it must be noted Grounding and circuit wiring.

TM7707 The printed circuit board must be designed according to specifications to ensure that the analog area and the digital area are separated and each limited in the circuit A certain area on the board. The ground plane can be used to easily separate them. It is better to use corrosion technology as the ground plane, because In this way, the shielding performance can be maximized. The analog and digital ground planes should be connected together in only one place to avoid Ground loop. Need for multiple devices in the system AGND-DGND In connected applications, TM7707 Analog and digital connections The ground plane should be as close as possible TM7707 of GND The star ground point is connected.

Avoid running digital lines under the device, as this will cause the on-chip noise to increase exponentially. The analog ground plane should be placed on Below the device. TM7707/8 The power cord should be thick enough to reduce the line impedance and reduce the sharpness of the power supply line. The influence of the peak signal. Fast transition signals such as the master clock should be shielded by digital grounding to prevent noise from radiating to other parts of the circuit. It part. The clock signal cannot pass near the analog input signal. Avoid crossover between analog signals and digital signals. The lines on both sides of the circuit board should be at right angles to reduce the feedthrough effect of the circuit board. Using microstrip technology is the best Yes, but we can't always use double-sided circuit boards. When applying this technology, put the components on the side of the circuit board On the ground plane, the signal is placed on the solder side of the circuit board.

Use high resolution ADC At times, good decoupling performance is very important. All analog power supplies should be decoupled by: use 10 μ F One in parallel 0.1 μ F Of ceramic capacitors GND Decoupling. To get the best effect of decoupling components, they should be placed as close as possible ADC ,in ADC Right above is ideal. All logic chips should be connected to DGND Up 0.1 μ F Decoupling of capacitors.

Forty-three, digital interface

As mentioned earlier, TM7707/8 The programming function is controlled by on-chip register settings. Write/read operations to these registers The work is done through the serial interface of the device.

TM7707/8 The serial interface includes 5 Signals: namely $\overline{CS}$, SCLK , DIN , DOUT with $\overline{DRDY}$. DIN Lines are used to transfer data to the on-chip registers, and DOUT The wire is used to access the data in the register. SCLK It is a serial clock input, all data transmission and SCLK Signal related. $\overline{DRDY}$ Line as a status signal to remind the data At that time, it is ready to read data from the register. When there is a new data word in the output register, $\overline{DRDY}$ Becomes low. in Before the output register data is updated, if $\overline{DRDY}$ Changes to high level, it prompts not to read data at this time, so as not to register Read data during the update process. $\overline{CS}$ Used to select devices. In applications where many devices are connected to the serial bus, it is also used In the system TM7707/8 To decode.

Figure 16 with 17 Is used $\overline{CS}$ Correct TM7707/8 Timing diagram for decoding. Figure 16 Shown is from TM7707/8 Lose The timing diagram of the shift register read data, and the diagram 17 Shown is the timing diagram of writing data to the input shift register. which is So that after the first read operation $\overline{DRDY}$ When the line returns to high level, the same data may be read twice from the output register Case. Care must be taken to ensure that the read operation has been completed before the next output update is performed.

Pass to $\overline{CS}$ Add low level, TM7707/8 The serial interface can work in three-wire mode. SCLK , DIN with DOUT Line used with TM7707/8 To communicate. $\overline{DRDY}$ The status can be accessed through the communication register MSB get. This solution is suitable for interfacing with a microcontroller. If required $\overline{CS}$ As a decoded signal, it can be generated by the port of the microcontroller. Correct For the interface with the microcontroller, it is recommended that between two adjacent data transmissions, SCLK Set to high level.

TM7707/8 Can also be $\overline{CS}$ Works when used as a frame synchronization signal. This scheme is suitable for DSP Interface in In this case, the first place (MSB) Was $\overline{CS}$ The timing is valid output because $\overline{CS}$ Usually at DSP On the SCLK Generated at the falling edge. If the timing does not change, SCLK It can also continue to run between two adjacent data transfers. through Add on TM7707/8 of $\overline{RESET}$ The reset signal on the pin can reset the serial interface. Can also pass to DIN Write a series of " 1 "To reset the serial interface, if at least 32 Serial clock cycles inward TM7707/8 of DIN Line write logic" 1 ", the serial interface is reset. This ensures that in a three-wire system, if a software error occurs Or the flashing signal in the system causes the interface to get lost, and the system interface can be reset to a known state. This is to make the interface back To TM7707/8 Waiting for a write operation to its communication register. This write operation itself does not reset any register The contents of the register, but because the interface has been lost, the information written to any register is unknown, so it is recommended to change all The register is reset once.

Some microprocessors or microcontrollers have only a single serial data line for the serial interface. In this case, you can To put TM7707/8 of DATAOUT with DATA IN Connect the wires together and connect them to the single data wire of the processor even. One must be used on this single data line 10kΩ The pull-up resistor. In this case, if the interface gets lost, Because read and write operations share the same wire, the process of resetting and restoring the interface to a known state is different from the previous description. This process requires twenty four Read operations with consecutive clocks and at least 32 Consecutive clock cycles of logic "1" To ensure that the serial interface returns to a known state.

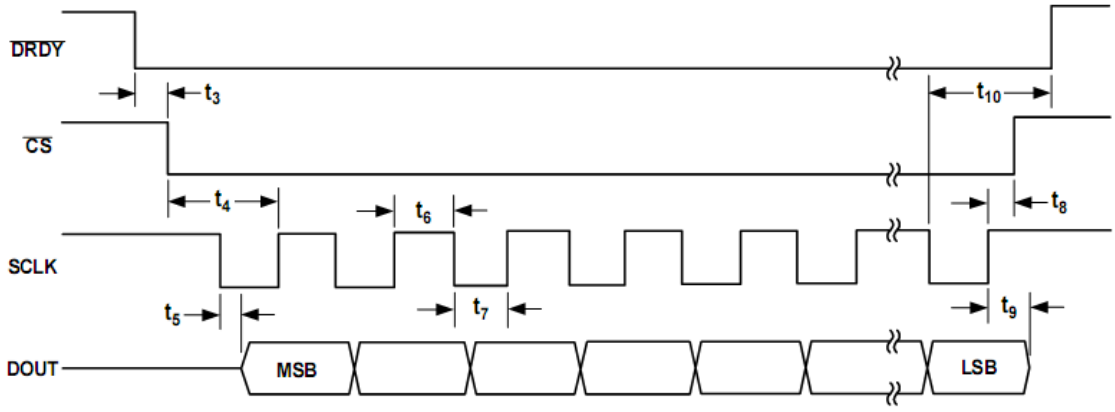


图16　读周期时序图

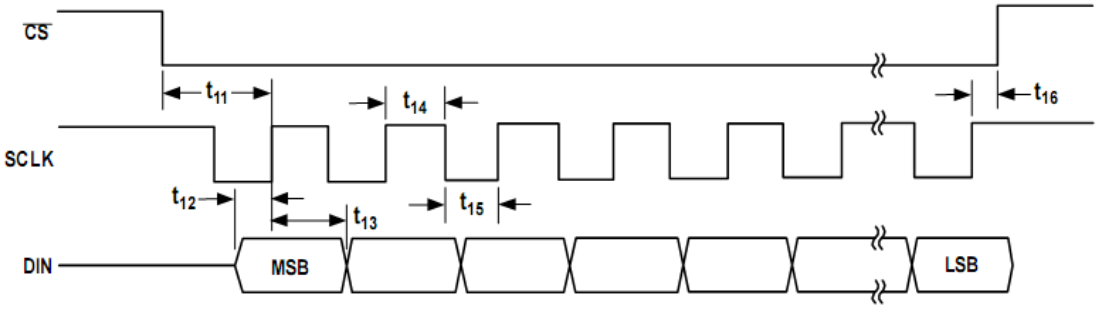


图17　写周期时序图

Forty-four, TM7707/8 Configuration

TM7707/8 Includes six on-chip registers that users can access through the serial interface. Communication with any register must first Write to the communication register first. Figure 18 Drawn right TM7707 After power-on or reset, the flow chart of the process of configuring all registers, the same process is also applicable to TM7708 . The flowchart also shows two different read options, the first one is query DRDY Pin to determine when the data register update is performed, the second is to query the communication register DRDY Bit To confirm whether the data register has been updated. The flowchart also includes the registers that must be written to set different working conditions A series of words. These working conditions mean that the gain is 1 , No filter synchronization, bipolar mode, no buffering, 4.9512MHz Clock and 50Hz The output rate.

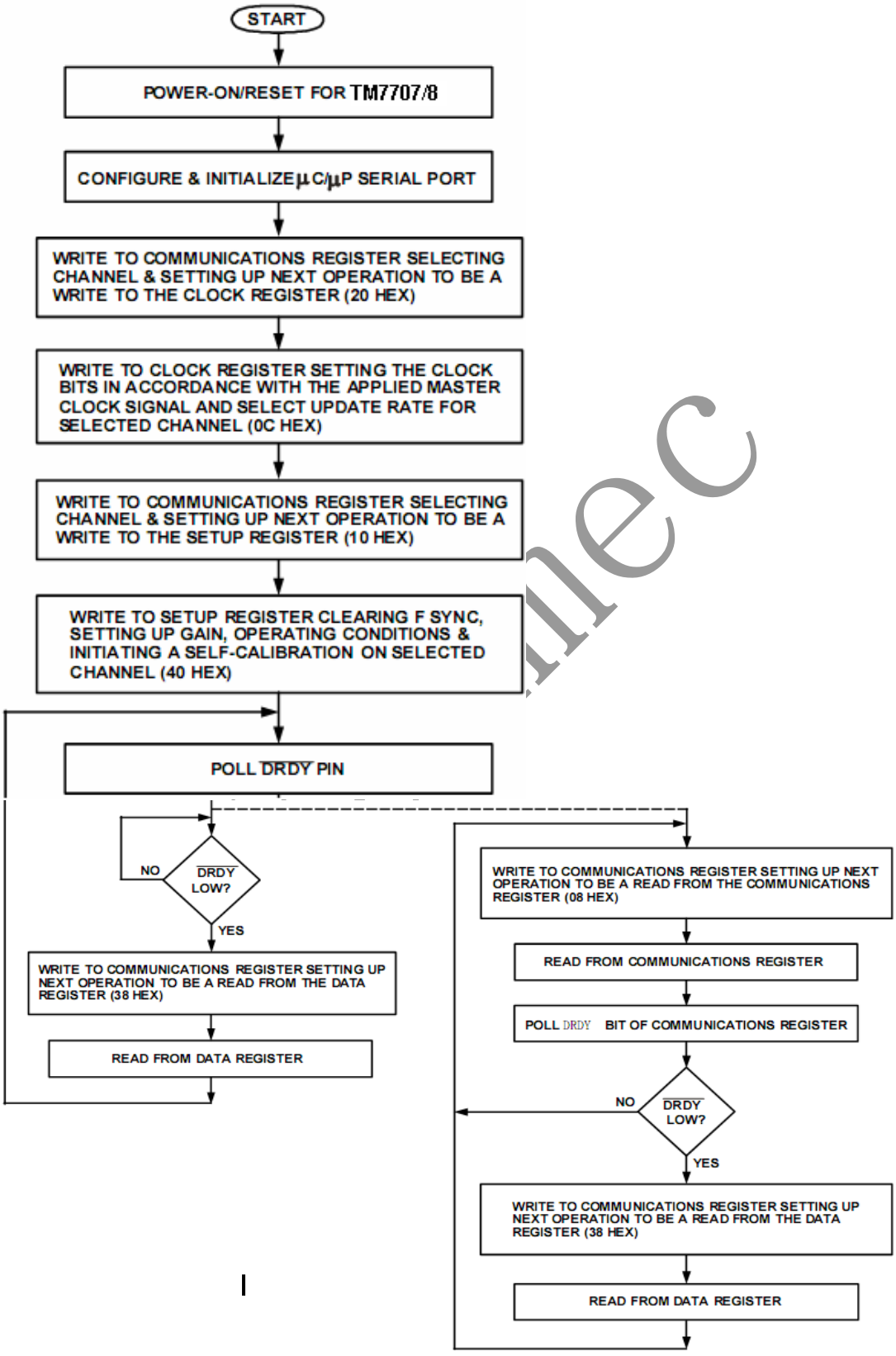


Figure 18 **TM7707 Flow chart of register setting and reading**

45. Microcomputer/microprocessor interface

TM7707/8 The flexible serial interface makes it easy to interface with most microcomputers and microprocessors.

Figure 10 Listed TM7707/8 Items that must be followed when interfacing with a microcontroller or microprocessor. Figure 19 , 20 with twenty one

Shown are some typical interface circuits.

TM7707/8 The serial interface can work with only three wires and is compatible with SPI The interface standard is compatible.

TM7707/8 The three-wire working method makes it ideal for applications in the following places: the isolation system that requires the least interface line

System to minimize the number of opto-isolators required by the system. The serial clock input signal is a Schmidt (Schmitt)touch

For signalling, it can adapt to the slow edge of the optocoupler. The rise and fall time of other digital input signals should not exceed 1

μ s .

TM7707TM7708 Most of the registers in are 8 Bit register, which makes with 8 Microcontroller interface with a bit serial interface is very easy. TM7707/8

The digital register on is twenty four Bit, offset and gain registers are also twenty four

Bit, the digital transfer to these registers and microcontroller ports contains multiple 8 Bit byte. DSP Processors and microprocessors usually transmit in serial

data operations 16 Bit data. Some processors such as ADSP-2105 In a serial data transmission, the number of cycles can be programmed. This allows the

user to increase or decrease the number of bits of the register in any transmission to match the requirements

Match.

in spite of TM7707/8 Some registers only have 8 Bit, but two such registers can be successfully connected, and the write operation can be used as

one 16 Bit data transmission processing. For example, if the setting register is to be updated, the processor must first

Write the communication register first, then write one 8 Bit data to the setting register. If needed, these can be

Single 16 Bit data transfer to complete, because written to the communication register 8 Once the bit serial data is completed, the device immediately sets

itself to a write operation state to the setting register.

Forty-six, TM7707/8 versus 89C51 interface

TM7707/8 versus 89C51 The microcontroller interface circuit is shown in the figure 20 Shown. In the picture $\overline{CS}$ Use when connected to low level 2 Wire

connection. DRDY The bits are monitored to determine when the data register is updated. Another option is to monitor DRDY

Output line, this will increase the interface line to 3 line. Correct DRDY Line monitoring methods are 2 Kinds: query method and interrupt method, similar to 68HC11

Interface method. 89C51 Configured as serial interface 0 Mode, this serial interface includes a single data line. the result is, TM7707/8 of DATA OUT with DATA

IN The pins must be connected together, one must also be connected 10kΩ The pull-up resistor.

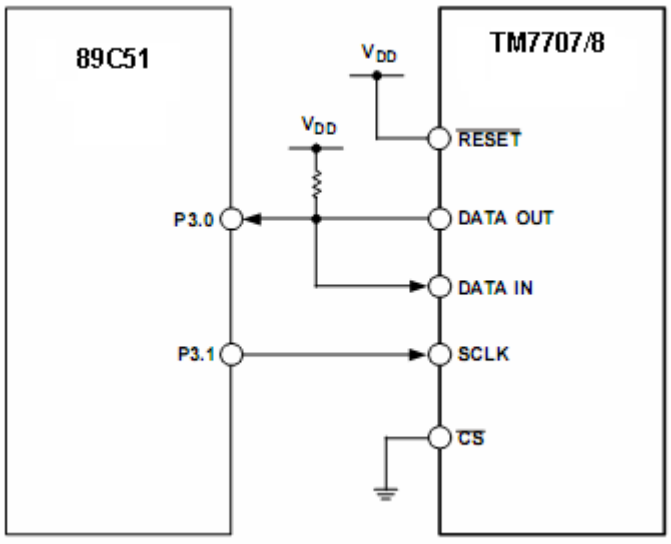


Figure 20TM7707/8 versus 89C51 interface

Forty-seven, settings TM7707/8 Program code

table 16 Gives TM7707 Use to interface with microcontroller C A set of read and write programs written in code. The steps of this procedure are:

1. Write data to the communication register, select the channel 1 As a valid channel, set the next operation to the register Perform a write operation.
2. For setting register write operation, select 16 Gain multiplier, none BUF Buffer, bipolar.
3. Write data to the communication register, select the channel 1 As a valid channel, set the next operation to register the filter low Write operation.
4. Write to filter low register 0X00 .
5. Write data to the communication register, select the channel 1 As a valid channel, set the next operation to register the filter high Write operation.
6. Write to filter high register 0X0F
7. Inquire DRDY Output.
8. Read data from the data register.
9. Jump back to 7 , The first 8 Step until the specified number of samples are taken from the selected channel.

table 16 TM7707 Interface with microprocessor C Language code

```
// MCU:          AT89S52
// Target: TM7707
# include<reg52.h>
# include<intrins.h>
# define uchar unsigned char
# define uint unsigned int sbit
 SCLK=P1^0;

sbit DIO=P1^1;
sbit RESET=P1^2;
sbit CS=P1^3;
sbit DRDY=P1^4;
uchar *intp;
uchar idata date8[180];
void write_byte1(uchar date)                    // Write one byte of data
{
      uchar i;
      CS=0;                                     //CS Pull down,
      for(i=0;i<8;i++)
      {
            SCLK=0;                             //SCLK Pull down and prepare to write data
            _nop_();
            if(date&0x80)
                  DIO=1;
            else
```

```
                DIO=0;
            SCLK=1;                 //SCLK Pull high, write one bit of data
            Date<<=1;
        }
            CS=1;                   // After writing a byte CS Pull up.
}
uchar read_byte1 () // Read one byte of data
{
        uchar j,b1;
        CS=0;
        for(j=0;j<8;j++)
        {
            SCLK=0;
            b1=(b1<<1)|DIO;
            SCLK=1;
        }
        return b1;
}
void save_data(void)
{
            uchar i0,i1;
            intp=date8;
            for(i0=0;i0<60;i0++)
            {
               while(DRDY);             // wait DRDT When low, data can be read
               write_byte1(0x38);       // Write data to the communication register, select the channel 1 As effective, the next
  One operation is set to read the data register.
               for(i1=0;i1<3;i1++)      // Store one piece of data continuously.
               {
                    * intp=read_byte1();
                     intp++;
               }
               CS=1;
            }
}
void init()         // initialization
{
        RESET=1;
        SCLK=1;
        CS=1;
        DRDY=1;
}
void main(void) // Main function
```

```
{
    init();
    write_byte1(0X10);          // Write data to the communication register, select the channel 1 As an effective channel, the next operation
Set to write the setting register.
    write_byte1(0X20);          // Write operation to the setting register, select 16 Gain multiplier, none BUF Buffer, bipolar.
    write_byte1(0X50);          // Write data to the communication register, select the channel 1 As an effective channel, the next operation
Set to write to the filter low register.
    write_byte1(0X00);          // Write to filter low register 0X00 .
    write_byte1(0X20);          // Write data to the communication register, select the channel 1 As an effective channel, the next operation
Set to write to the filter high register.
    write_byte1(0X0F);          // Write to filter high register 0X0F .
    save_data();                //MCU Continuous storage twenty four Bit data 60 One.
    while(1);                   // Wait in a loop.
}
```

48. Application examples

TM7707 Provide dual-channel, low-cost, high-resolution analog-to-digital conversion function. Due to Σ- Δ The structure realizes analog-to-digital conversion, so that the device can be protected from interference in a noisy environment, so it is very suitable for industrial and process control. At the same time it also Provides programmable gain amplifier, digital filter and calibration options. Therefore, it provides more points than ordinary ADC more Multiple system-level functions, and there is no need to have the shortcomings of high-quality integrating capacitors. will TM7707 Applied to the system , Can make the system designer obtain a high resolution, because TM7707 Integral of noise performance ratio ADC Is better.

Chip PGA allow TM7707 Processing as low as 10mV (Full scale) Analog input voltage (VREF=+1.25V). When the device works in unbuffered mode, the differential input makes the absolute value of the analog input range at GND with VDD Any value in between. This allows the user to connect the sensor directly to TM7707 The input terminal is connected. TM7707 Programmable gain front end allows processing 0 ~+ 20mV To 0 ~+ 2.5V Unipolar analog input signal and ±20mV To ±2.5V Bipolar signal. Because the device operates on a single power supply, the bipolar input range is related to the up-biased differential input.

Forty-nine, pressure measurement

TM7707 A typical application is pressure measurement. Figure twenty two Shown is TM7707 When used with a pressure sensor, it is Sensym the company's BP01 Manometer. The pressure sensor is installed in a bridge circuit, In it's OUT (+) and OUT The (-) terminal outputs the differential output voltage. When adding full scale pressure to the sensor (300mmHg), the differential output voltage (ie IN (+) and IN (-) The voltage between the two ends) is the input voltage 3mV/V . Assuming the excitation voltage is 5V , The full-scale output voltage of the sensor is 15mV . Excitation voltage of bridge circuit Also used for TM7707 Generate a reference voltage. Therefore, changes in the excitation voltage will not cause errors in the system. Figure twenty two In, when the two resistance values are 24k Ω with 15kΩ When the excitation voltage is 5V Time, TM7707 The generated reference voltage is 1.92V . The device has 128 When the programmable gain TM7707 The full-scale input amplitude should be 15mV . This value is related to the output range of the sensor. TM7707 The second channel can be used as an auxiliary channel to measure another change, such as temperature Degree, as shown twenty two Shown. This secondary channel can be used to adjust the output signal of the primary channel in order to eliminate temperature effects on the system Impact.

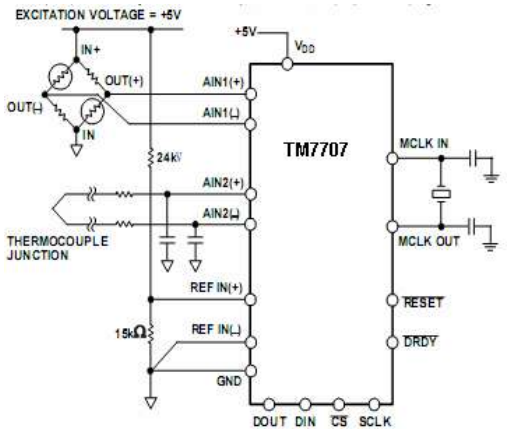


Figure twenty two use TM7707 Make pressure measurement

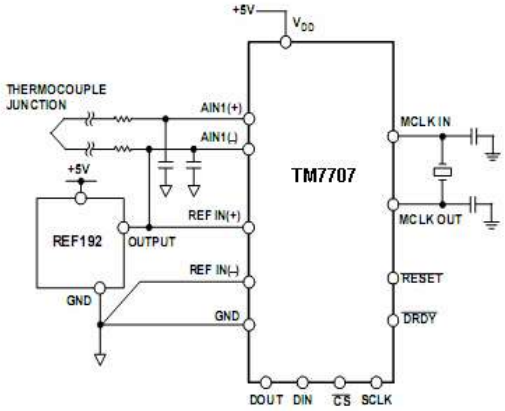


Figure twenty three use TM7707 Make temperature measurement

Fifty, temperature measurement

TM7707 Another area of application is temperature measurement. Figure twenty three Is a thermocouple with TM7707 Connection diagram. In this application, TM7707 Work in buffer mode to allow large decoupling capacitors on the front end to eliminate possible thermal coupling Pick up any noise on your feet. when TM7707 When working in buffer mode, its common mode input range is reduced. For the future The differential voltage of the thermocouple is placed on an appropriate common mode voltage. TM7707 of AIN 1 (-) The input terminal should be biased up to To reference voltage (+ 2.5V).

Figure twenty four Shown is TM7707 Another temperature measurement application. In this application, the sensor is a RTD (Thermistor), PT100 . It is a four-pin RTD . Resistance in the lead RL1 with RL4 There is a voltage drop, but this only shifts the common-mode voltage. when TM7707 When the input current is very low, the lead resistance RL2 with RL3 There is no voltage drop. The lead resistance presents a small source impedance, so it is generally not necessary to TM7707 The buffer in is opened. If requested To use a buffer, you must pass the RTD The bottom and TM7707 of GND Insert a small resistor between them to set the corresponding common mode voltage. In this application, external 400 μA The current source is PT100 Provide excitation power while passing 6.25kΩ Resistors. for TM7707 Generate a reference voltage. The change of excitation current does not affect the circuit operation, this is because the input voltage And the reference voltage changes with the excitation current. however, 6.25kΩ The resistor must have a small temperature coefficient to avoid temperature The error of the reference voltage within the range.

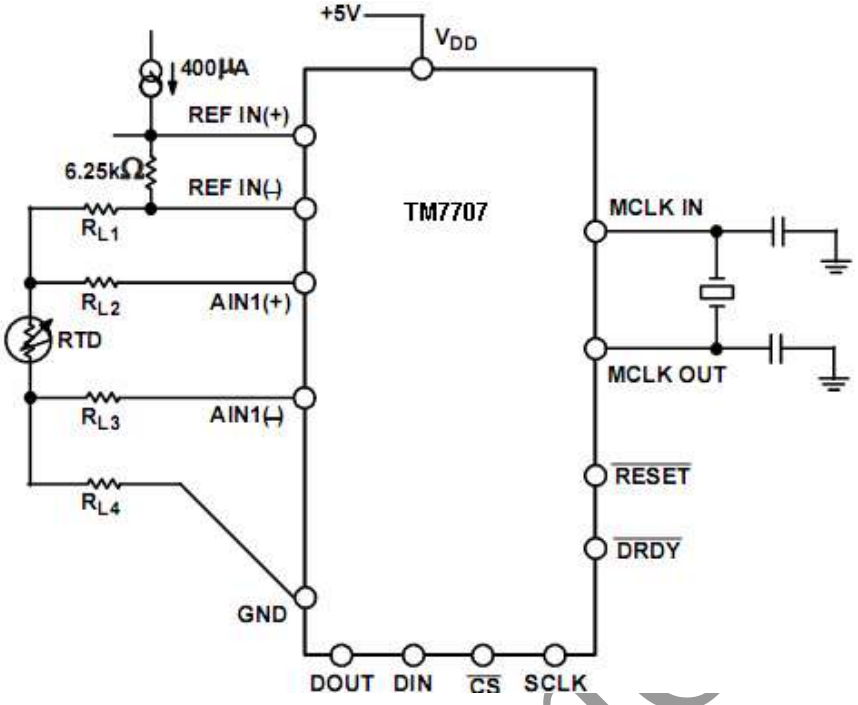


Figure twenty fouruse TM7707 get on RTD measuring

Fifty-one, smart transmitter

Another application area is in low-power, single-supply, three-wire interface smart transmitters. Here, the entire smart launch Device must be in 4 ~ 20mA Work in the loop. The loop allows the total current to be supplied to the transmitter as low as 3.5mA . among them TM7707 Consume only 320 μ A Current, leaving at least 3mA The current to the other parts of the transmitter. Figure 25 Shown is to contain TM7707 A block diagram of a smart transmitter. With dual input channels TM7707 It is especially suitable for systems that require auxiliary channels to measure variables to modify the main channel.

52. Battery monitoring

Another area that requires low-power, single-supply operation is battery monitoring in portable devices. Figure 26 Yes A block diagram of a battery monitor, including TM7707 And it is used to differentially measure the voltage across each battery. Router (multiplexer) TM7707 The second channel is used to monitor the leakage current of the battery. With dual input channels TM7707 It is suitable for measurement systems that require two input channels, as in this example, to monitor voltage and current. because TM7707 Can adapt to very weak input signals, so RSENSE A small resistance value can be used, so that unnecessary power loss can be reduced. This system works at a gain of 128 , The full scale is ±9.57mV The signal can be 2 μV The resolution is measured and gives 13.5 The stability of the bit. In order to obtain the rated characteristics in unbuffered mode, false Determine the absolute value of the analog input voltage GND-30mV with V_{DD} + 30mV between, The input common mode range is GND To V_{DD} . 25 At ℃, when the performance does not decrease, TM7707 Can bear GND-200mV Absolute voltage, but leakage current It will increase a lot when the temperature rises.

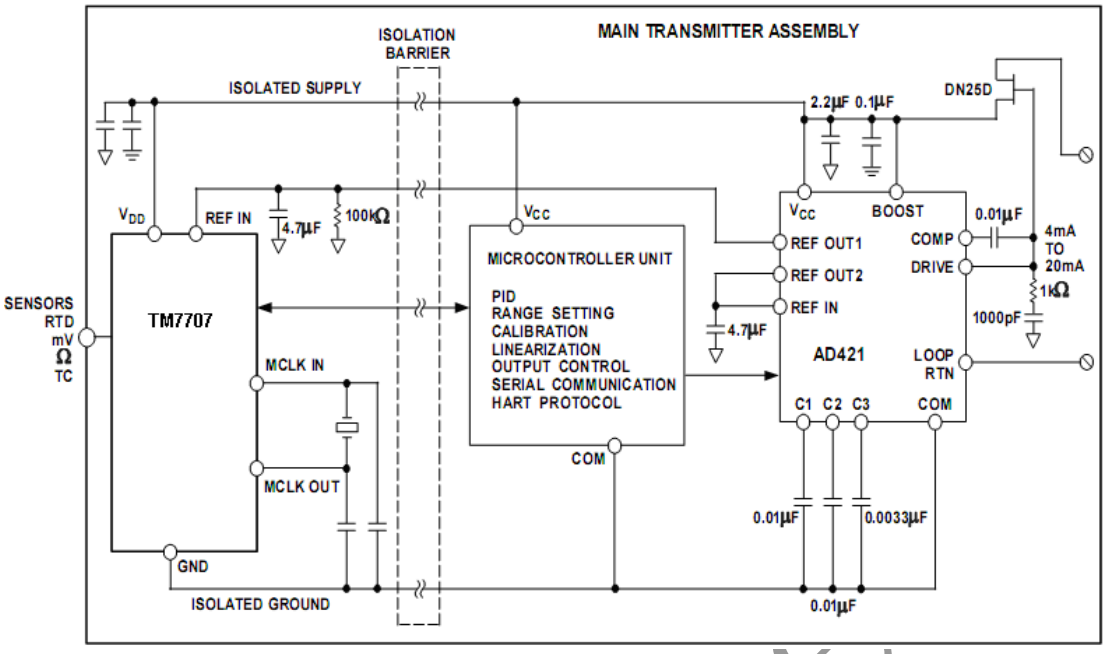


Figure 25 use TM7707 Smart transmitter

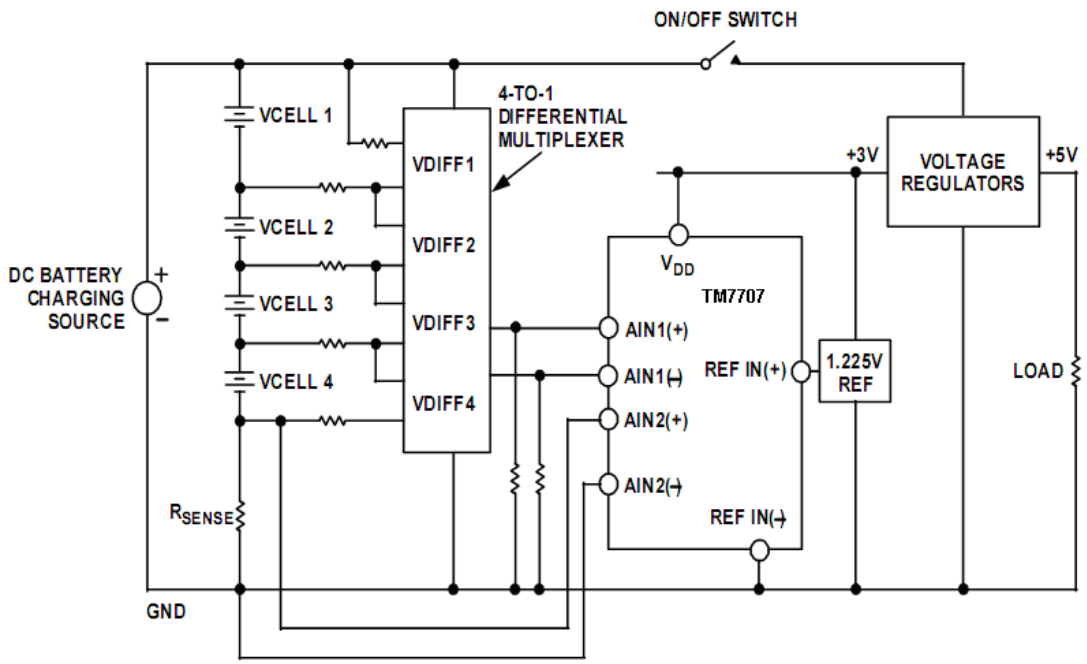
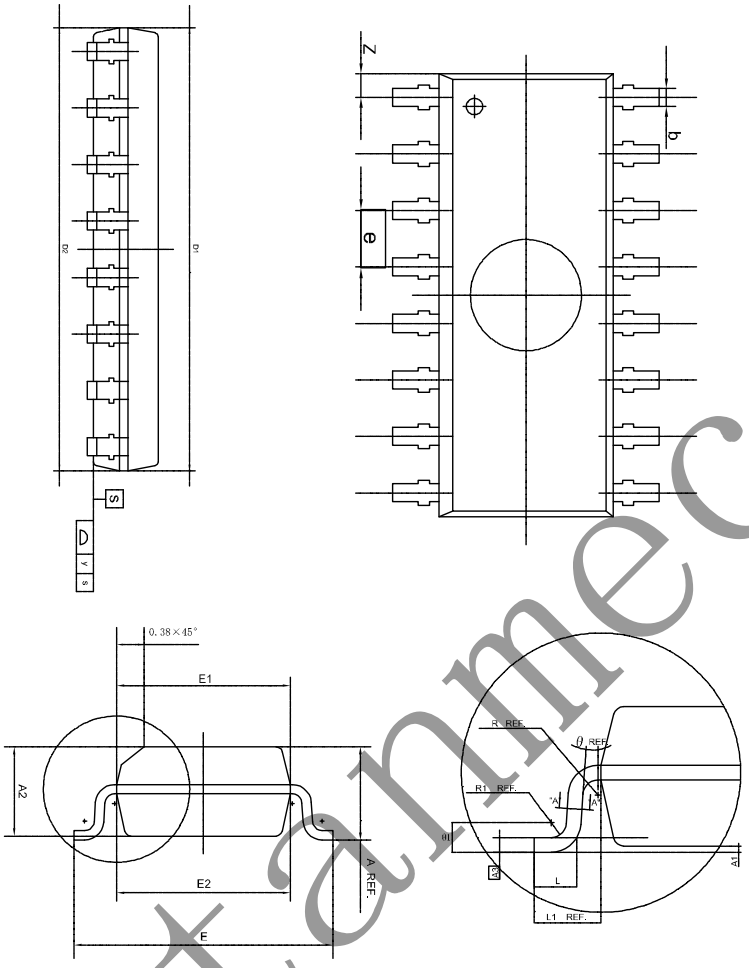


Figure 26 use TM7707 Battery monitoring

Device dimensions



Symbol	Min	Nom	Max
A	1.500	1.600	1.700
A1	0.100	0.150	0.200
A2	1.400	1.450	1.500
A3	--------	0.223	————
b	0.356	0.406	0.456
b1	0.366	0.426	0.486
c	-------	0.203	———
D1	9.700	9.900	10.10
D2	9.750	9.950	10.15
E	5.900	6.000	6.100
E1	3.800	3.900	4.000
E2	3.850	3.950	4.050
e	-------	1.270	------
L	0.600	0.660	0.700
L1	0.950	1.050	1.150
R	-------	0.200	------
R1	-------	0.300	------
θ	0	-------	8°
θ1	0	------	10°
y	------	------	0.1
Z	-------	0.505	———