十速科技股份有限公司
tenx technology inc.

TM8720

4-Bit Microcontroller

Data Sheet

AMENDMENT HISTORY

Version	Date	Description
V1.0	Apr, 2005	New release
V1.1	May, 2005	Add Typical Application Circuit diagram.
V1.2	Aug, 2005	Modify the IOA, B pull-low resistance to 100~1000 Kohm
V1.3	Sep, 2005	Revise voltage and operating condition in Segment Driver Output Characteristics section.
V1.4	Apr, 2012	Modify the operating temperature to -20℃~70℃.
V1.5	Jan, 2013	Add General Description.

CONTENTS

GENERAL DESCRIPTION

The TM8720 is an embedded high-performance 4-bit microcomputer with LCD driver. It contains all the necessary functions, such as 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock operation and LCD driver in a single chip.

FUNCTION

1. 1.5V operation only and with low power dissipation.

2. Powerful instruction set (86 instructions)

- Binary addition, subtraction, BCD adjustment, logical operation in direct.
- Single-bit manipulation (set, reset, decision for branch).
- Various conditional branches.
- 16 working registers and manipulation.
- LCD driver data transfer.

3. Memory capacity

- ROM capacity 1024 x 16 bits.
- RAM capacity 64 x 4 bits.

4. Input/output ports

- Port IOA 4 pins (with internal pull-low), IOA port has built-in the input signal chattering prevention circuitry.
- Port IOB2, 3, 4 3 pins (with internal pull-low), & mask option with BZB, BZ.

5. 4-level subroutine nesting.

6. Interrupt function

- One external factor (Pin IOA port).
- Two internal factors (Pre-Divider, Timer2).

7. Built-in Alarm, clock or single tone melody generator (BZB, BZ), & mask option with IOB3, 4.

8. One 6-bit programmable timer (Timer 2) with programmable clock source.

9. LCD driver output

- 12 LCD driver outputs (up to drive 48 LCD segments).
- 1/4 Duty and 1/2 Bias for LCD display.
- Single instruction to turn off all segments.
- 12 LCD Address

10. Built-in Voltage double charge pump circuit.

11. Clock oscillation can be defined as X’tal, external-R or internal-R 2 type oscillators by mask option.

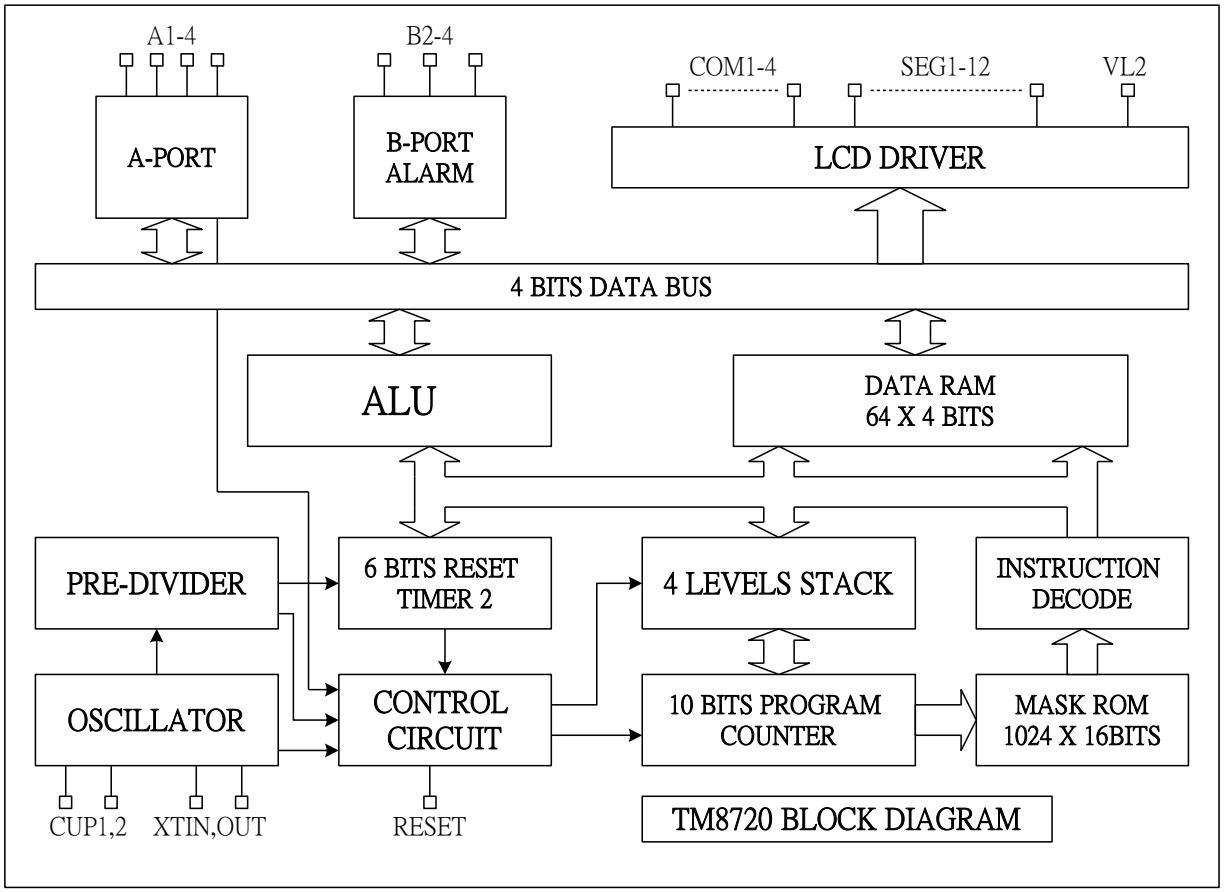
12. HALT function.

13. STOP function.

APPLICATION

- Thermometer

BLOCK DIAGRAM



PIN DESCRIPTION

Name	I/O	Description
VBAT	P	Positive power supply. Connect a 0.1 uF capacitor to GND.
VL2	P	LCD supply voltage. Connect a 0.1 uF capacitor to GND.
RESET	I	Input pin for chip reset request signal, with internal pull-down resistor.
TEST	I	Test signal input pin.
CUP1,2	O	Switching pins for supply the LCD driving voltage. Connect the CUP1 and CUP2 pins with a 0.1 uf non-polarized electrolytic capacitor for LCD mode.
COM1~4	O	Output pins for driving the common pins of the LCD .
SEG1~12	O	Output pins for driving the LCD panel segment or output.
IOA1~4	I/O	Input/Output port A.
IOB2~4	I/O	Input/Output port B.
BZB, BZ	O	Output port for alarm (Muxed with IOB3, 4).
XIN XOUT	I O	System clock oscillation. Connected with 32 KHz crystal oscillator or internal R or external R by mask option.
GND	P	Negative supply voltage.

FIXED LCD TABLE

SEG	**Lz**	**Bit0**	**Bit1**	**Bit2**	**Bit3**	SEG	**Lz**	**Bit0**	**Bit1**	Bit2	**Bit4**
SEG1	00H	com1	com2	com3	com4	**SEG7**	06H	com1	com2	com3	com4
SEG2	01H	com1	com2	com3	com4	**SEG8**	07H	com1	com2	com3	com4
SEG3	02H	com1	com2	com3	com4	**SEG9**	08H	com1	com2	com3	com4
SEG4	03H	com1	com2	com3	com4	**SEG10**	09H	com1	com2	com3	com4
SEG5	04H	com1	com2	com3	com4	**SEG11**	0AH	com1	com2	com3	com4
SEG6	05H	com1	com2	com3	com4	**SEG12**	0BH	com1	com2	com3	com4

FUNCTION DESCRIPTION

SRAM

There are 64 X 4 bits data SRAM (40h ~ 7Fh), can be used by direct addressing mode or index addressing mode; the last 16 addresses (70h ~ 7Fh) can be used as Working Register.

ROM

There are 1024 X 16 bits ROM, can be used to divide it for Instruction ROM.

I/O Ports

The IOA port can be selected by software separately as input or output and with/without internal pull-low and different chattering clock for HALT release / Interrupt trigger to reduce the bounce of key scan:

PH6: 512 Hz PH8: 128 Hz Ph10: 32 Hz

The pull-low of IOA will be masked off for those pins that are defined as output pins.

The IOB2~4 can be selected by software separately as input or output and with/without internal pull-low.

Reset

Reset Pin Reset function. There is no individual “Power On Reset” option because “RESET pin reset” is the only way to start up the program.

When the ‘H’ level signal is applied on the RESET pin, the reset cycle will finish after 64 ms automatically if PH0 = 32 KHz, even though the reset signal is longer than 64 ms.

Pre-Divider

The pre-divider contains a 15-stage counter using PH0 as clock source; the output of T-Flip-Flop is changed when input clock changes from H to L.

PH11~15 will be reset to L state when power on reset or external reset pin reset or PLC 100 instruction is executed.

When PH14 changes from H to L, the HALT release signal HRF3 is generated.

TIMER 2

This 6-bit programmable timer can select PH3 / PH9 / PH15 (Timer 2 can also select PH5 / PH7 / PH11 / PH13 by TM2X instruction) as clock source; when it is underflow, the HALT release signal HRF1/4 is generated.

Alarm

Alarm output from BZ/BZB.

HALT Function

The HALT instruction will disable the system clock and leave only pre-divider, frequency generator, timer and chattering clock for HALT release generation.

STOP Function

The STOP instruction will disable all clocks to minimize the stand-by current (<1 uA).

Absolute Maximum Ratings

At Ta=-20 to 70℃, GND= 0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	V_{BAT}	-0.3 to 2.0	V
	VL2	-0.3 to 4.0	V
Maximum Input Voltage	V_{in}	-0.3 to V_{BAT}+0.3	V
Maximum output Voltage	V_{out1}	-0.3 to V_{BAT}+0.3	V
	V_{out2}	-0.3 to VL2 +0.3	V
Maximum Operating Temperature	T_{opg}	-20 to +70	℃
Maximum Storage Temperature	T_{stg}	-25 to +125	℃

Allowable Operating Conditions

At Ta=-20 to 70℃, GND= 0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{BAT}		1.2	1.5	1.8	V
	VL2		2 x V_{BAT} x 0.9		2 x V_{BAT} + 0.1	V
Stand-by current	I_{sb}	STOP mode	-	-	1	uA
Input “H” Voltage	V_{ih1}	IOA and IOB port in input mode	V_{BAT} - 0.7	-	V_{BAT} + 0.7	V
Input “L” Voltage	V_{il1}		-0.7	-	0.7	V

Electrical Characteristics Internal RC Frequency Range

Option Mode	Min.	Typical	Max.
600 KHz	500 KHz	600 KHz	700 KHz

Input Resistance

(V_{BAT}=1.5V)

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
IOA1~4, IOB2~4 Pull-Down Tr.	R_{mad1}	Vi = V_{BAT}	100	300	1000	Kohm
RES Pull-Down R	R_{res1}	Vi = GND or V_{BAT}	10	50	100	Kohm

DC Output Characteristics

(V_{BAT}=1.2V)

Name	Symbol	Condition	Port	Min.	Typ.	Max.	Unit
Output “H” Voltage	V_{oh2c}	I_{oh} = -200 uA	IOA1~4, IOB2, IOB3, 4/ BZB, BZ	0.8	0.9	1.0	V
Output “L” Voltage	V_{ol2c}	I_{ol} = 400 uA		0.2	0.3	0.4	V

Segment Driver Output Characteristics

(V_{BAT} =1.2V)

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit.
1/2 Bias Display Mode							
Output "H" Voltage	V_{oh12f}	I_{oh} = -1 uA	SEG-n	2.2	2.4	---	V
Output "L" Voltage	V_{ol12f}	I_{ol} = 1 uA		---	0.0	0.2	V
Output "H" Voltage	V_{oh12g}	I_{oh} = -10 uA	COM-n	2.2	2.4	---	V
Output "M" Voltage	V_{om12g}	$I_{ol/h}$ = +/-10 uA		1.0	1.2	---	V
Output "L" Voltage	V_{ol12g}	I_{ol} = 10 uA		---	0.0	0.2	V

Analog Circuit Characteristics

(V_{BAT} =1.5V GND=0V, X'tal fosc= 32.768 KHz, Ta=25℃, always in operation mode.)

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal Voltage	VL2	Connects a 1 MΩ load resistance between GND and VL2 (No panel load)	2x V_{BAT} x0.9	3.0	2x V_{BAT} +0.1	V

Power Consumption

At Ta=-20℃ to 70℃, GND= 0V, V_{BAT}=1.5V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
HALT mode	I_{HALT}	Only 32.768 KHz Crystal oscillator operating, without loading.		2		uA
STOP mode	I_{STOP}				1	uA

Note: When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

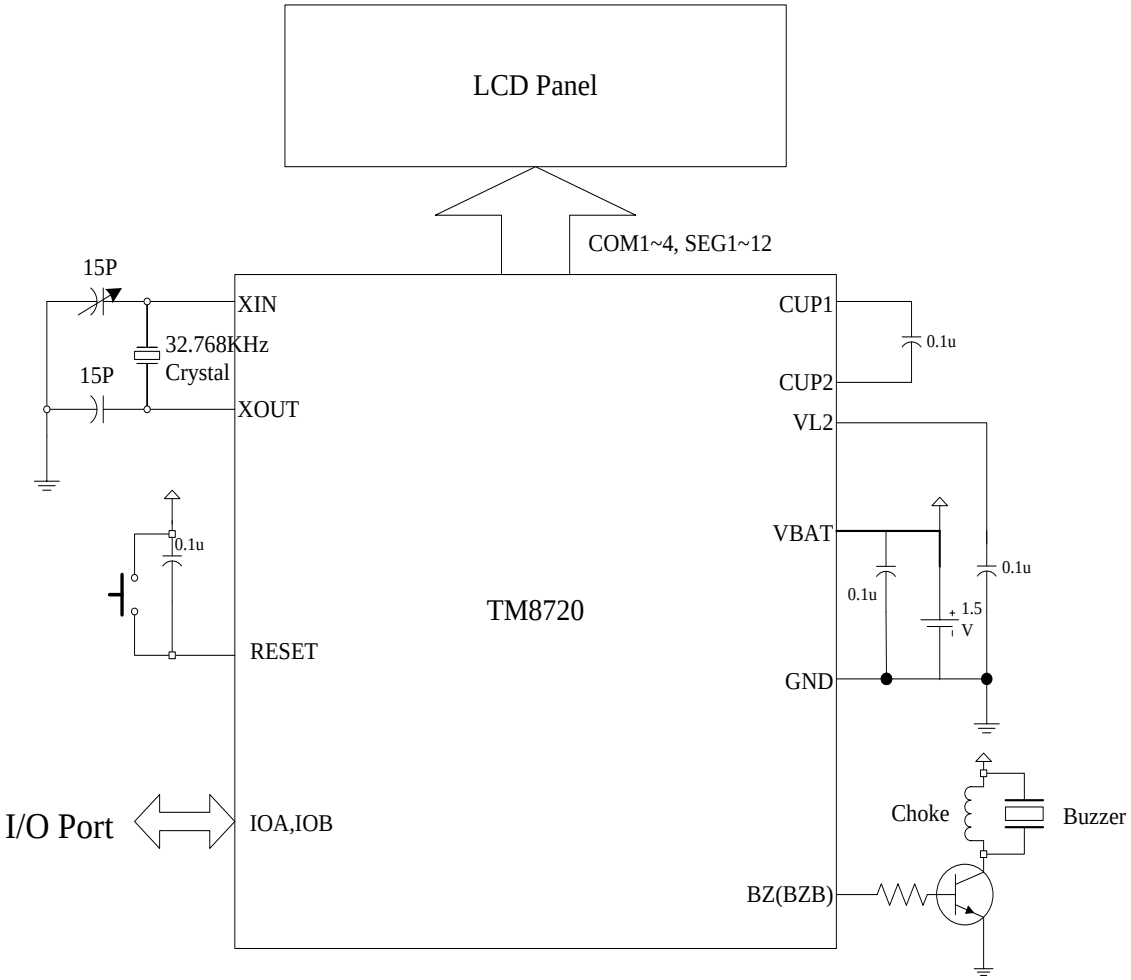
Allowable Operating Frequency

At Ta=-20℃ to 70℃, GND= 0V

Condition	Max, Operating Frequency
V_{BAT} =1.5V	700 KHz

Typical Application Circuit

This application circuit is simply an example, and is not guaranteed to work.



Ag power mode, 1/2 Bias, 1/4 Duty

Instruction Table

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCP	Lz,Ry	0000 0110 ZZZZ YYYY	Lz	← Ry	Lz : 00h~0Bh
OPA	Rx	0000 1010 01XX XXXX	PortA(IOA)	← Rx	
OPB	Rx	0000 1100 01XX XXXX	PortB(IOB)	← Rx	
ADC	Rx	0010 0000 01XX XXXX	AC	← Rx + AC + CF	CF
ADC*	Rx	0010 0001 01XX XXXX	AC,Rx	← Rx + AC + CF	CF
SBC	Rx	0010 0010 01XX XXXX	AC	← Rx + ACB + CF	CF
SBC*	Rx	0010 0011 01XX XXXX	AC,Rx	← Rx + ACB + CF	CF
ADD	Rx	0010 0100 01XX XXXX	AC	← Rx + AC	CF
ADD*	Rx	0010 0101 01XX XXXX	AC,Rx	← Rx + AC	CF
SUB	Rx	0010 0110 01XX XXXX	AC	← Rx + ACB + 1	CF
SUB*	Rx	0010 0111 01XX XXXX	AC,Rx	← Rx + ACB + 1	CF
ADN	Rx	0010 1000 01XX XXXX	AC	← Rx + AC	
ADN*	Rx	0010 1001 01XX XXXX	AC,Rx	← Rx + AC	
AND	Rx	0010 1010 01XX XXXX	AC	← Rx AND AC	
AND*	Rx	0010 1011 01XX XXXX	AC,Rx	← Rx AND AC	
EOR	Rx	0010 1100 01XX XXXX	AC	← Rx EOR AC	
EOR*	Rx	0010 1101 01XX XXXX	AC,Rx	← Rx EOR AC	
OR	Rx	0010 1110 01XX XXXX	AC	← Rx OR AC	
OR*	Rx	0010 1111 01XX XXXX	AC,Rx	← Rx OR AC	
ADCI	Ry,D	0011 0000 DDDD YYYY	AC	← Ry + D + CF	CF
ADCI*	Ry,D	0011 0001 DDDD YYYY	AC,Ry	← Ry + D + CF	CF
SBCI	Ry,D	0011 0010 DDDD YYYY	AC	← Ry + DB + CF	CF
SBCI*	Ry,D	0011 0011 DDDD YYYY	AC,Ry	← Ry + DB + CF	CF
ADDI	Ry,D	0011 0100 DDDD YYYY	AC	← Ry + D	CF
ADDI*	Ry,D	0011 0101 DDDD YYYY	AC,Ry	← Ry + D	CF
SUBI	Ry,D	0011 0110 DDDD YYYY	AC	← Ry + DB + 1	CF
SUBI*	Ry,D	0011 0111 DDDD YYYY	AC,Ry	← Ry + DB + 1	CF
ADNI	Ry,D	0011 1000 DDDD YYYY	AC	← Ry + D	
ADNI*	Ry,D	0011 1001 DDDD YYYY	AC,Ry	← Ry + D	
ANDI	Ry,D	0011 1010 DDDD YYYY	AC	← Ry AND D	
ANDI*	Ry,D	0011 1011 DDDD YYYY	AC,Ry	← Ry AND D	
EORI	Ry,D	0011 1100 DDDD YYYY	AC	← Ry EOR D	
EORI*	Ry,D	0011 1101 DDDD YYYY	AC,Ry	← Ry EOR D	
ORI	Ry,D	0011 1110 DDDD YYYY	AC	← Ry OR D	
ORI*	Ry,D	0011 1111 DDDD YYYY	AC,Ry	← Ry OR D	
INC*	Rx	0100 0000 01XX XXXX	AC,Rx	← Rx + 1	CF
DEC*	Rx	0100 0001 01XX XXXX	AC,Rx	← Rx - 1	CF
IPA	Rx	0100 0010 01XX XXXX	AC,Rx	← PortA(IOA4)	
IPB	Rx	0100 0100 01XX XXXX	AC,Rx	← PortB(IOB4~2)	
MAF	Rx	0100 1010 01XX XXXX	AC,Rx	← STS1	B3 : CF B2 : ZERO B1, B0 :(Unused)
MSB	Rx	0100 1011 01XX XXXX	AC,Rx	← STS2	B3 : (Unused) B2 : SCF2(HRx) B1 : (Unused) B0 : BCF

Instruction		Machine Code	Function		Flag/Remark
MSC	Rx	0100 1100 01XX XXXX	AC,Rx	← STS3	B3 : SCF7(PDV) B2 : PH15 B1, B0: (Unused)
MCX	Rx	0100 1101 01XX XXXX	AC,Rx	← STS3X	B3 : (Unused) B2 : SCF0(APT) B1 : SCF6(TM2) B0 : (Unused)
SR0	Rx	0101 0000 01XX XXXX	ACn, Rxn AC3, Rx3	← Rx(n+1) ← 0	
SR1	Rx	0101 0001 01XX XXXX	ACn, Rxn AC3, Rx3	← Rx(n+1) ← 1	
SL0	Rx	0101 0010 01XX XXXX	ACn, Rxn AC0, Rx0	← Rx(n-1) ← 0	
SL1	Rx	0101 0011 01XX XXXX	ACn, Rxn AC0, Rx0	← Rx(n-1) ← 1	
DAA		0101 0100 0000 0000	AC	← BCD(AC)	
DAA*	Rx	0101 0101 01XX XXXX	AC,Rx	← BCD(AC)	
DAS		0101 0110 0000 0000	AC	← BCD(AC)	
DAS*	Rx	0101 0111 01XX XXXX	AC,Rx	← BCD(AC)	
LDS	Rx,D	0101 1DDD D1XX XXXX	AC,Rx	← D	
STA	Rx	0110 1000 01XX XXXX	Rx	← AC	
LDA	Rx	0110 1100 01XX XXXX	AC	← Rx	
MRA	Rx	0110 1101 01XX XXXX	CF	← Rx3	
MRW	Ry,Rx	0111 0YYY Y1XX XXXX	AC,Ry	← Rx	
MWR	Rx,Ry	0111 1YYY Y1XX XXXX	AC,Rx	← Ry	
JB0	X	1000 00XX XXXX XXXX	PC	← X	if AC0 = 1
JB1	X	1000 10XX XXXX XXXX	PC	← X	if AC1 = 1
JB2	X	1001 00XX XXXX XXXX	PC	← X	if AC2 = 1
JB3	X	1001 10XX XXXX XXXX	PC	← X	if AC3 = 1
JNZ	X	1010 00XX XXXX XXXX	PC	← X	if AC ≠ 0
JNC	X	1010 10XX XXXX XXXX	PC	← X	if CF = 0
JZ	X	1011 00XX XXXX XXXX	PC	← X	if AC = 0
JC	X	1011 10XX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 00XX XXXX XXXX	STACK PC	← PC + 1 ← X	
JMP	X	1101 00XX XXXX XXXX	PC	← X	
RTS		1101 1000 0000 0000	PC	← STACK	CALL Return
SCC	X	1101 1001 0X10 0XXX	X6 = 1 X6 = 0 X2,1,0=001 X2,1,0=010 X2,1,0=100	: Cfq = BCLK : Cfq = PH0 : Cch = PH10 : Cch = PH8 : Cch = PH6	
SCA	X	1101 1010 00X0 0000	X5	: Enable SEF5	IOA4~1
SPA	X	1101 1100 000X XXXX	X4 X3~0	: Set A4-1 Pull-Low : Set A4-1 I/O	1:Output, 0: Input
SPB	X	1101 1101 000X XXX1	X4 X3~1	: Set B4-2 Pull-Low : Set B4-2 I/O	1:Output, 0: Input
TM2	Rx	1110 0100 01XX XXXX	Timer2	← Rx & AC	

Instruction		Machine Code	Function		Flag/Remark
TM2X	X	1110 011X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	
SHE	X	1110 1000 000X X000	X4 X3	: Enable HEF4 : Enable HEF3	TMR2 PDV
SIE*	X	1110 1001 000X X00X	X4 X3 X0	: Enable IEF4 : Enable IEF3 : Enable IEF0	TMR2 PDV APT
PLC	X	1110 101X 000X X00X	X8 X4 X3 X0	: Reset PH15~11 : Reset HRF4 : Reset HRF3 : Reset HRF0	 TMR2 PDV APT
SRE	X	1110 1101 0X00 0000	X6	: Enable SRF6	SRF6(APT)
SF		1111 0000 0000 00XX	X1 X0	: BCF Set : CF Set	BCF CF
RF		1111 0100 0000 00XX	X1 X0	: BCF Reset : CF Reset	BCF CF
SF2	X	1111 1000 0000 0X0X	X2 X0	: Close all Segments : Reload 2 Set	RSOFF RL2
RF2	X	1111 1001 0000 0X0X	X2 X0	: Release Segments : Reload 2 Reset	RSOFF RL2
ALM	X	1111 101X XXXX XXXX	X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: DC1 : PH3 : PH4 : PH5 : DC0 ← PH15~10	
HALT		1111 1110 0000 0000	Halt Operation		
STOP		1111 1111 0000 0000	Stop Operation		

Symbol Description

AC	: Accumulator	ACn	: Accumulator Bit n
BCF	: Back-up Flag	BCLK	: System clock, stop only in STOP
CF	: Carry Flag	Cch	condition
D	: Immediate Data	HEFn	: Clock source of Chattering Detector
HRFn	: HALT Release Flag	IEFn	: Halt Release Enable Flag
Lz	: LCD Latch	PC	: Interrupt Enable Flag
PDV	: Pre-Divider	Rx	: Program Counter
Rxn	: Memory Bit n of Address X	Ry	: Memory of Address X
SCFn	: Start Condition Flag	SEFn	: Memory of working register Y
SRFn	: STOP Release Enable Flag	TMR	: Switch Enable Flag
X	: Address	ZERO	: Timer Overflow Release Flag
()	: Content of Register		: Zero Flag