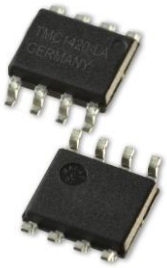
TMC1340-SO DATASHEET

Quad Complementary N & P-Channel 30V Enhancement Mode Power MOSFET with extremely low on-resistance. High energy efficiency and good thermal performance.



Applications

TMC1340-SO MOSFETs fit best with TRINAMIC 2-phase bipolar stepper motor drivers:

TMC262: up to 3A RMS motor current with 2xTMC1340-SO

TMC248: up to 2.5A RMS motor current with 2xTMC1340-SO

TMC249: up to 2.5A RMS motor current with 2xTMC1340-SO

Product Summary

	N-CH	P-CH
BV_{DSS}	30V	-30V
$R_{DS(ON)}$	33mΩ	55mΩ
I_D	5.5A	-4.1A

Features and Benefits

N & P-Channel MOSFET Full Bridge Device

Simple Drive Requirement

Low On-Resistance

Good Thermal Performance

Fast Switching Performance for quick motor reaction

SO-8 package, 5x6 mm

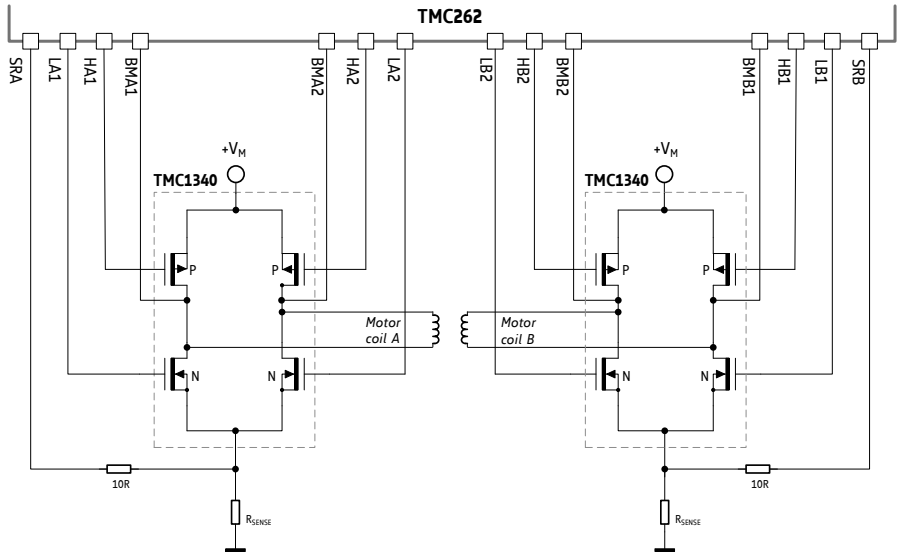
RoHS Compliant and Halogen-Free

Description

The TMC1340-SO N & P channel MOSFET full bridge (H-bridge) device achieves a very low on-state resistance combined with fastest switching performance. This device is intended for power conversion and power management applications that require high energy efficiency and power density while keeping costs down.

The SO-8 5x6 package is widely used for commercial and industrial surface-mounted applications, and it is well suited for, e.g., motor driver circuits.

TMC262 with 4x TMC1340-SO MOSFETs



Order code	Description	Size
TMC1340-SO	N and P-channel enhancement mode power MOSFET	5 x 6 mm²

TRINAMIC Motion Control GmbH & Co. KG
Hamburg, Germany

TRINAMIC MOTION CONTROL

Table of Contents

1 Pin Assignments

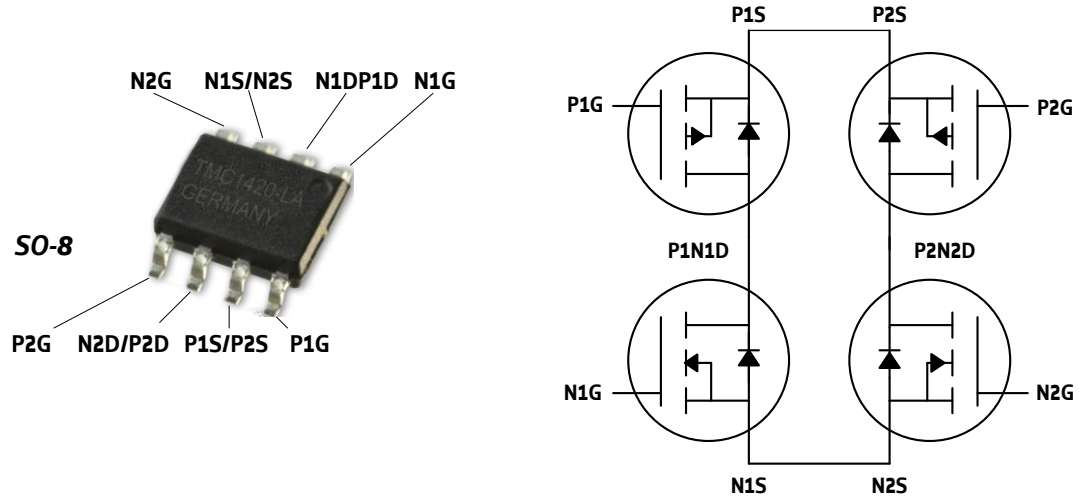


Figure 1.1 TMC1340-SO pin assignments and internal circuit

2 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances. Operating the circuit at or near more than one maximum rating at a time for extended periods shall be avoided by application design.

Parameter	Symbol	N-channel	P-channel	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current*[2]	I_D@T_A = 25°C	5.5	-4.1	A
Continuous Drain Current*[2]	I_D@T_A = 70°C	4.4	-3.3	A
Pulsed Drain Current*[1]	I_{DM}	20	-20	A
Total Power Dissipation	P_D@T_A = 25°C	1.38		W
Storage Temperature Range	T_{STG}	-55 to 150		°C
Operating Junction Temperature Range	T_J	-55 to 150		°C

*[1] Pulse width is limited by maximum junction temperature.
*[2] Surface mounted on 1 in² copper pad of FR4 board, t ≤ 10sec; 186°C/W when mounted on min. copper pad.

3 Thermal Data

Parameter	Symbol	Value	Unit
Max. Thermal Resistance, Junction-ambient*	Rthj-a	90	°C/W

* Surface mounted on 1 in² copper pad of FR4 board, t ≤ 10sec; 186°C/W when mounted on min. copper pad.

4 Electrical Characteristics

4.1 N-CH @t_j=25°C *(unless otherwise specified)*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250µA	30			V
Static Drain-Source On-Resistance*	$R_{DS(ON)}$	V_{GS}=10V, I_D=5A V_{GS}=4.5V, I_D=3A			33 60	mΩ mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250µA	1		3	V
Forward Transconductance	g_{fs}	V_{DS}= 10V, I_D=5A		5.2		S
Drain-Source Leakage Current	I_{DSS}	V_{DS}= 30V, V_{GS}=0V			1	µA
Drain-Source Leakage Current (t_j=70°C)		V_{DS}= 24V, V_{GS}=0V			25	µA
Gate-Source Leakage	I_{GSS}	V_{DS}= 0V, V_{GS}=±20V			±100	nA
Total Gate Charge	Q_g	I_D=5A		7	10	nC
Gate-Source Charge	Q_{gs}	V_{DS}=15V		2		nC
Gate-Drain ("Miller") Charge	Q_{gd}	V_{GS}=4.5V		4		nC
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=15V		7		ns
Rise Time	t_r	I_D=1A		10		ns
Turn-off Delay Time	$t_{d(off)}$	R_G=6Ω, V_{GS}=10V		18		ns
Fall Time	t_f	R_D=15Ω		8		ns
Input Capacitance	C_{iss}	V_{GS}=0V		600	960	pF
Output Capacitance	C_{oss}	V_{DS}=25V		229.8		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0MHz		94		pF

* Pulse width ≤ 300µs, duty cycle ≤ 2%

4.1.1 Source-Drain Diode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward On Voltage*	V_{SD}	V_{GS}=0V, I_S=1.2A			1.2	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V, I_S=1.7A		21		ns
Reverse Recovery Charge	Q_{rr}	dI/dt=100A/µs		16		nC

* Pulse width ≤ 300µs, duty cycle ≤ 2%

4.2 P-CH @t_j=25°C *(unless otherwise specified)*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250µA	-30			V
Static Drain-Source On-Resistance*	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-4A V_{GS}=-4.5V, I_D=-2A			55 100	mΩ mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250µA	-1		-3	V
Forward Transconductance	g_{fs}	V_{DS}= -10V, I_D=-4A		4		S
Drain-Source Leakage Current	I_{DSS}	V_{DS}= -30V, V_{GS}=0V			-1	µA
Drain-Source Leakage Current (t_j=70°C)		V_{DS}= -24V, V_{GS}=0V			-25	µA
Gate-Source Leakage	I_{GSS}	V_{DS}= 0V, V_{GS}=±20V			±100	nA
Total Gate Charge	Q_g	I_D=-4A		8	11	nC
Gate-Source Charge	Q_{gs}	V_{DS}=-24V		1.5		nC
Gate-Drain ("Miller") Charge	Q_{gd}	V_{GS}=-4.5V		4		nC
Turn-on Delay Time*	$t_{d(on)}$	V_{DS}=-15V		6.6		ns
Rise Time	t_r	I_D=-1A		7.7		ns
Turn-off Delay Time	$t_{d(off)}$	R_G=3.3Ω V_{GS}=-10V		22		ns
Fall Time	t_f	R_D=15Ω		9.3		ns
Input Capacitance	C_{iss}	V_{GS}=0V		570	790	pF
Output Capacitance	C_{oss}	V_{DS}=-25V		80		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0MHz		75		pF
Gate Resistance	R_g	f=1.0MHz		6	12	Ω

* Pulse width ≤ 300µs, duty cycle ≤ 2%

4.2.1 Source-Drain Diode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward On Voltage*	V_{SD}	V_{GS}=0V, I_S=-1.2A			-1.2	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V, I_S=-4A		18		ns
Reverse Recovery Charge	Q_{rr}	dI/dt=100A/µs		10		nC

* Pulse width ≤ 300µs, duty cycle ≤ 2%

5 N-Channel Diagrams

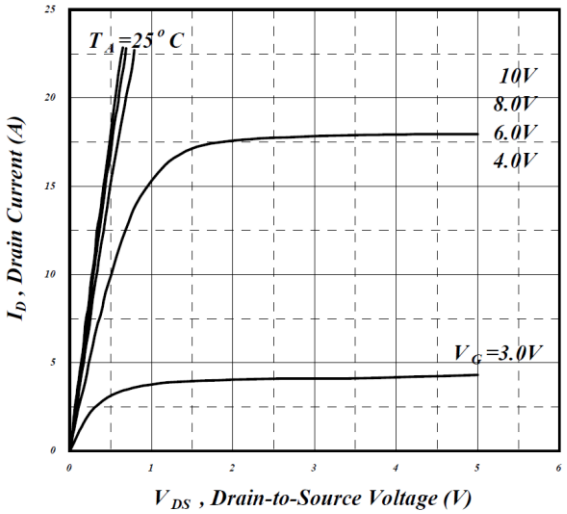


Figure 5.1 Typical output characteristics

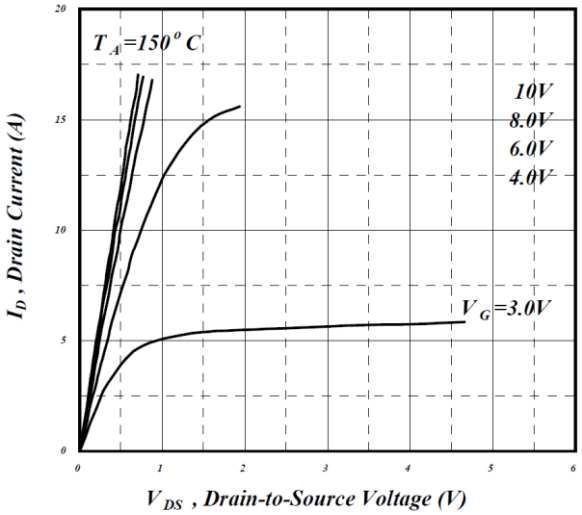


Figure 5.2 Typical output characteristics

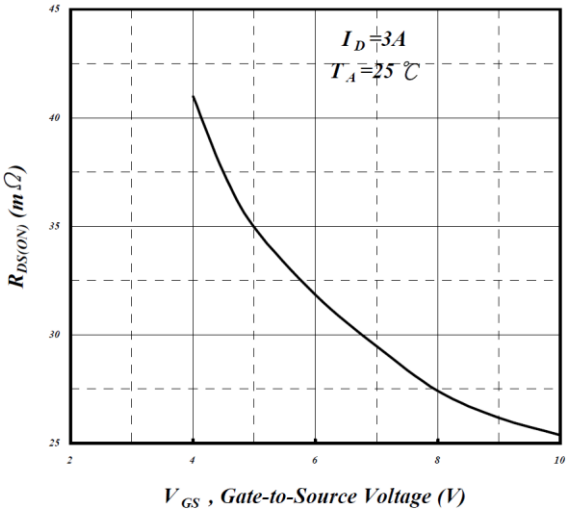


Figure 5.3 On-resistance v.s. gate voltage

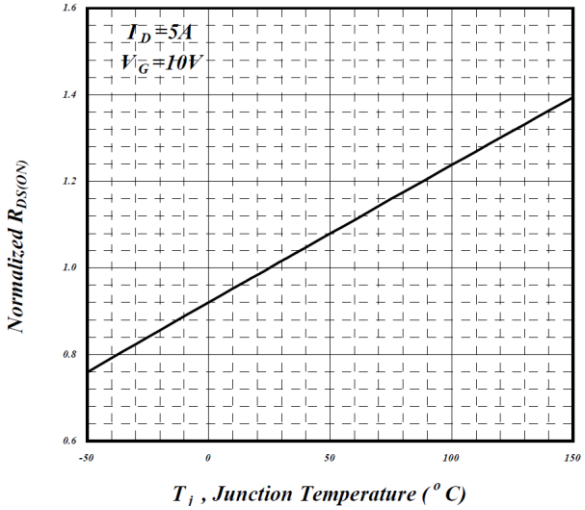


Figure 5.4 Normalized on-resistance v.s. junction temperature

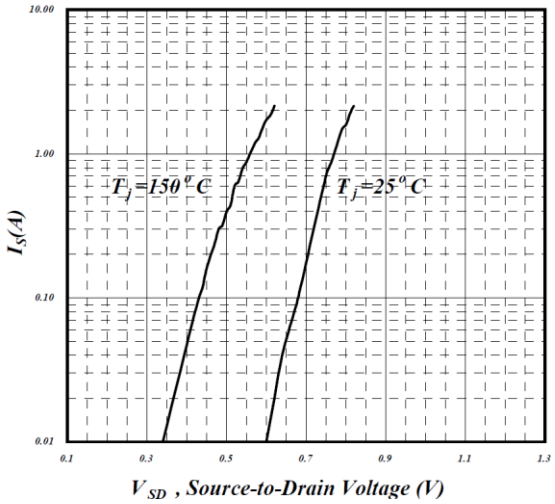


Figure 5.5 Forward characteristic of reverse diode

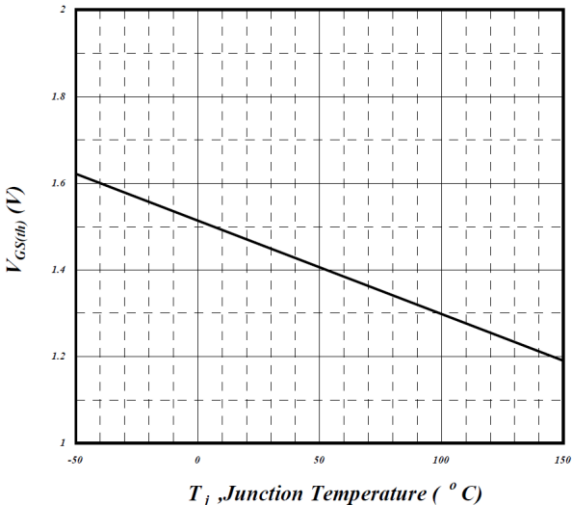


Figure 5.6 Gate threshold voltage v.s. junction temperature

N-Channel Diagrams

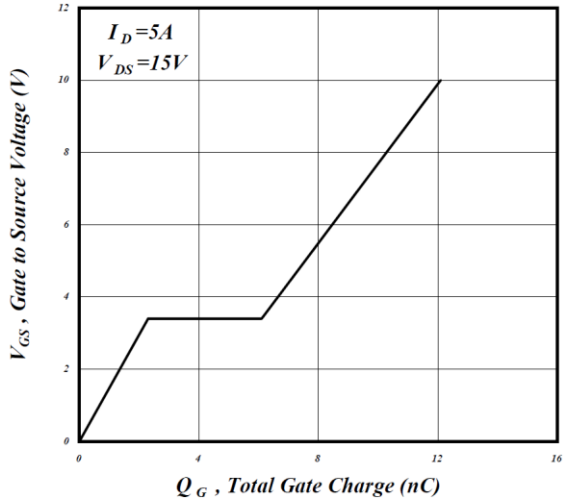


Figure 5.7 Gate charge characteristics

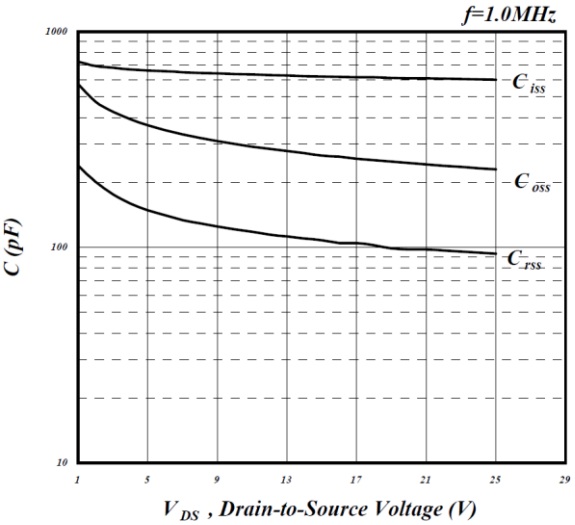


Figure 5.8 Typical capacitance characteristics

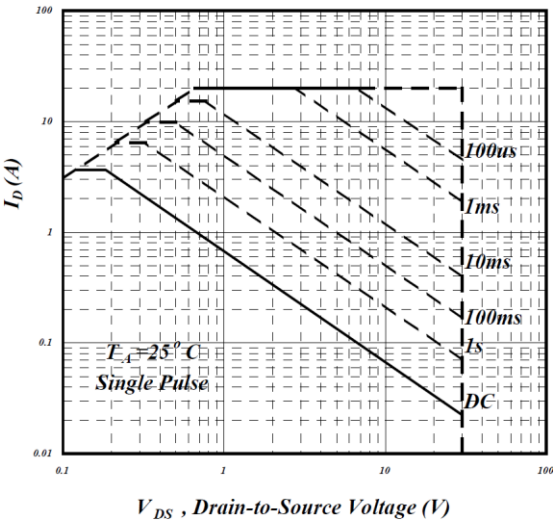


Figure 5.9 Maximum safe operating area

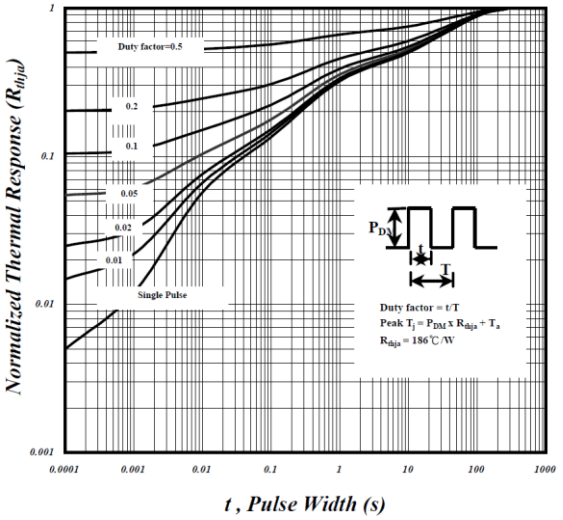


Figure 5.10 Effective transient thermal impedance

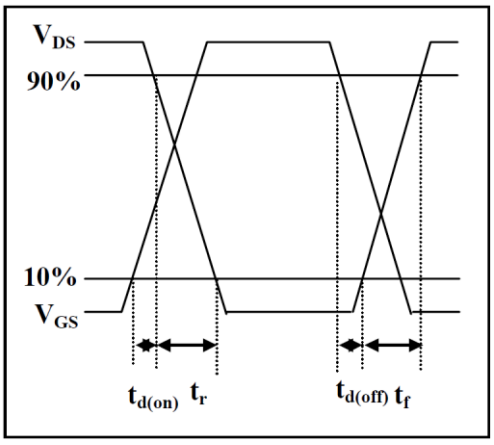


Figure 5.11 Switching time waveforms

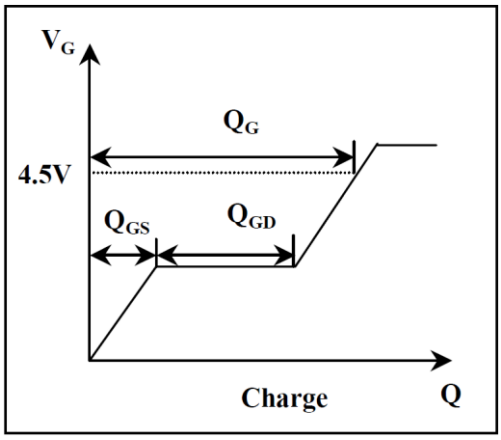


Figure 5.12 Gate Charge waveform

6 P-Channel Diagrams

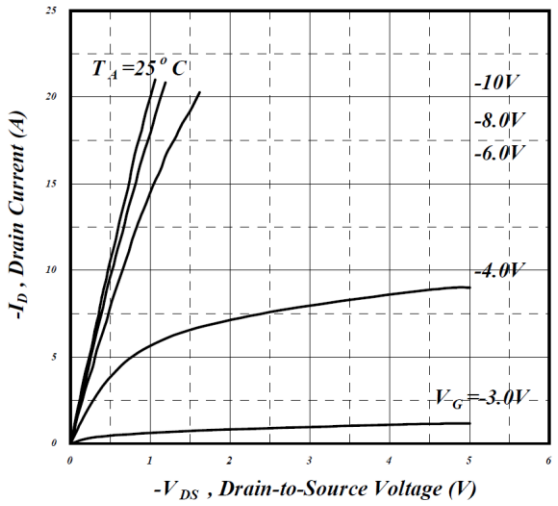


Figure 6.1 Typical output characteristics

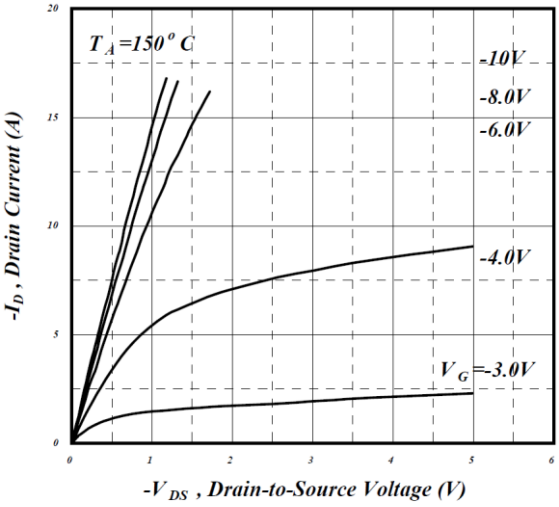


Figure 6.2 Typical output characteristics

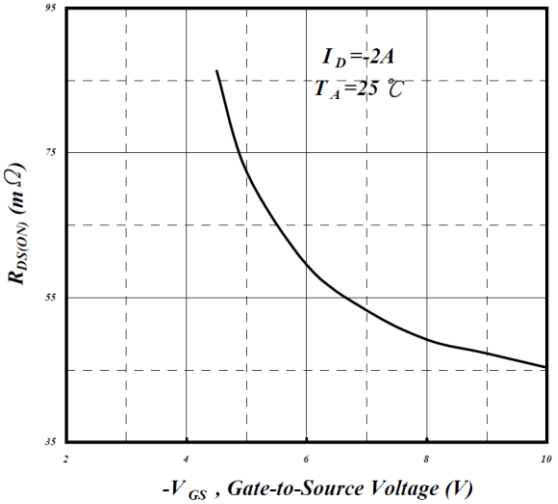


Figure 6.3 On-resistance v.s. gate voltage

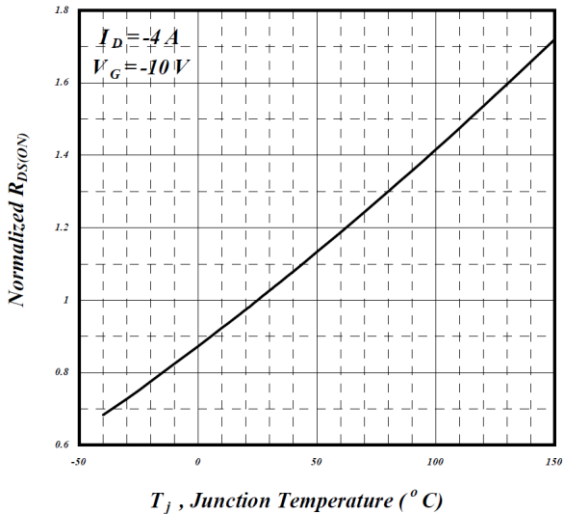


Figure 6.4 Normalized on-resistance v.s. junction temperature

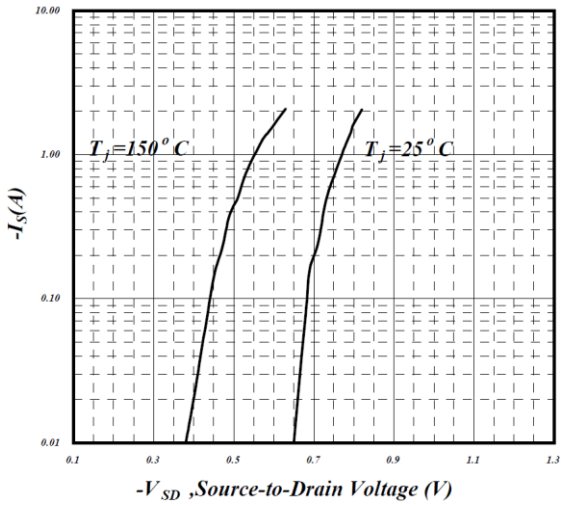


Figure 6.5 Forward characteristic of reverse diode

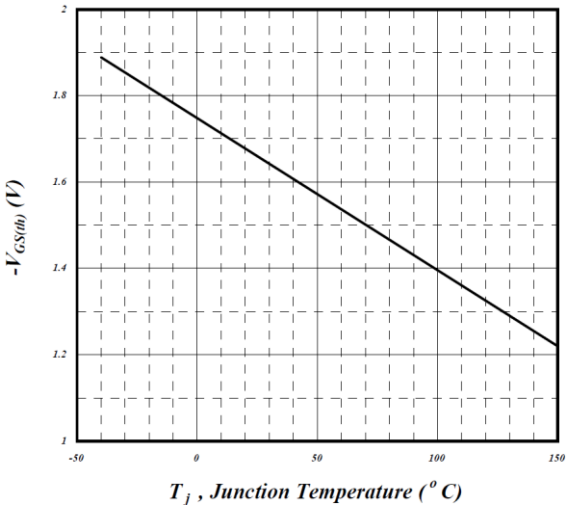


Figure 6.6 Gate Threshold voltage v.s. junction temperature

P-Channel Diagrams

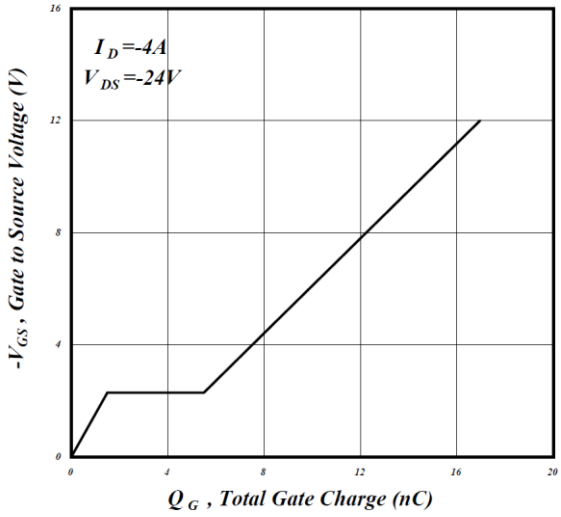


Figure 6.7 Gate charge characteristics

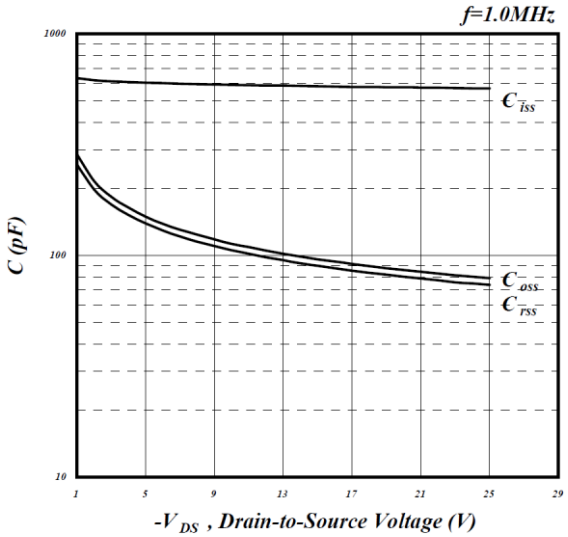


Figure 6.8 Typical capacitance characteristics

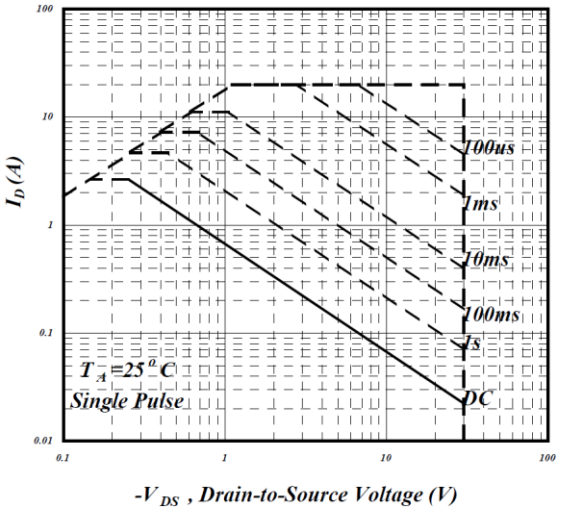


Figure 6.9 Maximum safe operating area

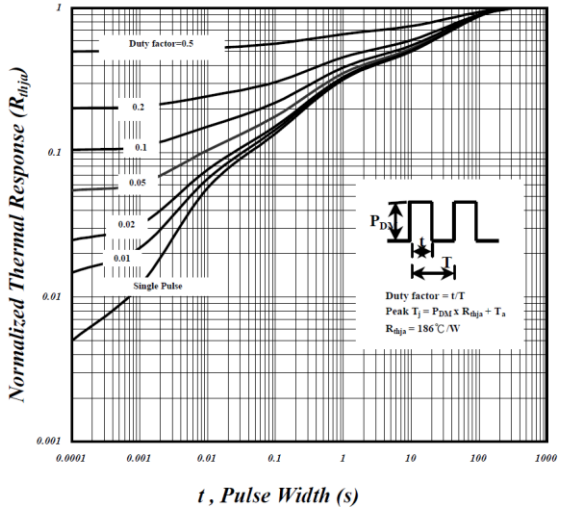


Figure 6.10 Effective transient thermal impedance

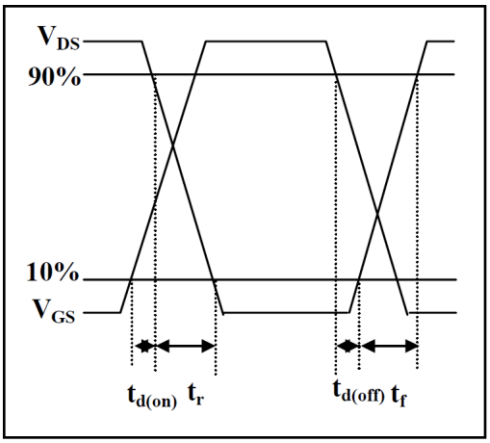


Figure 6.11 Switching time waveforms

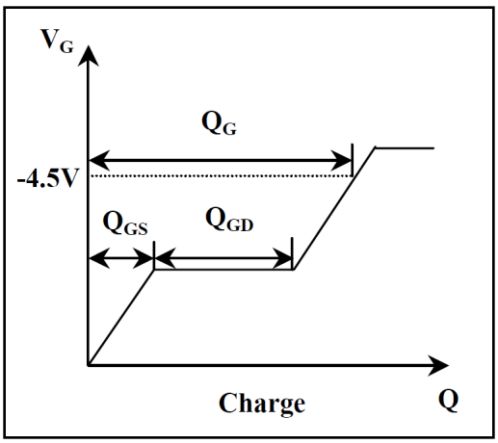
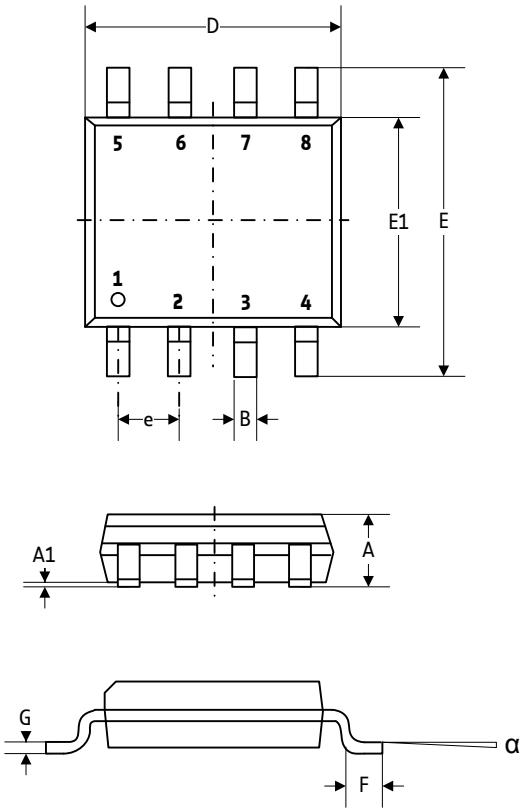


Figure 6.12 Gate charge waveform

7 Package Mechanical Data

7.1 PQFN 5x6 Dimensional Drawings



Note:
All dimensions are in millimeters.
Drawings are not to scale.
The dimensions do not include mold protrusions.

Symbols	Min	Nom	Max
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
D	4.80	4.90	5.00
E	5.80	6.15	6.50
E1	3.80	3.90	4.00
e		1.27 TYP	
G	0.19	0.22	0.25
F	0.38	0.71	1.27
α	0°	4°	8°

Figure 7.1 Dimensional drawings

7.2 Package Marking Information

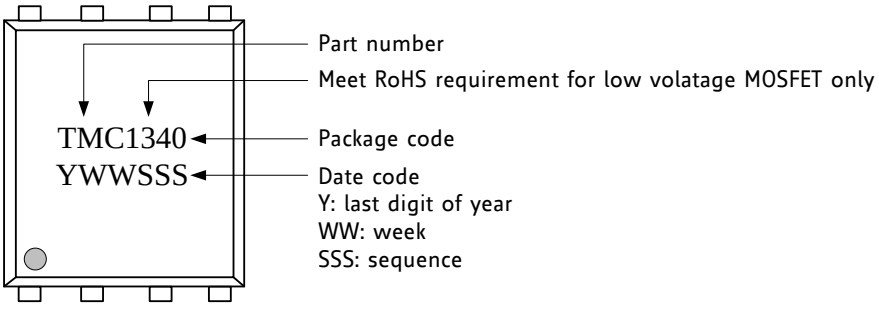


Figure 7.2 Package marking information

7.3 Package Code

Device	Package	Temperature range	Code/ Marking
TMC1340	PQFN 5x6	-55° to +150°C	TMC1340-SO

8 Disclaimer

TRINAMIC Motion Control GmbH & Co. KG does not authorize or warrant any of its products for use in life support systems, without the specific written consent of TRINAMIC Motion Control GmbH & Co. KG. Life support systems are equipment intended to support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.

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9 ESD Sensitive Device

The TMC1340-SO is an ESD sensitive CMOS device sensitive to electrostatic discharge. Take special care to use adequate grounding of personnel and machines in manual handling. After soldering the devices to the board, ESD requirements are more relaxed. Failure to do so can result in defect or decreased reliability.

10 Table of Figures

11 Revision History

Version	Date	Author SD – Sonja Dwersteg	Description
1.00	2013-MAR-18	SD	Initial version
1.01	2014-MAY-19	SD	Dimensional drawings updated.
1.02	2014-JUN-06	SD	Block diagram on front page corrected.

Table 11.1 Documentation revisions