TMC2491A

Digital Video Encoder with Macrovision™ Copy Protection

Features

- Macrovision™ Copy Protection Signal Processing
- All-Digital Video Encoding
- Internal Digital Synthesizer For Subcarrier Frequency Generation
- 8-Bit Parallel CCIR-601 / SMPTE 170M Format
- Closed Caption Data Insertion
- Switchable Chrominance Bandwidth
- Switchable Pedestal With Gain Compensation
- Pre-Programmed Horizontal And Vertical Timing
- 13.5 Mpps Pixel Rate
- Synchronizes To Incoming Data Stream
- Master Timing Generator Mode
- Internal Interpolation Filters Simplify Output Reconstruction Filters
- 9-Bit D/A Converters For Video Reconstruction
- Supports NTSC And PAL Standards
- Simultaneous S-Video (Y/C) Output
- Controlled Edge Rates
- Parallel And Serial Control Interface
- JTAG (IEEE Std 1149.1-1990) Test Interface
- Single +5V Power Supply
- 44 Lead PLCC Package

Applications

- Settop Digital Cable Television Receivers
- Settop Digital Satellite Television Receivers

Description

The TMC2491A video encoder converts digital component video (in 8-bit parallel CCIR-601 or ANSI/SMPTE 125M format) into a standard analog baseband television (NTSC, NTSC-EIA, all PAL standards) signal with a modulated color subcarrier. Both composite (single lead) and S-Video (separate chroma and luma) formats are active simultaneously at the three analog outputs.

The TMC2491A includes all of the features of the TMC2490A Digital Video Encoder, plus Macrovision™ copy protection signal processing. This datasheet is an addendum to the TMC2490A specification.

Block Diagram

Rev. 1.0.0
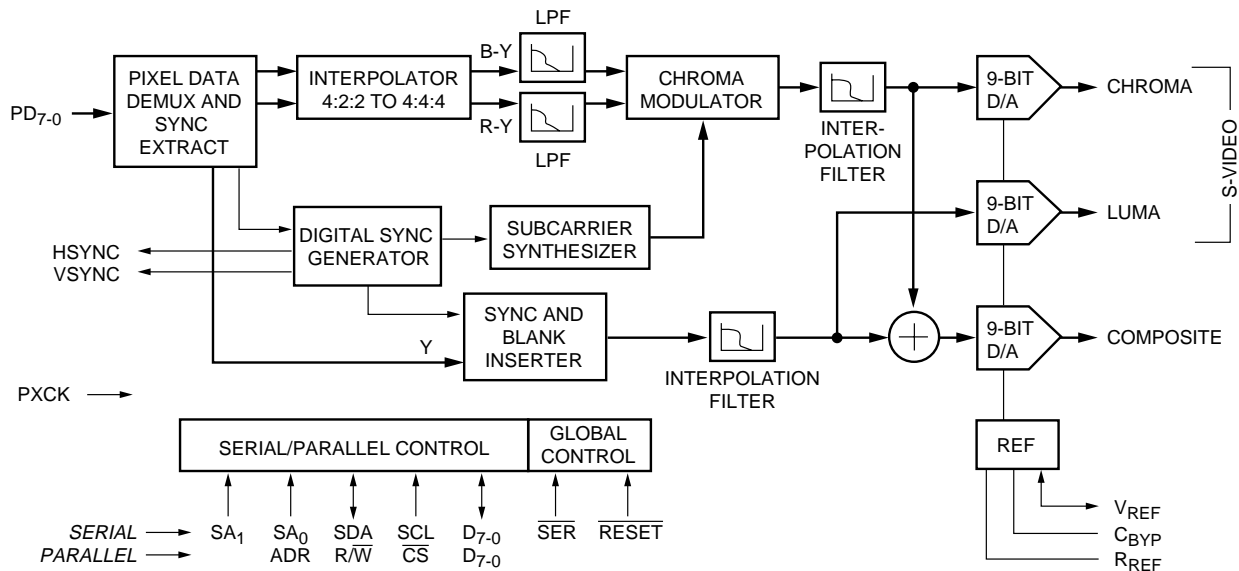
General Description

The TMC2491A can modify the analog composite and S-video signal in accordance with the Macrovision copy protection process, Revision 6.1. The outgoing video signal is altered is several ways:

1. Color burst inversion

2. Pseudo-sync (p-sync) pulses

3. AGC pulses

4. Back porch pulses before and after vertical sync

5. Elevated sync tip and blanking levels

The purpose of these alterations to the standard NTSC and PAL video signals is to render the modified video unrecordable and, therefore, copy protected.

Colorstripe Process

The color burst phase may be inverted for selected lines and groups of lines for odd and even fields (Figure 1). The starting line for each of two groups of lines in each of two fields is controlled via control register values The number of inverted phase lines in each group, the number of groups, and the spacing of groups are also controlled parameters.

A combination of eight bits jointly disable Colorstripe processing when set to a particular state: in all other 255 states, Colorstripe is enabled. To disable Colorstripe, set bit 7 HIGH and bit 6 LOW in registers 10, 11, 12, and 13.

Pseudo-Sync (p-sync) and AGC Pulse Pairs

Negative-going "p-sync" pulses extending from blanking to the Macrovision sync level of -30 IRE/-240mV (NTSC/PAL) are inserted on certain lines in the vertical field group. Positive-going "AGC" pulses extending from blanking to 117 IRE/800mV accompany each p-sync pulse. The location, duration, and spacing of these p-sync/AGC pulse pairs are controlled via control register settings. The lines on which

the p-sync/AGC pulse pairs are inserted are also selected by the control registers. The duration of the AGC pulse is fixed at 2.7 microseconds. Figure 2 shows a horizontal line with four p-sync/AGC pulse pairs.

Data Transmission mode is a technique for low-bandwidth communication through the presence or absence of the p-sync and AGC pulses. In Data Transmission mode, the p-sync and AGC pulse pairs may be turned off and on independently, and the amplitude of the AGC pulses is limited to 20 IRE/150mV above blanking.

Back Porch Pulses

Short pulses at the beginning of back porch segments are inserted on selected lines before and after vertical sync at the end of each field. These "back porch" pulses extend from blanking to 100 IRE/700mV and have a fixed duration of 2 microseconds. When applied to equalization pulses, the "back porch" pulses occur only after equalization pulses that follow the established H timing. Figure 3, Figure 4, and Figure 5 show back porch pulses just after equalization pulses.

Back porch pulses that coincide in time with color burst, shift that portion of the color burst that overlaps the back porch pulse. Figure 3 shows the "split" color burst.

Elevated Sync and Blanking

The TMC2491A can alter the amplitude of sync tips and blanking level. These levels are normally set to -40 and 0 IRE/-300 and 0mV respectively during the vertical blanking interval. The SYNC30 bit in the control register alters all sync tips and vertical interval blanking levels to -30 and +10 IRE/-240 and 60mV respectively (Macrovision defaults). The sync tip and blanking levels for active video lines remain at the standard levels.
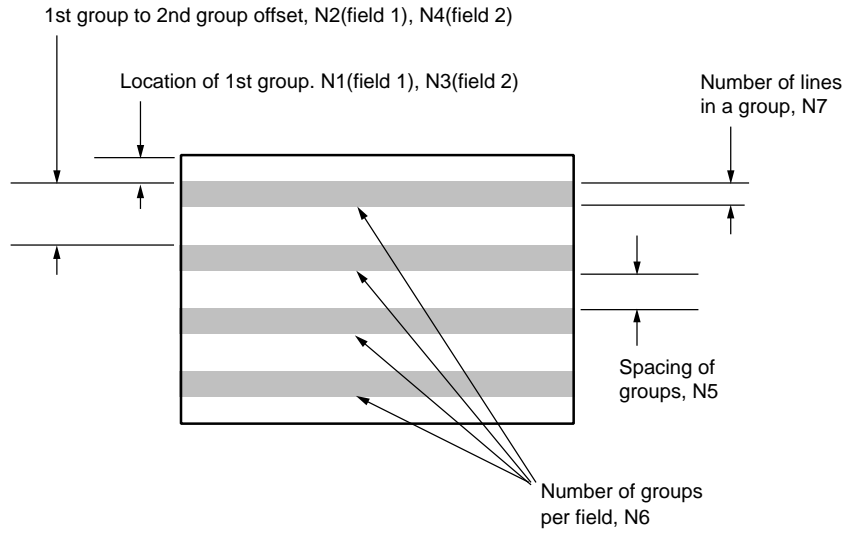
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1st group to 2nd group offset, N2(field 1), N4(field 2)

Location of 1st group. N1(field 1), N3(field 2)

Number of lines
in a group, N7

Spacing of
groups, N5

Number of groups
per field, N6

Figure 1. Location of Color Stripe Lines And Groups

P-sync/AGC pulse pair

P-sync/AGC pulse spacing, N10

Color Burst

AGC pulse duration

Blanking
level

Horizontal Sync

P-sync duration, N8

Location of first p-sync/AGC
pulse pair, N9
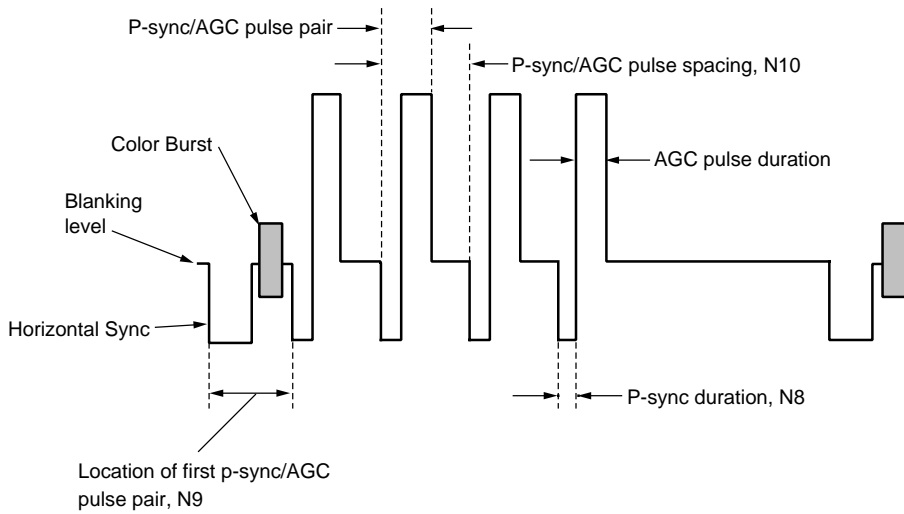
Figure 2. Pseudo-Sync and AGC Pulse Detail

Color Burst

Blanking level

Equalization
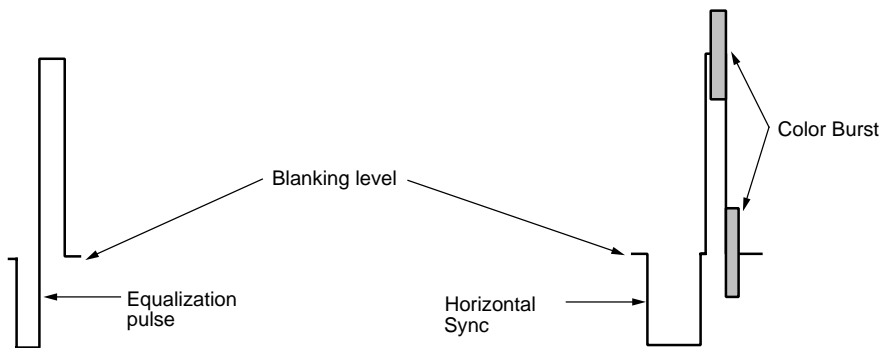pulse

Horizontal
Sync

Figure 3. Back Porch Pulse Detail

Control Registers

The TMC2490A is initialized and controlled by a set of registers which determine the operating modes.

An external controller is employed to write and read the Control Registers through either the 8-bit parallel or 2-line serial interface port. The parallel port, D7-0, is governed by pins $\overline{CS}$, R/$\overline{W}$, and ADR. The serial port is controlled by SDA and SCL.

Table 1. Control Register Map — Changes/Additions to the TMC2490

Reg	Bit	Mnemonic	Function
TMC2491A Identification Registers			
00	7-0	PARTID2	(Read only = 94h)
01	7-0	PARTID1	(Read only = 24h)
02	7-0	PARTID0	(Read only = 91h)
03	7-0	REVID	(Read only = revision #)
Encoder Control Registers			
04-0F	7-0	Controls	Same as in TMC2490
Macrovision Control Registers			
10	7-6	DBI$_{7-6}$	Phase inversion enable bits
10	5-0	N1	1st inverse phase line, 1st group, 1st field
11	7-6	DBI$_{5-4}$	Phase inversion enable bits
11	5-0	N2	1st inverse phase group to 2nd group offset, 1st field
12	7-6	DBI$_{3-2}$	Phase inversion enable bits
12	5-0	N3	1st inverse phase line, 1st group, 2nd field
13	7-6	DBI$_{1-0}$	Phase inversion enable bits
13	5-0	N4	1st inverse phase group to 2nd group offset, 2nd field
14	7-6	N7	No. lines per stripe group
14	5-3	N6	Number of phase inversion groups per field
14	2-0	N5	Phase inversion group spacing
15	7-6	reserved	
15	5-3	N8A	P-sync duration, A
15	2-0	N8B	P-sync duration, B

Reg	Bit	Mnemonic	Function
16	7	PULSE	Pulse / static select
16	6	reserved	
16	5-3	N9A	P-sync/AGC location, A
16	2-0	N9B	P-sync/AGC location, B
17	7	reserved	
17	6	SYNC30	Sync tip and blanking level
17	5-3	N10A	P-sync/AGC spacing, A
17	2-0	N10B	P-sync/AGC spacing, B
18	7-0	XMIT	Data transmit mode
19	7	reserved	
19	6-0	PSPAGC 14-8	P-sync/AGC line enable, MSBs
1A	7-0	PSPAGC 7-0	P-sync/AGC line enable, LSBs
1B	7-0	PSAGAB 14-8	P-sync/AGC pattern select A/B, MSBs
1C	7-0	PSAGAB 7-0	P-sync/AGC pattern select A/B, LSBs
1D	7-0	PSAGPATA	P-sync/AGC pattern A
1E	7-0	PSAGPATB	P-sync/AGC pattern B
1F	7-4	BPP1	Pulsed lines before VSYNC
1F	3-0	BPP2	Pulsed lines after VSYNC

Notes:

1. Functions are listed in the order of reading and writing.
2. For each register listed above, all bits not specified are reserved and should be set to zero to ensure proper operation.

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Table 2. Control Register Definitions — Changes/Additions to the TMC2490A

Reg	Bit	Mnemonic	Function
TMC2491A Identification Registers (Read only)			
00	7-0	PARTID2	(Read only = 78h)
01	7-0	PARTID1	(Read only = 38h)
02	7-0	PARTID0	(Read only = 91h)
03	7-0	REVID	(Read only = revision #) This specification applies to TMC2491A circuits with REVID >= to 02h. See revision B of this document for circuits with REVID - 01h.
Encoder Control Registers			
04-0F	7-0	Controls	Same as in TMC2490
Macrovision Control Registers			
10	7-6	DBI_{7-6}	Phase inversion enable bits. Subcarrier phase inversion on a line group-by-line group basis is enabled whenever DBI_{7-0} is not set equal to AAh.
10	5-0	N1	The 6-bit N1 value determines the location of the 1st phase inversion line of the 1st group of inverse phase lines in the 1st field. The position of this line can be from 1 to 64 lines from VSYNC. The default value for N1 is 18 (22h) for NTSC and 48 (30h) for PAL.
11	7-6	DBI_{5-4}	Phase inversion enable bits
11	5-0	N2	The 6-bit N2 value determines the offset of the 2nd group of inverse phase lines with respect to the start of the 1st group in the 1st field. The position of this line can be from 1 to 64 lines from the start of the 1st group. The default value for N2 is 20 (14h) for NTSC and 32 (20h) for PAL.
12	7-6	DBI_{3-2}	Phase inversion enable bits
12	5-0	N3	The 6-bit N3 value determines the location of the 1st phase inversion line of the 1st group of inverse phase lines in the 2nd field. The position of this line can be from 1 to 64 lines from VSYNC. The default value for N3 is 18 (22h) for NTSC and 48 (30h) for PAL.
13	7-6	DBI_{1-0}	Phase inversion enable bits

Reg	Bit	Mnemonic	Function
13	5-0	N4	The 6-bit N4 value determines the offset of the 2nd group of inverse phase lines with respect to the start of the 1st group in the 2nd field. The position of this line can be from 1 to 64 lines from the start of the 1st group. The default value for N2 is 20 (14h) for NTSC and 32 (20h) for PAL.
14	7-6	N7	The number of phase inversion lines per group varies by (2 + N7). The 2-bit N7 value allows the number of inverse phase lines per group to vary from 2 to 5. The default value for N7 is 2 (0 in data mode).
14	5-3	N6	The number of phase inversion groups per field varies by (6+N6). The 3-bit N6 value allows the number of groups per field to vary from 6 to 13. The default value for N6 is 4 for NTSC and 3 for PAL.
14	2-0	N5	The spacing of groups varies by (16+N5) for NTSC and (12+N5) for PAL. The 3-bit N5 value allows the spacing of groups to vary from 16 to 23 for NTSC and from 12 to 19 for PAL. The default value for N5 is 4.
15	7-6	reserved	
15	5-3	N8A	The A-pattern duration of p-sync/AGC pulse pairs varies by: (24+(2xN8A)) for NTSC and (16+(2xN8A)) for PAL. The 3-bit N8A value allows the duration of p-sync/AGC pulse pairs to vary from 24 to 38 for NTSC and from 16 to 30 for PAL. The default value for N8A is 3 for NTSC and 4 for PAL.
15	2-0	N8B	The B-pattern duration of p-sync/AGC pulse pairs varies by: (24+(2xN8B)) for NTSC and (16+(2xN8B)) for PAL. The 3-bit N8B value allows the duration of P-sync/AGC pulse pairs to vary from 24 to 38 for NTSC and from 16 to 30 for PAL. The default value for N8B is 0 for NTSC and PAL.

Reg	Bit	Mnemonic	Function
16	7	PULSE	Pulse / static select. When HIGH, the AGC pulse amplitudes varies in accordance with Macrovision specifications. When LOW, the amplitude of the AGC pulses is constant.
16	6	reserved	
16	5-3	N9A	The A-pattern location of p-sync/AGC pulse pairs varies by: (96+(8xN9A)) for NTSC and PAL. The 3-bit N9A value allows the location of p-sync/AGC pulse pairs to vary from 96 to 152. The default value for N9A is 2 for NTSC and 3 for PAL.
16	2-0	N9B	The B-pattern location of p-sync/AGC pulse pairs varies by: (96+(8xN9B)) for NTSC and PAL. The 3-bit N9B value allows the location of p-sync/AGC pulse pairs to vary from 96 to 152. The default value for N9B is 0 for NTSC and PAL.
17	7	reserved	
17	6	SYNC30	When HIGH, sync tip and blanking levels are elevated +10 IRE to -30 and +10 IRE respectively, during the vertical blanking interval only. When LOW, sync tip and blanking levels are at their normal levels of -40 and 0 IRE respectively. Macrovision default = 1.
17	5-3	N10A	The A-pattern spacing of p-sync/AGC pulse pairs varies by: (88+(8xN10A)) for NTSC and (56+(8xN10A)) for PAL. The 3-bit N10A value allows the spacing of p-sync/AGC pulse pairs to vary from 88 to 144 for NTSC and from 56 to 112 for PAL. The default value for N10A is 3 for NTSC and PAL.

Reg	Bit	Mnemonic	Function
17	2-0	N10B	The B-pattern spacing of p-sync/AGC pulse pairs varies by: (88+(8xN10B)) for NTSC and (56+(8xN10B)) for PAL. The 3-bit N10B value allows the spacing of p-sync/AGC pulse pairs to vary from 88 to 144 for NTSC and from 56 to 112 for PAL. The default value for N10B is 0 for NTSC and PAL.
18	7-0	XMIT	Data transmit mode is enabled when register 18 = D1h. When data transmit mode is selected, AGC pulses are limited in amplitude to +20 IRE/150mV. Normal Macrovision pulse levels occur for all other combinations.
19	7	reserved	
19	6-0	PSPAGC $_{14-8}$	P-sync/AGC line enable, MSBs. Each bit of PSPAGC$_{14-0}$ enables P-sync/AGC pulse pairs for one line in each field. Bit N enables line (N + 7) and (N + 270) for N = 0 to 14. In PAL, (N + 7) and (N + 319) will have P-sync/AGC pulse pairs. The default value for register 19 is 3 (03h) for NTSC and 31 (1Fh) for PAL.
1A	7-0	PSPAGC $_{7-0}$	P-sync/AGC line enable, LSBs. The default value for register 1A is 252 (FCh) for NTSC and 248 (F8h) for PAL.
1B	7	reserved	
1B	6-0	PSAGAB $_{14-8}$	P-sync/AGC pattern A/B select, MSBs. Each bit of PSAGAB$_{14-0}$ selects P-sync/AGC pattern A (HIGH) or B (LOW) for one line per field. Mapping precisely matches that of PSPAGC$_{14-0}$. Default is 7FFFh, which selects pattern A on all lines.
1C	7-0	PSAGAB $_{7-0}$	P-sync/AGC pattern A/B select, LSBs. Each bit of PSAGAB$_{14-0}$ selects P-sync/AGC pattern A (HIGH) or B (LOW) for one line per field. Mapping precisely matches that of PSPAGC$_{14-0}$. Default is 7FFFh, which selects pattern A on all lines.

Reg	Bit	Mnemonic	Function
1D	7-0	PSAGPATA	P-sync/AGC pattern A. These 8 bits determine which of up to 8 p-sync/AGC pulse pairs are enabled or suppressed for each line. If the Nth bit is HIGH, the Nth pulse pair will be active. If the Nth bit is LOW, the Nth p-sync pulse pair will be suppressed.
1E	7-0	PSAGPATB	P-sync/AGC pattern B. These 8 bits determine which of up to 8 p-sync/AGC pulse pairs are enabled or suppressed for each line. If the Nth bit is HIGH, the Nth pulse pair will be active. If the Nth bit is LOW, the Nth p-sync pulse pair will be suppressed.

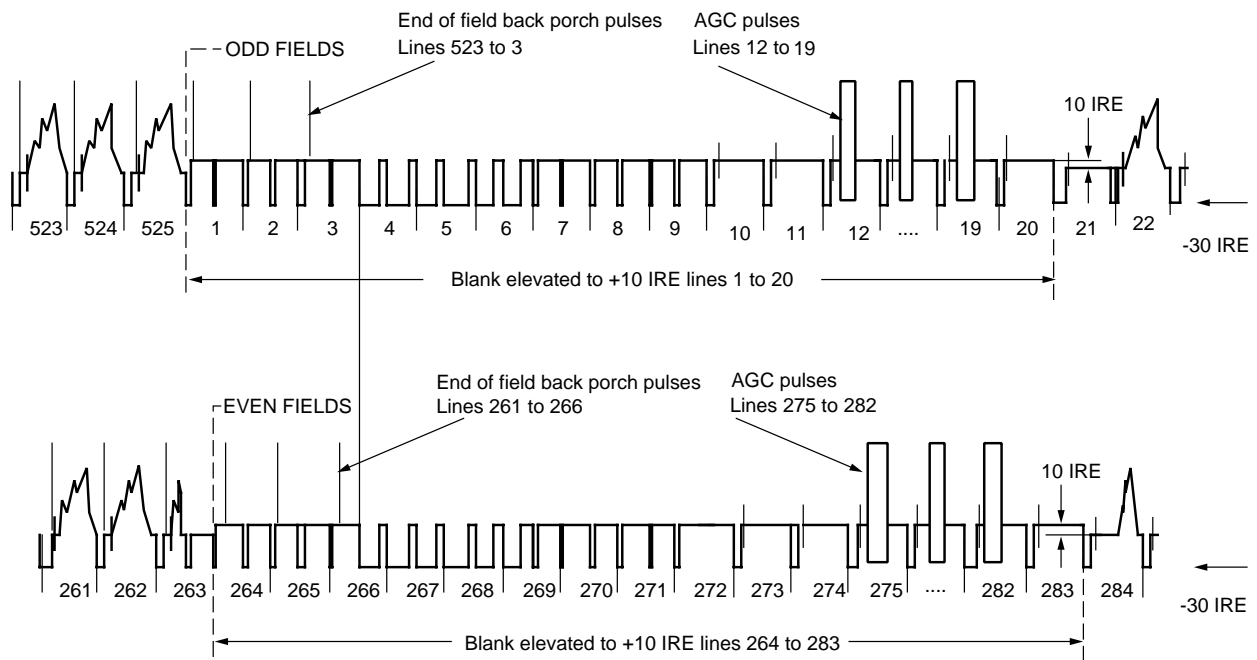| Reg	Bit	Mnemonic	Function
1F	7-4	BPP1	This 4-bit value determines the number of lines before VSYNC that have back porch pulses. See Table 3.
1F	3-0	BPP2	This 4-bit value determines the number of lines after VSYNC that have back porch pulses. See Table 3.

Figure 4. 525/60 (NTSC, PAL-M) Vertical Interval With Macrovision Copy Protection Process
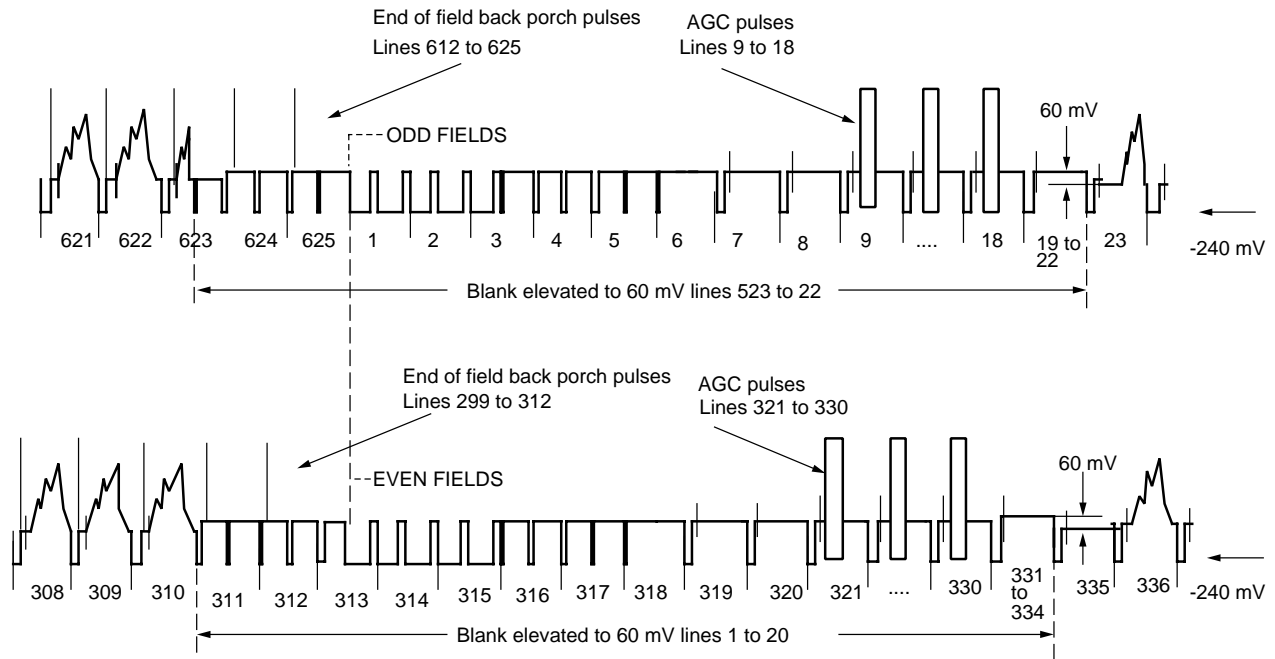
Figure 5. 625/50 (PAL-B,G,H,I,N) Vertical Interval With Macrovision Copy Protection Process

Table 3. Lines With Back Porch Pulses Determined By BPP1 And BPP2

BPP 4-bit value	NTSC		PAL	
	BPP1 lines before VSYNC	BPP2 lines after VSYNC	BPP1 lines before VSYNC	BPP2 lines after VSYNC
0	none	none	none	none
1	3, 266	7, 270	312, 625	4, 316
2	2, 3, 255, 266	7, 8, 270, 271	311, 312, 624, 625	4, 5, 316, 317
3	1-3, 264-266	7-9, 270-272	310-312, 623-625	4-6, 316-318
4	525, 1-3, 263-266	7-10, 270-273	309-312, 622-625	4-7, 316-319
N	(529-N) to 525, 1-3, (267-N) to 266	7 to (6+N), 270 to (269+N)	(313-N) to 312, (626-N) to 625	4 to (3+N), 316 to (315+N)

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Table 4. Default Parameters For Macrovision Copy Protection Process

| Register | Enabled | | | | Disabled | |
| | NTSC (Power-Up Default) | | PAL | | NTSC/PAL | |
	Binary	HEX	Binary	HEX	Binary	HEX
10	11010010	D2	10110000	B0	10XXXXXX	8X-BX
11	10010100	94	10100000	A0	10XXXXXX	8X-BX
12	00010010	12	10110000	B0	10XXXXXX	8X-BX
13	11010100	D4	10100000	A0	10XXXXXX	8X-BX
14	10100100	A4	10011100	9C	00000000	00
15	00011000	18	00100000	24	00XXXXXX	0X-3X
16	10010000	90	10011000	9B	00000000	00
17	01011 00	58	11011000	DB	00000000	00
18	01000000	40	00000000	00	00000000	00
19	00000011	03	00011111	1F	00000000	00
1A	11111100	FC	11111000	F8	00000000	00
1B	11110000	F0	11111100	FC	00000000	00
1C	11110000	F0	11111100	FC	00000000	00
1D	00000000	00	00000000	FC	00000000	00
1E	00000000	00	00000000	FC	00000000	00
1F	01100011	60	01110111	77	00000000	00

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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2491AR2C	0°C to 70°C	Commercial	44-Lead PLCC	2491AR2C

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