TMC389–DATASHEET

Energy saving high resolution microstepping three phase stepper driver with step and direction interface and external power stage

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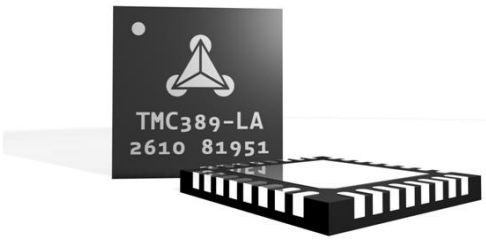

coolStep™

3 PHASE STEPPER

1 Features

The TMC389 is an energy efficient three phase stepper motor driver for high resolution microstepping applications. It integrates a low resonance three phase chopper for quiet motor operation. Its step and direction interface allows simple use. An SPI™ management interface allows for parameterization and diagnostics. The TMC389 directly drives 3 external N/P channel dual MOSFETs for motor currents up to 8A and up to 60V. Protection and diagnostic features further reduce system cost and increase reliability.

Highlights

- Up to 171 microsteps (256 sine wave steps) using step/direction interface or 20 Bit SPI™ interface
- High precision sensorless motor load measurement stallGuard2
- Energy efficiency and coolness by automatic load dependant motor current regulation coolStep™: Save up to 75% of energy!
- Internal microstep extrapolation allows 256 wave step smoothness with low frequency step input
- Dual edge step option allows half step frequency requirement, e.g. for opto-couplers
- Up to 8A Motor current using external N&P channel MOSFET pairs
- Synchronous rectification reduces transistor heating
- 9V to 60V operating voltage (peak)
- 3.3V or 5V interface
- QFN32 package for extremely small solution with superior thermal performance
- EMV optimized current controlled gate drivers – up to 45mA gate current
- Overcurrent, short to GND and overtemperature protection and diagnostics integrated

Applications

- Precision three phase stepper motor drives
- Stage lighting
- Medical applications
- Optical applications
- Robotics

Motor type

- 3 phase Stepper

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2.1 Disclaimer

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3 Principle of operation

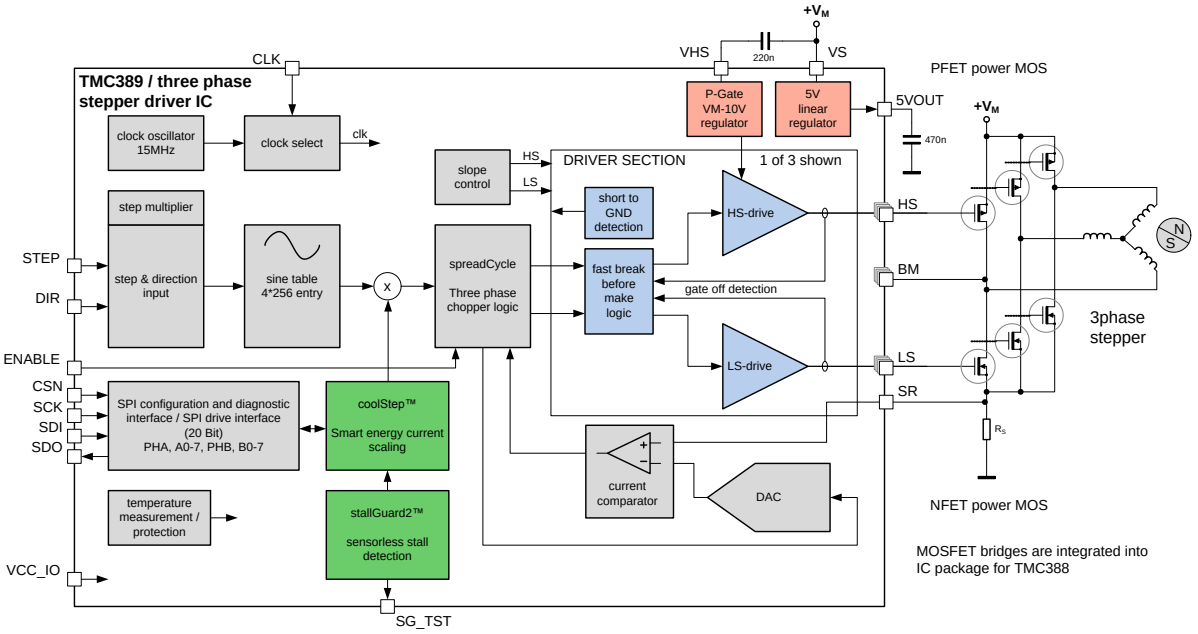


figure 1: Basic application block diagram

3.1 Moving the motor

3.1.1 Step and direction control

The TMC389 is a chopped stepper motor driver with integrated sequencer and SPI interface. It provides two possibilities to control the motor: The motor can be controlled by applying pulses on the step and direction interface, following an initialization phase which uses the SPI interface to parameterize the driver for the application. Control and diagnostic registers give the flexibility to react to changing operation conditions and to modify the behavior of the chip when it receives a step impulse. An internal microstep table supplies sine and cosine values which control the motor current for each step. Each step impulse advances the step pointer in the tables and hence leads to the IC executing the next microstep.

3.1.2 SPI control

A second mode of operation uses the SPI interface, only. The motor coil currents can be controlled via the SPI interface, while taking advantage of all other control and diagnostic functions. This mode is more flexible, as the microstep waves can be specially adapted to the motor to give the best fit for smoothest operation. It requires slightly more CPU overhead to look up the driver tables and to send out new current values for both coils. The SPI update rate corresponds to the step rate at low velocities. At highest velocities the update rate can be limited to a few 10kHz or some 100kHz, depending on the processor power, or alternatively to an update rate corresponding to a fullstep.

3.2 Chopped motor coil driver

The driver use a cycle by cycle chopper mode: The motor current becomes regulated by comparing the motor current to a set value for each chopper cycle. This constant off time chopper scheme allows highest dynamic. The spreadCycle chopper scheme automatically integrates a fast decay cycle and guarantees smooth zero crossing performance. In an optional operation mode, fast decay length per cycle can be selected by the user. In this classic constant off time mode, zero crossing can be optimized by setting a programmable current offset.

3.3 Energy efficient driver with load feedback

The TMC389 integrates a high resolution load measurement stallGuard2™, which allows sensing the mechanical load on the motor. This gives more information on the drive allowing functions like sensorless homing. Its coolStep™ feature uses load measurement information to reduce the motor current to the minimum motor current required in the actual load situation. This saves lots of energy and keeps components cool, making the drive an efficient and precise solution.

4 Pinning

4.1 TMC389-LA

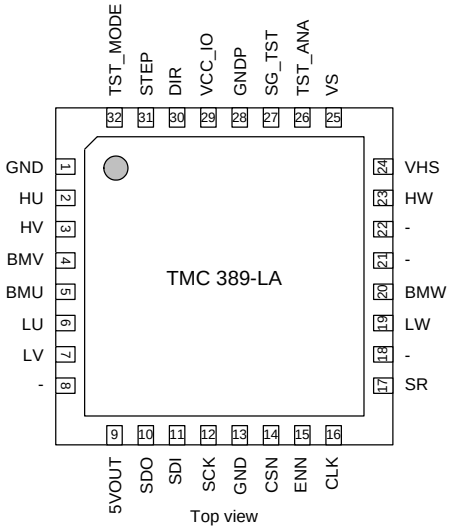


figure 2: TMC389 pinning

4.2 Package codes

Type	Package	Temperature range	Code/marking
TMC389	QFN32 (ROHS)	-40°C ... +125°C	TMC389-LA
TMC389 eng. sample	QFN32 (ROHS)	-40°C ... +125°C	TMC389-ES

4.3 Dimensional drawings

For drawings, see next page.
Attention: Drawings not to scale.

4.3.1 QFN32 dimensions

Parameter	Ref	Min	Nom	Max
total thickness	A	0.80	0.85	0.90
stand off	A1	0.00	0.035	0.05
mold thickness	A2	-	0.65	0.67
lead frame thickness	A3		0.203	
lead width	b	0.2	0.25	0.3
body size X	D		5.0	
body size Y	E		5.0	
lead pitch	e		0.5	
exposed die pad size X	J	3.2	3.3	3.4
exposed die pad size Y	K	3.2	3.3	3.4
lead length	L	0.35	0.4	0.45
package edge tolerance	aaa			0.1
mold flatness	bbb			0.1
coplanarity	ccc			0.08
lead offset	ddd			0.1
exposed pad offset	eee			0.1

All dimensions are in mm.

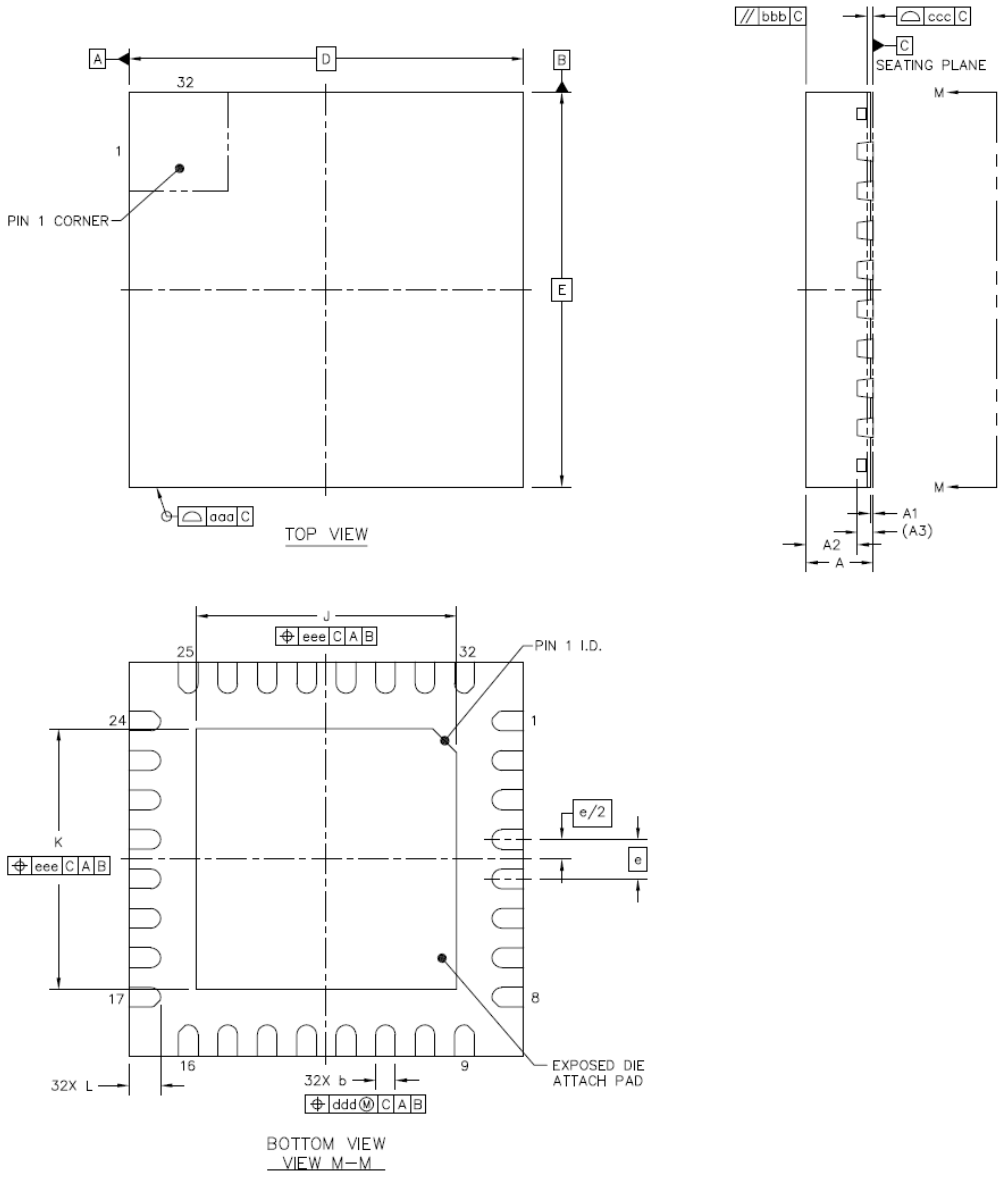


figure 3: QFN32 5x5 dimensions

5 Block diagram

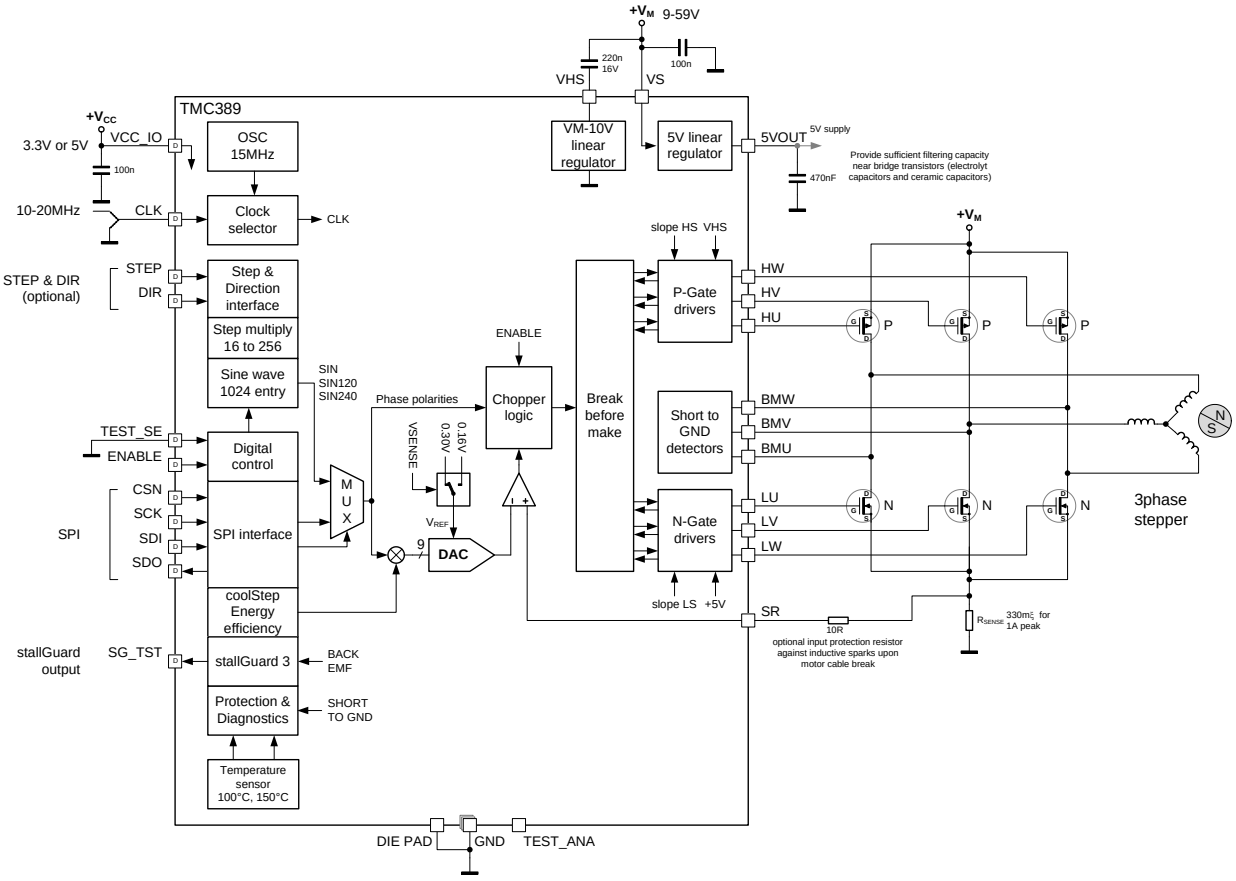


figure 4: TMC389 block and application schematic

The application schematic shows the basic building blocks of the IC and the connections to the power bridge transistors, as well as the power supply. The connection of the digital interface lines to the microcontroller and / or a motion controller is specific to the system architecture and the micro-controller type. Do not leave any input floating over extended periods of time, as there are no pull up or pull down resistors integrated. The choice of power MOSFETs for the TMC389 depends on the desired motor current and supply voltage. Please refer chapter 17.4. For even higher motor current capability, external MOSFET drivers can be added using full N channel bridges.

5.1 Pin description of TMC389-LA

Pin	Number	Type	Function
GND	1, 13		Digital and analog low power GND
HU HV HW	2, 3, 23	O (VS)	High side P-channel driver output. Becomes driven to VHS to switch on MOSFET.
BMV BMU BMW	4 5 20	I (VS)	Sensing input for bridge outputs. Used for short to GND protection. May be tied to VS if unused.
LU LV LW	6 7 19	O 5V	Low side MOSFET driver output. Becomes driven to 5VOUT to switch on MOSFET.
SR	17	AI	Sense resistor input of chopper driver.
5VOUT	9		Output of internal 5V linear regulator. This voltage is used to supply the low side drivers and internal analog circuitry. An external capacitor to GND close to the pin is required. Place the capacitor near to pin 9 and pin 13. 470nF ceramic are sufficient for most applications, an additional tantalum capacitor (10µF or more) improves performance with high gate charge MOSFETs.
SDO	10	DO VIO	Data output of SPI interface (Tristate)
SDI	11	DI VIO	Data input of SPI interface (Scan test input in test mode)
SCK	12	DI VIO	Serial clock input of SPI interface (Scan test shift enable input in test mode)
CSN	14	DI VIO	Chip select input of SPI interface
ENN	15	DI VIO	Enable not input for drivers. Switches off all MOSFETs.
CLK	16	DI VIO	Clock input for all internal operations. Tie low to use internal oscillator. A high signal disables the internal oscillator until power down.
VHS	24		High side supply voltage (motor supply voltage - 10V)
VS	25		Motor supply voltage
TST_ANA	26	AO VIO	Analog mode test output. Leave open or tie to GND for normal operation.
SG_TST	27	DO VIO	stallGuard2™ output. Signals motor stall (high active).
GNDP	28		Power GND for MOSFET drivers. Connect directly to GND
VCC_IO	29		Input / output supply voltage VIO for all digital pins. Tie to digital logic supply voltage. Allows operation in 3.3V and 5V systems.
DIR	30	DI VIO	Direction input. Is sampled upon detection of a step to determine stepping direction. An internal glitch filter for 60ns is provided.
STEP	31	DI VIO	Step input. An internal glitch filter for 60ns is provided.
TST_MODE	32	DI VIO	Test mode input. Puts IC into test mode. Tie to GND for normal operation.
Exposed die pad	-	GND	Connect the exposed die pad to a GND plane. It is used for cooling of the IC and may either be left open or be connected to GND.

6 SPI™ mode shift register

The TMC389 requires a configuration via SPI prior to operation. Its SPI interface also allows for reading back status flags. The SPI interface can operate up to the half clock frequency. The MSB (bit 19) is transmitted first. See chapter 6.6 and 19.2 for more details.

6.1 Overview (write)

Register/ Bit	DRVCTRL (*SDOFF*=1)	DRVCTRL (*SDOFF*=0)	CHOPCONF	SMARTEN	SGCSCONF	DRVCONF
19	0	0	1	1	1	1
18	0	0	0	0	1	1
17	PHU	-	0	1	0	1
16	CU7	-	TBL1	0	SFILT	TST
15	CU6	-	TBL0	SEIMIN	SSPD	SLPH1
14	CU5	-	-	SEDN1	SGT6	SLPH0
13	CU4	-	RNDTF	SEDN0	SGT5	SLPL1
12	CU3	-	CSYNC	-	SGT4	SLPL0
11	CU2	-	CDIR	SEMAX3	SGT3	-
10	CU1	-	NOSD	SEMAX2	SGT2	DISS2G
9	CU0	INTPOL	HYST5	SEMAX1	SGT1	TS2G1
8	PHV	DEDGE	HYST4	SEMAX0	SGT0	TS2G0
7	CV7	-	HYST3	-	-	*SDOFF*
6	CV6	-	HYST2	SEUP1	-	VSENSE
5	CV5	-	HYST1	SEUP0	-	*RDSEL1*
4	CV4	-	HYST0	-	CS4	*RDSEL0*
3	CV3	MRES3	TOFF3	SEMIN3	CS3	-
2	CV2	MRES2	TOFF2	SEMIN2	CS2	-
1	CV1	MRES1	TOFF1	SEMIN1	CS1	-
0	CV0	MRES0	TOFF0	SEMIN0	CS0	-

6.2 Overview (read)

Bit	*RDSEL*=00	*RDSEL*=01	*RDSEL*=10
19	MSTEP9	SG9	SG9
18	MSTEP8	SG8	SG8
17	MSTEP7	SG7	SG7
16	MSTEP6	SG6	SG6
15	MSTEP5	SG5	SG5
14	MSTEP4	SG4	SE4
13	MSTEP3	SG3	SE3
12	MSTEP2	SG2	SE2
11	MSTEP1	SG1	SE1
10	MSTEP0	SG0	SE0
9	-	-	-
8	-	-	-
7	STST		
6	-		
5	OL		
4	-		
3	S2G		
2	OTPW		
1	OT		
0	SG		

6.3 Driver control register bit assignment

The driver control register is used to operate the device in SPI mode by setting phase currents for Phase U and Phase V. Phase W is automatically calculated from the formula CW=-(CU+CV). In StepDir mode, it selects Step and Direction interface specific parameters. They need to be initialized once upon power up, and whenever basic parameters are required to be changed. Only write access is possible.

Notation of hexadecimal and binary numbers:
0x precedes a hexadecimal number, % precedes a multi-bit binary number

The meaning of register 0 depends on the mode selection between SPI mode and StepDir mode as selected by SDOFF (configuration register 11, bit 7).

6.3.1 Driver control register bit assignment in SPI mode

DRVCTRL		**write 0xxx, SDOFF=1**	
Bit	**Name**	**Function**	**Comment**
19	CFR	select configuration register	**0**: Operation mode dependent settings (see SDOFF)
18	-	reserved	set to 0
17	PHU	Polarity U	
16	CU7	Current U MSB	0 to max. 248 due to hysteresis setting. Depending on the hysteresis setting, the maximum value becomes even lower. The resulting value is not allowed to overflow 255.
15	CU6		
14	CU5		
13	CU4		
12	CU3		
11	CU2		
10	CU1		
9	CU0	Current U LSB	
8	PHV	Polarity V	
7	CV7	Current V MSB	0 to max. 248 due to hysteresis setting. Depending on the hysteresis setting, the maximum value becomes even lower. The resulting value is not allowed to overflow 255.
6	CV6		
5	CV5		
4	CV4		
3	CV3		
2	CV2		
1	CV1		
0	CV0	Current V LSB	

6.3.2 Driver control register bit assignment in StepDir mode

<table>
<tr><th colspan="2">DRVCTRL</th><th colspan="2">write 0xxx, SDOFF=0</th></tr>
<tr><th>Bit</th><th>Name</th><th>Function</th><th>Comment</th></tr>
<tr><td>19</td><td>CFR</td><td>select configuration register</td><td>0: Operation mode dependent settings (see SDOFF)</td></tr>
<tr><td>18</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>17</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>16</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>15</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>14</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>13</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>12</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>11</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>10</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>9</td><td>INTPOL</td><td>enable step interpolation</td><td>1: Enable step impulse multiplication by 16. Only in resolution 16x microsteps, the microstepping becomes extrapolated to 256 microsteps. Interpolation is possible starting below step distance of max. 2^20 CLK periods.</td></tr>
<tr><td>8</td><td>DEDGE</td><td>enable double edge step pulses</td><td>1: Enable step impulse at each step edge to reduce step frequency requirement</td></tr>
<tr><td>7</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>6</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>5</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>4</td><td>-</td><td>reserved</td><td>set to 0</td></tr>
<tr><td>3</td><td>MRES3</td><td rowspan="4">micro step resolution for step/direction mode</td><td rowspan="4">%0000 … %1000

<table>
<tr><th>MRES</th><th>electrical</th><th>mechanical</th></tr>
<tr><td>%0000</td><td>256</td><td>170.66</td></tr>
<tr><td>%0001</td><td>128</td><td>85.33</td></tr>
<tr><td>%0010</td><td>64</td><td>42.66</td></tr>
<tr><td>%0011</td><td>32</td><td>21.33</td></tr>
<tr><td>%0100</td><td>16</td><td>10.66</td></tr>
<tr><td>%0101</td><td>8</td><td>5.33</td></tr>
<tr><td>%0110</td><td>4</td><td>2.66</td></tr>
<tr><td>%0111</td><td>2</td><td>1.33</td></tr>
<tr><td>%1000</td><td>1</td><td>0.66</td></tr>
</table>

The electrical values given describe the number of steps taken per electrical quarter sine wave. The resulting mechanical microstep resolution which describes the number of microsteps between two motor fullsteps is 2/3 of the corresponding value. Please take into account, that the microstep position when switching to a lower resolution determines the sequence of patterns.
step width=2^MRES [electrical microsteps]
step width=2/3*2^MRES [motor microsteps]</td></tr>
<tr><td>2</td><td>MRES2</td></tr>
<tr><td>1</td><td>MRES1</td></tr>
<tr><td>0</td><td>MRES0</td></tr>
</table>

6.4 Configuration register bit assignment

The configuration registers select the mode of operation and set all motor and application dependent parameters. They need to be initialized once upon power up, and whenever basic parameters are required to be changed. Only write access is possible.

CHOPCONF		**write 100x: Chopper Configuration**		
Bit	**Name**	**Function**	**Comment**	
19	CFR	select configuration register	**1**: Configuration register	
18	CFRSEL1	select configuration register	**%00**: Chopper configuration register	
17	CFRSEL0			
16	TBL1	blank time select	%00 … %11:	
15	TBL0		Set comparator blank time to 16, 24, 36 or 54 clocks	
14	CHM	chopper mode	0	Standard mode
			1	unused
13	RNDTF	random TOFF time	0	Chopper off time is fixed as set by bits t_{OFF}
			1	Random mode, t_{OFF} is random modulated by dN_{CLK}= -12 … +3 clocks.
12	CSYNC	chopper synchronization	0	Chopper runs freely
			1	Chopper becomes synchronized to step frequency
11	CDIR	chopper direction	0	Chopper direction is WVU with DIR input=0 Choose for turn left in SPI operation
			1	Chopper direction is UVW with DIR input=0 Choose for turn right (U→V→W) in SPI operation and for StepDir operation
10	NOSD	skip slow decay phase	0	Each chopper on cycle is followed by a slow decay phase as set by TOFF
			1	Slow decay phases are skipped between the chopper phases, except directly following a short to GND or chopper synchronization. Minimum blank time then is 36 clocks.
9	HYST5	hysteresis value	DAC hysteresis setting: %000000 … %111111: 0 … 63 (1/512 of this setting adds to coil current setting) *Attention:* *Effective HYST/2 must be ≤ 255-sinewave peak (248 at max. current setting) – Reduce current setting to 28 for maximum hysteresis.* *Do not work with too small setting (poor performance).*	
8	HYST4			
7	HYST3			
6	HYST2			
5	HYST1			
4	HYST0			
3	TOFF3	off time and driver enable	Off time setting for constant t_{OFF} chopper N_{CLK}= 12 + 32*TOFF (Minimum is 64 clocks) %0000: Driver disable, all bridges off %0001: not allowed %0010 … %1111: 2 … 15	
2	TOFF2			
1	TOFF1			
0	TOFF0			

SMARTEN		write 1010: Smart energy control coolStep™	
Bit	**Name**	**Function**	**Comment**
19	CFR	select configuration register	**1**: configuration register
18	CFRSEL1	select configuration register	**%01**: coolStep configuration register
17	CFRSEL0		
16	-	reserved	set to 0
15	SEIMIN	minimum current for smart current control	0: 1/2 of current setting (CS) 1: 1/4 of current setting (CS)
14	SEDN1	current down step speed	%00: for each 32 stallGuard values decrease by one %01: for each 8 stallGuard values decrease by one %10: for each 2 stallGuard values decrease by one %11: for each stallGuard value decrease by one
13	SEDN0		
12	-	reserved	set to 0
11	SEMAX3	stallGuard hysteresis value for smart current control	If the stallGuard result is equal to or above (SEMIN+SEMAX+1)*32, the motor current becomes decreased to save energy. %0000 … %1111: 0 … 15
10	SEMAX2		
9	SEMAX1		
8	SEMAX0		
7	-	reserved	set to 0
6	SEUP1	current up step width	Current steps per measured stallGuard value %00 … %11: 1, 2, 4, 8
5	SEUP0		
4	-	reserved	set to 0
3	SEMIN3	minimum stallGuard value for smart current control and smart current enable	If the stallGuard result falls below SEMIN*32, the motor current becomes increased to reduce motor load angle. %0000: coolStep current control off %0001 … %1111: 1 … 15
2	SEMIN2		
1	SEMIN1		
0	SEMIN0		

SGCSCONF		write 110x: Load measurement stallGuard2 and Current Setting		
Bit	**Name**	**Function**	**Comment**	
19	CFR	select configuration register	**1**: Configuration register	
18	CFRSEL1	select configuration register	**%10**: stallGuard and current configuration register	
17	CFRSEL0			
16	SFILT	stallGuard filter enable	0	Standard mode, high time resolution for stallGuard
			1	Filtered mode, stallGuard signal updated for each six fullsteps only to compensate for motor tolerances
15	SSPD	stallGuard speed	0	Standard mode, high time resolution for stallGuard
			1	StallGuard uses more filtering, use for low motor velocity only
14	SGT6	stallGuard threshold value	This signed value controls stallGuard level for stall output and sets the optimum measurement range for readout. A lower value gives a higher sensitivity. Zero is the starting value working with most motors. -64 to +63: A higher value makes stallGuard less sensitive and requires more torque to indicate a stall.	
13	SGT5			
12	SGT4			
11	SGT3			
10	SGT2			
9	SGT1			
8	SGT0			
7	-	reserved	set to 0	
6	-	reserved	set to 0	
5	-	reserved	set to 0	
4	CS4	current scale (scales digital currents A and B)	Current scaling for SPI and step/direction operation %00000 … %11111: 1/32, 2/32, 3/32, … 32/32 *Attention: Maximum possible current scale setting might be below 31, depending on hysteresis setting.*	
3	CS3			
2	CS2			
1	CS1			
0	CS0			

DRVCONF		**write 111x: Driver Configuration**	
Bit	**Name**	**Function**	**Comment**
19	CFR	select configuration register	**1**: Configuration register
18	CFRSEL1	select configuration register	**%11**: Driver configuration register
17	CFRSEL0		
16	TST	reserved TEST mode	Set to 0. When 1, SG_TST outputs digital test values, and TEST_ANA outputs analog test values. Selection is done by SGT0 and SGT1 (%00 … %10): For TEST_ANA: anatest_2vth, anatest_dac_out, anatest_vdd_half. For SG_TST: comp_A, comp_B, CLK
15	SLPH1	Slope control high side	%00: min, %01: min + tc, %10: med + tc, %11: max In temperature compensated mode (tc), the driver strength is increased if the overtemperature prewarning temperature is reached. This compensates for temperature dependence of high side slope control.
14	SLPH0		
13	SLPL1	Slope control low side	00, 01: min, 10: med, 11: max
12	SLPL0		
11	-	reserved	set to 0
10	DISS2G	short to GND protection disable	0: Short to GND protection is on 1: Short to GND protection is disabled
9	TS2G1	short to GND detection timer	%00: 3.2µs %01: 1.6µs %10: 1.2µs %11: 0.8µs
8	TS2G0		
7	SDOFF	Step Direction input off	0: Enable step/direction mode (StepDir) 1: Enable SPI mode
6	VSENSE	sense resistor voltage based current scaling	0: Full scale sense resistor voltage is 305mV 1: Full scale sense resistor voltage is 165mV (refers to a current setting of 31 and DAC value 255)
5	RDSEL1	Select value for read out (RD bits)	%00 Microstep position read back
4	RDSEL0		%01 stallGuard level read back %10 stallGuard and smart current level read back %11 Reserved, do not use
3	-	reserved	set to 0
2	-	reserved	set to 0
1	-	reserved	set to 0
0	-	reserved	set to 0

6.5 Bit assignment for read

Information can be read back from the driver on each access. Different information may be required, depending on the application. This is selected by the bits RDSEL in the register DRVCONF.

DRVSTATUS		**read status information – Partially selected by RDSEL in DRVCONF**		
Bit	**Name**	**Function**	**Comment**	
19	RD9	microstep position in internal sine table for phase U or stallGuard bits 7 to 0 or stallGuard bits 7 to 5 and current control scale	RDSEL=%00	Actual microstep position in sine table for phase U in step/direction operation (MSTEP) (MSTEP9=PHA)
18	RD8			
17	RD7			
16	RD6		RDSEL=%01	Bits 9 … 0 of stallGuard result (SG)
15	RD5		RDSEL=%10	Bits 9 … 5 of stallGuard result (SG) and actual current control scaling Bits 4 … 0 for monitoring smart energy current setting (SE)
14	RD4			
13	RD3			
12	RD2			
11	RD1			
10	RD0			
9	0	reserved	-	
8	0	reserved	-	
7	STST	stand still step indicator	1: Indicates, that no step impulse occurred on the step input during the last 2^20 clock cycles.	
6	0	reserved	-	
5	OL	open load indicator	Flag becomes set, if no chopper event has happened during the last period with constant coil polarity. Only a current above 1/16 of maximum setting can reset this flag!	
4	0	reserved	-	
3	S2G	short to GND detection bits on high side transistors	1: Short condition is detected, driver is currently shut down (clear short condition by disabling driver) In a short circuit condition, the chopper cycle becomes terminated. The short counter is increased by each short circuit. It becomes decreased by one for each phase polarity change. The driver becomes shut down when the counter reaches 3, until the short condition becomes reset by disabling and re-enabling the driver.	
2	OTPW	Overtemperature pre-warning	1: Warning threshold is exceeded	
1	OT	Overtemperature	1: Driver is shut down due to overtemperature	
0	SG	stallGuard status	1: stallGuard threshold is reached, SG output high	

6.6 SPI™ timing

The SPI interface uses the system clock to synchronize all input and output signals. This limits the SPI clock frequency to at maximum half of the system clock frequency. For an asynchronous system using the internal clock, some 10 percent of safety margin should be used, assuming the minimum internal and maximum SPI master clock frequency, in order to ensure a reliable data transmission.

All SPI inputs as well as the ENN input are internally filtered to avoid triggering on short time glitches.

The minimum number of SCK clock pulses to be sent is 20. Additional clocks are possible – the additional bits shifted in on SDI become shifted through to the SDO pin delayed by 20 clocks via the internal shift register. The active CSN time (low) must span the whole data transmission. Upon CSN going inactive (high), the shift register content becomes latched into the internal control register.

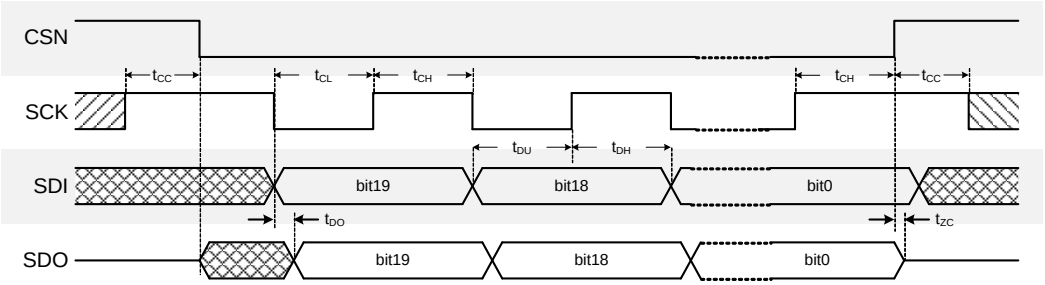


figure 5: SPI timing

Hint
Usually this SPI timing is referred to as SPI MODE 3

SPI interface timing	**AC-Characteristics** clock period is t_{CLK}					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
SCK valid before or after change of CSN	t_{CC}		10			ns
CSN high time	t_{CSH}	*) Min time is for synchronous CLK with SCK high one t_{CH} before CSN high only	t_{CLK}*)	>2t_{CLK} +10		ns
SCK low time	t_{CL}	*) Min time is for synchronous CLK only	t_{CLK}*)	>t_{CLK}+10		ns
SCK high time	t_{CH}	*) Min time is for synchronous CLK only	t_{CLK}*)	>t_{CLK}+10		ns
SCK frequency using internal clock	f_{SCK}	assumes minimum OSC frequency			4	MHz
SCK frequency using external 16MHz clock	f_{SCK}	assumes synchronous CLK			8	MHz
SDI setup time before rising edge of SCK	t_{DU}		10			ns
SDI hold time after rising edge of SCK	t_{DH}		10			ns
Data out valid time after falling SCK clock edge	t_{DO}	no capacitive load on SDO			t_{FILT}+5	ns
SDI, SCK and CSN filter delay time	t_{FILT}	rising and falling edge	12	20	30	ns

7 Step and direction interface

The step and direction interface allows easy movement of the motor and is a simple real time interface for a motion controller. Its pulse rate multiplier allows smooth motor operation even with reduced pulse bandwidth.

7.1 Timing

The step and direction interface pins are sampled synchronously with the clock signal. An internal analog filter removes disturbances caused by glitches on the signals, e.g. caused by long PCB traces. Despite this, the signals should be filtered and / or differentially transmitted, if the step source is far from the TMC389 and especially if the step signals are interconnected via cables.

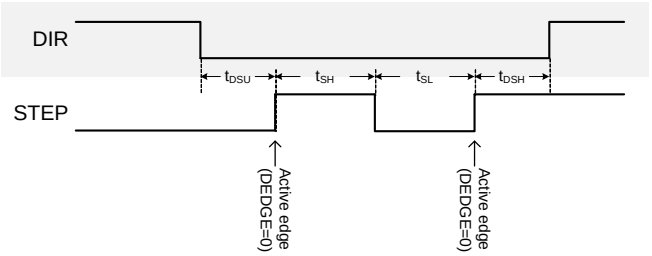


figure 6: STEP and DIR timing

STEP and DIR interface timing	**AC-Characteristics** clock period is t_{CLK}					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
step frequency (at maximum microstep resolution)	f_{STEP}	DEGDE=0			½ f_{CLK}	
		DEDGE=1			¼ f_{CLK}	
(electrical) fullstep frequency	f_{FS}				f_{CLK}/512	
STEP input low time	t_{SL}		max(t_{FILTSD}, t_{CLK}+20)			ns
STEP input high time	t_{SH}		max(t_{FILTSD}, t_{CLK}+20)			ns
DIR to STEP setup time	t_{DSU}		20			ns
DIR after STEP hold time	t_{DSH}		20			ns
STEP and DIR spike filtering time	t_{FILTSD}	rising and falling edge	36	60	85	ns
STEP and DIR sampling relative to rising CLK input	$t_{SDCLKHI}$	before rising edge of CLK input		t_{FILTSD}		ns

7.2 Internal microstep table

The internal microstep table uses 1024 sine wave entries to generate the wave. Its amplitude is +/-248 rather than +/-255, leaving some headroom for hysteresis setting within an 8 bit amplitude range. The step width depends on the microstep resolution setting. Depending on the DIR input, the microstep counter is increased (DIR=0) or decreased (DIR=1) with each STEP pulse by the step width. Due to the symmetry of the sine wave, only a quarter of the table needs to be stored. The phase V wave uses a phase shift of 120°. The W wave is calculated as CW=-(CU+CV). Despite many entries in the last quarter of the table being equal, the electrical angle continuously changes, because either sine wave or cosine wave is in an area, where the current vector changes monotonously from position to position.

Entry	0-31	32-63	64-95	96-127	128-159	160-191	192-223	224-255
0	1	49	96	138	176	207	229	243
1	2	51	97	140	177	207	230	244
2	4	52	98	141	178	208	231	244
3	5	54	100	142	179	209	231	244
4	7	55	101	143	180	210	232	244
5	8	57	103	145	181	211	232	245
6	10	58	104	146	182	212	233	245
7	11	60	105	147	183	212	233	245
8	13	61	107	148	184	213	234	245
9	14	62	108	150	185	214	234	246
10	16	64	109	151	186	215	235	246
11	17	65	111	152	187	215	235	246
12	19	67	112	153	188	216	236	246
13	21	68	114	154	189	217	236	246
14	22	70	115	156	190	218	237	247
15	24	71	116	157	191	218	237	247
16	25	73	118	158	192	219	238	247
17	27	74	119	159	193	220	238	247
18	28	76	120	160	194	220	238	247
19	30	77	122	161	195	221	239	247
20	31	79	123	163	196	222	239	247
21	33	80	124	164	197	223	240	247
22	34	81	126	165	198	223	240	248
23	36	83	127	166	199	224	240	248
24	37	84	128	167	200	225	241	248
25	39	86	129	168	201	225	241	248
26	40	87	131	169	201	226	241	248
27	42	89	132	170	202	226	242	248
28	43	90	133	172	203	227	242	248
29	45	91	135	173	204	228	242	248
30	46	93	136	174	205	228	243	248
31	48	94	137	175	206	229	243	248

figure 7: internal microstep table showing the first quarter of the sine wave

7.3 Switching between different microstep resolutions

In principle, the microstep resolution can be changed at any time. The microstep resolution determines the increment respectively the decrement, the TMC389 uses for advancing in the microstep table. At maximum resolution, it advances one step for each step pulse. At half resolution, it advances two steps and so on. This way, a change of resolution is possible transparently at each time. However, you may experience the motor behavior becoming direction dependant, when switching microstep resolutions. This behavior results from table sampling points not evenly shifted inside the microstep table with respect to the step width. To avoid this, always switch to a lower resolution, when the actual microstep position is a multiple of the desired table step width. This is always satisfied at position zero in the microstep table.

7.4 Step rate multiplier and stand still detection

The step rate multiplier can be enabled by setting the INTPOL bit. It supports a 16 microstep setting and Step/Dir mode, only. In this setting, each step impulse at the input causes the execution of 16 times 1/256 microsteps. The step rate for the 16 microsteps is determined by measuring the time interval of the previous step pulses and dividing it into 16 equal parts. This way, a smooth motor movement like in 256 microstep resolution is achieved. The maximum time between two microsteps corresponds to 2^20 i.e. roughly one million clock cycles, in order to reach evenly distributed 1/256 sine wave steps. At 16MHz clock frequency, this results in a minimum step input frequency of 16Hz for step rate multiplier operation, i.e. one and a half motor fullsteps per second. A lower step rate causes the stand still flag to become set as soon as the time is expired. Execution of microsteps will happen with a frequency of 1/(2^16) clock frequency.

Attention: The step rate multiplier will only give good results with a stable microstep frequency. Do not use the DEDGE option, if the step input does not have a 50% duty cycle.

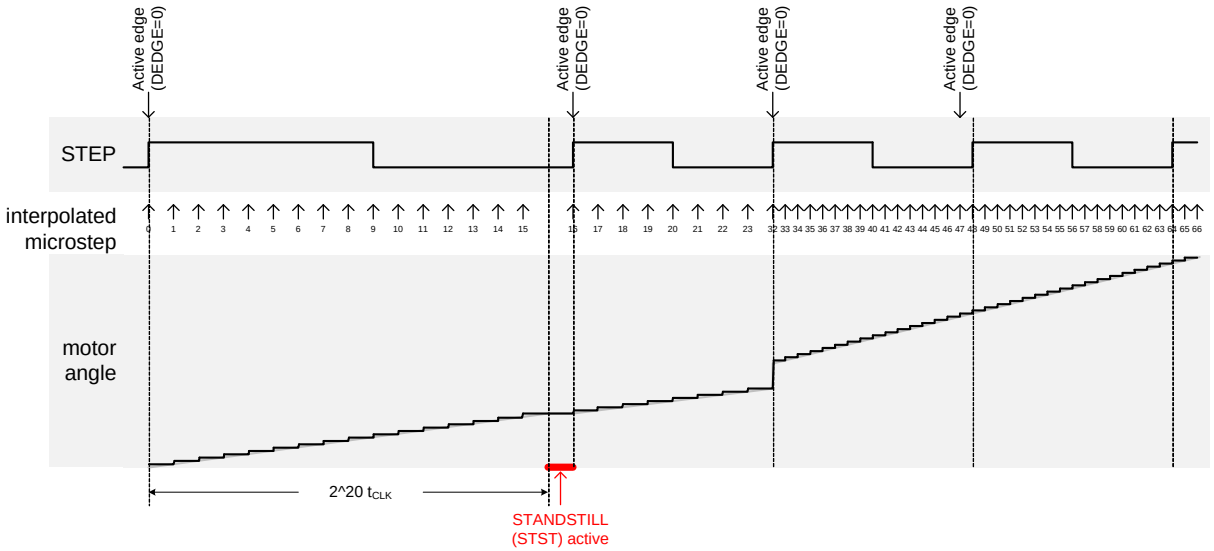


figure 8: Operation of the step multiplier in different situations

8 Current setting

The internal 5V supply voltage is used as a reference. To adapt the motor current, and to allow for different values of sense resistors, the voltage divider for full scale can be chosen as $V_{FS(HI)}$ =1/16 VDD or $V_{FS(LO)}$=1/30 of VDD. With this, the peak sense resistor voltage at a digital DAC control level of 248 is roughly 0.16V or 0.31V.

Using the internal sine wave table, which has the amplitude of 248, the RMS motor coil current thus can be calculated by:

$$I_{RMS} = \frac{CS+1}{32} * \frac{V_{FS}}{R_{SENSE}} * \frac{1}{\sqrt{2}}$$

The momentary motor current is calculated by:

$$I_{MOT} = \frac{CURRENT_{A/B}}{248} * \frac{CS+1}{32} * \frac{V_{FS}}{R_{SENSE}}$$

CS is the current scale setting as set by the CS bits and smart current scaler.

V_{FS} is the full scale voltage as determined by VSENSE control bit (please refer electrical characteristics).

$CURRENT_{A/B}$ is the value set by the current setting in SPI mode, or, the actual value from the internal sine wave table in Step/Dir mode.

Parameter	Description	Range	Comment
CS	*Current scale*. Scales both coil current values as taken from the internal sine wave table or from the SPI interface. For high precision motor operation, work with a current scaling factor in the range 16 to 28 (31), because scaling down the current values reduces the effective microstep resolution by making microsteps coarser. This setting also controls the maximum current value set by coolStep™. Keep in mind, that a value above 28 is only possible with reduced HYST setting: CS=31 requires HYST < 16 CS=30 requires HYST < 32 CS=29 requires HYST < 48	0 … 28 (… 31)	scaling factor: 1/32, 2/32, … 32/32
VSENSE	Allows control of the sense resistor *voltage range* or adaptation of one electronic module to different maximum motor currents.	0	310mV
		1	165mV

8.1 Considerations on the current sense resistors and layout

Sense resistors should be carefully selected. The full motor current flows through each sense resistor. They also see the switching spikes from the MOSFET bridges. A low inductance type resistor is required to prevent spikes causing ringing on the current measurement leading to instable measurement results. A low inductivity, low resistance layout is essential. Also, any common GND path of the sense resistors of different driver ICs needs to be prevented, because this would lead to coupling between both current sense signals. A massive GND plane is best. Especially for high current drivers or long motor cables, a spike damping with parallel capacitors can make sense (see figure 9). As the TMC389 is susceptible to negative overvoltages on the sense resistor inputs, an additional input protection resistor helps preventing damage in case of motor cable break or increased ringing on the motor lines in case of long motor cables.

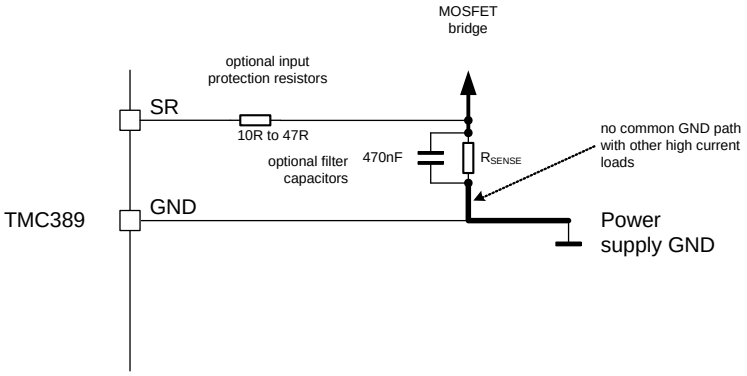


figure 9: Sense resistor grounding and optional parts

The sense resistor needs to be able to conduct the peak motor coil current in motor stand still situations, unless standby power is reduced. Under normal conditions, the sense resistor sees the coil RMS current.

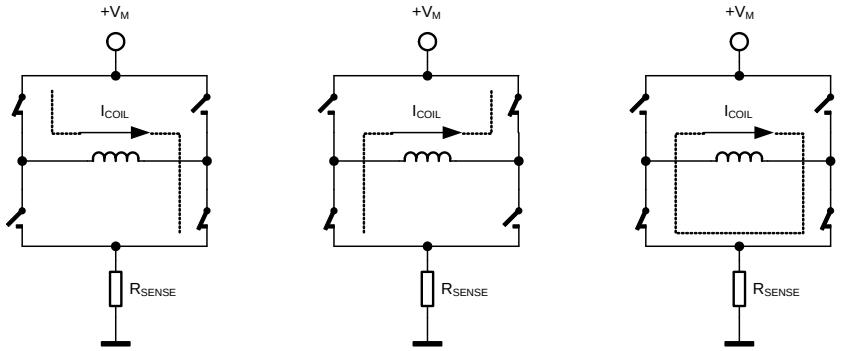
Peak sense resistor power dissipation:

$$P_{RSMAX} = \frac{\left(VSENSE * \frac{CS+1}{32}\right)^2}{R_{SENSE}}$$

For high current applications, power dissipation is halved by using the low VSENSE setting and using an adapted resistance value. Please be aware, that in this case any voltage drop in PCB traces has a larger influence on the result. A compact power stage layout with massive ground plane is best to avoid parasitic effects.

9 Chopper operation of the motor coils

The motor coils are operated using a chopper principle. The chopper regulates the current in the three coils by switching each coil in one of three different states. In figure 10 the different phases of a chopper cycle are shown for one coil, which is seen by each two half bridges. The figure assumes a triangle connection of the coils, but, a star connection of the coils virtually shows the same behavior. In the on-phase, the current is actively driven into the coils by connecting them to the power supply in the direction of the target current. A fast decay phase reverses the polarity of the coil voltage to actively reduce the current. The slow decay phase shorts the coil in order to let the current re-circulate. The current can be regulated using only on phases and fast decay phases. An optional slow decay phase can be inserted and might bring benefit for some low inductivity motors, by limiting the chopper frequency to an upper value. The current comparator can measure coil current, when the current flows through the sense resistor. Whenever the coil becomes switched, spikes at the sense resistors occur due to charging and discharging parasitic capacities. During this time (typically one or two microseconds), the current cannot be measured. It needs to be covered by the blank time setting.



on phase:	fast decay phase:	slow decay phase:
Current flows in direction of target current	Current flows in opposite direction of target current	Current re-circulation

figure 10: Chopper phases in motor operation

Parameter	Description	Range	Comment
TOFF	The *off time* setting controls the minimum chopper frequency. For most applications an off time will not be required. In this case, a dummy value needs to be programmed to this register to enable the driver and the NOSD flag shall be set. Setting this parameter to zero completely disables all driver transistors and the motor can free-wheel.	0	chopper off
		2…15	off time setting N_{CLK}=12+32*TOFF
HYST	The hysteresis setting is the main control for the chopper and determines the chopper frequency. A higher setting introduces more current ripple and thus reduces frequency. A too low setting will result in the coil current only loosely following the target current and thus reduced microstep performance, especially in the current zero crossing. A too high setting can cause audible chopper noise.	0 … 63	Hysteresis for the chopper
TBL	Selects the comparator *blank time*. This time needs to safely cover the switching event and the duration of the ringing on the sense resistor. For most low current drivers, a setting of 1 or 2 is good. For high current applications with large MOSFETs, a setting of 2 or 3 will be required.	0	16 t_{CLK}
		1	24 t_{CLK}
		2	36 t_{CLK}
		3	54 t_{CLK}
NOSD	Selection of the *TOFF* insertion	0	use TOFF setting for additional SD phases
		1	no slow decay phase
RNDTF	This bit switches on a *random off time* generator, which slightly modulates the off time t_{OFF} using a random polynomial giving a spread spectrum effect.	0	disable
		1	random modulation enable
CSYNC	This bit switches on *chopper synchronization*. If enabled, the chopper engine becomes reset with each motor fullstep, in order to avoid a beat occurring between full step sequence and chopper clock.	0	disable
		1	synchronization enable
CDIR	The *chopper direction* should match the motor direction, to allow highest motor velocities. *In Step/Dir mode, this is done automatically, when CDIR is set to 1.* In SPI mode, either the DIR input or CDIR should be used, to adapt the chopper direction. Both, DIR input and CDIR are XORed.	0	DIR=0: WVU DIR=1: UVW
		1	DIR=0: UVW DIR=1: WVU

9.1 spreadCycle chopper

The spreadCycle chopper scheme (pat.fil.) is a precise and simple to use chopper principle, which automatically determines the optimum fast decay portion for the motor. Anyhow, a number of settings can be made in order to optimally fit the driver to the motor.

Each chopper cycle is comprised of an on phase, a fast decay phase and a slow decay phase (see figure 11). Optional additional slow decay phases can be added (switch off using NOSD bit). The hysteresis determines the chopper frequency by forcing the driver to introduce some amount of current ripple into the motor coils. The motor inductivity determines the ability to follow a changing motor current. The duration of the on- and fast decay phase needs to cover at least the blank time, because the current comparator is disabled during this time. This is satisfied by choosing a positive value for the hysteresis as can be estimated by the following calculation:

$$f_{CHOP} = \frac{V_M}{2 * \frac{2}{3} L_{COIL} * I_{HYST}}$$

where f_{CHOP} is the resulting chopper frequency. I_{COIL} is the peak motor coil current at the maximum motor current setting CS, and R_{COIL} and L_{COIL} are motor coil inductivity and motor coil resistance.

The current hysteresis I_{HYST} results from the HYST setting as follows:

$$I_{HYST} = HYST * \frac{I_{COIL}}{2 * 248} * \frac{32}{CS + 1}$$

The calculated chopper frequency should preferably lie between 18kHz and 60kHz. If a too high chopper frequency results, you can try adding a slow decay phase.

Example:

For a 60mm stepper motor with 0.76mH, 0.32Ω phase and 5.8A RMS current at CS=28 and HYST=40 operating from a 24V supply:

$$I_{HYST} = 40 * \frac{5.8A}{496} * \frac{32}{29} = 516mA$$

$$f_{CHOP} = \frac{24V}{\frac{4}{3} * 0.76mH * 0.516A} = 46kHz$$

With this, the choice of a hysteresis setting of 40 results in a good chopper frequency, but a higher hysteresis also will not harm.

The setting can also be determined by experimenting with the motor: A too low setting will result in reduced microstep accuracy, while a too high setting will lead to more chopper noise and motor power dissipation. The correct setting can be determined best by rotating the motor slowly, and increasing hysteresis setting, until the motion of the motor is very smooth (feel with fingers or add a long pointer to the axis, e.g. laser pointer). Or, you can measure the motor currents with a current probe or with an oscilloscope at the sense resistor, and check the waves for a pure sine wave. A further increment of the hysteresis setting will lower chopper frequency and might at some point generate audible chopper noise. For high inductivity motors, audible noise might occur at optimum setting. Increase supply voltage, or choose a motor with a different, higher current winding.

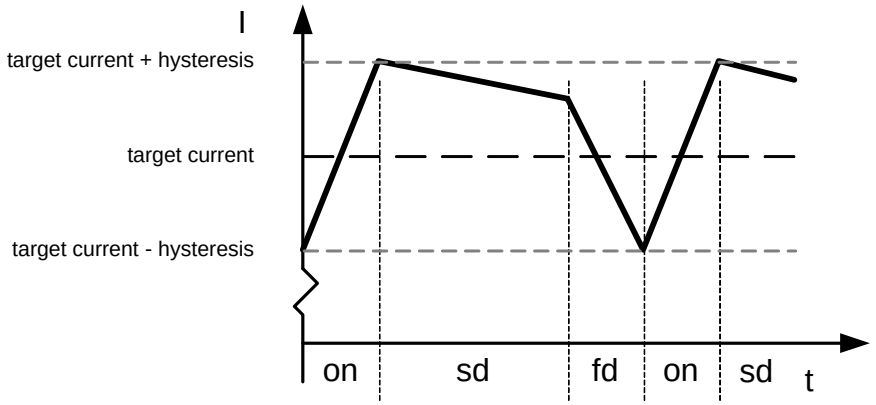


figure 11: spreadCycle (pat.fil.) chopper scheme showing the coil current within a chopper cycle

10 MOSFET driver stage

The TMC389 provides a three half bridge driver stage for N&P channel MOSFETs. The gate driver current for the power MOSFETs can be adapted to match the MOSFETs and to influence the slew rate at the coil outputs. Main features of the driver stage:

- 5V gate drive voltage for low side N MOS driver, 8V for high side P MOS driver.
- The drivers protect the bridges actively against cross conduction via an internal Q_{GD} protection that holds MOSFETs safely off.
- Automatic brake-before-make logic minimizes dead time and diode conduction time.
- Integrated short to ground protection detects a short of the motor wires and protects the driver.

10.1 Principle of operation

The low side gate driver is supplied by the 5VOUT pin. The low side driver supplies 0V to the MOSFET gate to close the MOSFET, and 5VOUT to open it. The high side gate driver voltage is supplied by the VS and the VHS pin. VHS is more negative than VS and allows opening the VS referenced high side MOSFET. The high side driver supplies VS to the P channel MOSFET gate to close the MOSFET, and VHS to open it. The effective low side gate voltage is roughly 5V; the effective high side gate voltage is roughly 8V.

Parameter	Description	Range	Comment
SLPL	Low side slope control. Controls the MOSFET gate driver current. Set a value fitting the external MOSFET gate charge and the desired slope.	0,1	min. setting
		1	med. setting
		2	max. setting
SLPH	High side slope control. Controls the MOSFET gate driver current. Set to a value fitting the external MOSFET gate charge and the desired slope.	0…3	min. setting… max. setting

10.2 Break-before-make logic

Each half-bridge has to be protected against cross conduction during switching events. When switching off the low-side MOSFET, its gate first needs to be discharged, before the high side MOSFET is allowed to be switched on. The same goes when switching off the high-side MOSFET and switching on the low-side MOSFET. The time for charging and discharging of the MOSFET gates depends on the MOSFET gate charge and the driver current set by SLPL resp. SLPH. The BBM (break-before-make) logic measures the gate voltage and automatically delays switching on of the opposite bridge transistor, until its counterpart is discharged. This way, the bridge will always switch with optimized timing independent of the MOSFETs used and independent of the slope setting.

10.3 ENN input

The motor driver outputs can be completely disabled by hardware, by pulling the ENN input high. This way, the motor can free-wheel. The function however is identical to a software disable, which is achieved by setting the register TOFF to zero. The hardware disable may be used in cases, where the motor is to be hot plugged.

For normal operation tie ENN low.

10.4 Slope control in TMC389

The TMC389 driver stage provides a constant current output stage slope control. This allows adapting driver strength to the drive requirements of the power MOSFETs and adjusting the output slope by providing for a controlled gate charge and discharge. A slower slope causes less electromagnetic emission, but at the same time power dissipation of the power transistors rises. The duration of the complete switching event depends on the total gate charge. The voltage transition of the output takes place during the so called miller plateau (see figure 12). The miller plateau results from the gate to drain capacity of the MOSFET charging / discharging during the switching. From the datasheet of the transistor it can be seen, that the miller plateau typically covers only a part (e.g. one quarter) of the complete charging event. The gate voltage level, where the miller plateau starts, depends on the gate threshold voltage of the transistor and on the actual load current.

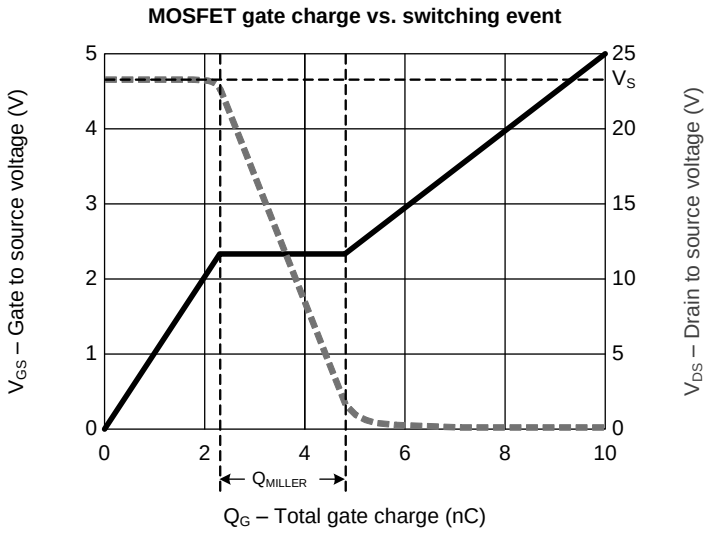


figure 12: MOSFET gate charge as available in device data sheet vs. switching event (dotted line)

The slope time t_{SLOPE} can be calculated as follows:

$$t_{SLOPE} = \frac{Q_{MILLER}}{I_{GATE}}$$

Whereas Q_{MILLER} is the charge the power transistor needs for the switching event, and I_{GATE} is the driver current setting of the TMC389.

Taking into account, that a slow switching event means high power dissipation during switching, and, on the other side a fast switching event can cause EMV problems, the desired slope will be in some ratio to the switching (chopper) frequency of the system. The chopper frequency is typically slightly outside the audible range, i.e. 18kHz to 40kHz. The lower limit for the slope is dictated by the reverse recovery time of the MOSFET internal diodes, unless additional Schottky diodes are used in parallel to the MOSFETs source-drain diode. Thus, for most applications a switching time between 100ns and 750ns is chosen.

Example:

A circuit using the transistor from the diagram above is operated with a gate current setting of 15mA. The miller charge of the transistor is about 2.5nC.

$$t_{SLOPE} = \frac{2.5nC}{15mA} = 166ns$$

11 Diagnostics and protection

11.1 Short to GND detection

The short to GND detection prevents the high side power MOSFETs to be destroyed by accidentally shorting the motor outputs to ground. It disables the driver, if a short condition persists, only. A temporary event like an ESD event could look like a short, too. This becomes sorted out by the short detection logic. In case of a short being detected, the bridge will be switched off instantaneously. The chopper cycle on the affected coil becomes terminated and the short counter is increased by each short circuit. It becomes decreased by one for each phase polarity change. The driver becomes shut down when the counter reaches 3, until the short condition is reset by disabling the driver and re-enabling it.

Status flag	Description	Range	Comment
S2G	This bit identifies a *short to GND condition* on B persisting for multiple chopper cycles. The flag becomes cleared when disabling the driver.	0 / 1	1: short condition detected

An overload condition of the high side MOSFET (“short to GND”) is detected by the TMC389, by monitoring the BM voltage during high side on time. Under normal conditions, the high side power MOSFET reaches the bridge supply voltage minus a small voltage drop during on time. If the bridge is overloaded, the voltage cannot rise to the detection level within a limited time, defined by the internal detection delay setting. Upon detection of an error, the bridge becomes switched off.

The short to GND detection delay needs to be adapted to the slope time, because it must cover the slope, but should not be unnecessarily long.

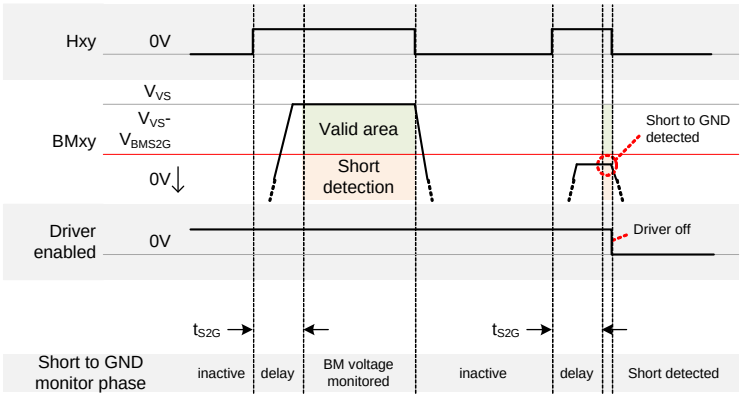


figure 13: Timing of the short to GND detector

Parameter	Description	Range	Comment
TS2G	This setting controls the short to GND detection delay time. It needs to cover the switching slope time. A higher setting reduces sensitivity to capacitive loads.	0…3	0: maximum time… 3: minimum time

11.2 Open load detection

The open load detection detects, if a motor coil has an open condition, for example due to a loose contact. When driving in fullstep mode (via SPI), the open load detection will also detect when the motor current cannot be reached within each step, i.e. due to a too high motor velocity where the back EMF voltage exceeds the supply voltage. The flag just has an informational character and an active open load condition does not in all cases indicate that the motor is not working properly. The flag becomes updated during normal operation of the motor whenever the polarity of the respective phase toggles.

Status flag	Description	Range	Comment
OL	This bit indicates an *open load condition*. The flag becomes set, if no chopper event has happened during the last period with constant coil polarity. It will flicker, if only one coil is detached during motor operation. The flag is not updated with too low actual coil current below 1/16 of maximum setting.	0 / 1	1: open load detected

11.3 Temperature measurement

The TMC389 integrates a two level temperature sensor (100°C prewarning and 150°C thermal shutdown) for diagnostics and for protection of the driver stage. The temperature detector can detect heat accumulation on the board, i.e. due to missing convection cooling. It cannot detect overheating of the power transistors in all cases, because heat transfer between power transistors and driver chip depends on the PCB layout and environmental conditions. Most critical situations, where the driver MOSFETs could be overheated, are avoided when enabling the short to GND protection. For many applications, the overtemperature prewarning will indicate an abnormal operation situation and can be used to initiate user warning or power reduction measures. If continuous operation in hot environments is necessary, a more precise processor based temperature measurement should be used to realize application specific overtemperature detection. The thermal shutdown is just an emergency measure and temperature rising to the shutdown level should be prevented by design.

The highside P-channel gate drivers within the TMC389 have a temperature dependency, which can be compensated up to some extent by increasing driver current as soon as the warning temperature threshold is reached. The TMC389 automatically corrects the temperature dependency at two settings, marked as +tc in the SPI register documentation. In these settings, the driver current is increased by one step when the temperature warning threshold is reached.

Status flag	Description	Range	Comment
OTPW	Overtemperature pre-warning. This bit indicates that the pre-warning level is reached. The controller can react to this setting by reducing power dissipation.	0 / 1	1: temperature prewarning level reached
OT	Overtemperature warning. This bit indicates that the overtemperature threshold has been reached and that the driver is switched off due to overtemperature.	0 / 1	1: driver shut down due to overtemperature

11.4 Undervoltage detection

The undervoltage detector monitors both, the internal logic supply voltage and the driver supply voltage. It prevents operation of the chip at voltages, where a proper control of the MOSFET switches cannot be guaranteed due to too low gate drive voltage.

In undervoltage conditions, the logic control block becomes reset and the driver is disabled. All MOSFETs become switched off. The processor thus also should monitor the supply voltage to detect an undervoltage condition. If the processor does not have an access to the voltage, the TMC389 can directly be monitored via its SPI interface sending out only zero bits and not shifting through information. A reset due to undervoltage or an actual undervoltage condition can be determined for example by monitoring the current setting via its read back function. The current setting CS becomes reset to zero, which can be seen when reading back the actual SE value.

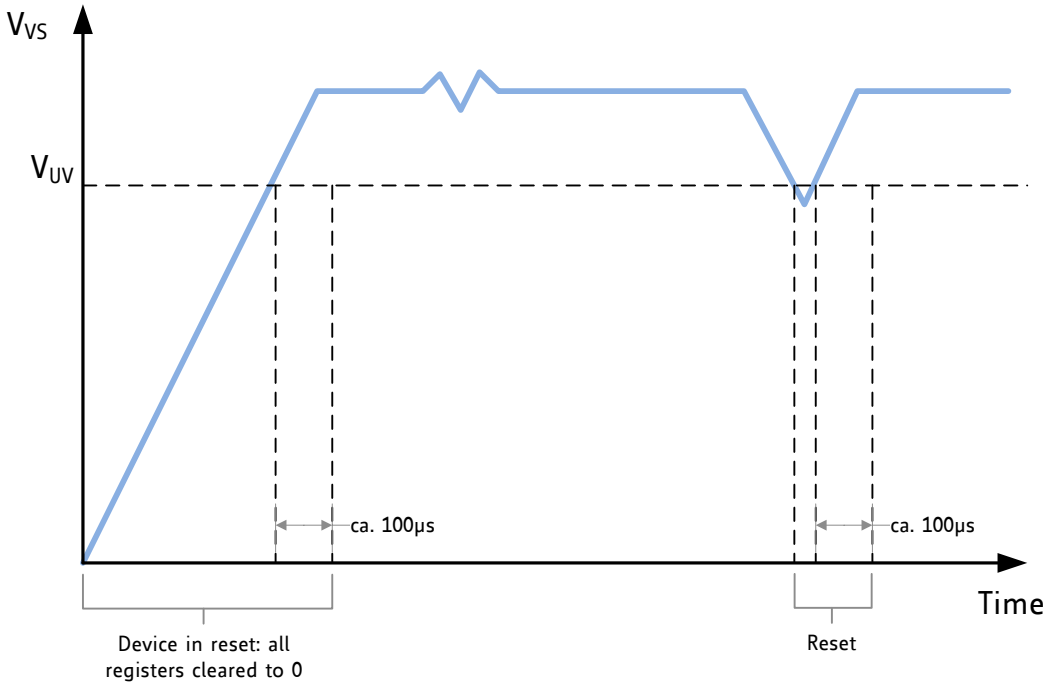


figure 14 Undervoltage reset timing

Be sure to operate the IC significantly above the undervoltage threshold in order to assure reliable operation! Check for SE read back at zero to detect an undervoltage event.

12 stallGuard2™ sensorless load measurement

stallGuard2™ delivers a sensorless load measurement of the motor as well as a stall detection signal available via the SG_TST output. The measured value changes linear with the load on the motor in a wide range of load, velocity and current settings. At maximum motor load the stallGuard™ value goes to zero. This corresponds to a load angle of 90° between the magnetic field of the stator and magnets in the rotor. This also is the most energy efficient point of operation for the motor.

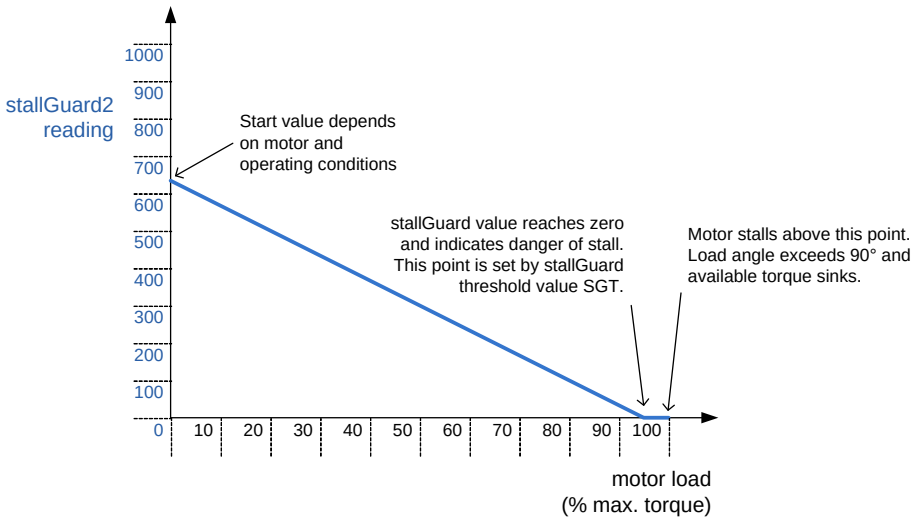


figure 15: Principle function of stallGuard2

In order to use stallGuard2™ and coolStep™, the stallGuard2™ sensitivity should first be tuned using the SGT setting.

12.1 Tuning the stallGuard2™ threshold SGT

The sensorless motor measurement depends on a number of motor specific parameters and operation parameters. The easiest way to find a parameter set which fits to a specific motor type and operating conditions is interactive tuning:

Operate the motor at a reasonable velocity (taking into account your application) and monitor the stallGuard™ value (SG). Now, apply slowly increasing mechanical load to the motor. Now, try best setting for SSPD and SFILT to have low noise on the signal, but high amplitude. If the motor stalls before the stallGuard™ value reaches zero, decrease the stallGuard threshold value (SGT). A good starting value is zero. You can apply negative values and positive values. If the SG value reaches zero far before the motor stalls, increase the SGT value.

The optimum setting is reached, when the stallGuard2™ value reaches zero at increasing load shortly before the motor stalls due to overload. However, this point can be shifted above 100% load, too. In this case, activation of the stall output indicates, that a step has been lost. In order not to miss this point, SFILT should to be turned off.

Please be aware, that the driver clock frequency influences the SG results. You should provide an external stabilized clock for best performance. As the measurement has a high resolution, there are a number of additional possibilities to enhance the absolute precision in order to give a good match to the mechanical load on the motor. The optimum SGT value depends on a number of operating parameters which can be compensated for, as shown in the next chapters.

12.1.1 Variable velocity operation

At varying velocities, SSPD and SFILT may be adapted to the actual velocity value in order to provide the best results. Also an adaptation of the stallGuard2™ threshold value SGT can improve the exactness of the load measurement and thus of coolStep™, which is based on the load measurement value. At very low velocities, a reliable load measurement is not possible. At high velocities, where the

motor back EMF reaches the supply voltage, load angle increases and the measurement response is lower. This can be seen in the example taken with a motor in an acceleration phase.

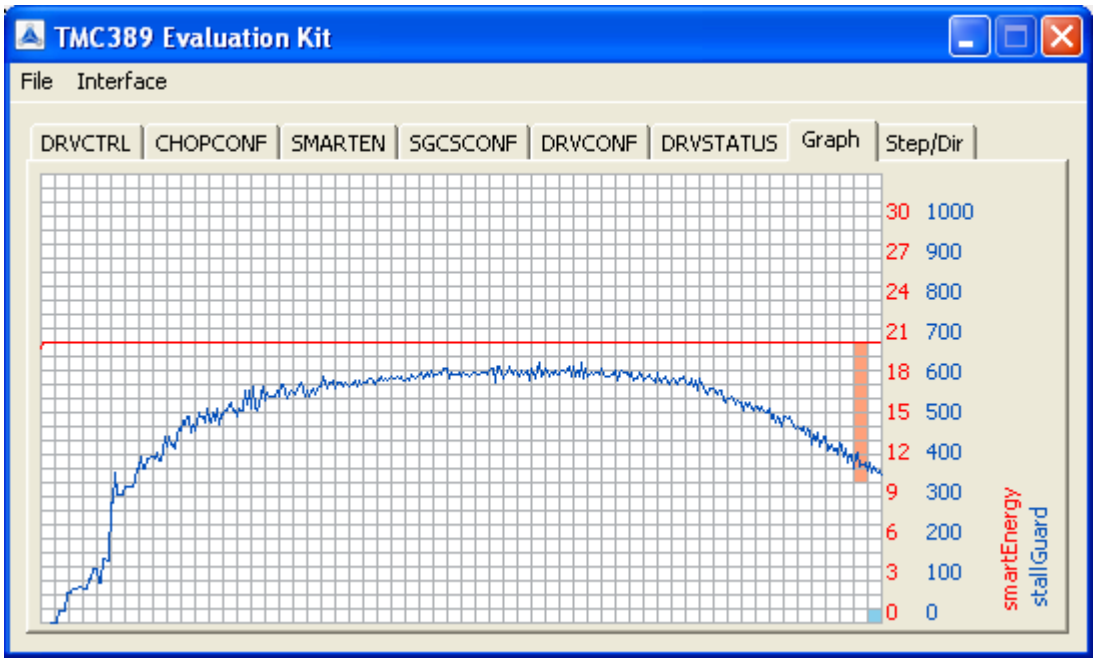


figure 16: Example SG result with a 60mm 3 phase motor without load accelerated from 0 to 375 RPM

12.1.2 Accuracy and reproducibility of stallGuard2™ measurement

Most of the stray in stallGuard2™ reading will result from motor production stray. Other factors which can be compensated for are motor temperature, motor driver supply voltage and TMC389 clock frequency. A stabilized driver supply voltage and an external clock source should be used in these applications. The measurement error of stallGuard2™ – provided that all other parameters remain stable – can be assumed as low as:

$$stallGuard\ measurement\ error = \pm 1$$

12.2 stallGuard2™ measurement frequency and filtering

The stallGuard2™ value becomes updated with each two fullsteps of the motor. This is enough to safely detect a stall, as stalling of the motor always means the loss of six full steps. In a practical application, especially when using coolStep™, a more precise measurement might be more important than an update for each fullstep, taking into account that mechanical load never changes instantaneously from one step to the next. Therefore, a filtering function is available: The SFILT bit enables filtering of the motor load measurement over a number of 3 measurements. The filter should always be enabled when a precise measurement is desired. It compensates for anisotropies in the construction of the motor, e.g. due to misalignment of the magnet poles. Only if very fast response to increasing load is required, the bit should be cleared.

12.3 Detecting a motor stall

In order to safely detect a motor stall a stall threshold must be determined using a specific SGT setting. Therefore, you need to determine the maximum load the motor can drive without stalling and to monitor the SG value at this load, e.g. some value within the range 0 to 100. The stall threshold should be a value safely within the operating limits, to allow for parameter stray. So, you should set a stall threshold in your microcontroller software, which is slightly higher than the minimum value seen before an actual motor stall occurs. The response at an SGT setting at or near 0 gives some idea on the quality of the signal: Check the SG value without load and with maximum load. They should show a difference of at least 100 or a few 100, which shall be large compared to the offset. If you set the SGT value in a way, that a reading of 0 occurs at maximum motor load, an active high stall output signal is available at SG_TST output.

12.4 Limits of stallGuard2™ operation

Please bear in mind, that stallGuard2™ will not operate reliable at extreme motor velocities: Very low motor velocities (e.g. for many motors less than one round per second) generate a low back EMF in the motor and make the measurement instable and dependent on environment conditions like temperature, etc. Inappropriate conditions will also lead to extreme settings of SGT and low response of the SG result to the motor load. On the other hand, very high motor velocities, where the driver is not able to drive the full sinusoidal current into the motor coils also will lead to a low response in the SG result. These velocities are typically characterized by the motor back EMF reaching the driver supply voltage.

Parameter	**Description**	**Setting**	**Comment**
SGT	This signed value controls *stallGuard2™ threshold* level for stall output and sets the optimum measurement range for readout. A lower value gives a higher sensitivity. Zero is the starting value working with most motors. A higher value makes stallGuard less sensitive and requires more torque to indicate a stall.	0	indifferent value
		+1… +63	less sensitivity
		-1…-64	higher sensitivity
SFILT	Enables the *stallGuard2™ filter* for more precision of the measurement. If set, reduces the measurement frequency to one measurement per six fullsteps. In standard mode, a measurement is taken each two fullsteps.	0	standard mode
		1	filtered mode
SSPD	Selects the filtering for less noise at low motor velocities.	0	standard mode
		1	low velocity mode
Status word	**Description**	**Range**	**Comment**
SG	This is the *stallGuard2™ result*. A higher reading indicates less mechanical load. A lower reading indicates a higher load and thus a higher load angle. Tune the SGT setting to show a SG reading of 0 at maximum load before motor stall. This is also signaled by the output SG_TST.	0… 1023	0: maximum load low value: high load high value: less load

13 coolStep™ smart energy operation

In order to use coolStep™, you should first tune the stallGuard2™ sensitivity. coolStep™ uses the stallGuard2™ measurement, to operate the motor near the optimum load angle of +90°.
See example figure.

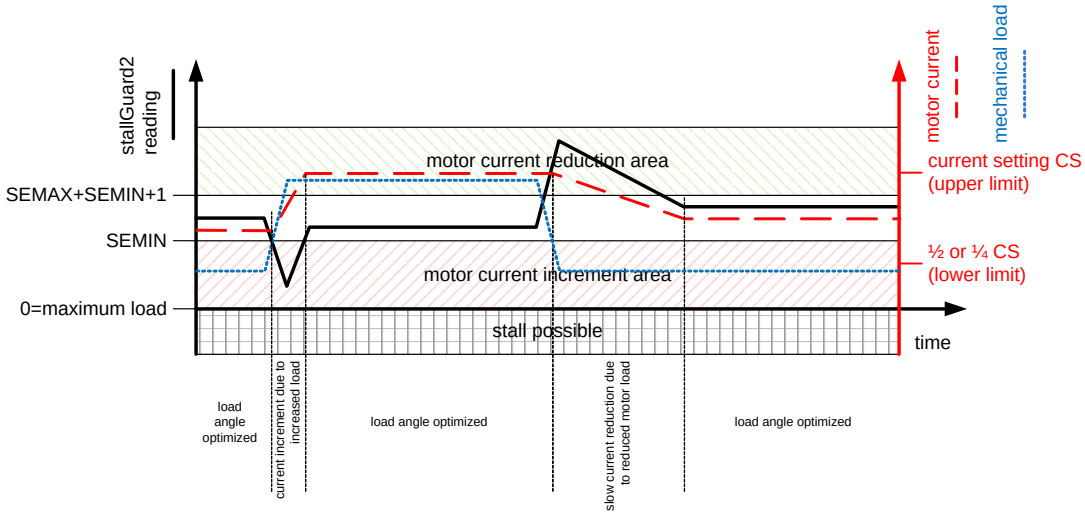


figure 17: Motor current control via coolStep adapts motor current to motor load

13.1 coolStep™ smart energy current regulator

The coolStep™ current regulator allows to control the reaction of the driver to increasing or decreasing load. The internal regulator uses two thresholds to determine the minimum and the maximum load angle for optimum motor operation. The current increment speed and the current decrement speed can be adapted to the application. Additionally, the lower current limit can be set in relation to the upper current limit set by the current scale parameter CS.

13.1.1 Adaptation to the load situation

To allow the motor current to quickly respond to increasing motor load, use a high current increment step. If the motor load changes only slowly, a lower current increment step can be used. The current decrement can then be adapted to work as quickly as possible, while avoiding oscillations of the motor. Keep in mind, that enabling the stallGuard2™ filter via SFILT reduces the measurement speed and thus the regulation speed.

13.1.2 Low velocity and standby operation

Since coolStep™ is not able to detect the motor load in standstill and at very low RPM operation, the current at low velocities should be set to an application specific default value and should be combined with a stand still current reduction. Switch off coolStep™ at low velocities, to avoid reaction to false stallGuard™ reading.

Parameter	Description	Setting	Comment
SEMIN	Sets the *lower threshold* for stallGuard2™ reading. Below this value, the motor current becomes increased. Set SEMIN to zero to disable coolStep™.	0…15	lower stallGuard threshold: SEMIN*32
SEMAX	Sets the *distance* between the lower and the *upper threshold* for stallGuard2™ reading. Above the upper threshold the motor current becomes decreased.	0…15	upper stallGuard threshold: (SEMIN+SEMAX+1)*32
SEUP	Sets the *current increment step*. The current becomes incremented for each measured stallGuard2™ value below the lower threshold.	0…3	step width is 1, 2, 4, 8
SEDN	Sets the number of stallGuard2™ readings above the upper threshold necessary for each *current decrement* of the motor current.	0…3	number of stallGuard measurements per decrement: 32, 8, 2, 1
SEIMIN	Sets the *lower motor current limit* for coolStep™ operation by scaling the CS value.	0	1/2 of CS
		1	1/4 of CS
Status word	**Description**	**Range**	**Comment**
SE	This status value provides the *actual motor current* setting as controlled by coolStep™. The value goes up to the CS value and down to the portion of CS as specified by SEIMIN.	0…31	1/32, 2/32, … 32/32

13.2 User benefits, save energy, reduce power and cooling infrastructure

coolStep™ allows saving a lot of energy, especially for motors which see varying loads and operate at a high duty cycle. Taking into account that a stepper motor application needs to work with a torque reserve of 30% to 50%, even a constant load application allows saving lots of energy, because the driver automatically enables torque reserve when required. The reduction in power dissipation further keeps the system cooler and increases life time and allows savings in the power supply and cooling infrastructure. Keep in mind, that half motor current means a quarter of the power dissipation in the motor coils. This power dissipation makes up for most of the stepper motor losses!

The following figure shows shows the efficiency gain of a 42mm stepper motor when using coolStep compared to standard operation with 50% of torque reserve. coolStep is enabled above 60rpm in the example.

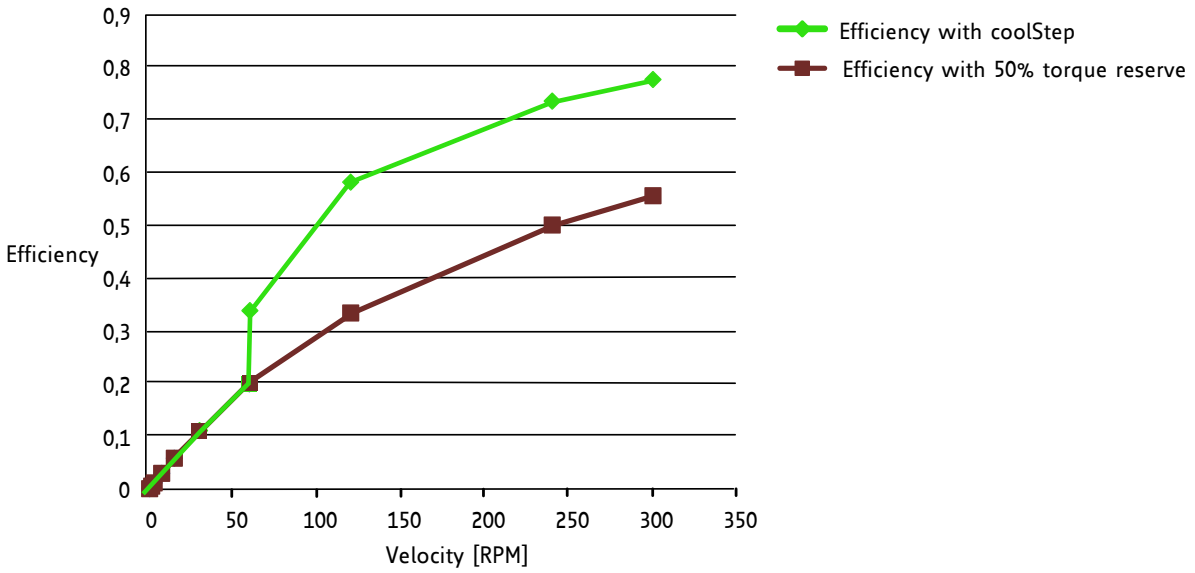


figure 18: Energy efficiency with coolStep (example)

14 Power Supply Sequencing

The TMC389 generates its own 5V supply for all internal operations. The internal reset of the chip is derived from the supply voltage regulator in order to ensure a clean start-up of the device after power up. During start up, the SPI unit is in reset and cannot be addressed. All registers become cleared.

VCC_IO limits the voltage allowable on the inputs and outputs and is used for driving the outputs, but input levels thresholds are not depending on the actual level of VCC_IO. Therefore, the startup sequence of the VCC_IO power supply with respect to VS is not important.

15 Clock oscillator and clock input

The internal clock frequency for all operations is nominal 15MHz. An external clock of 10MHz to 20MHz (16MHz recommended for optimum performance) can be supplied for more exact timing, especially when using coolStep™ and stallGuard2™. Alternatively, the internal clock frequency can be measured, by measuring the delay time after the last step, until the TMC389 raises the STANDSTILL flag. From this measurement, chopper timing parameters can be corrected, as the internal oscillator is relatively stable over a wide range of environment temperatures.

An external clock frequency of up to 20MHz can be supplied. The external clock is enabled with the first positive polarity seen on the CLK input. Tie the CLK input to GND near to the TMC389 if the internal clock oscillator is to be used. Switching off the external clock frequency prevents the driver from operating normally. Be careful to switch off the motor before switching off the clock (e.g. using the enable input), because otherwise the chopper would stop and the motor current level could rise uncontrolled. The short to GND detection stays active even without clock, if enabled.

15.1 Considerations on the frequency

A higher frequency allows faster step rates, faster SPI operation and higher chopper frequencies. On the other hand, it may cause more electromagnetic emission and causes more power dissipation in the TMC389 digital core. Generally a frequency of 8MHz to 16MHz should be sufficient for most applications, unless the motor is to operate very fast. For reduced requirements concerning the motor dynamics, a clock frequency of 4 to 8MHz should be considered.

16 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances. Operating the circuit at or near more than one maximum rating at a time for extended periods shall be avoided by application design.

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{VS}	-0.5	60	V
Supply voltage max. 20000s		-0.5	65	V
Logic supply voltage	V_{VCC}	-0.5	6.0	V
I/O supply voltage	V_{VIO}	-0.5	6.0	V
Logic input voltage	V_I	-0.5	V_{VIO}+0.5	V
Analog input voltage	V_{IA}	-0.5	V_{CC}+0.5	V
Voltages on low side driver pins (LX)	V_{OLS}	-0.7	V_{CC}+0.7	V
Voltages on high side driver pins (HX)	V_{OHS}	V_{HS} - 0.7	V_{VM}+0.7	V
Voltages on BM pins (BMX)	V_{IBM}	-5	V_{VM}+5	V
Relative high side driver voltage (V_{VM} – V_{HS})	V_{HSVM}	-0.5	15	V
Maximum current to / from digital pins and analog low voltage I/Os	I_{IO}		+/-10	mA
Non destructive short time peak current into input / output pins	I_{IO}		500	mA
5V regulator output current	I_{5VOUT}		50	mA
5V regulator peak power dissipation (V_{VM}-5V) * I_{5VOUT}	P_{5VOUT}		1	W
Junction temperature	T_J	-50	150	°C
Storage temperature	T_{STG}	-55	150	°C
ESD-Protection (Human body model, HBM), in application	V_{ESDAP}		1	kV
ESD-Protection (Human body model, HBM), device handling	V_{ESDDH}		300	V

17 Electrical Characteristics

17.1 Operational Range

Parameter	Symbol	Min	Max	Unit
Junction temperature	T_J	-40	125	°C
Supply voltage	V_{VS}	9	59	V
I/O supply voltage	V_{VIO}	3.00	5.25	V

17.2 DC Characteristics and Timing Characteristics

DC characteristics contain the spread of values guaranteed within the specified supply voltage range unless otherwise specified. Typical values represent the average value of all parts measured at +25°C. Temperature variation also causes stray to some values. A device with typical values will not leave Min/Max range within the full temperature range.

Power supply current	**DC-Characteristics** V_{VS} = 24.0V					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Supply current, operating	I_{VS}	f_{CLK}=16MHz, 40kHz chopper, Q_G=10nC		13		mA
Supply current, driver disabled	I_{VS}	f_{CLK}=16MHz		10		mA
Supply current, driver disabled, dependency on CLK frequency	I_{VS}	f_{CLK} variable, *additional to I_{VS0}*		0.37		mA/ MHz
Static supply current	I_{VS0}	f_{CLK}=0Hz, digital inputs at +5V or GND		3.1	4	mA
Part of supply current NOT consumed from 5V supply	I_{VSHV}	driver disabled		1.1		mA
IO supply current	I_{VIO}	no load on outputs, inputs at V_{IO} or GND		0.3		µA

NMOS low side driver	**DC-Characteristics** V_{LSX} = 2.5V, slope setting controlled by SLPL					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Gate drive current LX low side switch ON [a)]	I_{LSON}	SLPL=00/01		12		mA
Gate drive current LX low side switch ON [a)]	I_{LSON}	SLPL=10		21		mA
Gate drive current LX low side switch ON [a)]	I_{LSON}	SLPL=11	20	31	50	mA
Gate drive current LX low side switch OFF [a)]	I_{LSOFF}	SLPL=00/01		-13		mA
Gate drive current LX low side switch OFF [a)]	I_{LSOFF}	SLPL=10		-25		mA
Gate drive current LX low side switch OFF [a)]	I_{LSOFF}	SLPL=11	-25	-37	-60	mA
Gate Off detector threshold	V_{GOD}	V_{LSX} falling		1		V
Q_{GD} protection resistance after detection of gate off	$R_{LSOFFQGD}$	SLPL=11 V_{LSX} = 1V		26	50	Ω
Driver active output voltage	V_{LSON}			V_{VCC}		V

Notes:

a) Low side drivers behave similar to a constant current source between 0V and 2.5V (switching on) resp. between 2.5V and 5V (switching off), because switching MOSFETs go into saturation. At 2.5V, the output current is about 85% of peak value. This is the value specified.

PMOS high side driver	**DC-Characteristics** V_{VS} = 24.0V, V_{VS} - V_{HSX} = 2.5V, slope setting controlled by SLPH					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Gate drive current HX high side switch ON [b]	I_{HSON}	SLPH=00/01		-15		mA
Gate drive current HX high side switch ON [b]	I_{HSON}	SLPH=10		-29		mA
Gate drive current HX high side switch ON [b]	I_{HSON}	SLPH=11	-25	-42	-70	mA
Gate drive current HX high side switch OFF [c]	I_{HSOFF}	SLPH=00/01		15		mA
Gate drive current HX high side switch OFF [c]	I_{HSOFF}	SLPH=10		29		mA
Gate drive current HX high side switch OFF [c]	I_{HSOFF}	SLPH=11	28	43	70	mA
Gate Off detector threshold	V_{GOD}	V_{HSX} rising		V_{VS}-1		V
Q_{GD} protection resistance after detection of gate off	$R_{HSOFFQGD}$	SLPH=11 V_{HSX} = V_{VS} - 1V		32	60	Ω
Driver active output voltage	V_{HSON}	I_{OUT} = 0mA	V_{VHS}-2.8	V_{VHS}-2.3	V_{VHS}-1.8	V

Notes:

b) High side switch on drivers behave similar to a constant current source between V_{VS} and V_{VS} – 2.5V. At V_{VS}-2.5V, the output current is about 90% of peak value. This is the value specified.

c) High side switch off drivers behave similar to a constant current source between V_{VS} - 8V and V_{VS}-2.5V. At V_{VS}-2.5V, the output current is about 65% of peak value. This is the value specified.

High side voltage regulator	**DC-Characteristics** V_{VS} = 24.0V					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Output voltage	V_{VHS}	I_{OUT} = 0mA T_J = 25°C	9.3	10.0	10.8	V
Output resistance	R_{VHS}	Static load		50		Ω
Deviation of output voltage over the full temperature range	$V_{VHS(DEV)}$	T_J = full range		60	200	mV
DC Output current	I_{VHS}				4	mA
Current limit	I_{VHSMAX}			15		mA
Series regulator transistor output resistance (determines voltage drop at low supply voltages)	R_{VHSLV}			400	1000	Ω

Linear regulator	**DC-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Output voltage	V_{5VOUT}	I_{5VOUT} = 10mA T_J = 25°C	4.75	5.0	5.25	V
Output resistance	R_{5VOUT}	Static load		3		Ω
Deviation of output voltage over the full temperature range	$V_{5VOUT(DEV)}$	I_{5VOUT} = 10mA T_J = full range		30	60	mV
Output current capability (attention, do not exceed maximum ratings with DC current)	I_{5VOUT}	V_{VS} = 12V	100			mA
		V_{VS} = 8V	60			mA
		V_{VS} = 6.5V	20			mA

Clock oscillator and input	**Timing-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Clock oscillator frequency	f_{CLKOSC}	t_J=-50°C	10.0	14.3		MHz
Clock oscillator frequency	f_{CLKOSC}	t_J=50°C	10.8	15.2	20.0	MHz
Clock oscillator frequency	f_{CLKOSC}	t_J=150°C		15.4	20.3	MHz
External clock frequency (operating)	f_{CLK}		4		20	MHz
External clock high / low level time	t_{CLK}		12			ns

Detector levels	**DC-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{VS} undervoltage threshold	V_{UV}		6.5	8	8.5	V
Short to GND detector threshold (V_{VS} - V_{BMx})	V_{BMS2G}		1.0	1.5	2.3	V
Short to GND detector delay (low side gate off detected to short detection)	t_{S2G}	TS2G=00	2.0	3.2	4.5	µs
		TS2G=10		1.6		µs
		TS2G=01		1.2		µs
		TS2G=11		0.8		µs
Overtemperature prewarning	t_{OTPW}		80	100	120	°C
Overtemperature shutdown	t_{OT}	Temperature rising	135	150	170	°C

Sense resistor voltage levels	**DC-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Sense input peak threshold voltage (low sensitivity)	$V_{SRTRIPL}$	VSENSE=0 Cx=248; Hyst.=0	290	310	330	mV
sense input peak threshold voltage (high sensitivity)	$t_{SRTRIPH}$	VSENSE=1 Cx=248; Hyst.=0	153	165	180	mV

Digital logic levels	**DC-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input voltage low level [d)]	V_{INLO}		-0.3		0.8	V
Input voltage high level [d)]	V_{INHI}		2.4		V_{VIO}+0.3	V
Output voltage low level	V_{OUTLO}	I_{OUTLO} = 1mA			0.4	V
Output voltage high level	V_{OUTHI}	I_{OUTHI} = -1mA	$0.8V_{VIO}$			V
Input leakage current	I_{ILEAK}		-10		10	µA

Notes:

d) Digital inputs left within or near the transition region substantially increase power supply current by drawing power from the internal 5V regulator. Make sure that digital inputs become driven near to 0V and up to the V_{IO} I/O voltage.

17.3 ESD sensitive device

The TMC389 is an ESD sensitive CMOS device and also MOSFET transistors used in the application schematic are very sensitive to electrostatic discharge. Take special care to use adequate grounding of personnel and machines in manual handling. After soldering the devices to the board, ESD requirements are more relaxed. Failure to do so can result in defect or decreased reliability.

Note: In a modern SMD manufacturing process, ESD voltages well below 100V are standard. A major source for ESD is plugging the motor during operation. As the TMC389 power MOSFETs are external, the device in fact is very rugged concerning any ESD event. All other connections are typically protected due to external circuitry on the PCB.

17.4 MOSFET examples

There is a number of N&P channel paired MOSFETs available, which fit the TMC389, as well as single N and P devices. The user choice will depend on the electrical data (voltage, current, RDSon) and on the package and configuration (single / dual). The following table gives a few examples of SMD MOSFET pairs for different motor voltages and currents. The MOSFETs explicitly are modern types with a low total gate charge. For the actual application, we suggest to calculate static and dynamic power dissipation for a given MOSFET pair.

A total gate charge Q_G below 20nC (at 5V) is best for reaching reasonable slopes.
The performance (Q_G and R_{DSon}) of the low-side MOSFET contributes to 70% to the overall efficiency.

Transistor Type	Manu-facturer	Voltage V_{DS}	Max. RMS Current (*)	Package	R_{DSon} N (5V)	R_{DSon} P (8V)	Q_G N	Q_G P	Test board size
Unit		**V**	**A**		**mΩ**	**mΩ**	**nC**	**nC**	**cm²**
QM6006D QM6015D	UBIQ	60	8	DPAK	16	22	19	25	e160
AOD4130 AOD409	A&O	60	7	DPAK	30	35	13	22	e160
SUD23N06 SUD19P06	Vishay	60	6	DPAK	35	50	8	22	e160
AP4575-GH	APEC	60	4	TO252-4L	31	64	13	14	64
AOD603A	A&O	60	3	TO252-4L	67	95	4	16	e70
SI7414 SI7415	Vishay	60	3	PPAK1212	28	60	9	12	35
QM6301S	UBIQ	60	3	SO8	30	65	13	10	27
AO4612	A&O	60	2.5	SO8	64	90	5	8	e27
SI4559ADY	Vishay	60	2.5	SO8	55	110	7	12	e27
AOD4184A AOD4189	A&O	40	10	TO252	9	20	14	15	e70
AOD4186 AOD4185	A&O	40	8	DPAK	15	14	9	19	70
FDD8647L FDD4243	Fairchild	40	7	DPAK	13	40	12	18	e100
QM4302D	UBIQ	40	5.5	TO252-4L	15	30	11	12	e40
QM4803D	UBIQ	40	4	TO252-4L	28	35	6	9	e40
FDD8424H	Fairchild	40	4	DPAK-4L	23	45	9	14	40
AOD609	A&O	40	4	TO252-4L	31	40	5	9	e40
AP4525GEH	APEC	40	3.5	TO252-4L	32	45	9	9	40
AO4618	A&O	40	3.5	SO8	21	22	3	8	e27
SI4564	Vishay	40	3.5	SO8	17	20	10	22	e27
AO4614B	A&O	40	3	SO8	38	45	4	8	e27
SI4599DY	Vishay	40	3	SO8	36	45	5	12	e27
FDS8960C	Fairchild	35	3.5	SO8	20	45	6	9	e27
BSZ050N03 BSZ180P03	Infineon	30	11	S3O8	7	18	13	15	70
AOD607	A&O	30	4	TO252-4L	34	37	10	10	40
AO4616	A&O	30	3.5	SO8	24	24	9	16	e27
FDS8958A	Fairchild	30	3.5	SO8	25	45	6	9	e27
AON7611	A&O	30	3	DFN3x3EP	53	35	2	5	15
AP4503BGM	APEC	30	3	SO8	35	35	6	12	e27
SI4532CDY	Vishay	30	3	SO8	50	80	3	4	e27

(*) Remark: The maximum motor current applicable in a given design depends upon PCB size and layout, since all of these transistors are mainly cooled via the PCB. The data given implies adequate cooling measures taken by the user, especially for higher current designs. The maximum RMS current rating is meant as a hint. It takes into account package power dissipation, on resistances and gate charges.

18 Using an external power stage for higher voltage or current

The TMC389 uses a completely complementary driving scheme for power transistors. This allows attaching an external gate driver, using the low side driver output information, only. Therefore, the external gate driver needs to bring brake-before make capability. You can directly attach gate driver ICs like TMC603 as gate drivers for high current NMOS transistor bridges. The TMC603 also supplies a gate drive voltage regulator and allows 100% duty cycle. Please refer TMC603 datasheet. The example shows the TMC603 driver boosting TMC389. The higher gate driving capability allows addressing designs for more than 20A. Different gate driver ICs are available on the market which also allow for higher voltages.

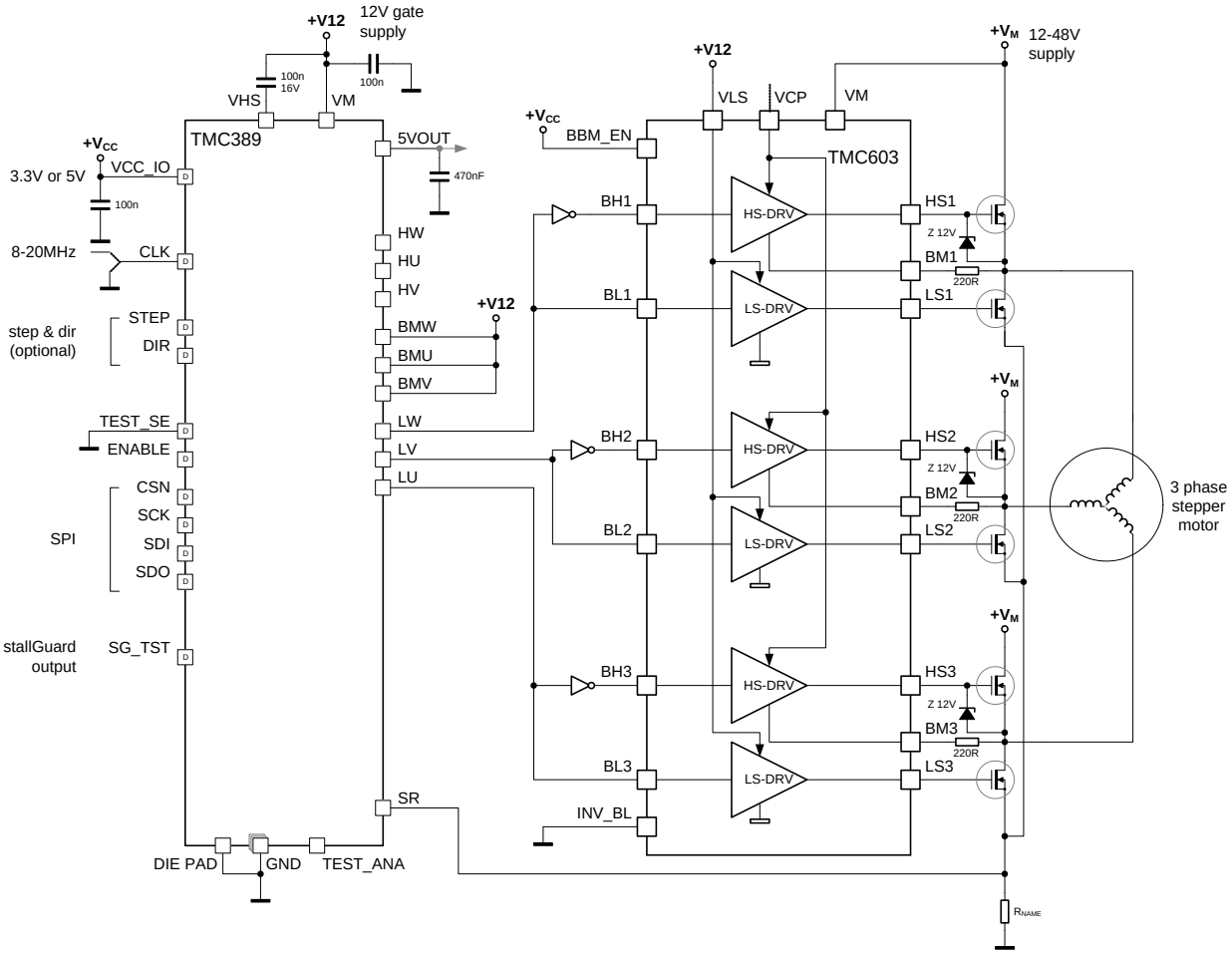


figure 19: High current high voltage power stage using additional gate drivers (example)

Please be aware, that the short to GND protection of the TMC389 cannot be used in this scheme: The driver cannot be fully disabled, because the external gate driver just switches on either high side MOSFET or low side MOSFET. An external short to GND protection could use a series resistor to measure power bridge current and to disable the high side MOSFETs by using the TMC389 enable input ENN. Use a gate driver like TMC603 to provide additional short to GND protection without the need for a high side shunt.

19 Getting started

19.1 Initialization of the driver

Initialization SPI datagram example sequence to enable the driver and initialize the chopper:

```
//SPI Datagrams for configuring the TMC389
//Creation date: 23.11.2010 12:18:43
//DRVCTRL register (1/16 microstep with interpolation to 256 microsteps)
unsigned char DRVCTRL[3] = {0x00, 0x02, 0x04};

//CHOPCONF register (NOSD, HYST=40)
unsigned char CHOPCONF[3] = {0x09, 0x8E, 0x85};

//SMARTEN register (off)
unsigned char SMARTEN[3] = {0x0A, 0x00, 0x00};

//SGSCONF register (current setting=19)
unsigned char SGSCONF[3] = {0x0D, 0x00, 0x13};

//DRVCONF register
unsigned char DRVCONF[3] = {0x0E, 0xF0, 0x00};
```

First test of coolStep™ current control:

```
//SMARTEN register (SEMIN=2, SEMAX=2)
unsigned char SMARTEN[3] = {0x0A, 0x02, 0x02};
```

Please note, that the configuration parameters should be tuned to the motor and application for optimum performance.

19.2 Sending SPI data from a CPU

SPI slaves can either be chained or be used with a single chip select line. If slaves are chained, they behave like a long shift register, e.g. a chain of two drivers requires 40 bits to be sent. The last bits shifted to each register in the chain are clocked into the holding register with the rising CSN signal. This means, that for example 24 or 32 bit can be sent to a single driver, but it latches just the lower 20 bits.

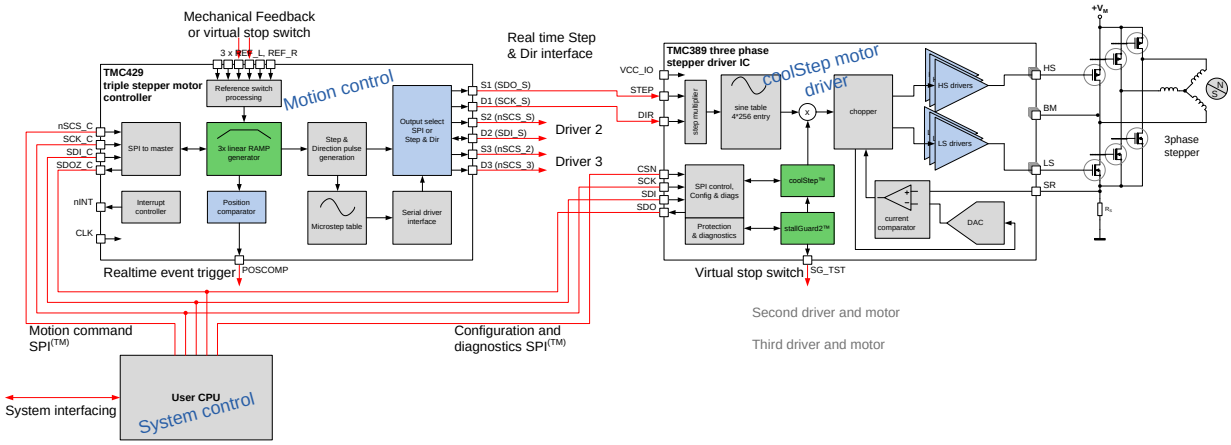


figure 20: Sample system showing SPI interconnection and TMC429 StepDir controller IC

20 Table of figures

21 Revision History

21.1 Documentation Revision

Version	Date	Author BD=Bernhard Dwersteg	Description
0.2	2010-APR-28	BD	Register map corresponds to test chip
0.3	2010-OKT-10	BD	updated schematic and register bits
0.4	2010-NOV-03	BD	removed TMC388 information, added preliminary
1.02	2010-NOV-23	BD	First release of complete datasheet
1.03	2010-NOV-26	BD	added disclaimer, SPI details
1.05	2011-FEB-16	BD	minor corrections
1.06	2011-MAR-09	BD	Corrected undervoltage threshold, chopper thresholds
1.07	2011-APR-22	BD	Slightly corrected gate driver current levels, corrected pinning table according to pinout
1.08	2011-JUL-26	BD	Updated MOSFET list, typ. f_{CLKOSC} is 15MHz (old: 13MHz)
1.09	2011-DEC-29	BD	Minor modifications in look of tables, added % for binary
1.10	2012-FEB-06	BD	Minor Fix, added coolStep efficiency example
1.11	2012-MAY-29	BD	Minor Fix concerning wording “Fullstep”
1.12	2012-JUN-27	BD	Added / revised power supply sequencing
1.13	2012-AUG-13	SD	figure 14 (undervoltage reset timing) new
1.14	2013-MAY-14	BD	Updated MOSFET list Updated current ratings after tests / more coarse rating
1.15	2015-OCT-27	BD	Updated MOSFET list

Table 1: Documentation Revisions