TMD3721

ALS/Color and Proximity Sensor Module for Behind OLED Applications

General Description

The TMD3721 features ambient light, color (RGB) sensing and proximity detection. The device integrates an IR VCSEL and an advanced VCSEL driver within a compact 4.65mm x 1.86mm x 0.90mm OLGA package.

The ambient light and color sensing function provides four concurrent ambient light sensing channels: Red, Green, Blue, and Clear. The RGB and Clear channels are covered with an UV/IR blocking filter. This architecture accurately measures ambient light and enables the calculation of illuminance and color temperature to manage display appearance.

The proximity function synchronizes IR emission and detection to sense nearby objects. The architecture of the engine features self-maximizing dynamic range, ambient light subtraction, advanced crosstalk cancellation, and interrupt-driven I^2C communication. Sensitivity, power consumption, and noise can be optimized with adjustable IR VCSEL timing and power. The proximity engine recognizes detect/release events and produces a configurable interrupt whenever the proximity result crosses upper or lower threshold settings.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD3721 are listed below:

Figure 1:
Added Value of Using TMD3721

Benefits	Features
• Proximity detection behind OLED displays	• Integrated factory calibrated 940nm IR VCSEL • Display synchronization with highly programmable Proximity Start Delay (PSD) • Crosstalk and ambient light cancellation • Optimized sensitivity and noise level • Wide configuration range
• Ambient light sensing behind OLED displays	• Red, green, blue and clear ALS channels with improved sensitivity • Highly programmable gain and integration time • Display synchronization with highly programmable ALS Start Delay (ASD) • 737kHz ALS clock rate • 1KB FIFO
• Low power consumption	• 1.8V power supply with 1.8V I^2C bus • Configurable sleep mode • Interrupt driven device
• Integrated status checking for all functions	• Proximity saturation flag • Digital and analog ALS saturation flags • VSYNC status check

Applications

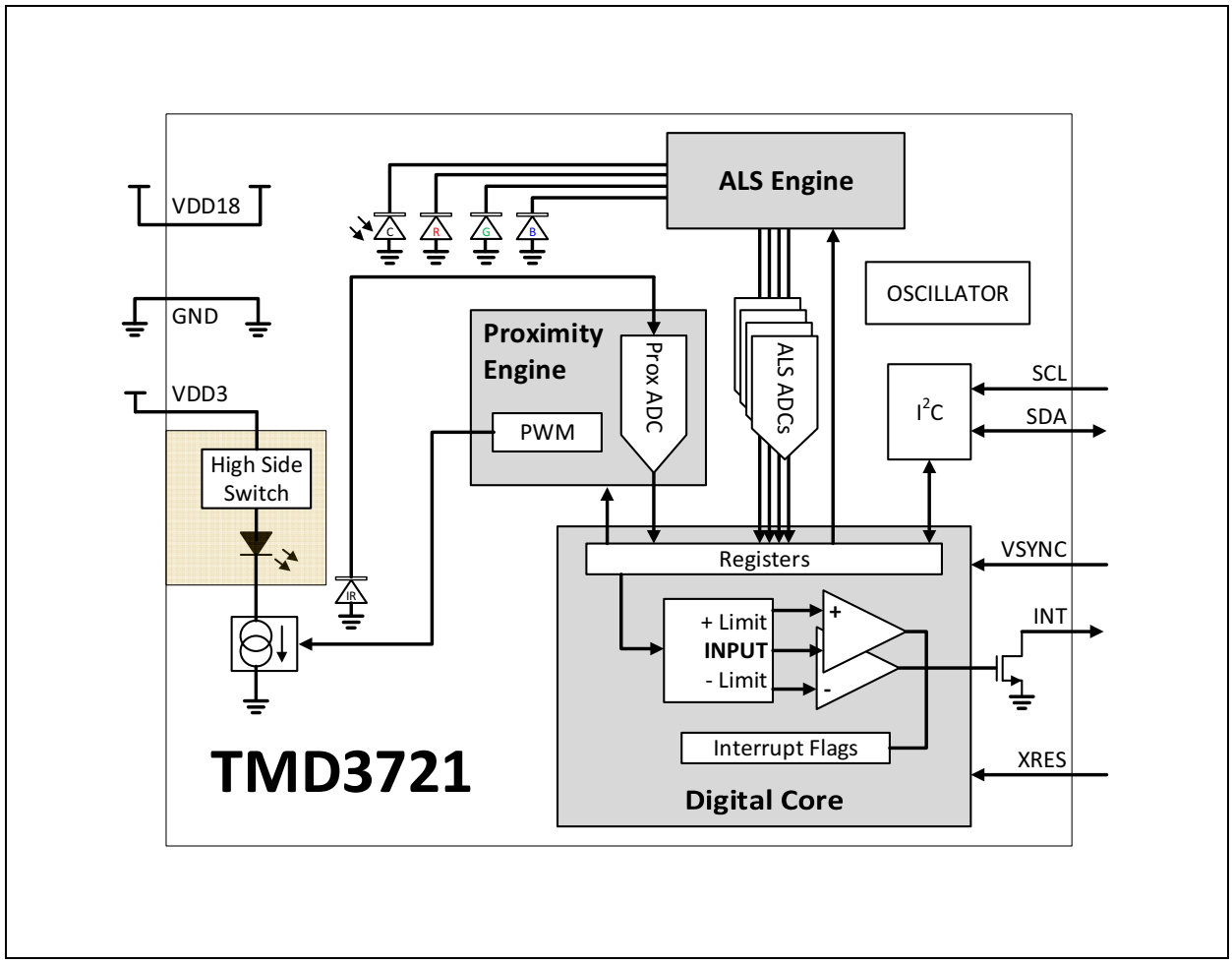
The TMD3721 applications include:

- Brightness management for displays
- Color management for displays
- Proximity detection for mobile phones

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMD3721



Pin Assignments

Figure 3:
Pin Diagram

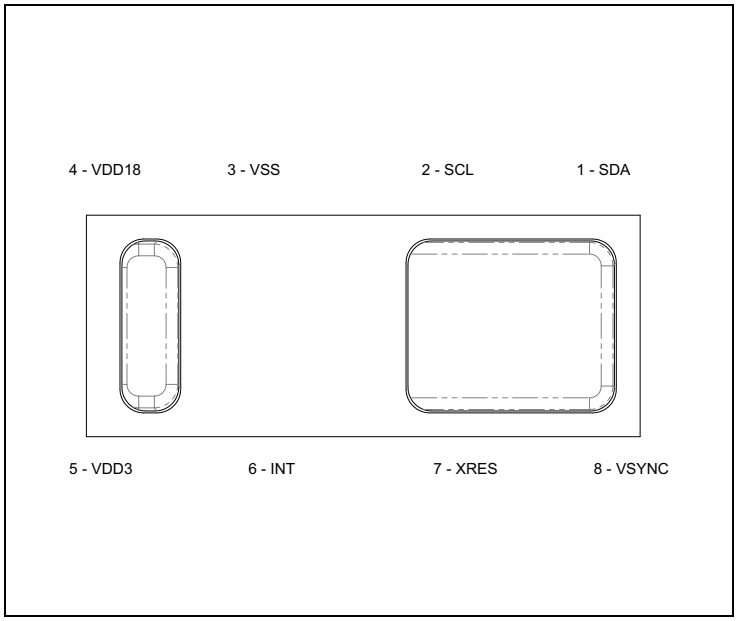


Figure 4:
Pin Description of TMD3721

Pin No.	Pin Name	Description	If Not Use
1	SDA	I^2C serial data I/O terminal	Mandatory
2	SCL	I^2C serial clock input terminal	Mandatory
3	VSS	Ground. All voltages are referenced to VSS	Mandatory
4	VDD18	Supply voltage for sensor (1.8V)	Mandatory
5	VDD3	Supply voltage for IR emitter (3.0/3.3V)	Connect to VDD18
6	INT	Interrupt. Open drain output (active low)	Connect to GND
7	XRES	Hardware reset or PWM input. Need to enable in the register.	Connect to GND
8	VSYNC	VSYNC input	Connect to GND

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD18	Supply Voltage to GND	-0.3	1.98	V	
VDD3	IR Emitter Voltage to GND	-0.3	3.6	V	
V_{IO}	Digital I/O Terminal Voltage	-0.3	3.6	V	INT, XRES, VSYNC, SDA, SCL
I_{IO}	Digital Output Terminal Current	-1	20	mA	
Electrostatic Discharge					
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JEDEC JESD78E Class II
ESD_{HBM}	HBM Electrostatic Discharge	± 2000		V	ANSI/ESDA/JEDEC JS-001-2017
ESD_{CDM}	CDM Electrostatic Discharge	± 500		V	ANSI/ESDA/JEDEC JS-002-2018
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”
RH_{NC}	Relative Humidity (non-condensing)		85	%	
MSL	Moisture Sensitivity Level	3			Represents a max. floor life time of 168h

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD18	Supply Voltage to Sensor	1.7	1.8	1.98	V
VDD3	Supply Voltage to IR Emitter	2.9	3.3	3.6	V
T_A	Operating Ambient Temperature (1)	-30		85	°C

Note(s):

1. While the device is operational across the temperature range, performance will vary with temperature. Operational characteristics are at 25°C, unless otherwise noted.

Figure 7:
Operating Characteristics, VDD18 = 1.8V, VDD3 = 3.0V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator frequency		7.9	8.1	8.3	MHz
I_{DD}	Supply Current (1)	Active Proximity State (PON=PEN=1, AEN=0) (2)		584	684	µA
		Active ALS State (PON=AEN=1, PEN=0) (2)		275	355	
		Idle State (PON=1, AEN=PEN=0) (3)		76	100	
		Sleep State (PON = 0) (4)		0.7	5	
V_{OL}	INT, SDA output low voltage	6mA sink current			0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT		-5		5	µA
V_{IH}	SCL, SDA, VSYNC, XRES input high voltage		1.26			V
V_{IL}	SCL, SDA, VSYNC, XRES input low voltage				0.54	V
T_{Active}	Time from power-on to ready to receive I^2C commands			1.6		ms

Note(s):

1. Values are shown at the VDD18 pin and do not include current through the IR VCSEL emitter.
2. Active state occurs when PON =1 and the device is actively integrating either proximity or ALS.
3. Idle state occurs when PON =1 and all functions are not enabled.
4. Sleep state occurs when PON = 0 and I^2C bus is idle. If sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Optical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (statistical Quality Control) methods. Device parameters are guaranteed with V_{DD18}=1.8V, V_{DD3}=3.0V and T_A=25°C unless otherwise noted.

Figure 8:
ALS/Color Characteristics (AGAIN = 1024x, Integration Time = 13.9ms, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Dark ADC count value (1)	Ee =0µw/cm^2 ALS gain: 1024x Integration time: 50ms	0	0	3	counts
ALS gain ratios (2)	1x	1/142.23	1/129.4	1/116.36	
	2x	1/71.12	1/64.43	1/58.18	
	4x	1/35.56	1/32.26	1/29.09	
	8x	1/17.78	1/15.55	1/14.54	
	16x	1/8.89	1/8.07	1/7.27	
	32x	1/4.45	1/4.03	1/3.63	
	64x	1/2.23	1/2.02	1/1.90	
	256x	1.80	1.92	2.10	
	512x	3.50	3.82	4.20	
	1024x	6.00	7.57	10.00	
	2048x	9.60	14.61	22.40	
	4096x	12.80	26.78	51.20	
Clear channel irradiance responsivity (3)	White LED, 2700K (4) ALS gain: 1024x Integration time: 13.9ms	1523	1792	2061	counts/ (µW/cm^2)
Red channel irradiance responsivity			1209		
Green channel irradiance responsivity			515		
Blue channel irradiance responsivity			300		
Lux accuracy (5)	Integration time: 100ms	90	100	110	%
ADC noise (6)	White LED, 2700K ALS gain: 4096x Integration time: 100ms		0.01		%

Parameter	Conditions	Min	Typ	Max	Unit
Red/Clear channel ratios	White LED, 2700K	49	67	86	%
	Blue LED, λ_D = 465nm (7)	0	7	20	
	Red LED, λ_D= 615nm (8)	73	96	119	
Green/Clear channel ratios	White LED, 2700K	17	29	41	%
	Green LED, λ_D = 525nm (9)	56	76	96	
	Red LED, λ_D = 615nm	1	11	21	
Blue/Clear channel ratios	White LED, 2700K	3	17	31	%
	Blue LED, λ_D = 465nm	67	87	107	
	Red LED, λ_D = 615nm	0	5.5	16	

Note(s):

1. Dark ADC count refers to the full ALS count with ENAB_RES_BITS =0.
2. The gain ratios are calculated relative to the response with integration time = 13.9ms and ALS gain = 128x.
3. Representative result by lab characterization.
4. The White LED is an InGaN light-emitting diode with integrated phosphor and the following characteristic: correlated color temperature = 2700K.
5. Lux accuracy is an illuminance estimated using the red, green, blue, and clear channels and is not production tested.
6. ADC noise is representative result by lab characterization and calculated as the standard deviation of 1000 readings relative to full scale.
7. The Blue LED is an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 22nm.
8. The Red LED is an AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 615nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 15nm.
9. The Green LED is an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 35nm.

Figure 9:
Proximity Optical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Response: Absolute (1)	PTIME =528µs PGAIN =2x; PGAIN2 =2.5x PLDRIVE0 =10mA PPULSE =1pulse PPULSE_LEN =45µs PROX_DATA_AVG =8 BINSRCH_TARGET =15 APC =disabled ORE =disabled Electrical Calibration No glass above module Target Material: 18% reflective surface Target Size: 100mm x100mm Target Distance: 30mm		480		counts
Part to Part Variation (2)	Same as Response: Absolute except the followings: PGAIN2=5x Target Material: broadband diffusor Target Size: 2 inch diameter Target Distance: 85.75mm			±25	%
Response: No Target (3)	Same as Response: Absolute except the followings: PGAIN2=5x No Target		14		counts
Noise /Signal (4)	Same as Response: Absolute except the followings: PGAIN2=5x Target Material: broadband diffusor Target Size: 2 inch diameter Target Distance: 85.75mm		0.11	2	%

Note(s):

1. Representative result by lab characterization with VDD3 = 3.3V.
2. Optically trimmed at factory final test.
3. Response with no target varies with power supply characteristics and system noise.
4. Production tested results is the standard deviation of 10 readings divided by the average response.

Typical Operating Characteristics

Figure 10:
Angular Response to 2700K White LED

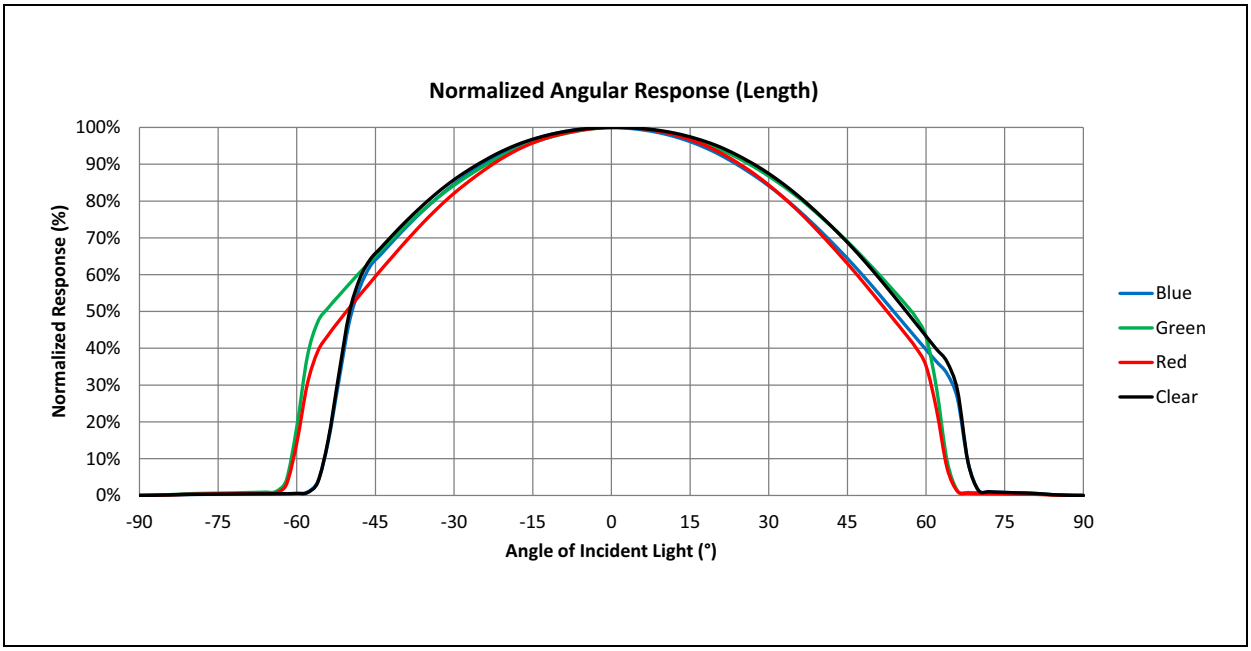


Figure 11:
Spectral Responsivity

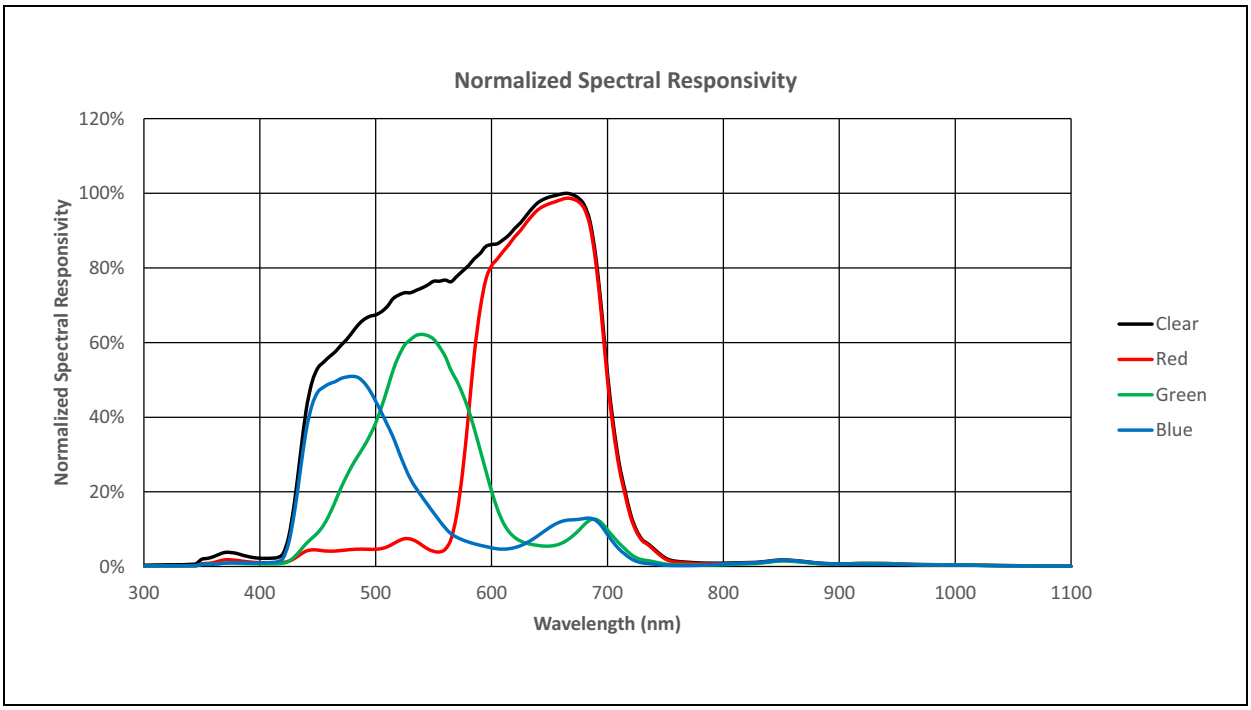
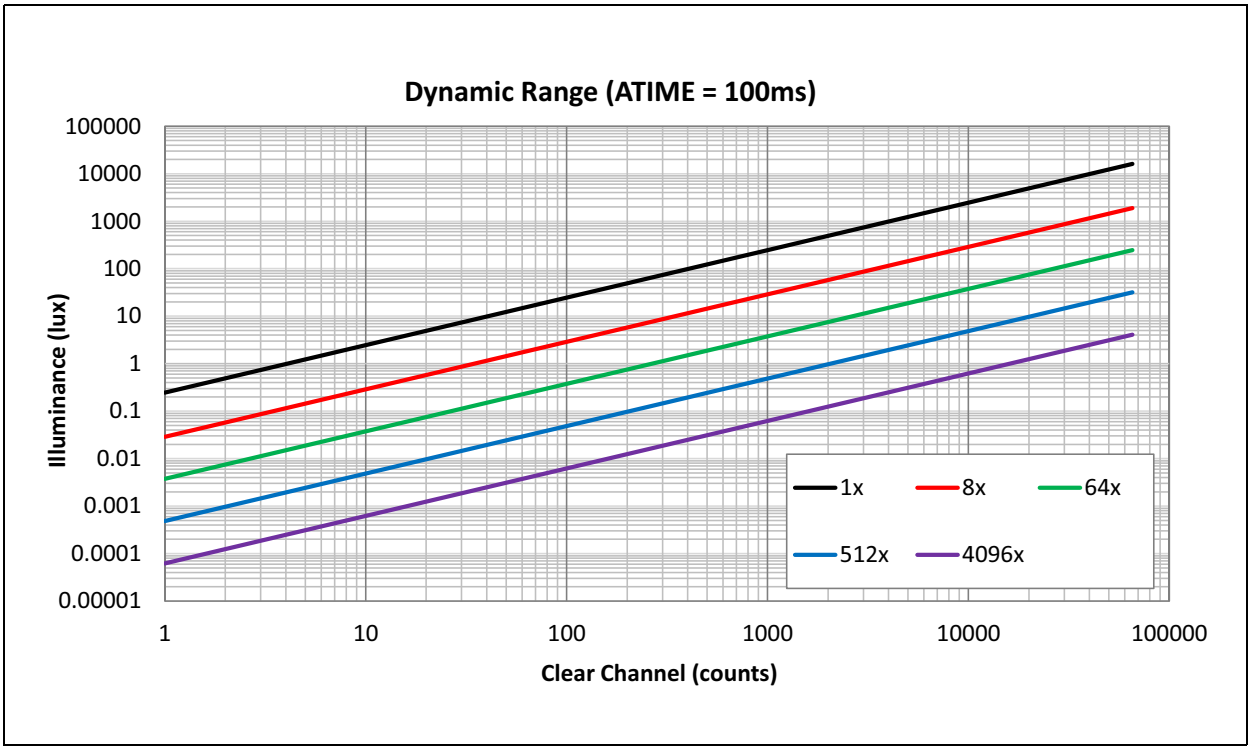


Figure 12:
Illuminance (Lux) vs Counts (Clear Channel)



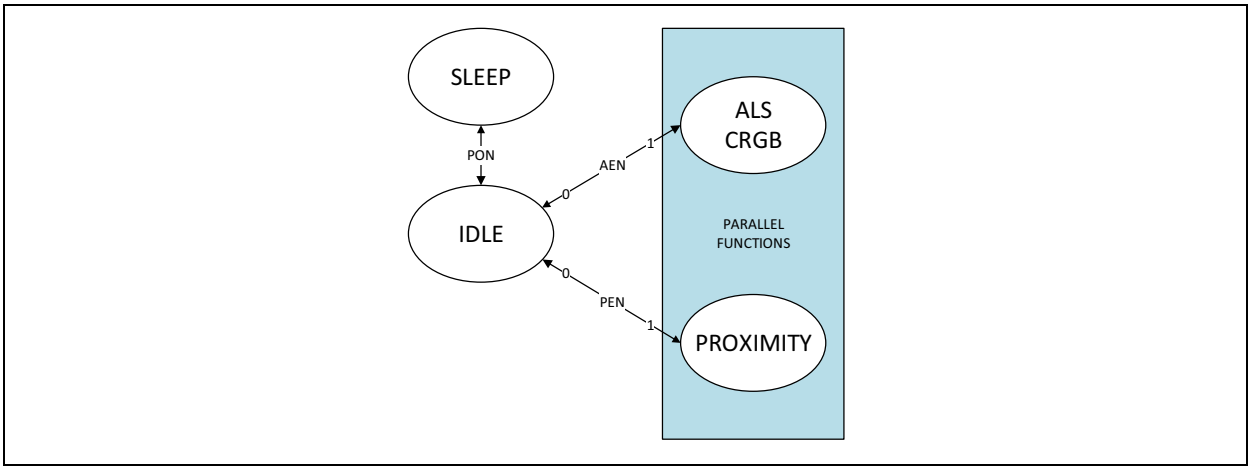
Detailed Description

Power Up

Upon power-up, device initialization occurs. During initialization, the device cannot accept I²C transactions and will deterministically send NAK for any I²C requests. All communication with the device must be delayed, and all outputs from the device (i.e. interrupts) must be ignored until initialization completes. After initialization, the device enters the SLEEP state in which the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I²C transaction occurs during the SLEEP state, the I²C core wakes up temporarily to service the communication. When the Power ON bit, PON, is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. After PON is set, there is a 100µs wait time required before enabling PEN, AEN. This allows the device time to settle the internal node voltages and currents before starting the Proximity and ALS measurements. When a function is enabled (PEN=1 and/or AEN =1), the device exits the IDLE state. When both functions are disabled (PEN=0 & AEN=0), the device returns to the IDLE state.

As depicted in Figure 13, the proximity and CRGB color sensing functions can operate in parallel when both are enabled (PEN = AEN = 1). Each function is individually configured (e.g. gain, ADC integration time, wait time, persistence, thresholds, etc.). When a proximity calibration is requested, it will take precedence over the proximity measurement function. If Sleep After Interrupt is enabled (SAI = 1 in register 0xAB, available only in sequential mode), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP will not change any of the register settings (e.g. PON will still be high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the interrupt status register is cleared (the status bit is in register 0xA0-0xA2).

Figure 13:
Simplified State Diagram



Proximity

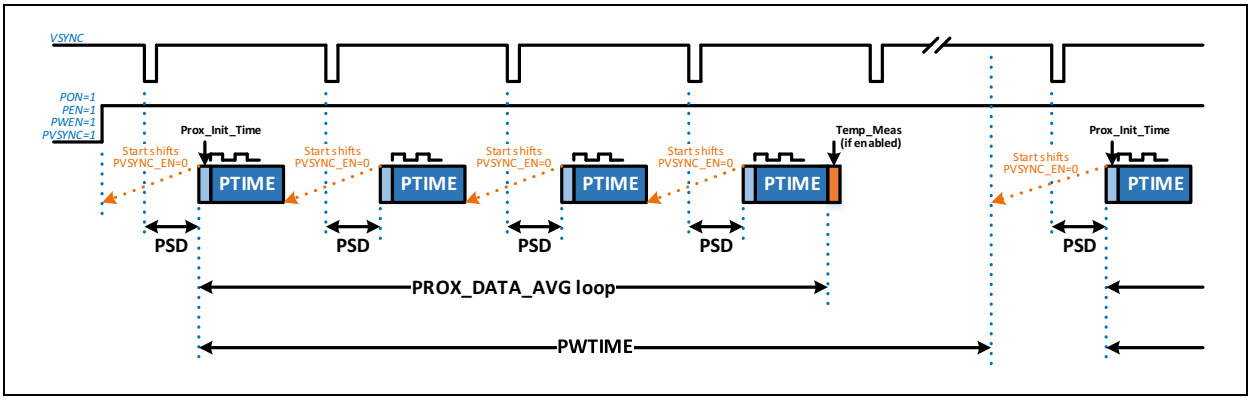
The proximity system consists of an IR VCSEL and its driver generating periodic IR pulses which are reflected and received by the proximity photodiode and modulator sub-system. The reflected energy is measured by integrating the photodiode current and translating it to an ADC input voltage. The presence of a reflective object at some distance can be extracted as a function of ADC output data which represents the reflected signal intensity.

Proximity results are affected by three fundamental factors: the integrated IR VCSEL emission, IR reception (signal + crosstalk), and environmental factors, including target distance and surface reflectivity. The IR reception signal path begins with IR detection from a photodiode and ends with the 14-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or crosstalk compensation is accomplished by adjustment to the POFFSET register. The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation, therefore a positive offset value has the effect of decreasing the PDATA value. The integrated offset calibration feature performs this crosstalk compensation.

The proximity IR VCSEL emission is designed to be able to synchronize to the display VSYNC signal with a delay time defined by PSD when PVSYNC_EN=1. PTIME defines the duration of one proximity sample. PTIME needs to be programmed to a value greater than the sample integration time, otherwise it will be ignored. Using PTIME, proximity sample timing can be programmed to skip VSYNC periods. The device hardware allows to collect and average multiple proximity samples for a single proximity measurement result by programming the PROX_DATA_AVG register. Device temperature is measured and updated in the TDATA register after every proximity measurement cycle when TEN=1 and ENAB_TEMP_SENSOR =1. PWTIME provides the ability to add wait time and defines the repetition period of one proximity measurement cycle. The subsequent proximity cycle will occur on the first VSYNC after the end of the PWTIME period, plus the delay defined by PSD.

Figure 14 shows an example of proximity integration and data sampling for the TMD3721.

Figure 14:
Proximity Integration and Data Sampling in TMD3721



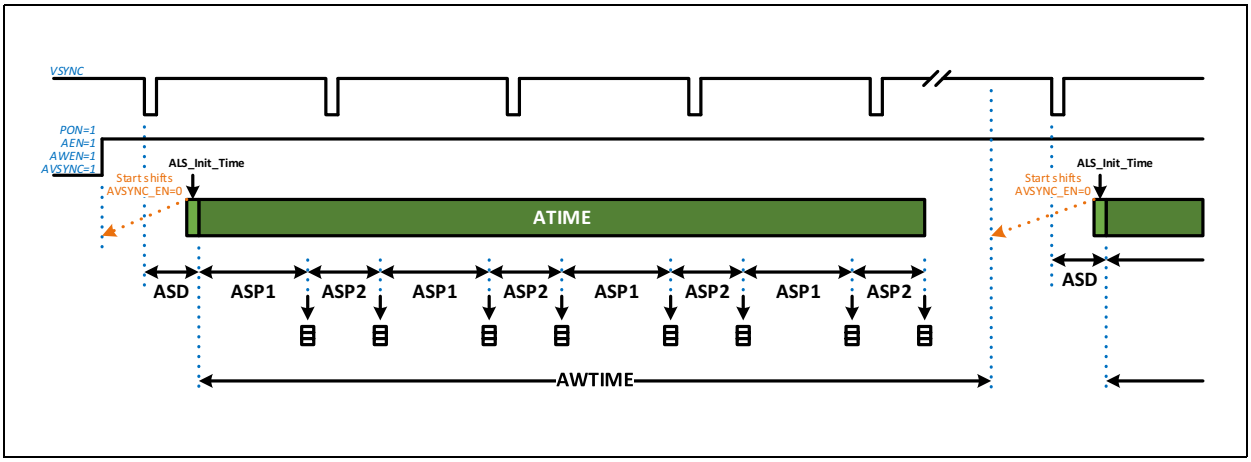
Color and Ambient Light Sensing

The color and ALS reception signal path begins as the photodiodes receive filtered light and ends with 16-bit results. In addition to the RGB absorption filters applied to RGB channels, there is also a UV-IR blocking filter applied to all ALS channels including Clear channel for accurately measuring ambient light levels. Signals from all photodiodes are simultaneously accumulated for a period of time set by the value in ATIME (or ASP1, ASP2 if enabled) before the results are available. Gain is adjustable in the range of 1x to 4096x to facilitate operation over a wide range of lighting conditions, including under dark glass or OLED displays with low optical transmissivity. Based on the optical glass or OLED display used over of the device, custom equations based on the ALS data are empirically derived to calculate the amount of ambient light and the correlated color temperature.

The ALS integration is designed to be able to synchronize to the display VSYNC signal with a delay time defined by ASD (when AVSYNC_EN=1). ASD must be programmed greater than the ALS initialization time, otherwise ASD is ignored. ALS initialization time requires 24 ALS clocks, resulting in 32.568µs (typical). If ASP1, ASP2 are enabled, the device allows for quick sampling over the integration time (ATIME) in intervals of ASP1, ASP2 and stores the ALS data in the FIFO. With ASP1 and ASP2 disabled, the ALS data will be collected once at the end of the full ALS integration time. AWTIME allows the addition of a wait time and defines the ALS repetition period. The subsequent ALS cycle will occur on the first VSYNC after the end of the AWTIME period, plus the delay defined by ASD.

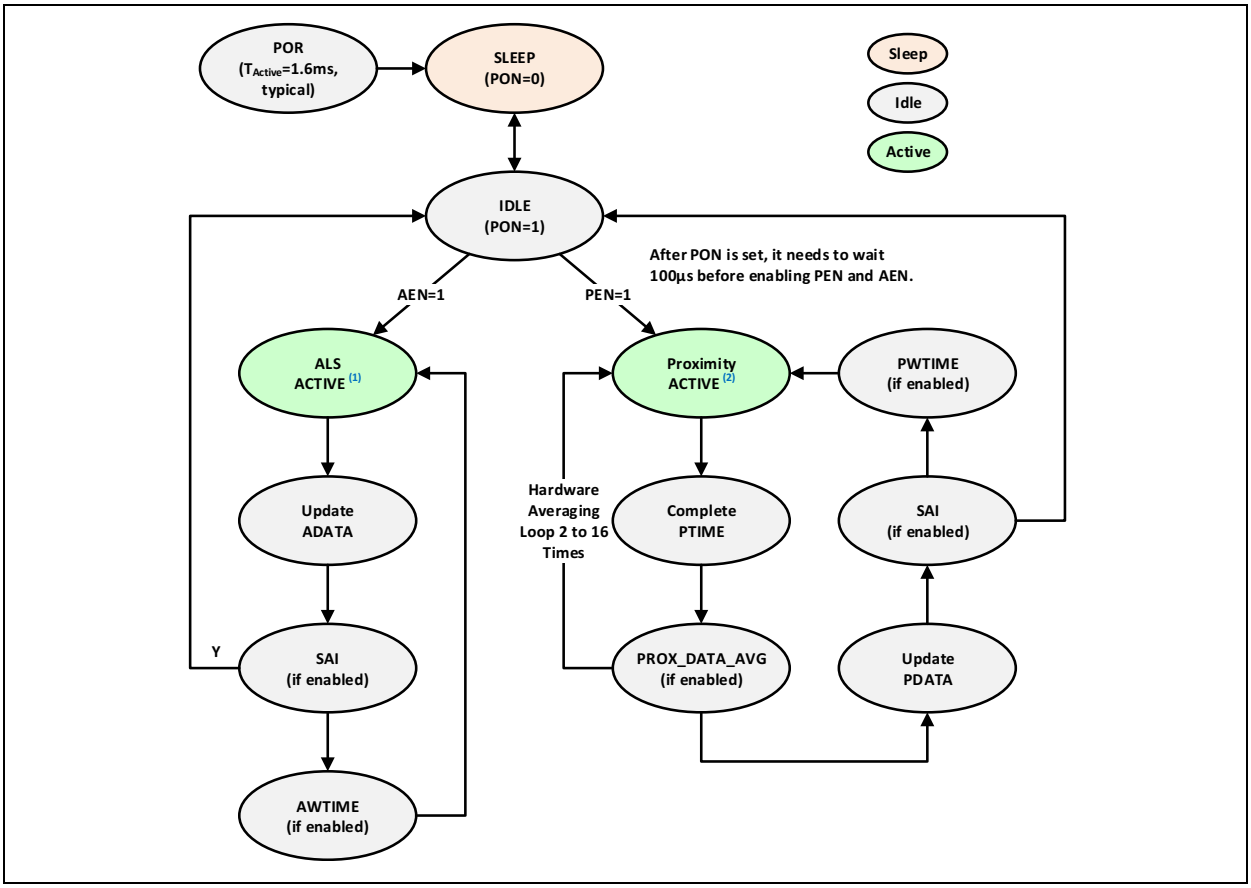
Figure 15 shows an example of ALS integration and data sampling for the TMD3721.

Figure 15:
ALS Integration and Data Sampling in TMD3721



Operational State Diagram

Figure 16:
Operational State Diagram



Note(s):

1. ALS active time =32.568µs + ALS integration time (ATIME).
2. Proximity active time = PPULSE x(2 x(PPULSE_LEN +42.15µs)) +78.75µs
3. All numbers in the above equations are typical values

When ALS and proximity measurements are both enabled, there are three operating modes available in the device: sequential mode, full parallel mode and concurrent mode.

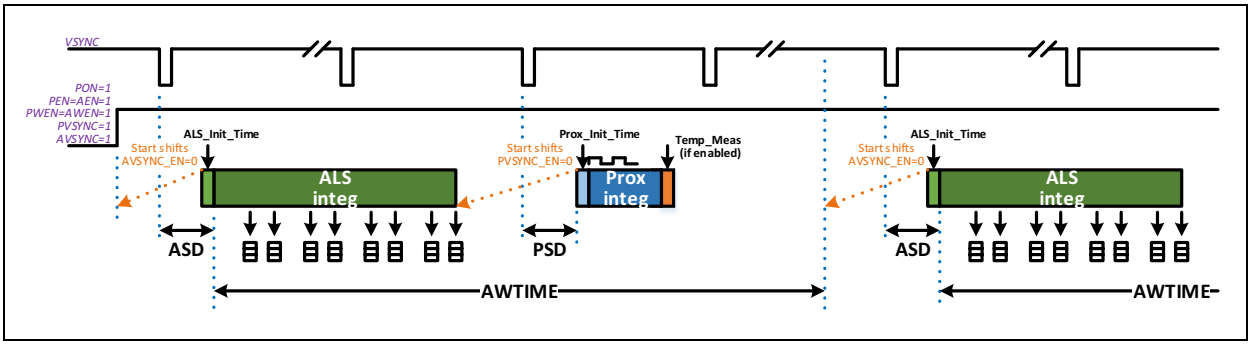
In the "sequential" operating mode, ALS and proximity measurements run sequentially. When the device is operating non-synchronously, the ALS measurement starts after ALS enabled, and the proximity measurement starts after the completion of ALS measurement. When the device is operating synchronously (i.e. the ALS and proximity measurements are triggered by an external VSYNC signal) the ALS and proximity start timing is determined by the following:

- For ALS, AVSYNC_EN=1 enables synchronous mode and ASD defines the delay from VSYNC until the ALS measurement begins.
- For proximity, PVSYNC_EN=1 enables synchronous mode and PSD defines the delay from the first VSYNC after the completion of ALS measurement until the proximity measurement begins.

AWTIME defines the ALS and proximity repetition period. In non-synchronous mode, the subsequent measurement cycle will begin at the end of the AWTIME period. In synchronous mode, the subsequent measurement cycle will occur on the first VSYNC after the end of the AWTIME period, plus the delay defined by ASD. PWTIME in the sequential mode is ignored.

Figure 17 shows the ALS and proximity timing during sequential mode.

Figure 17:
ALS and Proximity Measurement in Sequential Mode



In the "full parallel" operating mode, ALS and proximity measurements run completely independent of each other. When the device is operating non-synchronously, the ALS and proximity measurements start after AEN=PEN=PON=1. When the device is operating synchronously (i.e. the ALS and proximity measurements are triggered by an external VSYNC signal) the ALS and proximity start timing is determined by the following:

- For ALS, AVSYNC_EN=1 enables synchronous mode and ASD defines the delay from VSYNC until the ALS measurement begins.

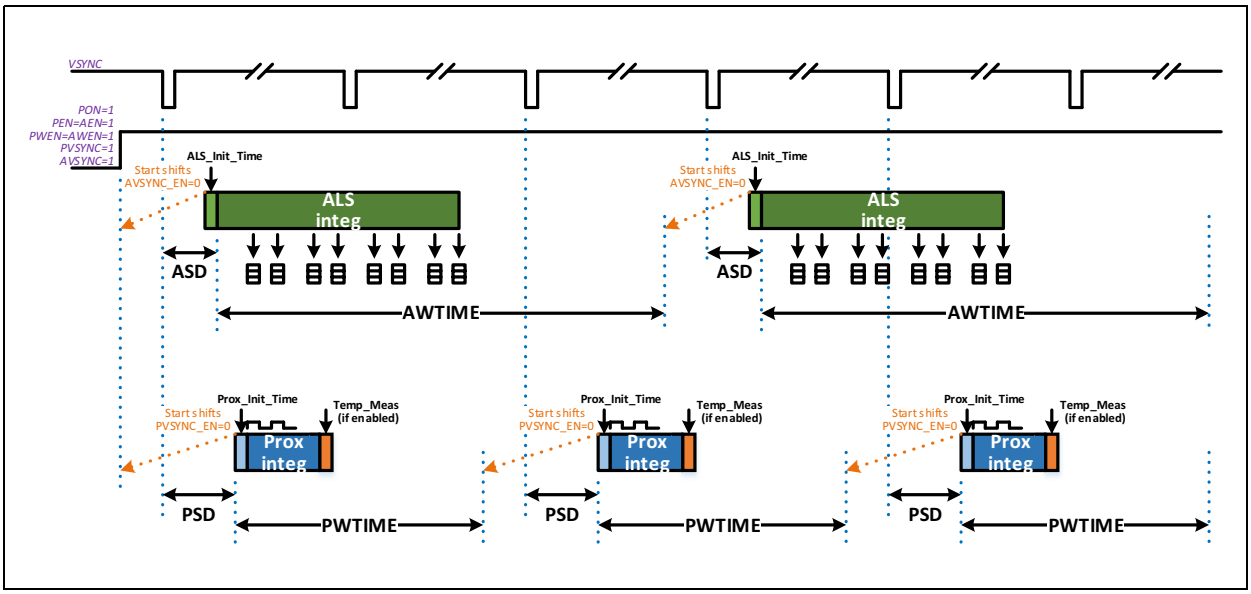
- For proximity, PVSYNC_EN=1 enables synchronous mode and PSD defines the delay from VSYNC until the proximity measurement begins.

AWTIME defines the ALS repetition period. In non-synchronous mode, the subsequent ALS cycle will begin at the end of the AWTIME period. In synchronous mode, the subsequent ALS cycle will occur on the first VSYNC after the end of the AWTIME period, plus the delay defined by ASD.

PWTIME defines the proximity repetition period. In non-synchronous mode, the subsequent proximity cycle will begin at the end of the PWTIME period. In synchronous mode, the subsequent proximity cycle will occur on the first VSYNC after the end of the PWTIME period, plus the delay defined by PSD.

Figure 18 shows the ALS and proximity timing during full parallel mode.

Figure 18:
ALS and Proximity Measurement in Full Parallel Mode



In the "concurrent" operating mode, ALS and proximity measurements run at the same time, with the ALS measurement "paused" while the proximity measurement is running. When the device is operating non-synchronously, the ALS and proximity measurements start after AEN=PEN=PON=1. When the device is operating synchronously (i.e. the ALS and proximity measurements are triggered by an external VSYNC signal) the ALS and proximity start timing is determined by the following:

- For ALS, AVSYNC_EN=1 enables synchronous mode and ASD defines the delay from VSYNC until the ALS measurement begins.
- For proximity, PVSYNC_EN=1 enables synchronous mode and PSD defines the delay from VSYNC until the proximity measurement begins.

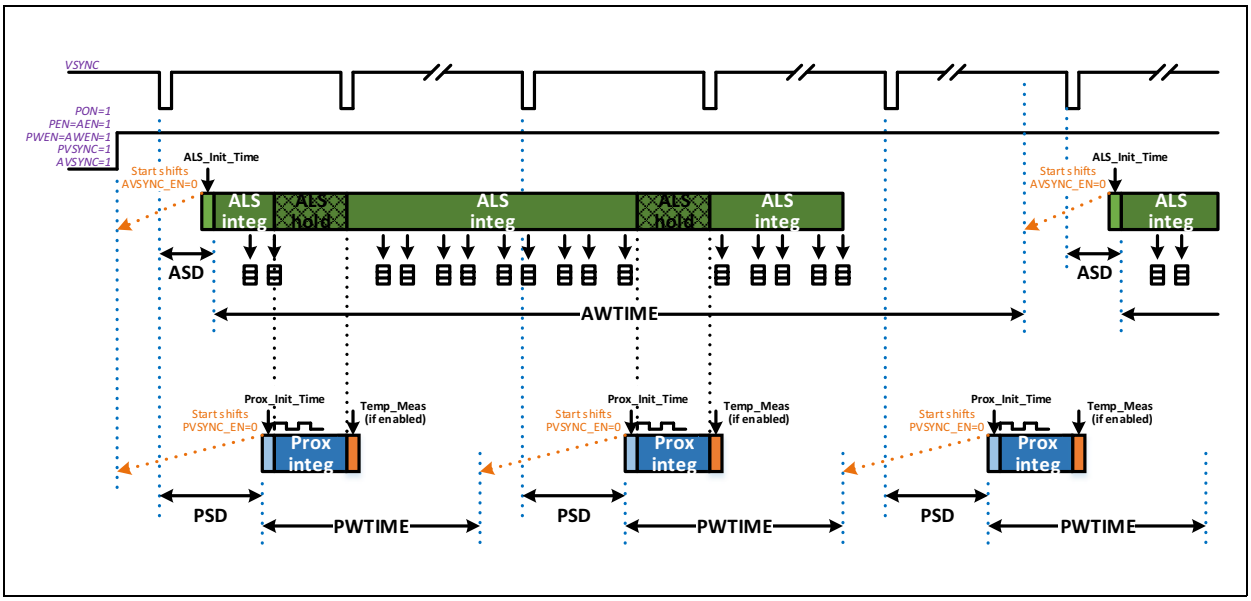
AWTIME defines the ALS repetition period. In non-synchronous mode, the subsequent ALS cycle will begin at the end of the AWTIME period. In synchronous mode, the subsequent ALS cycle will occur on the first VSYNC after the end of the AWTIME period, plus the delay defined by ASD.

PWTIME defines the proximity repetition period. In non-synchronous mode, the subsequent proximity cycle will begin at the end of the PWTIME period. In synchronous mode, the subsequent proximity cycle will occur on the first VSYNC after the end of the PWTIME period, plus the delay defined by PSD.

Figure 19 shows the ALS and proximity timing during concurrent mode.

In concurrent mode, it is important to configure ALS hold (CFG2 (0xA7), bit 3) correctly in order to avoid a situation where ALS is constantly interrupted and cannot complete in a timely manner. It is recommended to pause ALS only during the time the emitter is pulsing (CFG2, bit 3=1). This may result in a slight increase in ALS data noise, but the trade-off is a shorter pause time.

Figure 19:
ALS and Proximity Measurement in Concurrent Mode



I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes. Read and write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/ NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without “re”-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9th clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:

https://www.i2c-bus.org/references/

I²C Timing Characteristics

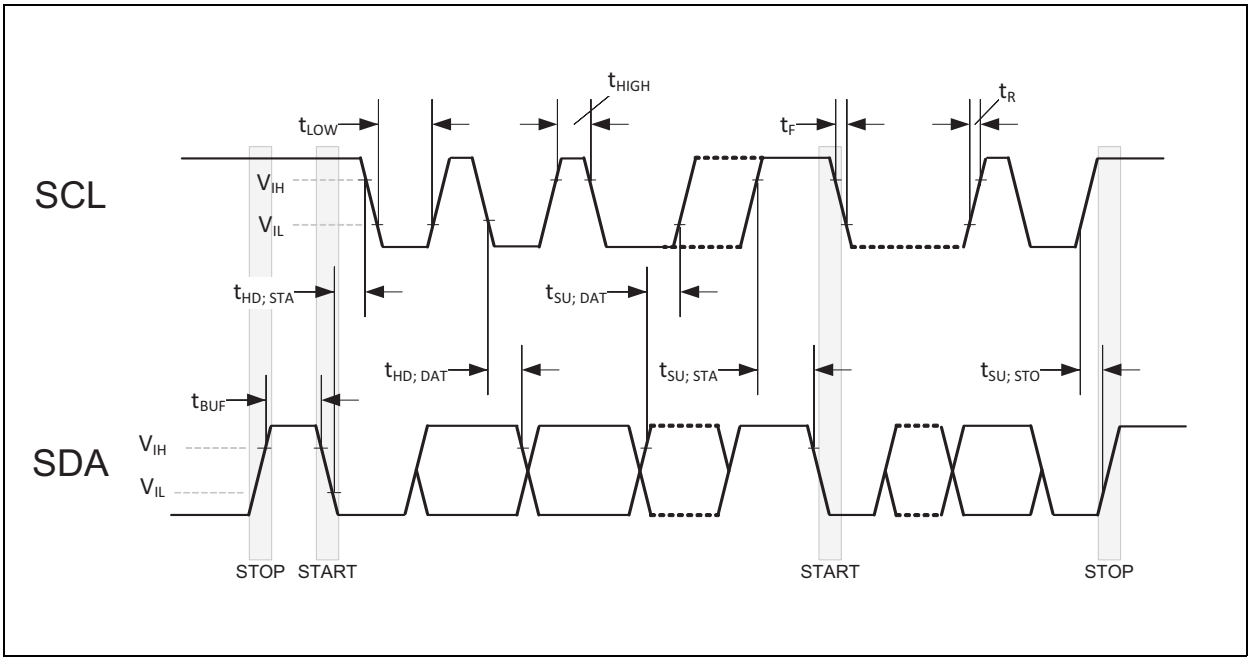
The timing parameters are specified by design and characterization and are not production tested unless otherwise noted. All parameters are measured with V_{DD}=1.8V and T_A= 25°C unless otherwise noted.

Figure 20:
I²C Timing Characteristics

Symbol	Parameter	Min	Type	Max	Unit
f_{SCL}	I²C clock frequency	0		400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3			µs
$t_{HD;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated	0.6			
$t_{SU;STA}$	Repeated start condition setup time	0.6			
$t_{SU;STO}$	Stop condition setup time	0.6			
t_{LOW}	SCL clock low period	1.3			
t_{HIGH}	SCL clock high period	0.6			
$t_{HD;DAT}$	Data hold time	0			ns
$t_{SU;DAT}$	Data setup time	100			
t_F	Clock/data fall time			300	
t_R	Clock/data rise time			300	

I²C Timing Diagram

Figure 21:
I²C Timing Diagram



Register Overview

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide device control functions and are read to determine device status and acquire device data.

Register Map

The register set is summarized in Register Map. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. The power-on reset values of each bit are indicated in these columns. Two-byte fields are always latched with the low byte followed by the high byte.

Figure 22:
Register Map

Address	Register Name	Type	Description	Reset
0x07	LOTL	R	Lot ID low byte	0x00
0x08	LOTH	R	Lot ID high byte	0x00
0x09	SNL	R	Serial number low byte	0x00
0x0A	SNH	R	Serial number high byte	0x00
0x1A	IPTAT	RW	IPTAT code	0x07
0x80	ENABLE	RW	Enables device states	0x00
0x82	PTIME	RW	Proximity time	0x1F
0x84	AILTL	RW	ALS interrupt low threshold low byte	0x00
0x85	AILTH	RW	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	RW	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	RW	ALS interrupt high threshold high byte	0x00
0x88	PILTL	RW	Proximity interrupt low threshold low byte	0x00
0x89	PILTH	RW	Proximity interrupt low threshold high byte	0x00
0x8A	PIHTL	RW	Proximity interrupt high threshold low byte	0x00
0x8B	PIHTH	RW	Proximity interrupt high threshold high byte	0x00
0x8C	PERS	RW	ALS and proximity interrupt persistence filters	0x00
0x8D	CFG0	RW	Configuration zero	0x10
0x8E	PCFG0	RW	Proximity configuration zero	0x43
0x8F	PCFG1	RW	Proximity configuration one	0x00
0x90	PCFG2	RW	Proximity configuration two	0x20
0x91	REVID	R	Revision ID	0x01

Address	Register Name	Type	Description	Reset
0x92	ID	R	Device ID	0x82
0x93	REVID2	R	Auxiliary ID	0x02
0x94	CFG1	RW	Configuration one	0x00
0x95	AGAIN_1_0	RW	ALS gain control of channel 1 and 0	0xCC
0x96	AGAIN_3_2	RW	ALS gain control of channel 3 and 2	0xCC
0x9A	LDR0_CFG	RW	Proximity LDR0 drive strength configuration	0x52
0x9E	EYE_SAFETY_CFG	RW	Eye safety configuration	0x40
0x9F	EYE_SAFETY_ STATUS	R	Eye safety status	0x00
0xA0	STATUS	R,SC	Device status	0x00
0xA1	STATUS_2	R,SC	Device status two	0xC0
0xA2	STATUS_3	R,SC	Device status three	0x00
0xA5	PID_L	RW	Programmable ID low byte	0x00
0xA6	PID_H	RW	Programmable ID high byte	0x00
0xA7	CFG2	RW	Configuration two	0x43
0xA8	RESET	RW	RESET	0x00
0xAB	CFG3	RW	Configuration three	0x41
0xAE	CFG6	RW	Configuration six	0x76
0xB0	PWM_CFG	RW	PWM configuration	0x00
0xB1	VSYNC_CFG	RW	VSYNC configuration	0x00
0xB2	VSYNC_PRD_L	RW	VSYNC period low data	0x00
0xB3	VSYNC_PRD_H	RW	VSYNC period high data	0x00
0xB5	PWM_PRD_L	R	PWM period low data	0x00
0xB6	PWM_PRD_H	R	PWM period high data	0x00
0xB7	PWM_HIP_L	R	Low byte of PWM signal high period	0x00
0xB8	PWM_HIP_H	R	High byte of PWM signal high period	0x00
0xC0	POFFSET	RW	POFFSET data	0x00
0xC1	POFFSET_SIGN	RW	POFFSET sign	0x00
0xD6	AZ_CONFIG	RW	Auto-zero configuration	0x7F
0xD7	CALIB	RW	Proximity offset calibration	0x00
0xD8	CALIB_OFFSET	RW	Proximity offset extension	0x00

Address	Register Name	Type	Description	Reset
0xD9	CALIBCFG	RW	Proximity offset calibration control	0x50
0xDA	PCFG4	RW	Proximity configuration four	0x00
0xDC	CALIBSTAT	R	Proximity offset calibration status	0x00
0xDD	INTENAB	RW	Interrupt enables	0x00
0xDE	INTENAB_2	RW	Interrupt enables two	0x00
0xE0	ASD_L	RW	ALS start delay low data	0x00
0xE1	ASD_H	RW	ALS start delay high data	0x00
0xE2	ASP1_L	RW	ASP1 time low data	0x00
0xE3	ASP1_H	RW	ASP1 time high data	0x00
0xE4	ASP2_L	RW	ASP2 time low data	0x00
0xE5	ASP2_H	RW	ASP2 time high data	0x00
0xE6	ATIME	RW	ALS integration time	0x00
0xE7	AWTIME	RW	ALS wait time	0x00
0xE8	ACFG	RW	ALS configuration	0x00
0xEA	PSD_L	RW	Proximity start delay low data	0x00
0xEB	PSD_H	RW	Proximity start delay high data	0x00
0xEC	PWTIME	RW	Proximity wait time	0x00
0xF0	FIFO_STATUS_1	R	FIFO status	0x00
0xF1	FIFO_CONTROL	RW	FIFO control	0x02
0xF4	PDATA_L	R	Proximity low data	0x00
0xF5	PDATA_H	R	Proximity high data	0x00
0xF6	TDATA_L	R	Temperature low data	0x00
0xF7	TDATA_H	R	Temperature high data	0x00
0xF8	FIFO_ADATA_7	R	FIFO ALS data read out register 7	0x00
0xF9	FIFO_ADATA_6	R	FIFO ALS data read out register 6	0x00
0xFA	FIFO_ADATA_5	R	FIFO ALS data read out register 5	0x00
0xFB	FIFO_ADATA_4	R	FIFO ALS data read out register 4	0x00
0xFC	FIFO_ADATA_3	R	FIFO ALS data read out register 3	0x00
0xFD	FIFO_ADATA_2	R	FIFO ALS data read out register 2	0x00
0xFE	FIFO_ADATA_1	R	FIFO ALS data read out register 1	0x00

Address	Register Name	Type	Description	Reset
0xFF	FIFO_ADATA_0	R	FIFO ALS data read out register 0	0x00

Note(s):

1. R = Read Only; WO = Write Only; RW = Read or Write; SC = Self Clearing after access.

Detailed Register Description

LOTL Register (Address 0x07)

Figure 23:
LOTL Register

Addr: 0x07		LOTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	LOTL	0x00	R	The low byte of the 16-bit lot ID.

LOTH Register (Address 0x08)

Figure 24:
LOTH Register

Addr: 0x08		LOTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	LOTH	0x00	R	The high byte of the 16-bit lot ID.

SNL Register (Address 0x09)

Figure 25:
SNL Register

Addr: 0x09		SNL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SNL	0x00	R	The low byte of the 16-bit serial number.

SNH Register (Address 0x0A)

Figure 26:
SNH Register

Addr: 0x0A		SNH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SNH	0x00	R	The high byte of the 16-bit serial number.

IPTAT Register (Address 0x1A)

Figure 27:
IPTAT Register

Addr: 0x1A		IPTAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	000	RW	Reserved. Must be set to default value.
4:0	IPTAT	00111	RW	The IPTAT value needs to be changed from its default value to be “00011b” during device initialization.

Enable Register (Address 0x80)

Figure 28:
ENABLE Register

Addr: 0x80		ENABLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PVSYNC_EN	0	RW	This bit enables proximity integration synced with VSYNC
6	AVSYNC_EN	0	RW	This bit enables ALS integration synced with VSYNC
5	TEN	0	RW	This bit activates temperature measurement after every proximity measurement.
4	PWEN	0	RW	This bit activates the proximity wait feature which is set by the PWTIME register. Active high.
3	AWEN	0	RW	This bit activates the ALS wait feature which is set by the AWTIME register. Active high.
2	PEN	0	RW	This bit activates the proximity detection. Active high.
1	AEN	0	RW	This bit actives the ALS function. Active high.
0	PON	0	RW	Power ON. This field activates the internal oscillator and ADC channels. Active high.

Preset each applicable registers and its bits as per required operation before activating PON. After PON is set, it is required to wait 100µs settling time and then enable AEN and /or PEN. In order to modify register configurations during operation, it is required to set AEN=PEN=PON=0 firstly to avoid any unexpected behavior or corrupted ALS and proximity results. Disabling PON resets the device state machine, but all the register values will retain. After the configuration change done, set the PON bit and wait 100µs settling time, and then enable AEN and /or PEN to re-activate the corresponding functionalities.

PTIME Register (Address 0x82)

Figure 29:
PTIME Register

Addr: 0x82		PTIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PTIME	0x1F	RW	This register defines the duration of 1 Prox Sample, which is (PTIME + 1)*88µs. PTIME needs to be programmed greater than proximity integration time, otherwise it's ignored.

AILTL Register (Address 0x84)

Figure 30:
AILTL Register

Addr: 0x84		AILTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTL	0x00	RW	This register sets the low byte of the LOW ALS threshold.

AILTH Register (Address 0x85)

Figure 31:
AILTH Register

Addr: 0x85		AILTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTH	0x00	RW	This register sets the high byte of the LOW ALS threshold.

The ALS clear channel is compared against low-going 16-bit threshold value set by AILTL and AILTH. The contents of the AILTH and AILTL registers are combined and treated as a sixteen-bit threshold value. If the value generated by the ALS clear channel is below the AILTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.

When setting the 16-bit ALS threshold AILTL must be written first, immediately followed by AILTH. Internally, the lower 8 bits are buffered until the upper 8 bits are written. As the upper 8 bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

When residue bits are enabled by ENAB_RES_BITS, the data format for AILT should be U13.3 and when residue bits are not required, it should be U16.0.

When DOUBLE_DATA_MODE is used, the data AILTH register should be 0, only the data AILTL register is used. The data format when residue bits are enabled is U7.1. When residue bits are disabled, the data format should be U8.0.

AIHTL Register (Address 0x86)

Figure 32:
AIHTL Register

Addr: 0x86		AIHTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTL	0x00	RW	This register sets the low byte of the HIGH ALS threshold.

AIHTH Register (Address 0x87)

Figure 33:
AIHTH Register

Addr: 0x87		AIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTH	0x00	RW	This register sets the high byte of the HIGH ALS threshold.

The ALS clear channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH. The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen-bit threshold value. If the value generated by the ALS clear channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.

When setting the 16-bit ALS threshold AIHTL must be written first, immediately followed by AIHTH. Internally, the lower 8 bits are buffered until the upper 8 bits are written. As the upper 8 bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

When residue bits are enabled by ENAB_RES_BITS, the data format for AIHT should be U13.3 and when residue bits are not required, it should be U16.0

When DOUBLE_DATA_MODE is used, the data AIHTH register should be 0, only the data AIHTL register is used. The data format when residue bits are enabled is U7.1. When residue bits are disabled, the data format should be U8.0

PILTL Register (Address 0x88)

Figure 34:
PILTL Register

Addr: 0x88		PILTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PILTL	0x00	RW	This register contains the low byte of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register contains the LOW threshold which is an 8-bit value which is compared against the upper 8 bits of the 10-bit proximity value.

PILTH Register (Address 0x89)

Figure 35:
PILTH Register

Addr: 0x89		PILTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	PILTH	000000	RW	This register contains the upper 6 bits of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register is ignored.

The contents of the PILTH and PILTL registers are combined and treated as a fourteen (14) bit threshold low value. If the value generated by the proximity ADC (PDATA) is below the PILTL/H threshold and the PPERS value is reached, then the low proximity threshold is breached. When setting the 14-bit proximity threshold, PILTL must be written first, immediately follow by PILTH. Internally, the lower 8 bits are buffered until the upper 8 bits are written. As the upper 8 bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PILTL contains an 8-bit threshold which is compared against the upper 8 bits of the 10-bit value. PILTH is ignored.

PIHTL Register (Address 0x8A)

Figure 36:
PIHTL Register

Addr: 0x8A		PIHTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHTL	0x00	RW	This register contains the low byte of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register contains the HIGH threshold which is an 8-bit value which is compared against the upper 8 bits of the 10-bit proximity value.

PIHTH Register (Address 0x8B)

Figure 37:
PIHTH Register

Addr: 0x8B		PIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	PIHTH	000000	RW	This register contains the upper 6 bits of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register is ignored.

The contents of the PIHTH and PIHTL registers are combined and treated as a fourteen (14) bit threshold high value. If the value generated by the proximity ADC (PDATA) is above the PIHTL/H threshold and the PPERS value is reached, then the high proximity threshold is breached. When setting the 14-bit proximity threshold, PIHTL must be written first, immediately follow by PIHTH. Internally, the lower 8 bits are buffered until the upper 8 bits are written. As the upper 8 bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PIHTL contains an 8-bit threshold which is compared against the upper 8 bits of the 10-bit value. PIHTH is ignored.

PERS Register (Address 0x8C)

Figure 38:
PERS Register

Addr: 0x8C		PERS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	PPERS	0000	RW	This register sets the proximity persistence filter.	
				Value	**Interrupt**
				0	Every proximity cycle
				1	Any value outside proximity thresholds
				2	2 consecutive proximity values out of range
				3	3 consecutive proximity values out of range
				…	….
				15	15 consecutive proximity values out of range
3:0	APERS	0000	RW	This register sets the ALS persistence filter.	
				Value	**Interrupt**
				0	Any value outside ALS thresholds
				1	Any value outside ALS thresholds
				2	2 consecutive ALS values out of range
				3	3 consecutive ALS values out of range
				4	5 consecutive ALS values out of range
				5	10 consecutive ALS values out of range
				6	15 consecutive ALS values out of range
				7	20 consecutive ALS values out of range
				…	…
				13	50 consecutive ALS values out of range
				14	55 consecutive ALS values out of range
				15	60 consecutive ALS values out of range

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPERS value. If the counter is equal to the PPERS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared.

The frequency of consecutive ALS clear channel results outside of threshold limits are counted; this count value is compared against the APERS value. If the counter is equal to the APERS setting an interrupt is asserted. Any time an ALS clear channel result is inside the threshold values the counter is cleared.

CFG0 Register (Address 0x8D)

Figure 39:
CFG0 Register

Addr: 0x8D		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ENAB_16_BIT_OP	0	RW	Enables output of PDATA to be a 16-bit value when APC is on. See PDATA (0xF4 and 0xF5) for details.
6:4	Reserved	001	RW	Reserved. Must be set to default value.
3	PWLONG	0	RW	When PWLONG (PROX Wait Long) is asserted the wait period as set by PWTIME is increased by a factor of 12
2	AWLONG	0	RW	When AWLONG (ALS Wait Long) is asserted the wait period as set by AWTIME is increased by a factor of 12
1:0	Reserved	00	RW	Reserved. Must be set to default value.

PCFG0 Register (Address 0x8E)

Figure 40:
PCFG0 Register

Addr: 0x8E		PCFG0			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	PGAIN	010	RW	This field sets proximity first stage gain control.	
				Value	**Stage 1 Gain**
				0 (000)	1x
				1 (001)	2x
				2 (010)	4x
				3 (011)	8x
				4 (100)	16x
4:2	Reserved	000	RW	Reserved. Must be set to default value.	
1:0	PGAIN2	11	RW	This field sets proximity second stage gain control.	
				Value	**Stage 2 Gain**
				0 (00)	2.5x
				1 (01)	5x
				2 (10)	Reserved, must not use
				3 (11)	10x

PCFG1 Register (Address 0x8F)

Figure 41:
PCFG1 Register

Addr: 0x8F		PCFG1			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	PPULSE_LENH	00	RW	These bits are the 2 most significant bits of the 10-bit Pulse Length control setting. The lower 8 bits are in the PCFG2 register. See the PCFG2 register for details.	
5:0	PPULSE	000000	RW	Maximum number of pulses in a single proximity cycle.	
				Value	**Maximum Number of Pulses**
				0 (000000)	1
				1 (000001)	2
				2 (000010)	3
				...	...
				63 (111111)	64

The PPULSE field sets the maximum number of IR VCSEL pulses that may occur in a proximity cycle. The proximity engine will automatically continue to add IR VCSEL pulses, up to the value set in PPULSE or if a near-saturation condition occurs if Automatic Pulse Control (APC) is enabled. The dynamic range of the sensor is automatically adjusted to detect distant targets as well as prevent saturation from close targets. This operation also reduces power consumption because proximity integration period is automatically shortened when a target is close to the sensor.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then PPULSE always determines the number of proximity pulses to be transmitted.

PCFG2 Register (Address 0x90)

Figure 42:
PCFG2 Register

Addr: 0x90		PCFG2			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	PPULSE_LENL	0x20	RW	These bits are the 8 least significant bits of the 10-bit Pulse Length control setting. The upper 2 bits are in the PCFG1 register. See the PCFG1 register for details. Pulse Length needs to be greater than 16µs.	
				Value	**Pulse Length**
				14 (0000001110)	16µs
				15 (0000001111)	17µs
				Pulse Length = (PPULSE_LEN + 2)µs	
				1023 (1111111111)	1025µs

REVID Register (Address 0x91)

Figure 43:
REVID Register

Addr: 0x91		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	000	R	Reserved
4:3	FUNC_ID	00	R	Device function identification
2:0	REV_ID	001	R	Device revision number

ID Register (Address 0x92)

Figure 44:
ID Register

Addr: 0x92		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ID	0x82	R	Device identification

REVID2 Register (Address 0x93)

Figure 45:
REVID2 Register

Addr: 0x93		REVID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	R	Reserved. Must be set to default value.
3:0	AUX_ID	1010	R	Auxiliary ID

CFG1 Register (Address 0x94)

Figure 46:
CFG1 Register

Addr: 0x94		CFG1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RW	Reserved. Must be set to default value.
3:1	PD_MUX_SEL	000	RW	This field sets photodiode connection to ALS channels. See Figure 47 for the details.
0	ENAB_TEMP_SENSOR	0	RW	This field activates temperature sensor. Set PEN =TEN =ENAB_TEMP_SENSOR =1 to enable temperature measurement.

Figure 47:
PD_MUX_SEL

Value (1)	Mode	Channel 0	Channel 1	Channel 2	Channel 3
PD_MUX_SEL = 000b	TWO_CHANN_MODE	Clear + Green	Red + Blue	N.C.	N.C.
PD_MUX_SEL = 011b	COLOR_MODE	Clear	Red	Green	Blue

Note(s):

1. All other PD_MUX_SEL values are reserved and should not be used.

AGAIN_1_0 Register (Address 0x95)

Figure 48:
AGAIN_1_0 Register

Addr: 0x95		AGAIN_1_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	AGAIN1	1100	RW	This field sets the gain of ALS channel 1. **Value** / **AGAIN1** 0 / 1x 1 / 2x 2 / 4x 3 / 8x 4 / 16x 5 / 32x 6 / 64x 7 / 128x 8 / 256x 9 / 512x 10 / 1024x 11 / 2048x 12 / 4096x All other values / Reserved
3:0	AGAIN0	1100	RW	This field sets the gain of ALS channel 0. See AGAIN1 for the detailed settings.

AGAIN_3_2 Register (Address 0x96)

Figure 49:
AGAIN_3_2 Register

Addr: 0x96		AGAIN_3_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	AGAIN3	1100	RW	This field sets the gain of ALS channel 3. See AGAIN1 for the detailed settings.
3:0	AGAIN2	1100	RW	This field sets the gain of ALS channel 2. See AGAIN1 for the detailed settings.

LDR0_CFG Register (Address 0x9A)

Figure 50:
LDR0_CFG Register

Addr: 0x9A		LDR0_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0	RW	Reserved. Must be set to default value.
6	EN_LDR_0	1	RW	Enables the LDR0.
5:4	ISINK_LSB	01	RW	This field sets VCSEL drive current resolution **Value** / **VCSEL Drive Current Resolution** 00 / 0.5mA 01 / 1.0mA 10 / 1.5mA 11 / 2.0mA
3:0	PLDRIVE0	0010	RW	This field sets the drive current of the VCSEL driver 0. The formula is shown below: Drive Current 0=(PLDRIVE0+1) x ISINK_LSB. The drive current should be configured within the range of 7mA ~12mA. The values are the nominal current. The actual current through the VCSEL is factory trimmed to normalize the IR intensity.

EYE_SAFETY_CFG Register (Address 0x9E)

Figure 51:
EYE_SAFETY_CFG Register

Addr: 0x9E		EYE_SAFETY_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	EYE_SAFETY_CHKS_ENAB	0	RW	Enables VDD and VSS short check for PLDRIVE0, and also the analog watch dog timer. Eye safety runs only once at the beginning when PON and PEN are enabled.
6	DISABLE_PROX_ON_WD_FAIL	1	RW	Disable the high side switch when the eye safety watch dog expires.
5:0	Reserved	0	RW	Reserved. Must be set to default value.

EYE_SAFETY_STATUS Register (Address 0x9F)

Figure 52:
EYE_SAFETY_STATUS Register

Addr: 0x9F		EYE_SAFETY_STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	0	R	Reserved. Must be set to default value.
4	EYE_SAFETY_WD_STATUS_SYNCED	0	R	When the flag is set, it indicates that the watchdog has triggered. When DISABLE_PROX_ON_WD_FAIL is set, the PLDRIVER0 is disabled when this flag is set.
3:2	Reserved	0	R	Reserved. Must be set to default value.
1	PLDRIVE0_PAD_SHORT_VSS_FAIL	0	R	When the flag is set, it indicates that the VSS check during eye safety check failed for PLDRIVER0. The PLDRIVER0 is disabled (no pulses are sent) in case of failure but the proximity timing is maintained. When ESIEN is 1, an interrupt is generated in the final state after PROX_DATA_AVG is complete. The flag is cleared when PON is made 0. Writing a 1 to this field will clear the flag. To enable clear-by-read function, INT_READ_CLEAR in the register CFG3 must be set to 1.

Addr: 0x9F		EYE_SAFETY_STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	PLDRIVER0_PAD_SHORT_VDD_FAIL	0	R	When the flag is set, it indicates that the VDD check during eye safety check failed for PLDRIVER0. The PLDRIVER0 is disabled (no pulses are sent) in case of failure but the proximity timing is maintained. When ESIEN is 1, an interrupt is generated in the final state after PROX_DATA_AVG is complete. The flag is cleared when PON is made 0. Writing a 1 to this field will clear the flag. To enable clear-by-read function, INT_READ_CLEAR in the register CFG3 must be set to 1.

STATUS Register (Address 0xA0)

Figure 53:
STATUS Register

Addr: 0xA0		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PINT_GRT_HTH	0	R, SC	Proximity interrupt is due to PDATA exceeds the high threshold (PIHT). Clearing PINT flag will clear this flag as well.
6	PINT_LES_LTH	0	R, SC	Proximity interrupt is due to PDATA exceeds the low threshold (PILT). Clearing PINT flag will clear this flag as well.
5	PSAT	0	RW, SC	Proximity saturation flag indicates that a PSAT_2STG or AMBCOMP_LVL_SAT or PSAT_1STG_PULSE or PSAT_1STG_AMB event occurred during a previous proximity cycle.
4	PINT	0	RW, SC	Proximity interrupt flag indicates that proximity results have exceeded thresholds and persistence settings.
3	CINT	0	RW, SC	Calibration interrupt flag indicates that calibration has completed.
2	ZINT	0	RW, SC	Zero detection interrupt flag indicates that a zero value in PDATA has caused the proximity offset to be decremented (if PROX_AUTO_OFFSET_ADJUST = 1).
1	PSAT_2STG	0	RW, SC	Proximity saturation interrupt is from second stage of proximity engine.
0	AMBCOMP_LVL_SAT	0	RW, SC	Proximity saturation interrupt is from ambcomp_lvl comparator.

STATUS_2 Register (Address 0xA1)

Figure 54:
STATUS_2 Register

Addr: 0xA1		STATUS_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	VSYNC_LOST	1	R, SC	This flag indicates that VSYNC is not present.
6	POWER_ON_ RESET	1	R, SC	This flag indicates that power on cycle has happened. 0 - No power on reset happened from last read 1 - Power on reset happened from last read This flag is clear-by-read by default.
5	PWINT	0	RW, SC	This flag is set when PWTIME is completed if PWIEN =1. This flag is set only in parallel/concurrent mode and only when PWEN = 1.
4	Reserved	0	RW, SC	Reserved. Must be set to default value.
3	PSAT_1STG_AMB	0	RW, SC	This flag indicates proximity saturation is from first stage of proximity engine due to ambient in subtraction phase.
2	PSAT_1STG_ PULSE	0	RW, SC	This flag indicates proximity saturation is from first stage of proximity engine when VCSEL pulse is emitted.
1	VSYNC_LOST_INT	0	RW, SC	Interrupt when VSYNC watchdog timeout happens or internal oscillator is stopped e.g PON=0. This interrupt generated on event based.
0	VSYNC_CHG_INT	0	RW, SC	Interrupt when there is a change in VSYNC period

STATUS_3 Register (Address 0xA2)

Figure 55:
STATUS_3 Register

Addr: 0xA2		STATUS_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PWM_PRD_CHG_INT	0	RW, SC	Interrupt when there is a change in PWM period
6:5	Reserved	00	RW, SC	Reserved. Must be set to default value.
4	ATINT	0	RW, SC	Interrupt when ATIME is completed.
3	FTINT	0	RW, SC	Interrupt when FIFO_LVL crosses FIFO_THR_LVL. FTIEN needs to be set.
2	AWINT	0	RW, SC	Interrupt when AWTIME is completed. To enable AWINT, both AWEN and AWIEN have to be set.
1	ASAT	0	RW, SC	ALS analog saturation.
0	AINT	0	RW, SC	ALS interrupt flag indicates that ALS results have exceeded the AILT or AIHT thresholds and persistence settings.

All flags with access type of RW, SC in STATUS, STATUS_2, and STATUS_3 registers can be cleared by setting the bit high. Alternatively, if the INT_READ_CLEAR in the CFG3 register bit is set, then simply reading these registers automatically clears all flags.

PID_L Register (Address 0xA5)

Figure 56:
PID_L Register

Addr: 0xA5		PID_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PID_L	0x00	RW	The low byte of the 16bit programmable Proximity ID. Whenever a proximity pulse is triggered during ASP1 ASP2 sampling period in Full Parallel Mode, PID is written into the FIFO instead of the actual ALS data if PID_EN is 1.

PID_H Register (Address 0xA6)

Figure 57:
PID_H Register

Addr: 0xA6		PID_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PID_H	0x00	RW	The high byte of the 16bit programmable Proximity ID.

CFG2 Register (Address 0xA7)

Figure 58:
CFG2 Register

Addr: 0xA7		CFG2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0	RW	Reserved. Must be set to default value.
3	HOLD_ONLY_IN_PULSE_ST	0	RW	It is recommended to set the bit to "1" during device initialization. In concurrent mode, ALS integration is only on hold during Proximity pulsing period. If the bit is "0", in concurrent mode, ALS integration is on hold until Proximity completes the entire measurement which includes the initialization time, integration time or PTIME whichever is longer, hardware averaging loops if enabled and ADC conversion time. Also, ALS is kept on hold during proximity is waiting for VSYNC signal detection and PSD time when PVSYNC is enabled.
2	Reserved	0	RW	Reserved. Must be set to default value.
1	SKIP_IDAC_SAR	1	RW	If set, the IDAC_SAR is skipped.
0	DISABLE_IDAC	1	RW	If set, the IDAC is disabled. If SKIP_IDAC_SAR =DISABLE_IDAC =0, it enables the IDAC to automatically remove most of the ambient IR light to avoid a saturation caused by high ambient IR components. The function runs before every PTIME, and the time required is given by the formula: prox_init_time =7 x (PPULSE_LEN +42.15µs).

RESET Register (Address 0xA8)

Figure 59:
RESET Register

Addr: 0xA8		RESET		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RW	Reserved. Must be set to default value.
3	INV_XRES	0	RW	Inverts XRES pin input.
2	ENAB_XRES	0	RW	Enable XRES as a hardware reset pin. By default, level high triggers a device reset.
1	HARD_RESET	0	RW	Perform a POR cycle when this bit is set.
0	SOFT_RESET	0	RW	Software Reset. Writing a '1' triggers a reset of all I^2C registers to default states, including SOFT_RESET bit itself. Due to the reset of PON, a running ALS and Proximity is aborted and the oscillator is turned off. SOFT_RESET will not set POWER_ON_RESET status bit.

CFG3 Register (Address 0xAB)

Figure 60:
CFG3 Register

<table>
<tr><th colspan="2">Addr: 0xAB</th><th colspan="3">CFG3</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td>7</td><td>INT_READ_CLEAR</td><td>0</td><td>RW</td><td>If set, the interrupt flag bits in the STATUS register will be reset whenever the STATUS register is read over I²C.</td></tr>
<tr><td rowspan="6">6:5</td><td rowspan="6">MODE_CFG</td><td rowspan="6">10</td><td rowspan="6">RW</td><td>The register sets the operational mode of ALS and Proximity measurement of the device.</td></tr>
<tr><td>
<table>
<tr><th>Value</th><th>Operational Mode</th></tr>
<tr><td>00</td><td>Sequential Mode</td></tr>
<tr><td>01</td><td>Concurrent Mode</td></tr>
<tr><td>10</td><td>Full Parallel Mode</td></tr>
<tr><td>11</td><td>Unused Setting</td></tr>
</table>
</td></tr>
<tr><td rowspan="6">4</td><td rowspan="6">SAI</td><td rowspan="6">0</td><td rowspan="6">RW</td><td>The Sleep After Interrupt bit is used to place the device into a low power mode at the end of the proximity /ALS cycle if an interrupt has been generated. SAI doesn't modify any register bits directly, it rather uses the interrupt signal to turn off the oscillator. The device will appear as if PON=0, however, PON will read as 1. The way to wake up the device from SAI-sleep is by clearing the interrupts in the status registers. Note that SAI is only available in sequential mode.</td></tr>
<tr><td>
<table>
<tr><th>PON</th><th>SAI</th><th>INT (low active)</th><th>Oscillator</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>PID_EN</td><td>0</td><td>RW</td><td>When this bit is set, whenever a proximity pulse is triggered during ASP1 ASP2 sampling period in Full Parallel Mode, PID is written into the FIFO instead of the actual ALS data.
Configure {PID_H, PID_L} for the PID value.</td></tr>
<tr><td>2:0</td><td>Reserved</td><td>001</td><td>RW</td><td>Reserved. Must be set to default value.</td></tr>
</table>

CFG6 Register (Address 0xAE)

Figure 61:
CFG6 Register

Addr: 0xAE		CFG6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0	RW	Reserved. Must be set to default value.
6	DISABLE_APC	1	RW	Proximity automatic pulse control (APC) disable. 0 = APC enable 1 = APC disable This bit should be set to 1 when calibration needs to be performed
5:0	Reserved	111111	RW	Reserved. Must be set to default value.

PWM_CFG Register (Address 0xB0)

Figure 62:
PWM_CFG Register

Addr: 0xB0		PWM_CFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:3	Reserved	00000	RW	Reserved. Must be set to default value.	
2:1	PWM_CHG_DET_STP	00	RW	PWM period change detection step. Once PWM period changes from previous cycle by step of period mentioned in the following table, PWM_CHG_INT interrupt is generated if PWMIEN=1. PWM_PRD={PWM_PRD_H, PWM_PRD_L}	
				Value	**Timing**
				0	Compare with PWM_PRD[13:9]
				1	Compare with PWM_PRD[13:8]
				2	Compare with PWM_PRD[13:10]
				3	Compare with PWM_PRD[13:11]
0	PWM_IN_EN	0		Enable XRES as a PWM input pin.	

VSYNC_CFG Register (Address 0xB1)

Figure 63:
VSYNC_CFG Register

Addr: 0xB1		VSYNC_CFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	Reserved	00	RW	Reserved. Must be set to default value.	
5:4	VSYNC_CHG_DET_STP	00	RW	VSYNC period change detection step. Once VSYNC period changes from previous cycle by step of period mentioned in the following table, VSYNC_CHG_INT interrupt is generated if VSIEN=1. VSYNC_PRD ={VSYNC_PRD_H, VSYNC_PRD_L}	
				Value	**Timing**
				0	Compare with VSYNC_PRD[15:10]
				1	Compare with VSYNC_PRD[15:9]
				2	Compare with VSYNC_PRD[15:11]
				3	Compare with VSYNC_PRD[15:12]
3	INT_VSYNC_EN	0	RW	Enables internal VSYNC. It will be cleared automatically when VSYNC signal is detected on the device VSYNC pin.	
2	VSYNC_INVERT	0	RW	This bit inverts VSYNC input. 0 – Not inverted; 1 – Inverted;	
1:0	VSYNC_WD_TH	0	RW	VSYNC watch dog time out. The expiration generates VSYNC_LOST_INT interrupt if VSIEN=1.	
				Value	**Timing**
				0	88.92ms
				1	11.12ms
				2	22.23ms
				3	44.46ms

VSYNC_PRD_L Register (Address 0xB2)

Figure 64:
VSYNC_PRD_L Register

Addr: 0xB2		VSYNC_PRD_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	VSYNC_PRD_L	0x00	RW	The low byte of the 16-bit VSYNC period data.

VSYNC_PRD_H Register (Address 0xB3)

Figure 65:
VSYNC_PRD_H Register

Addr: 0xB3		VSYNC_PRD_H		
Bit	Bit Name	Default	Access	Bit Description
7:0	VSYNC_PRD_H	0x00	RW	The high byte of the 16-bit VSYNC period data.

VSYNC_PRD stores the last VSYNC signal period. This is 16-bit divided into 2 registers {VSYNC_PRD_H, VSYNC_PRD_L} with resolution of 1.357µs/bit. It is recommended that VSYNC signal is in the frequency range of 11.25Hz to 1KHz with minimum active pulse width 16µs, although the counter is able to detect a much higher frequency. Once external VSYNC signal is lost, VSYNC_LOST_INT interrupt is generated if VSIEN =1. Then software has option to enable internal VSYNC by enabling INT_VSYNC_EN. The internal VSYNC will generate with frequency of last period stored in VSYNC_PRD registers. Users can write VSYNC_PRD registers for a desired frequency before enabling the internal VSYNC feature. Once the device detects external VSYNC signal, the INT_VSYNC_EN bit will be cleared automatically, VSYNC_PRD value will update according to the period detected.

PWM_PRD_L Register (Address 0xB5)

Figure 66:
PWM_PRD_L Register

Addr: 0xB5		PWM_PRD_L		
Bit	Bit Name	Default	Access	Bit Description
7:0	PWM_PRD_L	0x00	R	The low byte of the 14-bit PWM period data.

PWM_PRD_H Register (Address 0xB6)

Figure 67:
PWM_PRD_H Register

Addr: 0xB6		PWM_PRD_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	R	Reserved. Must be set to default value.
5:0	PWM_PRD_H	000000	R	The upper 6 bits of the 14-bit PWM period data

PWM_PRD register stores the last PWM period. This is 14bit divided into 2 registers {PWM_PRD_H, PWM_PRD_L} with resolution of 1.357µs/bit.

PWM_HIP_L (Address 0xB7)

Figure 68:
PWM_HIP_L

Addr: 0xB7		PWM_HIP_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PWM_HIP_L	0x00	R	The low byte of the 14-bit PWM signal high period data.

PWM_HIP_H (Address 0xB8)

Figure 69:
PWM_HIP_H

Addr: 0xB8		PWM_HIP_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	R	Reserved. Must be set to default value.
5:0	PWM_HIP_H	000000	R	The upper 6 bits of the 14-bit PWM signal high period data.

PWM_HIP register stores the last PWM high period. This is 14bit divided into 2 registers {PWM_HIP_H, PWM_HIP_L} with resolution of 1.357µs/bit. It is recommended that PWM signal is in the frequency range of 45Hz to 10KHz with minimum active pulse length 16µs.

POFFSET Register (Address 0xC0)

Figure 70:
POFFSET Register

Addr: 0xC0		POFFSET		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	POFFSET	0x00	RW	This register contains the magnitude portion of proximity offset adjust value.

POFFSET_SIGN Register (Address 0xC1)

Figure 71:
POFFSET_SIGN Register

Addr: 0xC1		POFFSET_SIGN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0000000	RW	Reserved. Must be set to default value.
0	POFFSET_ SIGN	0	RW	This register contains the sign portion of proximity offset adjust value.

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSET /POFFSET_SIGN registers provide a mechanism to remove system crosstalk from the proximity data. POFFSET /POFFSET_ SIGN contains the magnitude and sign of a value that adjusts PDATA in the AFE. An offset value in the range of ± 255 is possible.

AZ_CONFIG Register (Address 0xD6)

Figure 72:
AZ_CONFIG Register

Addr: 0xD6		AZ_CONFIG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	START_MAN_AZ	0	RW, SC	Starts ALS manual auto zero once the bit is set. Once auto zero is completed, it's self cleared. This manual trigger needs to be enabled only when PON=1 and AEN=0. The user first needs to set PON=1 and then set this bit.
6:0	AZ_NTH_ ITERATION	1111111	RW	Run autozero automatically every n^{th} ALS iteration (0=never, 7Fh=only at first ALS cycle, n=every n^{th} time)

CALIB Register (Address 0xD7)

Figure 73:
CALIB Register

Addr: 0xD7		CALIB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	OFFCAL_ENAB_AVG	0	RW	Enables proximity hardware averaging as selected with PROX_DATA_AVG during calibration. 0 = No hardware averaging 1 = Hardware averaging enabled
6	Reserved	0	RW	Reserved. Must be set to default value.
5	ELECTRICAL_ CALIBRATION	0	RW	Selects proximity calibration type. 0 = Electrical and optical crosstalk. 1 = Electrical crosstalk only.
4	PTIME_IN_CALIB	0	RW	Enables PTIME during calibration. Useful when averaging is enabled. 0 = PTIME ignored during calibration 1 = PTIME enabled during calibration
3:1	Reserved	000	RW	Reserved. Must be set to default value.
0	START_OFFSET_CAL	0	RW	Set to 1 to start a calibration sequence.

Proximity response in systems with electrical and optical crosstalk may be improved by using the calibration feature. Optical crosstalk is caused when the photodiode receives a portion of the VCSEL IR, which was unintentionally reflected by a surface other than the target. Electrical offset is caused by electrical disturbance in the sensor AFE, and influences the proximity result as well. Before starting the calibration, it is required to set PEN, AEN and PON to 0 to bring the state machine idle, and set DISABLE_APC to 1 to disable the auto pulse control. The calibration target, BINSRCH_TARGET, needs to be configured to a desired value, the calibration routine adjusts the value in POFFSET /POFFSET_SIGN until the proximity result is as close to the BINSRCH_TARGET as possible.

The calibration needs to run with the same settings as regular proximity measurement, such as PPULSE, PPULSE_LEN, PGAIN, PGAIN2, PLDRIVE0. If PTIME_IN_CALIB is enabled, the same PTIME used for regular proximity measurement is also enabled during the calibration. If OFFCAL_ENAB_AVG is enabled, the hardware averaging as selected with PROX_DATA_AVG is enabled as well during the calibration. The calibration needs to run 9 proximity measurement cycles. If every cycle of the 9 cycles needs to be synchronized to the VSYNC signal with PSD delay, PROX_CAL_VSYNC_EN has to be enabled. After all the settings properly configured, PON needs to be enabled again

in order to run the calibration successfully. An electrical calibration can be initiated at any time by setting the ELECTRICAL_CALIBRATION and START_OFFSET_CAL bits. To perform an optical (and electrical) calibration do not set the ELECTRICAL_CALIBRATION bit when setting the START_OFFSET_CAL bit. Electrical and optical calibration functions are identical, except that during an electrical calibration the proximity photodiode is disconnected from the AFE.

Upon completion of the calibration, proximity offset registers are automatically loaded with calibration result, START_OFFSET_CAL bit will be self-cleared, the CINT flag will assert. If CIEN is enabled, an interrupt is generated on the INT pin.

CALIB_OFFSET Register (Address 0xD8)

Figure 74:
CALIB_OFFSET Register

Addr: 0xD8		CALIB_OFFSET		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0	RW	Reserved. Must be set to default value.
6	EN_AUTO_ORE_CAL	0	RW	Setting this bit to a 1 enables automatic calculation for PRX_OFFSET_RANGE_EXTENSION during proximity calibration. When the bit is 0, the automatic calculation is disabled, and the PRX_OFFSET_RANGE_EXTENSION value has to be provided by users.
5	EN_PRX_OFFSET_RANGE_EXTENSION	0	RW	Setting this bit to a 1 enables the proximity offset range extension functionality. See the PRX_OFFSET_RANGE_EXTENSION bits. If this bit is set to 0, the offset range extension is disabled.
4:0	PRX_OFFSET_RANGE_EXTENSION	00000	RW	Offset range extension selection. For PGAIN2=2.5x, all 5 bits are used. For PGAIN2=5x, the LSB is ignored. For PGAIN2=10x, 2 LSBs are ignored.

Value	**Selection**
0 (00000)	Nominal
1 (00001)	Nominal + 1 Step
2 (00010)	Nominal + 2 Steps
3 (00011)	Nominal + 3 Steps
Nominal + (Value) Steps	
31 (11111)	Nominal + 31 Steps

For applications with high optical proximity crosstalk (the emitted IR optical signal appears at the IR sensor), the offset range can be extended in discrete steps. To determine the best range extension step for the application, a proximity calibration cycle is initiated and the resulting proximity offset is captured in the POFFSET /POFFSET_SIGN registers.

CALIBCFG Register (Address 0xD9)

Figure 75:
CALIBCFG Register

Addr: 0xD9		CALIBCFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	BINSRCH_ TARGET	010	RW	Proximity offset calibration result target.	
				Value	**PDATA Target**
				0 (000)	3
				1 (001)	7
				2 (010)	15
				3 (011)	31
				4 (100)	63
				5 (101)	127
				6 (110)	255
				7 (111)	511
4	Reserved	1	RW	Reserved. Must be set to default value.	
3	PROX_AUTO_ OFFSET_ ADJUST	0	RW	If set, then in proximity mode, whenever an ADC measurement yield zero, the pertinent offset register will be decreased. Will set the OFFSET_ADJUSTED flag if it happened. Note that if a diode is disabled, this mechanism is disabled as well.	

Addr: 0xD9		CALIBCFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
2:0	PROX_DATA_AVG	0 (000)	RW	PROX_DATA_AVG defines the number of ADC samples collected and hardware averaged during a proximity cycle.	
				Value	**Sample Size**
				0 (000)	Disable
				1 (001)	2
				2 (010)	4
				3 (011)	8
				4 (100)	16
				All other values	Reserved

The BINSRCH_TARGET field is used by the calibration feature to set the baseline value for PDATA when no target is present. For example, calibration of a device in open air, with no target, and BINSRCH_TARGET setting of 2 causes the PDATA value will be approximately 15 counts. This feature is useful because it forces PDATA result to always be above zero.

The PROX_DATA_AVG field sets the number of ADC samples that are averaged. Each ADC sample causes the programmed number of proximity pulses to be transmitted. Once all samples have been completed and the average is calculated, the proximity state machine will then pass this value either directly to PDATA.

PCFG4 Register (Address 0xDA)

Figure 76:
PCFG4 Register

Addr: 0xDA		PCFG4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0	RW	Reserved. Must be set to default value.
0	PROX_CAL_ VSYNC_EN	0	RW	The bit enables proximity calibration synchronized to the VSYNC signal with PSD delay. The proximity calibration consists of 9 measurement cycles. If the bit is set to 1, every cycle of the 9 measurement cycles are synchronized to the VSYNC signal with PSD delay. If the bit is set to 0 and PVSYNC_EN is 1, only the first measurement cycle is synchronized to the VSYNC signal with PSD delay, the successive measurement cycles run immediately after the first measurement cycle. If the bit is set to 0 and PVSYNC_EN is 0, all 9 measurement cycles of the proximity calibration run immediately pulse burst irrespective of VSYNC signal.

CALIBSTAT Register (Address 0xDC)

Figure 77:
CALIBSTAT Register

Addr: 0xDC		CALIBSTAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	00000	R	Reserved. Must be set to default value.
2	OFFSET_ ADJUSTED	0	R	Bit is set when the proximity offset has been automatically decremented if PROX_AUTO_ OFFSET_ADJ = 1 (see CALIBCFG register). This bit can be cleared by writing 1 to it or setting PROX_AUTO_OFFSET_ADJ to 0.
1	Reserved	0	R	Reserved. Must be set to default value.
0	CALIB_FINISHED	0	R	This flag indicates that calibration has finished. This bit is a copy of the CINT bit in the STATUS register. It will be cleared when the CINT bit is cleared.

INTENAB Register (Address 0xDD)

Figure 78:
INTENAB Register

Addr: 0xDD		INTENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASIEN	0	RW	ALS Saturation Interrupt Enable
6	PSIEN	0	RW	Proximity Saturation Interrupt Enable
5	PIEN	0	RW	Proximity Interrupt Enable
4	AIEN	0	RW	ALS/Color Interrupt Enable
3	CIEN	0	RW	Calibration Interrupt Enable
2	ZIEN	0	RW	Zero Detect Interrupt Enable
1	HYS_PIEN	0	RW	1 = Enables hysteresis based proximity interrupt 0 = Enables level based proximity interrupt
0	VSIEN	0	RW	VSYNC related interrupt enable

INTENAB_2 Register (Address 0xDE)

Figure 79:
INTENAB_2 Register

Addr: 0xDE		INTENAB_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PWMIEN	0	RW	PWM period change interrupt enable
6:5	Reserved	00	RW	Reserved. Must be set to default value.
4	ESIEN	0	RW	Eye safety failure interrupt enable
3	ATIEN	0	RW	ATIME completion interrupt enable
2	FTIEN	0	RW	FIFO threshold crosses interrupt enable
1	PWIEN	0	RW	PWTIME completion interrupt enable
0	AWIEN	0	RW	AWTIME completion interrupt enable

ASD_L Register (Address 0xE0)

Figure 80:
ASD_L Register

Addr: 0xE0		ASD_L				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
7:0	ASD_L	0x00	RW	ASD_L is lower byte of ASD (ALS Start Delay).		
				Value	**Delay Cycles**	**Delay Time**
				0x0000	0	ALS init time
				0x0018	24	ALS init time
				0x0019	25	1.357µs x 25
				0x001A	26	1.357µs x 26
				…	…	…
				0xFFFF	65535	1.357µs x 65535

ASD_H Register (Address 0xE1)

Figure 81:
ASD_H Register

Addr: 0xE1		ASD_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ASD_H	0x00	RW	ASD_H is upper byte of ASD (ALS Start Delay).

The ASD (ALS Start Delay) timing registers control the start of ALS integration after detect of VSYNC signal. It is a 16-bit value split into two registers {ASD_H [7:0], ASD_L [7:0]}.

ASD is recommended to be programmed greater than ALS initialization period (24 cycles), otherwise it is ignored. ASD needs to be programmed less than VSYNC period, since the counter will reset once VSYNC signal is detected. If VSYNC is changed, ASD period and other configurations need to be changed accordingly by bringing device in IDLE mode by stopping integration.

ASP1_L Register (Address 0xE2)

Figure 82:
ASP1_L Register

<table>
<tr><th colspan="2">Addr: 0xE2</th><th colspan="4">ASP1_L</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="3">Bit Description</th></tr>
<tr><td rowspan="8">7:0</td><td rowspan="8">ASP1_L</td><td rowspan="8">0x00</td><td rowspan="8">RW</td><td colspan="3">ASP1_L is lower byte of the ASP1 (ALS data Sampling Period 1).
It is a 14bit value split into 2 registers {ASP1_H[5:0], ASP1_L[7:0]}.
ASP1 is in multiples of 1.357us resolution, and should be programmed >12us.
If ASP1 is 0, ASP1 takes the value of ATIME and ASP2 disabled irrespective of the programmed value.</td></tr>
<tr><td>Value</td><td>Sampling Cycles</td><td>Sampling Period</td></tr>
<tr><td>0x0000</td><td>0</td><td>ATIME (sampled only once at end of ATIME)</td></tr>
<tr><td>0x0009</td><td>9</td><td>1.357µs x9</td></tr>
<tr><td>0x000A</td><td>10</td><td>1.357µs x10</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>0x3FFF</td><td>16383</td><td>1.357µs x16383</td></tr>
</table>

ASP1_H Register (Address 0xE3)

Figure 83:
ASP1_H Register

Addr: 0xE3		ASP1_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	ASP1_H	000000	RW	ASP1_H is upper byte of the ASP1 (ALS data Sampling Period 1). See ASP1_L for the value settings.

ASP2_L Register (Address 0xE4)

Figure 84:
ASP2_L Register

Addr: 0xE4		ASP2_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ASP2_L	0x00	RW	ASP2_L is lower byte of the ASP2 (ALS data Sampling Period 2). It is a 14bit value split into 2 registers {ASP2_H[5:0], ASP2_L[7:0]}. ASP2 is in multiples of 1.357us resolution, and should be programmed >12us. ASP2 should not be programmed 0. If only ASP1 is required, ASP2 needs to be programmed same as ASP1.

Value	Sampling Cycles	Sampling Period
0x0009	9	1.357µs x9
0x000A	10	1.357µs x10
…	…	…
0x3FFF	16383	1.357µs x16383

ASP2_H Register (Address 0xE5)

Figure 85:
ASP2_H Register

Addr: 0xE5		ASP2_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	ASP2_H	000000	RW	ASP2_H is upper byte of the ASP2 (ALS data Sampling Period 2). See ASP2_L for the value settings.

ASP1 ASP2 are ALS data Sampling Periods in addition to ATIME. It allows for short integration time with 1.357µs resolution. ASP1 ASP2 need to be programmed greater than 12µs.

Once enabled, the ALS data sampling sequence is ASP1–>ASP2–>ASP1–>ASP2–>…

If ASP1 is 0, ASP1 and ASP2 are disabled. The ALS data sampling sequence is ATIME–>ATIME–>ATIME–>…

ASP2 should not be programmed 0. If only ASP1 period is required, ASP2 needs to be programmed same as ASP1.

Although ASP1, ASP2, ATIME are programmed with high flexibility, it always recommend to program ATIME to be an integer multiple of ASP1+ASP2. Explained by a formula: ATIME =N x(ASP1 +ASP2), where N is a positive integer.

ATIME Register (Address 0xE6)

Figure 86:
ATIME Register

<table>
<tr><th colspan="2">Addr: 0xE6</th><th colspan="6">ATIME</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="4">Bit Description</th></tr>
<tr><td rowspan="9">7:0</td><td rowspan="9">ATIME</td><td rowspan="9">0x00</td><td rowspan="9">RW</td><td colspan="4">The ATIME value specifies the ALS integration time in 2.779ms intervals. 0x00 indicates 2.779ms. The maximum ALS count value depends on the integration time. For every 2.779ms, the maximum value increases by 2048. This means that to be able to reach ALS full scale, the integration time has to be at least 32*2.779ms.</td></tr>
<tr><td>Value</td><td>Integration Cycles</td><td>Integration Time</td><td>Maximum ALS Value</td></tr>
<tr><td>0x00</td><td>1</td><td>2.779ms</td><td>2047</td></tr>
<tr><td>0x01</td><td>2</td><td>5.558ms</td><td>4095</td></tr>
<tr><td>0x02</td><td>3</td><td>8.336</td><td>6143</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>0x1F</td><td>32</td><td>88.923ms</td><td>65535</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>0xFF</td><td>256</td><td>711.381ms</td><td>65535</td></tr>
</table>

The ATIME register controls the integration time of the ALS ADCs. The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.779ms nominal rate. Loading 0x00 will generate a 2.779ms integration time, loading 0x01 will generate a 5.558ms integration time, and so forth.

By default, ALS data are sampled and stored in FIFO registers by every ATIME period. If enable ASP1 ASP2, ALS data sampling period is defined by ASP1 ASP2.

AWTIME Register (Address 0xE7)

Figure 87:
AWTIME Register

Addr: 0xE7		AWTIME				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
7:0	AWTIME	0x00	RW	Value that specifies the wait time in 2.779ms increments		
				Value	**Wait Cycles**	**Wait Time**
				0x00	1	2.779ms (33.346ms)
				0x01	2	5.558ms (66.692ms)
				0x02	3	8.336ms (100.038ms)
				…	…	…
				0x1F	32	88.923ms (1.067s)
				…	…	…
				0xFF	256	711.381ms (8.537s)

The AWTIME is implemented using a down counter and starts counting from very beginning of every ALS integration cycle. If enabled, AWTIME needs to be programmed greater than ATIME, otherwise ATIME takes precedence over AWTIME.

AWTIME = Wait Cycles x2.779ms.

If AWLONG is enabled, then AWTIME =Wait Cycles x2.779ms x12.

ACFG Register (Address 0xE8)

Figure 88:
ACFG Register

Addr: 0xE8		ACFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	000	RW	Reserved. Must be set to default value.
4	DOUBLE_DATA_MODE	0	RW	If set, the data stored in FIFO per channel is only 8 bits.
3	AINT_DATA_SEL	0	RW	The bit selects data used for APERS calculation. 0 = ASP1 C channel data is used for APERS calculation. 1 = ASP2 C channel data is used for APERS calculation.
2	ENAB_RES_BITS	0	RW	Enable the residue bits. If enabled, the data format in FIFO is U13.3 that consists of 13-bit full counts and 3-bit residual counts if DOUBLE_DATA_MODE is 0. When DOUBLE_DATA_MODE is 1, the data format in FIFO is U7.1 that consists of 7-bit full counts and 1-bit residual counts.
1:0	ADAVG	00	RW	ALS sampling data averaging. ASP1 and ASP2 sampled data are averaged accordingly before written into FIFO. When ASP1=0, the averaging is ignored.

ENAB_RES_BITS	DOUBLE_DATA_MODE	DATA FORMAT
0	0	U16.0
0	1	U8.0
1	0	U13.3
1	1	U7.1

Value	Average
0	1
1	2
2	4
3	8

PSD_L Register (Address 0xEA)

Figure 89:
PSD_L Register

Addr: 0xEA		PSD_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PSD_L	0x00	RW	This is lower byte of Proximity Start Delay time. It's 16-bit value split into 2 registers {PSD_H[7:0],PSD_L[7:0]}. It is in multiples of 1.357µs.

Value	Delay Cycles	Delay Time
0x0000	0	Disabled
0x0001	1	1.357µsx1
0x0002	2	1.357µsx2
…	…	…
0x3FFF	16383	1.357µsx16383
…	…	…
0xFFFF	65535	1.357µsx65535

PSD_H Register (Address 0xEB)

Figure 90:
PSD_H Register

Addr: 0xEB		PSD_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PSD_H	0x00	RW	This is upper byte of Proximity Start Delay time. See PSD_L for details.

The PSD (Proximity Start Delay) timing registers control the start of proximity measurement after detect of VSYNC signal. It is a 16-bit value split into two registers {PSD_H [7:0], PSD_L [7:0]}. PSD needs to be programmed less than VSYNC period, since the counter will reset once VSYNC signal is detected. If VSYNC is changed, PSD period and other configurations need to be changed accordingly by bringing device in IDLE mode by stopping integration.

PWTIME Register (Address 0xEC)

Figure 91:
PWTIME Register

Addr: 0xEC		PWTIME				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
7:0	PWTIME	0x00	RW	Value that specifies the proximity wait time in 2.779ms increments.		
				Value	**Wait Cycles**	**Wait Time**
				0x00	1	2.779ms (33.346ms)
				0x01	2	5.558ms (66.692ms)
				0x02	3	8.336ms (100.038ms)
				…	…	…
				0x1F	32	88.923ms (1.067s)
				…	…	…
				0xFF	256	711.381ms (8.537s)

The PWTIME is implemented using a down counter and starts counting from very beginning of every proximity measurement cycle including the initialization time. If enabled, PWTIME needs to be programmed greater than proximity measurement time, otherwise it's ignored.

PWTIME = Wait Cycles x2.779ms.

If PWLONG is enabled, then PWTIME =Wait Cycles x2.779ms x12.

Note that PWTIME is available in Full Parallel Mode and Concurrent Mode, but ignored in Sequential Mode.

FIFO_STATUS_1 Register (Address 0xF0)

Figure 92:
FIFO_STATUS_1 Register

<table>
<tr><th colspan="2">Addr: 0xF0</th><th colspan="4">FIFO_STATUS_1</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="3">Bit Description</th></tr>
<tr><td rowspan="6">7:0</td><td rowspan="6">FIFO_LVL</td><td rowspan="6">0x00</td><td rowspan="6">R</td><td colspan="3">FIFO level indication. The FIFO level is not a number of bytes, but rather sets of data from all the active channels.
In TWO_CHANN_MODE (PD_MUX_SEL=0), FIFO level of 1 indicates one data set of the two channels.
In COLOR_MODE (PD_MUX_SEL=3), FIFO level of 1 indicates one data set of CRGB channels.
When DOUBLE_DATA_MODE=0, the value in {FIFO_LVL} is the FIFO level.
When DOUBLE_DATA_MODE=1, the value in {FIFO_LVL, FIFO_LVL_LSB} is the FIFO level.</td></tr>
<tr><td>PD_MUX_SEL</td><td>DOUBLE_DATA_MODE</td><td>FIFO_LVL SATURATION</td></tr>
<tr><td>0</td><td>0</td><td>256</td></tr>
<tr><td>0</td><td>1</td><td>512</td></tr>
<tr><td>3</td><td>0</td><td>128</td></tr>
<tr><td>3</td><td>1</td><td>256</td></tr>
</table>

FIFO_CONTROL Register (Address 0xF1)

Figure 93:
FIFO_CONTROL Register

Addr: 0xF1		FIFO_CONTROL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0	RW	Reserved. Must be set to default value.
6	FIFO_LVL_LSB	0	R	Contains the LSB of FIFO_LVL when DOUBLE_DATA_MODE is used. See FIFO_LVL for details.
5:3	FIFO_THR_LVL	000	RW	FIFO level threshold. When FIFO_LVL is greater than or equal to FIFO_THR_LVL, FTINT flag is set, and an interrupt is generated if FTIEN is enabled.

Value	FIFO Level Threshold
0	No intermediate levels to generate interrupt. Full FIFO is available.
1	16 (32 when DOUBLE_DATA_MODE=1)
2	32 (64 when DOUBLE_DATA_MODE=1)
3	48 (96 when DOUBLE_DATA_MODE=1)
4	64 (128 when DOUBLE_DATA_MODE=1)
5	80 (160 when DOUBLE_DATA_MODE=1)
6	96 (192 when DOUBLE_DATA_MODE=1)
7	112 (224 when DOUBLE_DATA_MODE=1)

2	FIFO_CLR	0	RW	When this bit is set, the FIFO is cleared, the read and write pointers are reset to 0, any read from FIFO will return 0. It has to be noted that FIFO_CLR doesn't clear FIFO_OVF flag if it's set. It requires a dummy read to FIFO data before or after FIFO_CLR command to clear FIFO_OVF flag. This bit needs to be set when ALS is disabled.
1	FIFO_EMPTY	1	R	Indicates that the FIFO is empty. When FIFO is empty, data read from FIFO returns 0.
0	FIFO_OVF	0	R	Indicates that the FIFO is full. When FIFO is full, no new data is written into the FIFO.

PDATA_L Register (Address 0xF4)

Figure 94:
PDATA_L Register

Addr: 0xF4		PDATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATA_L	0x00	R	If APC is enabled, this register contains the low byte of the 14-bit proximity data. If APC is disabled, this register contains the upper 8 most significant bits of the 10-bit proximity data.

PDATA_H Register (Address 0xF5)

Figure 95:
PDATA_H Register

Addr: 0xF5		PDATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATA_H	0x00	R	If APC is enabled, this register contains the high byte of the 14-bit proximity data. If APC is disabled, bits 1:0 contain the lower 2 bits of the 10-bit proximity value.

Proximity detection uses an Automatic Pulse Control (APC) mechanism that adjusts the number of pulses per measurement based on the magnitude of the reflected IR signal. As the magnitude of the signal increases, the number of pulses decreases.

Dependent on the configurations, proximity data can be stored as a 10-bit, 14-bit, or 16-bit value (two bytes). Reading the low byte first latches the high byte.

When Automatic Pulse Control (APC) is enabled by setting DISABLE_APC=0 (bit6 of CFG6), proximity detection uses a 10-bit ADC that is extended to a 14-bit or 16-bit dynamic range for PDATA.

If ENAB_16_BIT_OP =0, PDATA is a 14-bit value,
PDATA = ADCvalue x (16 / actual number of pulses transmitted);

If ENAB_16_BIT_OP =1, PDATA is a 16-bit value,
PDATA = ADCvalue x (64 / actual number of pulses transmitted);

PDATA is therefore proportional to the reflected energy independent of the number of pulses transmitted.

When Automatic Pulse Control (APC) is disabled by setting DISABLE_APC=1 (bit6 of CFG6), then the proximity data converts to a 10-bit value. PDATAL contains the 8 most significant bits of the 10-bit value and PDATAH bit locations 1:0

contain the lower 2-bits. When APC is disabled, only the upper 8-bits are compared against the threshold values contained in PILTL and PIHTL.

TDATA_L Register (Address 0xF6)

Figure 96:
TDATA_L Register

Addr: 0xF6		TDATA_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	TDATA_L	0x00	R	Temperature ADC data LSB[7:0] Temperature data is stored as a 10-bit value split into two registers. Once PEN =TEN =ENAB_TEMP_SENSOR =1, temperature measurement is activated, and TDATA is updated automatically after every proximity measurement. T(ºC)=(399-TDATA)/1.48

TDATA_H Register (Address 0xF7)

Figure 97:
TDATA_H Register

Addr: 0xF7		TDATA_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	TDATA_H	0x00	R	Temperature ADC data MSB[9:8] See TDATA_L for details.

FIFO_ADATA_7 Register (Address 0xF8)

Figure 98:
FIFO_ADATA_7 Register

Addr: 0xF8		FIFO_ADATA_7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_ADATA_7	0x00	R	FIFO ALS data read out register 7

FIFO_ADATA_6 Register (Address 0xF9)

Figure 99:
FIFO_ADATA_6 Register

Addr: 0xF9		FIFO_ADATA_6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_ADATA_6	0x00	R	FIFO ALS data read out register 6

FIFO_ADATA_5 Register (Address 0xFA)

Figure 100:
FIFIO_ADATA_5 Register

Addr: 0xFA		FIFO_ADATA_5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_ADATA_5	0x00	R	FIFO ALS data read out register 5

FIFO_ADATA_4 Register (Address 0xFB)

Figure 101:
FIFIO_ADATA_4 Register

Addr: 0xFB		FIFO_ADATA_4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_ADATA_4	0x00	R	FIFO ALS data read out register 4

FIFO_ADATA_3 Register (Address 0xFC)

Figure 102:
FIFO_ADATA_3 Register

Addr: 0xFC		FIFO_ADATA_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_ADATA_3	0x00	R	FIFO ALS data read out register 3

FIFO_ADATA_2 Register (Address 0xFD)

Figure 103:
FIFO_ADATA_2 Register

Addr: 0xFD		FIFO_ADATA_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_ADATA_2	0x00	R	FIFO ALS data read out register 2

FIFO_ADATA_1 Register (Address 0xFE)

Figure 104:
FIFO_ADATA_1 Register

Addr: 0xFE		FIFO_ADATA_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_ADATA_1	0x00	R	FIFO ALS data read out register 1

FIFO_ADATA_0 Register (Address 0xFF)

Figure 105:
FIFO_ADATA_0 Register

Addr: 0xFF		FIFO_ADATA_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FIFO_ADATA_0	0x00	R	FIFO ALS data read out register 0

ALS data are stored in FIFO and read out from the register FIFO_ADATA_7 to FIFO_ADATA_0. The data definition is based on the configurations of TWO_CHANN_MODE and DOUBLE_DATA_MODE as described in the following table. Depending on the configurations, reading undefined registers returns zeros. The data values will stay in registers until the FIFO_ADATA0 (0xFF) is read. Whenever the FIFO_ADATA0 (0xFF) is read, the next set of data is updated into all the ADATA registers. For the I^2C block read, when the address hits 0xFF, it wraps back according to the configurations described in the Figure 106.

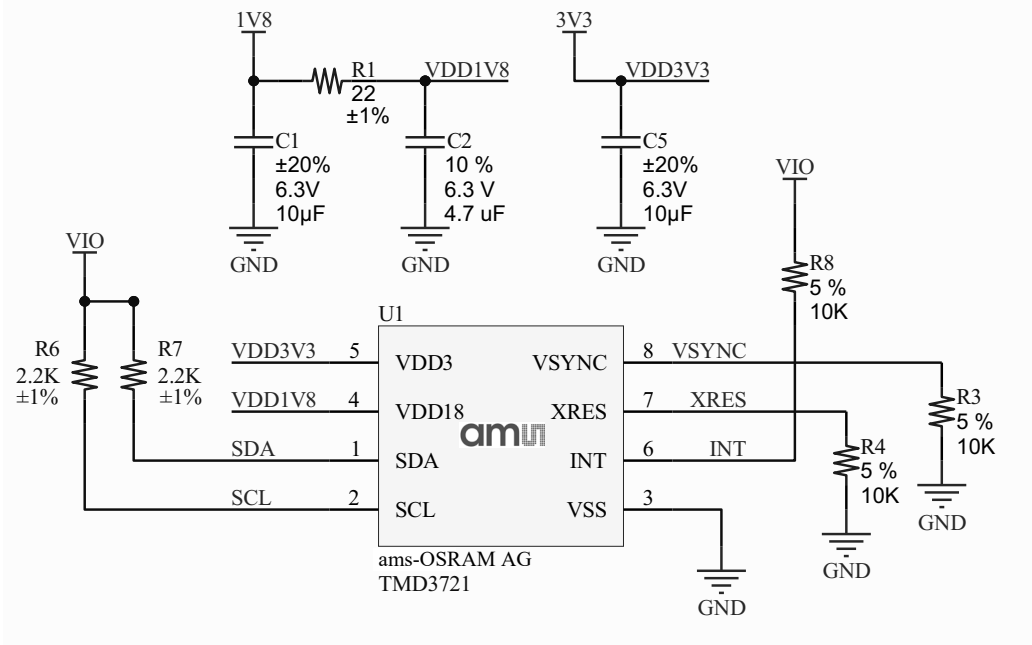
Figure 106:
FIFO ADATA Read Configuration

Register Name	TWO_CHAN_MODE=0 DOUBLE_DATA_MODE=0	TWO_CHAN_MODE=0 DOUBLE_DATA_MODE=1	TWO_CHAN_MODE=1 DOUBLE_DATA_MODE=0	TWO_CHAN_MODE=1 DOUBLE_DATA_MODE=1
FIFO_ADATA_7	BLUE data low byte	Undefined	Undefined	Undefined
FIFO_ADATA_6	BLUE data high byte	Undefined	Undefined	Undefined
FIFO_ADATA_5	GREEN data low byte	Undefined	Undefined	Undefined
FIFO_ADATA_4	GREEN data high byte	Undefined	Undefined	Undefined
FIFO_ADATA_3	RED data low byte	BLUE data (8-bit)	CH1 (R+B) data low byte	Undefined
FIFO_ADATA_2	RED data high byte	GREEN data (8-bit)	CH1 (R+B) data high byte	Undefined
FIFO_ADATA_1	CLEAR data low byte	RED data (8-bit)	CH0 (C+G) data low byte	CH1 (R+B) data (8-bit)
FIFO_ADATA_0	CLEAR data high byte	CLEAR data (8-bit)	CH0 (C+G) data high byte	CH0 (C+G) data (8-bit)

Application Information

Schematic

Figure 107:
TMD3721 Typical Application Circuit

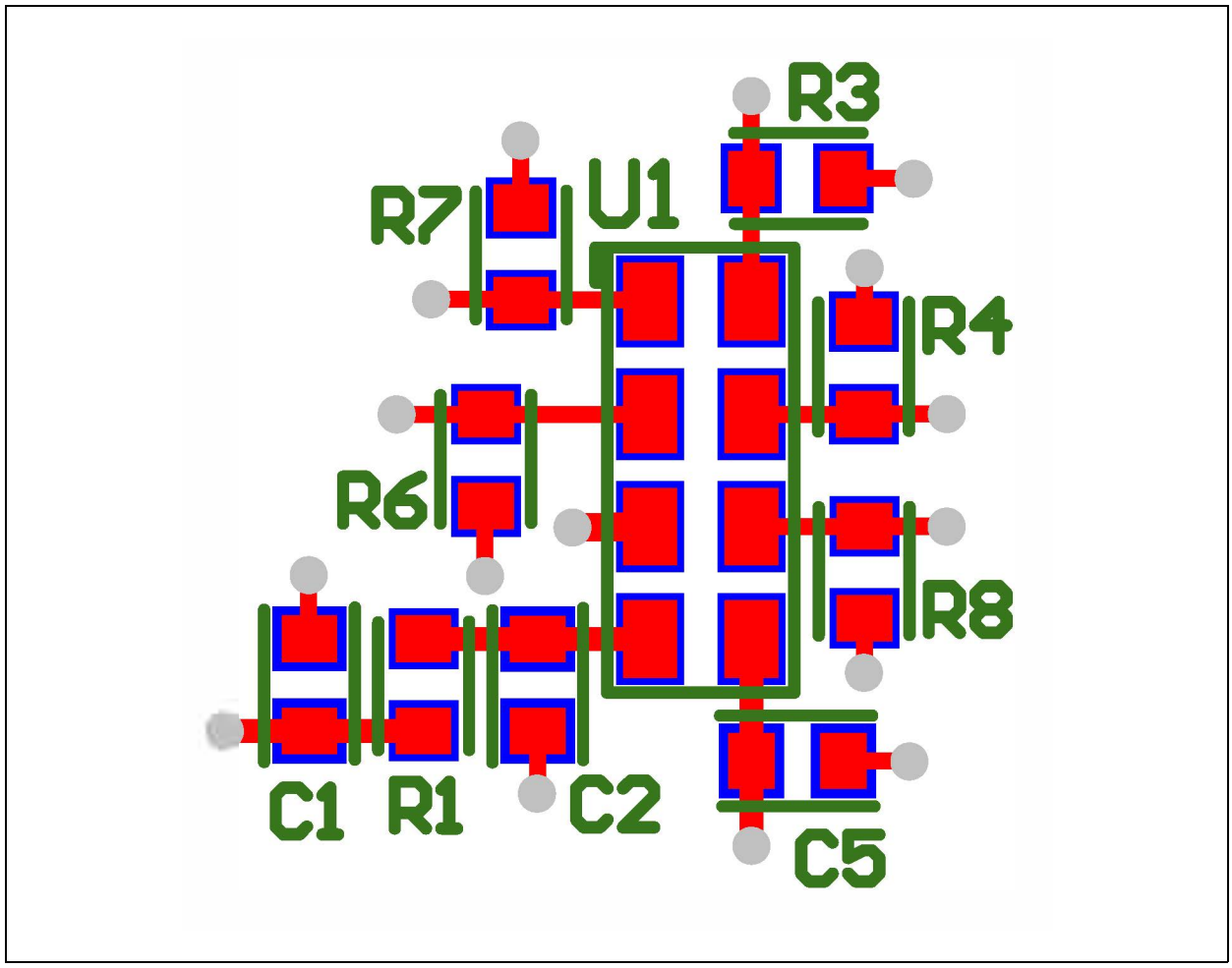


Note(s):

1. Place VDD18 filter (R1, C1, C2) and VDD3 filter (C5) as close as possible to the module.
2. The value of the I²C pull up resistors (R6, R7) should be based on the bus voltage, system bus speed and trace capacitance.
3. R1, C1, C2, C5 are critical components to protect the device during high voltage ESD strikes.
4. In systems subjected to high voltage ESD strikes, it is recommended to connect XRES to a host GPIO pin to allow the device reset.

Recommended Circuit Layout

Figure 108:
TMD3721 Recommended Circuit Layout

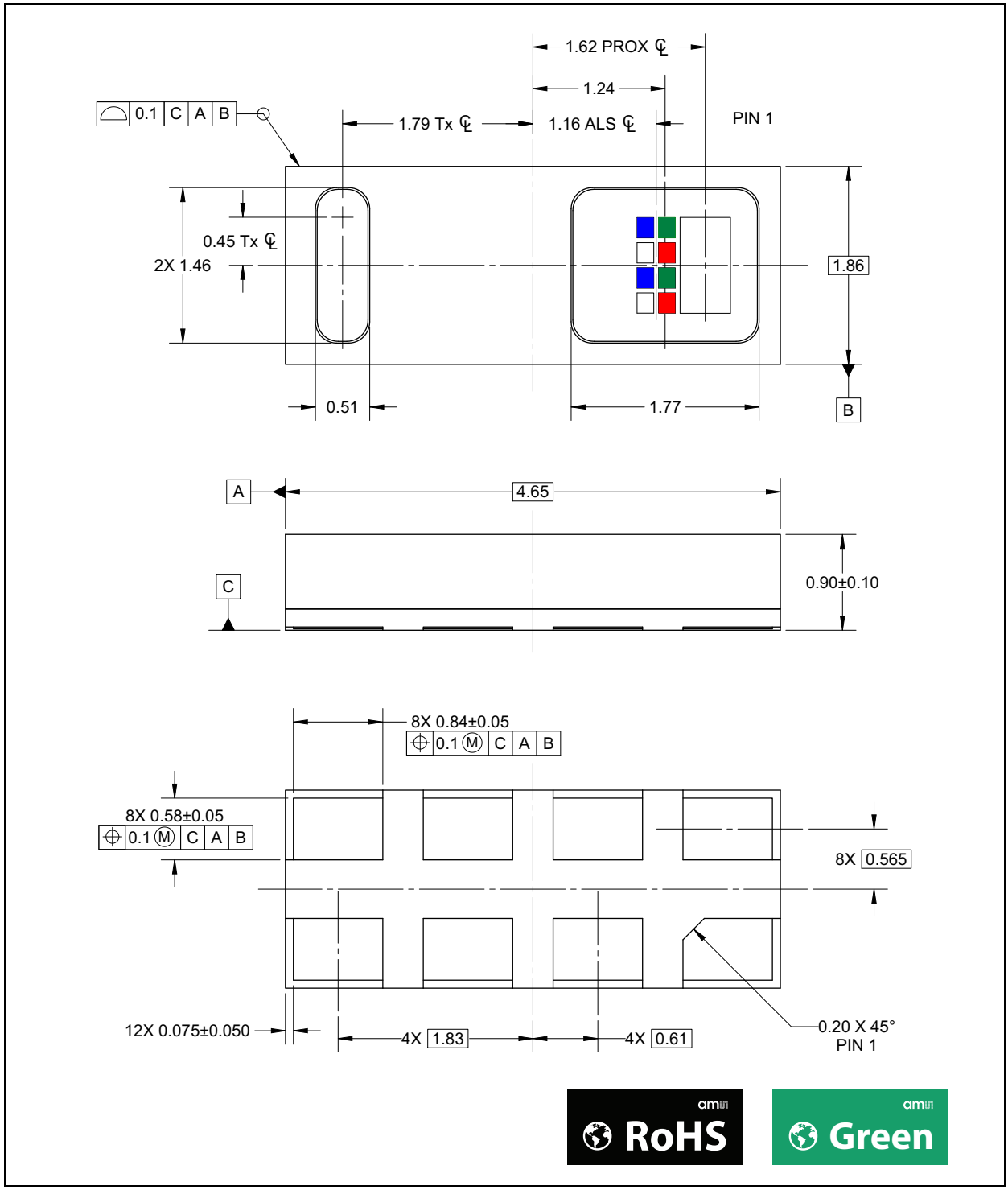


Note(s):

1. The placement of the decoupling capacitors are critical. Place the components on the same side of PCB as device as shown in the figure above. Make connections as close as possible to minimize series inductance and resistance.

Package Drawings & Markings

Figure 109:
TMD3721 Package Drawings



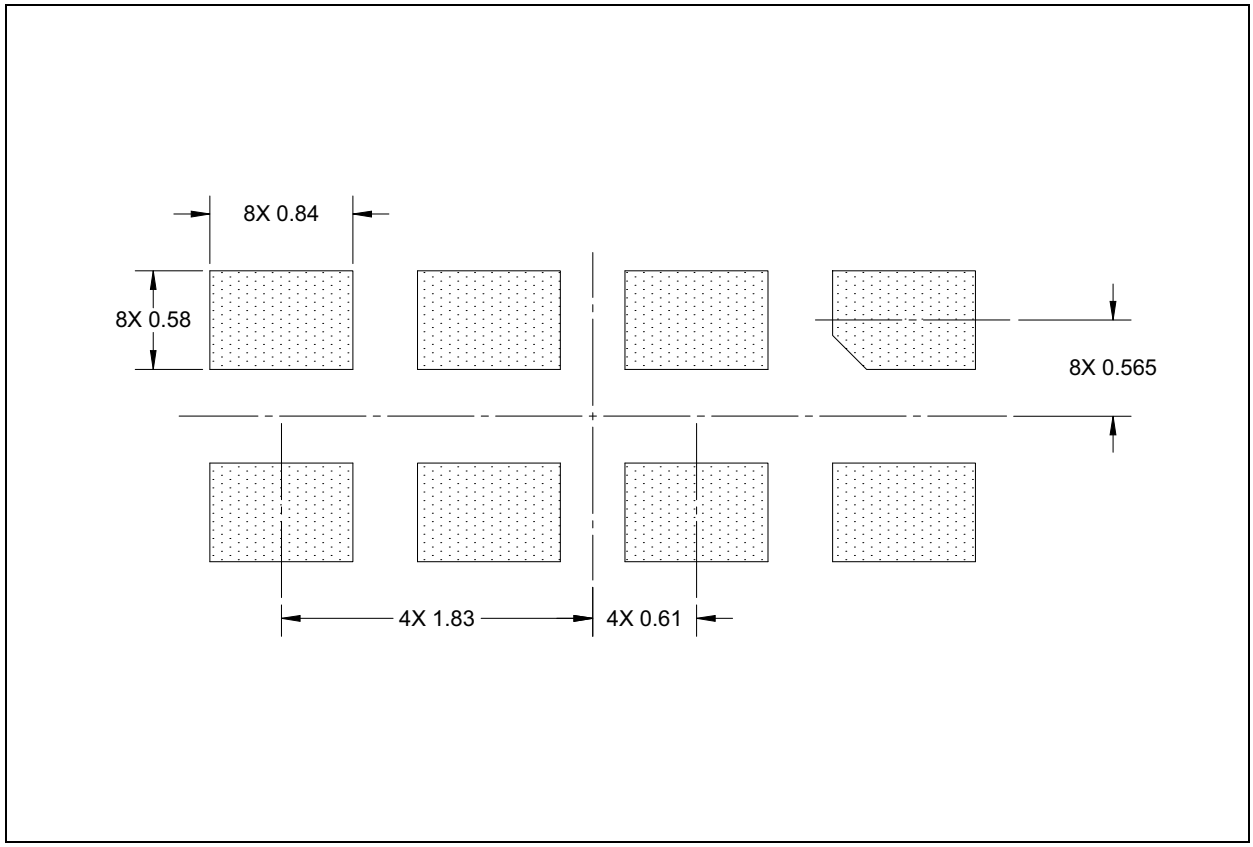
Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. Contact finish is Au.
4. This package contains no lead (Pb).
5. This drawing is subject to change without notice.

Recommended PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 110:
Recommended PCB Pad Layout

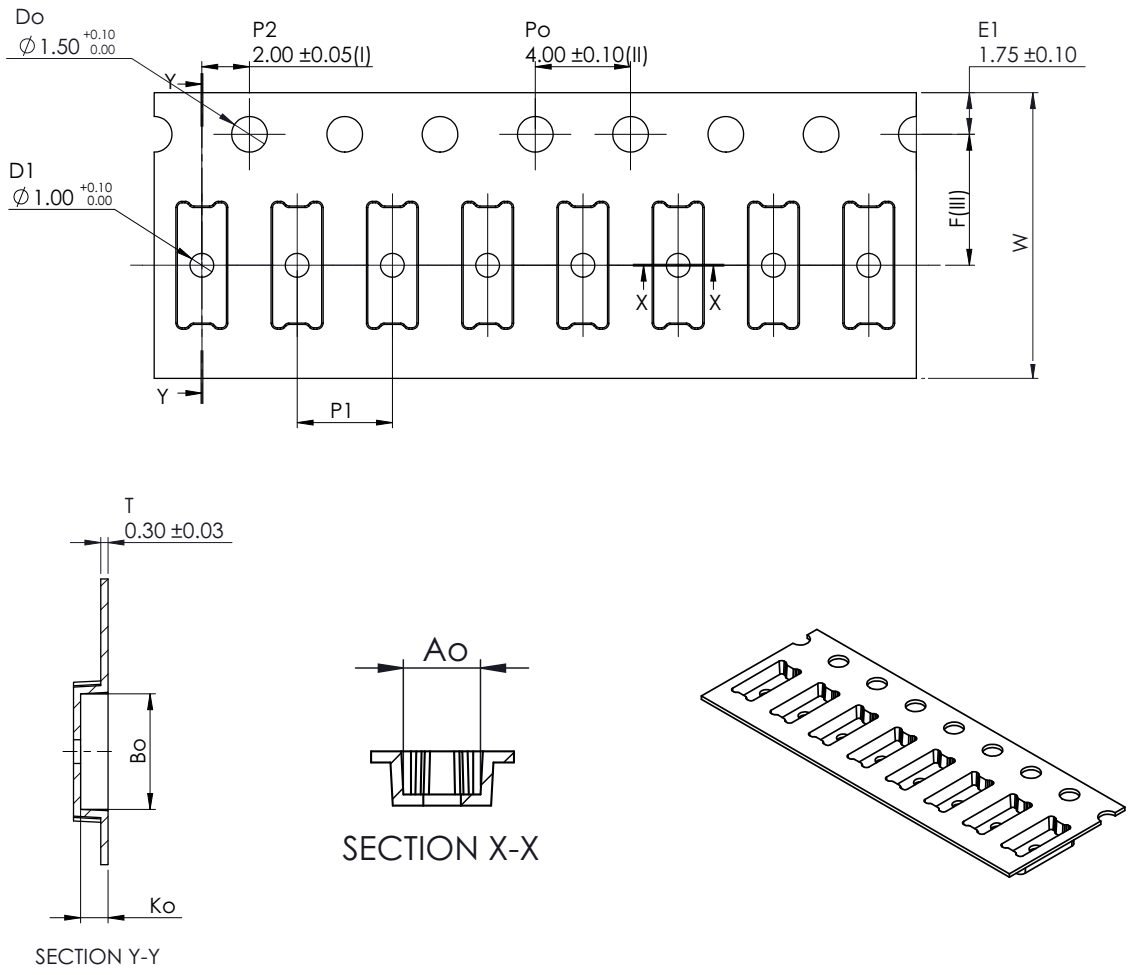


Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are 0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

Tape & Reel Information

Figure 111:
TMD3721 Tape and Reel Information



Ao	2.06	+/- 0.05
Bo	4.85	+/- 0.05
Ko	1.15	+/- 0.10
F	5.50	+/- 0.05
P1	4.00	+/- 0.10
W	12.00	+0.30/-0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension with ( ) is used for design reference purposes, No measurement required.

Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481-B 2001
4. ams OSRAM packaging tape and reel conform to the requirements of EIA Standard 481-B.
5. In accordance with EIA standard device pin 1 is located next to the sprocket holes in the tape.
6. This drawing is subject to change without notice.

Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

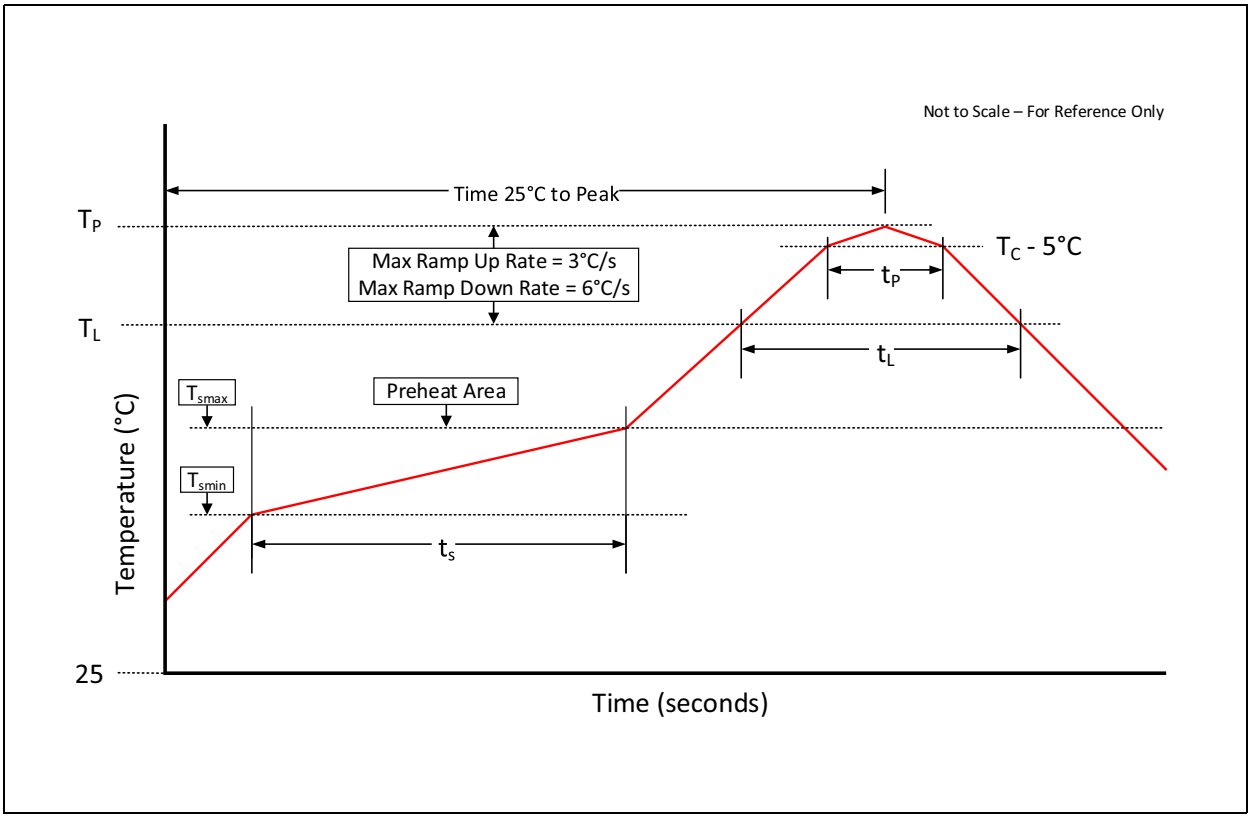
Figure 112:
Solder Reflow Profile

Profile Feature Preheat/ Soak	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Temperature Min (T_{smin})	100 °C	150 °C
Temperature Max (T_{smax})	150 °C	200 °C
Time (t_s) from (T_{smin} to T_{smax})	60-120 s	60-120 s
Ramp-up rate (T_L to T_P)	3 °C/s max.	3 °C/s max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 s	217 °C 60-150 s
Peak package body temperature (T_P)	For users T_P must not exceed the classification temp. of 235 °C. For suppliers T_P must equal or exceed the classification temp. of 235 °C	For users T_P must not exceed the classification temp. of 260 °C. For suppliers T_P must equal or exceed the classification temp. of 260 °C
Time (t_P)[(1)] within 5 °C of the specified classification temperature (T_c)	20[(1)] s	30[(1)] s
Ramp-down rate (T_P to T_L)	6 °C/s max.	6 °C/s max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note(s):

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

Figure 113:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 24 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

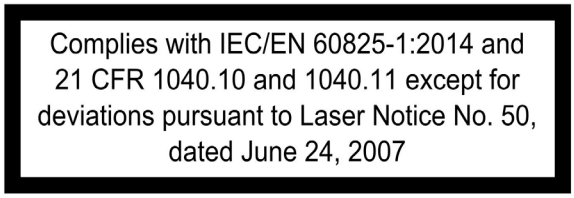
- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Laser Eye Safety



The TMD3721 is designed to meet the Class 1 laser safety limits including single faults in compliance with IEC/EN 60825-1:2014. In an end application system environment, the system may need to be tested to ensure it remains compliant. The system must not include any additional lens to concentrate the laser light or parameters set outside of the recommended operating conditions or any physical modification to the module during development could result in hazardous levels of radiation exposure.

Ordering & Contact Information

Figure 114:
Ordering Information

Ordering Code	I²C Bus	I²C Address	Delivery Form	Delivery Quantity
TMD37213	1.8V	0x39	Tape & Reel (13”)	10000 pcs/reel
TMD37213M	1.8V	0x39	Tape & Reel (7”)	1000 pcs/reel

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
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Revision Information

Changes from 2-00 (2021-Oct-12) to current revision 3-00 (2023-May-26)	Page
Document security class changed to “Public” from “Confidential”	
Updated figure 8	7
Updated figure 9	9
Added “I^2C Timing Characteristics”	19
Updated Register Map and added description for 0x9E and 0x9F registers	21, 39
Updated description for ENABLE register	26
Updated description for PERS register	31
Updated AUX_ID	36
Updated VSYNC_WD_TH	48
Updated “Shelf Life” to 24 months	79
Updated “Rebaking Instructions”	80
Updated Ordering Information	81

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide