

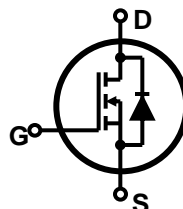
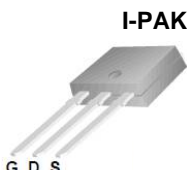
Features

- Low gate charge
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant
- Halogen free package
- JEDEC Qualification

$$V_{DSS} = 880 \text{ V} @ T_{jmax}$$

$$I_D = 3 \text{ A}$$

$$R_{DS(on)} = 4.2 \Omega(\text{max}) @ V_{GS} = 10 \text{ V}$$



Device	Package	Marking	Remark
TMD3N80G/TMU3N80G	D-PAK/I-PAK	TMD3N80G/TMU3N80G	Halogen Free

Absolute Maximum Ratings

Parameter	Symbol	TMD3N80G/TMU3N80G	Unit
Drain-Source Voltage	V_{DSS}	800	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	$T_C = 25 \text{ }^\circ\text{C}$	3
		$T_C = 100 \text{ }^\circ\text{C}$	1.83
Pulsed Drain Current (Note 1)	I_{DM}	12	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	283	mJ
Repetitive Avalanche Current (Note 1)	I_{AR}	3	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	9.4	mJ
Power Dissipation	P_D	$T_C = 25 \text{ }^\circ\text{C}$	94
		Derate above $25 \text{ }^\circ\text{C}$	0.75
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	T_L	300	$^\circ\text{C}$

* Limited only by maximum junction temperature

Thermal Characteristics

Parameter	Symbol	TMD3N80G/TMU3N80G	Unit
Maximum Thermal resistance, Junction-to-Case	$R_{\theta JC}$	1.33	$^\circ\text{C}/\text{W}$
Maximum Thermal resistance, Junction-to-Ambient	$R_{\theta JA}$	110	$^\circ\text{C}/\text{W}$

Electrical Characteristics : $T_C=25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test condition	Min	Typ	Max	Units
OFF						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	800	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 640\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
Forward Gate-Source Leakage Current	I_{GSSF}	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
Reverse Gate-Source Leakage Current	I_{GSSR}	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

ON

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	--	4	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$	--	3.36	4.2	Ω
Forward Transconductance ^(Note 4)	g_{FS}	$V_{DS} = 30\text{ V}, I_D = 1.5\text{ A}$	--	3.7	--	S

DYNAMIC

Input Capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	696	--	pF
Output Capacitance	C_{oss}		--	65	--	pF
Reverse Transfer Capacitance	C_{rss}		--	10.2	--	pF

SWITCHING

Turn-On Delay Time ^(Note 4,5)	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 3\text{ A},$ $R_G = 25\ \Omega$	--	48	--	ns
Turn-On Rise Time ^(Note 4,5)	t_r		--	36	--	ns
Turn-Off Delay Time ^(Note 4,5)	$t_{d(off)}$		--	106	--	ns
Turn-Off Fall Time ^(Note 4,5)	t_f		--	41	--	ns
Total Gate Charge ^(Note 4,5)	Q_g	$V_{DS} = 640\text{ V}, I_D = 3\text{ A},$ $V_{GS} = 10\text{ V}$	--	19	--	nC
Gate-Source Charge ^(Note 4,5)	Q_{gs}		--	4	--	nC
Gate-Drain Charge ^(Note 4,5)	Q_{gd}		--	7.6	--	nC

SOURCE DRAIN DIODE

Maximum Continuous Drain-Source Diode Forward Current	I_S	----	--	--	3	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}	----	--	--	12	A
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 3\text{ A}$	--	--	1.5	V
Reverse Recovery Time ^(Note 4)	t_{rr}	$V_{GS} = 0\text{ V}, I_S = 3\text{ A}$	--	372	--	ns
Reverse Recovery Charge ^(Note 4)	Q_{rr}	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	1.8	--	μC

Note :

1. Repeated rating : Pulse width limited by safe operating area
2. $L = 59\text{ mH}, I_{AS} = 3\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega,$ Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 3\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DS},$ Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s},$ Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

