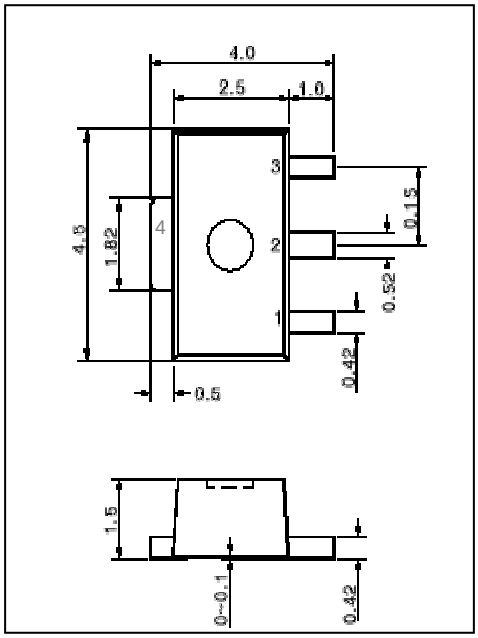
AUK Semiconductor

TMF8901F

Si RF LDMOS Transistor

SOT-89 **Unit in mm**



☐ *Applications*

- VHF and UHF wide band amplifier

☐ *Features*

- Power gain

G_P = 12.5 dB at V_{DS} = 4.5 V, I_{Dset} = 200 mA, f = 470 MHz

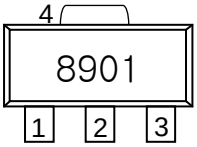
- Output power

P_{OUT} = 32 dBm at V_{DS} = 4.5 V, I_{Dset} = 200 mA, f = 470 MHz

- Drain efficiency

η_D = 60 % (typ.)

☐ *Marking*



Pin Configuration

1. Gate
2. Source
3. Drain
4. Source

☐ *Absolute Maximum Ratings* (T_A = 25 ℃)

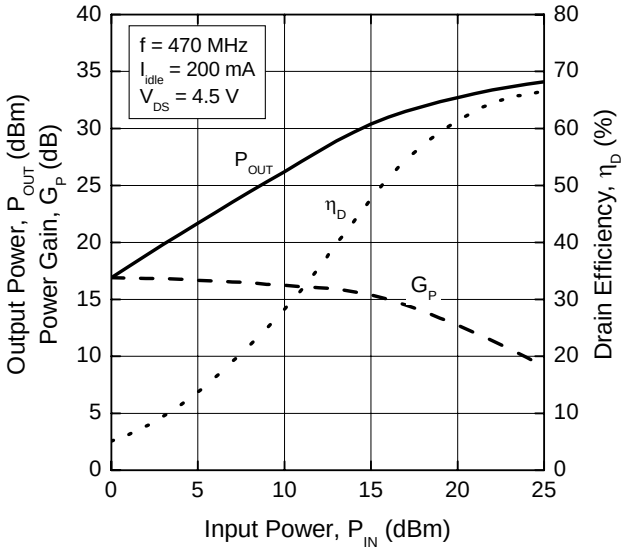
Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	13.0	V
Gate to Source Voltage	V_{GS}	4.0	V
Drain Current	I_D	1.2	A
Total Power Dissipation	P_{tot}	3	W
Channel Temperature	Tch	150	℃
Storage Temperature	T_{stg}	-65 ~ 150	℃

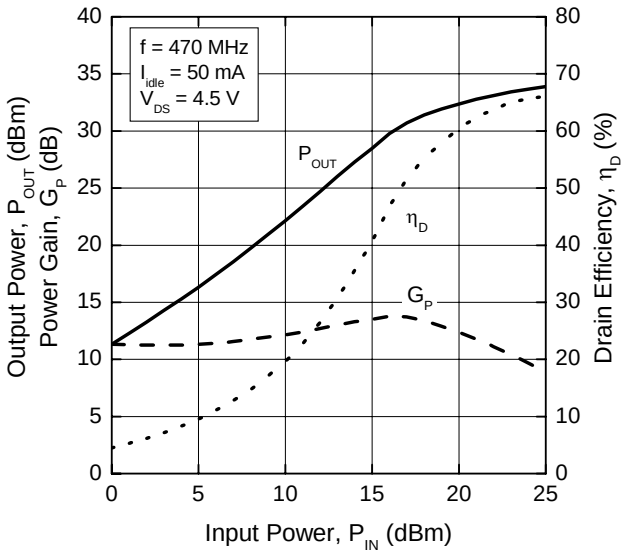
☐ *Electrical Characteristics* (T_A = 25 ℃)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Gate to Source Leakage Current	I_{GSS}	V_{GSS} = 3.0 V			1	μA
Drain to Source Leakage Current	I_{DSS}	V_{DSS} = 8.5 V, V_{GS} = 0 V			10	μA
Threshold Voltage	V_{th}	V_{DS} = 4.8 V, I_D = 1 mA	0.8	1.0	1.4	V
Transconductance	G_m	V_{DS} = 4.8 V, I_D = 400 mA		700		mS
Drain to Source Breakdown Voltage	BV_{DSS}	I_{DSS} = 10 μA	13			V
Drain to Source On-Voltage	V_{DSon}	V_{GS} = 4 V, I_D = 600 mA		0.4		V
Power Gain	G_P	f = 470 MHz, P_{IN} = 20 dBm V_{DS} = 4.5 V, I_{Dset} = 200 mA		12.5		dB
Output Power	P_{OUT}	f = 470 MHz, P_{IN} = 20 dBm V_{DS} = 4.5 V, I_{Dset} = 200 mA		32		dBm
Operating Current	I_{op}			670		mA
Drain Efficiency	η_D			60		%
Power Gain	G_P	f = 470 MHz, P_{IN} = 15 dBm V_{DS} = 4.5 V, I_{Dset} = 50 mA		14		dB
Output Power	P_{OUT}	f = 470 MHz, P_{IN} = 15 dBm V_{DS} = 4.5 V, I_{Dset} = 50 mA		29		dBm
Operating Current	I_{op}			400		mA
Drain Efficiency	η_D			44		%

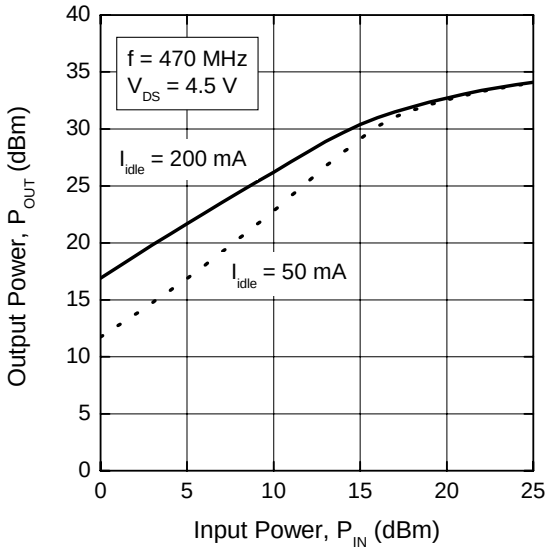
□ *Typical Characteristics (T_A = 25 ℃, unless otherwise specified)*

Output Power, Power Gain, Drain Efficiency vs. Input Power

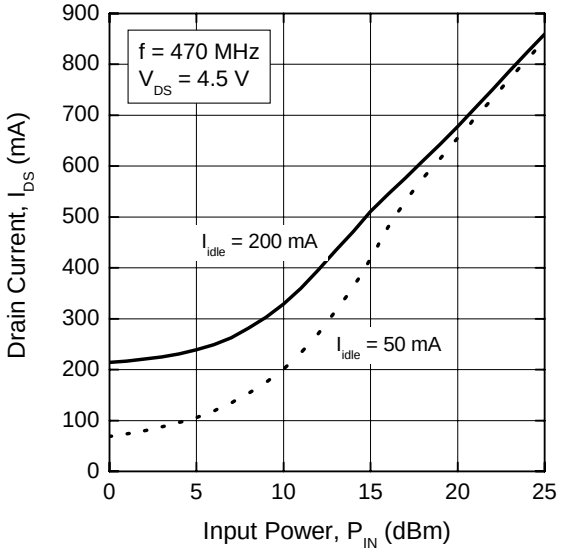




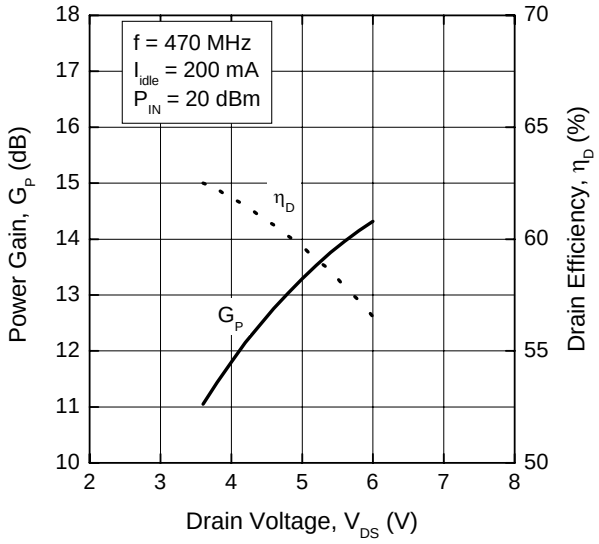
Output Power vs. Input Power



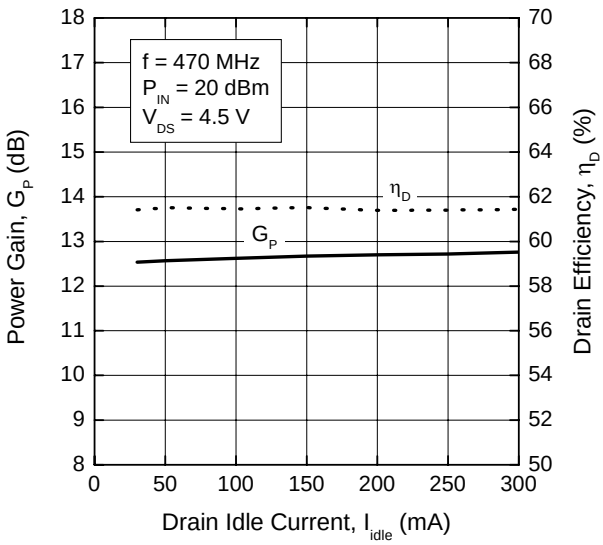
Drain Current vs. Input Power



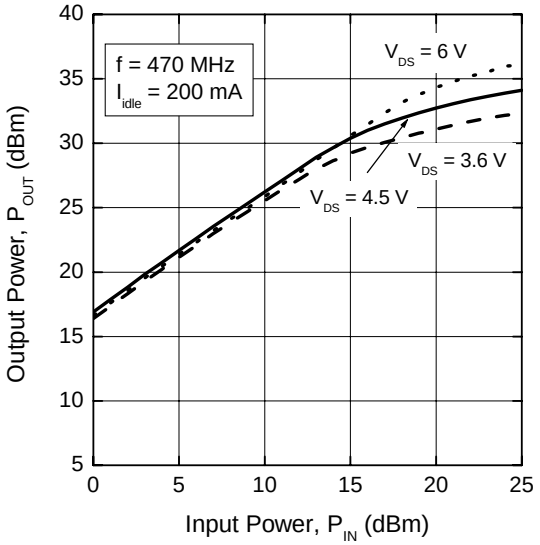
Power Gain, Drain Efficiency vs. Drain Voltage



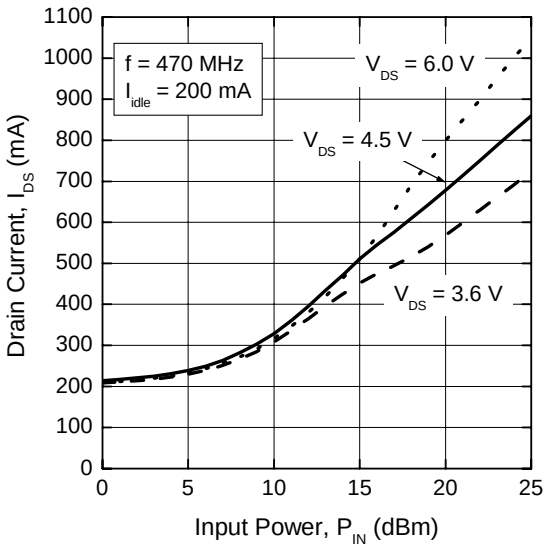
Power Gain, Drain Efficiency vs. Drain Current



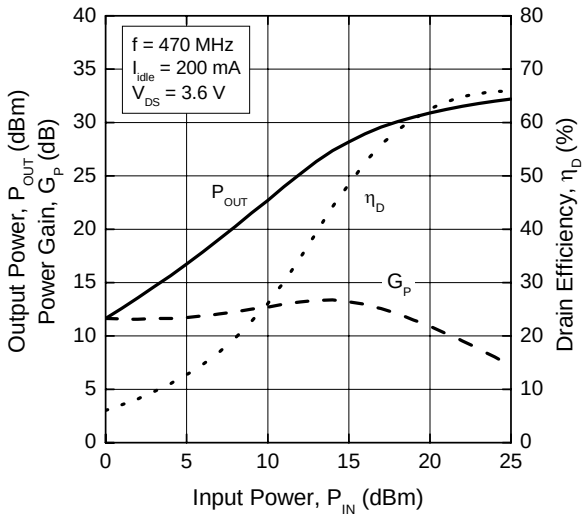
Output Power vs. Input Power

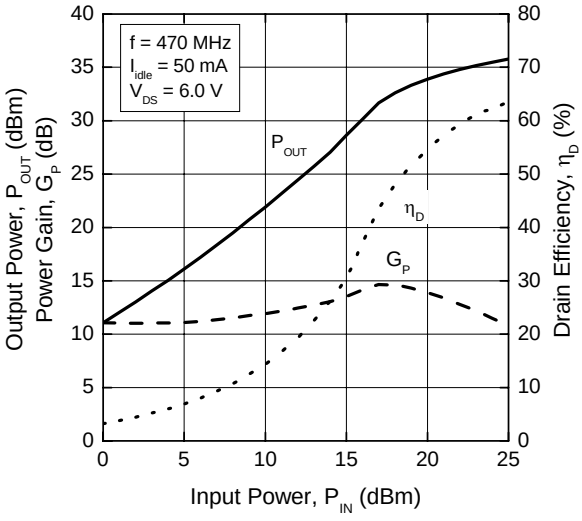


Drain Current vs. Input Power

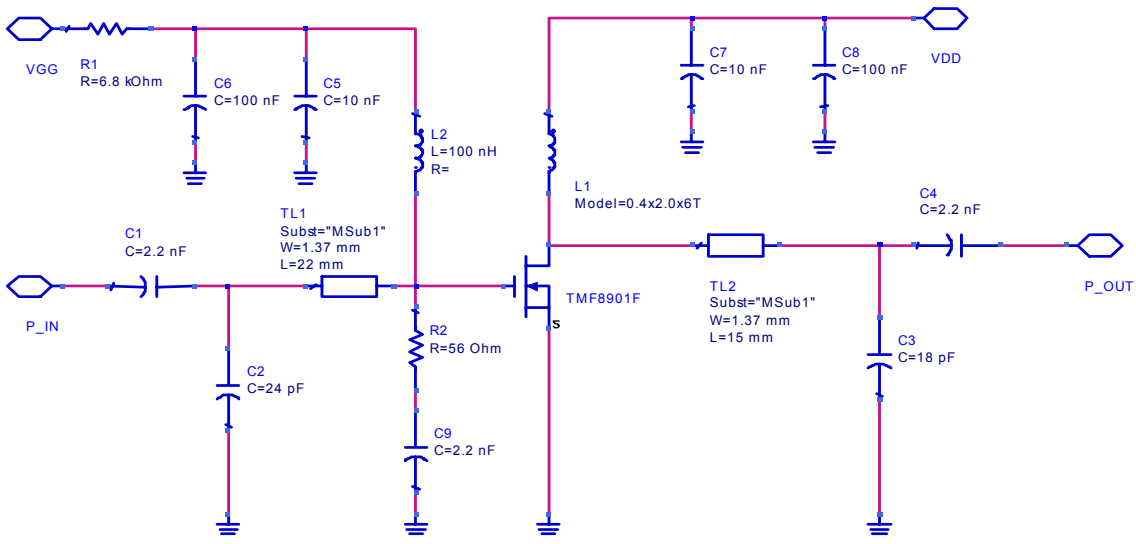


Output Power, Power Gain, Drain Efficiency vs. Input Power





☐ *Test Circuit Schematic Diagram*



Test Board : 0.8mm FR4 glass epoxy