TMI8721-Q1 Automotive Single-Channel Smart Gate Driver

Product Features

ÿ AEC-Q100 compliant for automotive applications:

– Temperature Grade 1: –40°C to +125°C, TA

ÿ 5.5V to 38V operating voltage range

ÿ Single channel H-bridge gate driver

– Drives 4 external N-MOSFETs

– Support 100% PWM

ÿ Three control modes available

- PWM

– PH/EN

– Independent half-

bridge ÿ Gate drive capability

– Peak drive source current: 10mA to 220mA – Peak drive sink

current: 20mA to 440mA

ÿ Integrated current sampling and regulation

– Sampling gain adjustable: 10, 20, 40, 80 V/V

ÿ Support 1.8V, 3.3V, 5V logic input

ÿ Ultra-low power sleep mode

ÿ Protection features

– VM undervoltage lockout (UVLO) –

Charge pump undervoltage protection (CPUV)

– VDS Over Current Protection (OCP)

– VGS Gate Fault Protection (GDF) –

Watchdog Timer – Fault

Indication Pin (nFAULT) – Thermal

Shutdown (TSD) ÿ

Package Size

– QFN5x5-32

application

ÿ Automotive brushed DC motor

ÿ Seat module

ÿ Electric lifting window

ÿ Electric sunroof

Product Overview

The TMI8721-Q1 is an integrated single-channel H-bridge gate driver that drives a brushed DC motor using four external N-MOSFETs.

The TMI8721-Q1 input control modes provide PWM, PH/EN, and independent half-bridge. The independent bridge mode can control multiple DC motors simultaneously. The integrated charge pump supports 100% duty cycle. The internal sensing amplifier provides adjustable current control, and the corresponding circuit is built in to achieve PWM current chopping with fixed off time to regulate the motor winding current.

The TMI8721-Q1 provides a range of protection features including VM undervoltage protection, charge pump undervoltage protection, VDS overcurrent protection and VGS gate fault protection for the external MOSFET, and internal thermal shutdown.

The package is QFN 5mmx5 mm, with exposed pads to enhance heat dissipation. It complies with ROHS regulations and the lead frame is 100% lead-free.

Typical application circuit

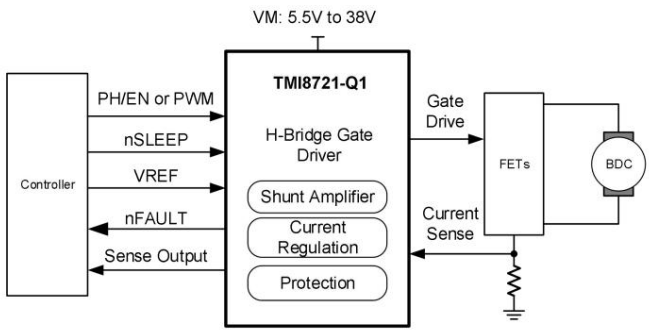


Figure **1.** Typical application circuit diagram

Absolute Maximum Ratings(1)

Parameter		Min	Max	Unit
Driver supply voltage (VM, VDRAIN) Drain	VM	-0.3	40	V
pin voltage (VDRAIN) Charge	VDRAIN	-0.3	40	V
pump voltage (VCP)	VVCP	-0.3	52	V
Internal digital regulator voltage (DVDD)	VDVDD	-0.3	5.75	V
Internal analog regulator voltage (AVDD)	VAVDD	-0.3	3.8	V
Logic input voltage (IN1, IN2, nSLEEP, nFAULT, VREF, MODE, nSCS, SCLK, SDI, SDO, nWDFLT)	COME	-0.3	5.75	V
High-side gate drive pin voltage (GHx) Low-	VGHx	-0.3	52	V
side gate drive pin voltage (GLx) High-side	VGLx	-0.3	12	V
source voltage (OUTx)	VOUTx	-1.2	40	V
Amplifier input pin voltage (SP, SL2, SN)	VSP, VSL2	-0.5	1.2	V
	VSN	-0.3	0.3	V
Amplifier output pin voltage (SO) Amplifier	ALL	-0.3	5.75	V
output pin current (SO) Operating ambient	ISO	0	5	mA
temperature Junction	FACING	-40	125	°C
temperature (2)	TJ	-40	150	°C
Storage temperature	Tstg	-60	150	°C

(1) Absolute Maximum Ratings are those values at which the life of the device may be impaired. Stresses beyond the Absolute Maximum Ratings may cause permanent damage to the device.

Extended operation at absolute maximum rating conditions may affect device reliability.

(2) TJ is calculated from the ambient temperature TA and the power dissipation PD according to the following formula: TJ = TA + PD x ÿJA. The maximum allowable continuous

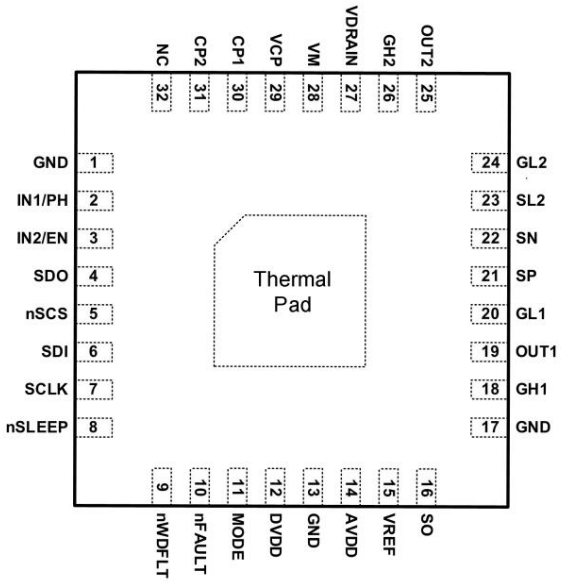
The continuous power dissipation is calculated by PD (MAX) = (TJ(MAX) - TA) / ÿJA.

ESD Level

parameter		value	unit
THROW IT	Description Human Body Model HBM, AEC	±2000	V
	Q100-002(1) Charged Device Model CDM, AEC Q100-011	±750	V

(1) AEC Q100-002 states that HBM stress should comply with ANSI/ESDA/JEDEC JS-001 specification.

Package pin definition



QFN5x5-32

Order Information

Product model packaging type silk screen			Packing quantity
TMI8721-Q1	QFN5x5-32	TMI8721-Q1 XXXXX	5000/plate

The TMI8721-Q1 product meets the lead-free requirements and RoHS standards.

Pin Function

Pin No.	Pin Name	**Input/Output**	describe
1ÿ13ÿ17	GND	-	Systematically.
2	IN1/PH	Input control pin. The logic of this pin depends on the MODE pin. Internal pull-down	
3	IN2/EN	Input resistance.	
4	SDO	Output	SPI - Serial data output. Data is updated on the rising edge of SCLK. Internal pull-up resistor.
5	nSCS	enter	SPI - Chip Select. An active low signal on this pin enables the serial interface Oral communication.
6	SDI	Input SPI - Serial Data In. Data is captured on the falling edge of SCLK.	
7	SCLK	Input SPI - Serial Clock Input.	
8	nSLEEP	Input enable pin. Logic low puts the device into sleep mode.	
9	nWDFLT	Open Drain	Watchdog fault indication pin. When a watchdog fault is detected, this pin is pulled Low. External pull-up resistor required.
10	nFAULT	Open Drain	Fault indication pin. When a fault is detected, this pin is pulled low. Pull resistor.
11	MODE	enter	Mode control pin. This pin is locked at power-up or when exiting sleep mode. Internal pull-up and pull-down resistors.
12	DVDD	Output	Digital regulator. 3.3V logic power regulator. Connect this pin to GND. Connect a 6.3V, 1µF ceramic capacitor.
14	DEPARTMENT	Output	Analog Regulator. 5V analog power regulator. Connect this pin to GND. A 6.3V, 1µF ceramic capacitor.
15	VREF	Enter the reference input voltage.	
16	SO	Output Current Sense Amplifier Output.	
18	GH1	Output High-side gate drive output. Connect to the gate of the high-side MOS.	
19	OUT1	Output high-side source. Connect to the source of the high-side MOS.	
20	GL1	Output Low-side gate drive output. Connect to the gate of the low-side MOS.	
21	SP	Input amplifier positive input. Connect to one end of the sampling resistor.	
22	SN	Input amplifier negative input. Connect to one end of the sampling resistor.	
23	SL2	- Low-Side Source. Connect to the source of the low-side MOS.	
24	GL2	Output Low-side gate drive output. Connect to the gate of the low-side MOS.	
25	OUT2	Output high-side source. Connect to the source of the high-side MOS.	
26	GH2	Output High-side gate drive output. Connect to the gate of the high-side MOS.	
27	VDRAIN	Input high-side drain connection. Common for both half-bridges.	
28	VM	enter	Power input. Connect a 0.1µF ceramic capacitor to GND and a A capacitor of at least 22µF is required.
29	VCP	Input/Output Charge Pump Output. Connect a 1µF ceramic capacitor from this pin to VM.	
30	CP1	Input/output charge pump switching node. Connect a 0.1µF ceramic resistor between CP1 and CP2.	
31	CP2	Input/output ceramic capacitors.	
32	NC	-	No connection.

Recommended operating conditions

parameter	symbol	Minimum	maximum	unit
Operating voltage	VM	5.5	38	V
range Logic input	COME	0	5.5	V
voltage Reference	VREF	0.3(1)	3.6	V
input voltage Logic operating frequency range (IN1/IN2)	f(PWM)		100	kHz
AVDD Load Capacity	IAVDD	0	30(2)	mA
DVDD Load Capacity	IDVDD	0	30(2)	mA
Operating Ambient	FACING	-40	125	°C

Temperature (1) When operating at VREF = 0 to about 0.3V, the accuracy will be reduced;

(2) Comply with power consumption and heat dissipation limits;

Thermal performance parameters

Thermal Indicators	TMI8721-Q1 QFN5x5-32 32 PINS	unit
RÿJ Junction-to-ambient thermal resistance	33.5	°C/W
RÿJC(top) junction to case (top) thermal resistance	20.1	°C/W
RÿJB Junction-to-Board Thermal Resistance	7.0	°C/W
ÿJT Junction-Top Characterization Parameters	0.35	°C/W
ÿJB Connected to Board Characterization Parameters	7.0	°C/W
RÿJC(bot) junction to case (bottom) thermal resistance	1.95	°C/W

Electrical characteristics parameters

Unless otherwise specified, TA **= 25°C.**

	symbol	condition	Min.	Typ.	Max.	Unit
Parameters **Power supply parameters (VM, DVDD, AVDD, VCP)**						
VM operating voltage	EIA	Driver module working	5.5		38	V
		Digital module operation	4.5		38	
VM operating current	IVM	VM = 13.5V, nSLEEP=1	3	5	7	mA
VM sleep current	IVMS DRAG	VM = 13.5V, nSLEEP=0, TA=25°C			2	µA
		VM = 13.5V, nSLEEP=0, TA=125°C			10	
Internal digital regulator voltage	VDVDD	2mA load	3	3.3	3.5	V
		30mA load, VM = 13.5 V	2.9	3.2	3.5	
Internal analog regulator voltage	VAVDD	2mA load	4.7	5	5.3	V
		30mA load, VM = 13.5 V	4.6	5	5.3	
Charge Pump (VCP, CP2, CP1)						
VCP Voltage	VVCP	VVM = 13.5 V; IVCP = 0 to 12 mA	22.5	23.5	24.5	
		VVM = 8 V; IVCP = 0 to 10 mA	13.7	14	14.8	V
		VVM = 5.5 V; IVCP = 0 to 8 mA	8.9	9.1	9.5	
VCP Load Capacity	IVCP	VVM > 13.5 V	12			mA
		8 V < VVM < 13.5 V	10			
		5.5 V < VVM < 8 V	8			
Charge pump frequency	fs(VCP)			90		kHz
Sleep time	tsleep	nSLEEP = 0 V to sleep mode			100	µs
Wake-up time	his	nSLEEP = 5 V to operating mode			1	ms
Logic input parameters (IN1/PH, IN2/EN, nSLEEP, MODE, nSCS, SCLK, SDI)						
Input low level	WILL		0		0.8	V
Input high level	HIV		1.5		5	V
Input hysteresis	VHYS		100			mV
Input low level current	IIL	VIN = 0V	-5		5	ÿA
Input high level current	IIH	VIN = 5V			50	ÿA
Pull-down resistor	RPD	IN1/PH, IN2/EN, nSLEEP, nSCS, SCLK, SDI		100		kÿ
		MODE		65		kÿ
Pull-up resistor	RPU MODE			48		kÿ
Open-drain output parameters **(nFAULT, nWDFLT, SDO)**						
Output low level voltage	VOL	I = 2 mA			0.5	V
Output high level current	IOD	VOD = 5V	-2		2	ÿA

Electrical characteristics parameters (continued)

Unless otherwise specified, TA **= 25°C.**

parameter	symbol	condition	Min.	Typ.	Max.	Unit
Gate drive parameters (GH1, **GH2, GL1, GL2)**						
High side VGS voltage	VGSH	VVM > 13.5 V; VGSH with respect to OUTx			10.5	V
		VVM = 8 V; VGSH with respect to OUTx			6.9	
		VVM = 5.5 V; VGSH with respect to OUTx			4.3	V
Low side VGS voltage	VGSL	VVM > 10.5 V			10.5	V
		VVM < 10.5 V			EIA	
High side peak drive current (SOURCE)	IDRIVE(SRC_ HS)	IDRIVE = 3'b000			10	mA
		IDRIVE = 3'b001			20	
		IDRIVE = 3'b010			50	
		IDRIVE = 3'b011			70	
		IDRIVE = 3'b100			100	
		IDRIVE = 3'b101			150	
		IDRIVE = 3'b110			200	
		IDRIVE = 3'b111			240	
High side peak drive current (SINK)	IDRIVE(SRC_ HS)	IDRIVE = 3'b000			20	mA
		IDRIVE = 3'b001			40	
		IDRIVE = 3'b010			95	
		IDRIVE = 3'b011			130	
		IDRIVE = 3'b100			180	
		IDRIVE = 3'b101			280	
		IDRIVE = 3'b110			380	
		IDRIVE = 3'b111			460	
Low side peak drive current (SOURCE)	IDRIVE(SRC_ HS)	IDRIVE = 3'b000			10	mA
		IDRIVE = 3'b001			20	
		IDRIVE = 3'b010			45	
		IDRIVE = 3'b011			70	
		IDRIVE = 3'b100			90	
		IDRIVE = 3'b101			130	
		IDRIVE = 3'b110			180	
		IDRIVE = 3'b111			225	

Electrical characteristics parameters (continued)

Unless otherwise specified, TA **= 25°C.**

parameter	symbol	condition	Min.	Typ.	Max.	Unit
Low side peak drive current (SINK)	IDRIVE(SRC_ HS)	IDRIVE = 3'b000			20	mA
		IDRIVE = 3'b001			40	
		IDRIVE = 3'b010			95	
		IDRIVE = 3'b011			130	
		IDRIVE = 3'b100			180	
		IDRIVE = 3'b101			280	
		IDRIVE = 3'b110			350	
		IDRIVE = 3'b111			440	
Holding current	IHOLD	Source current after tDRIVE			10	mA
		Sink current after tDRIVE			40	
Strong pull-down current	STRONG	GHx			750	mA
		GLx			1000	
Gate pull-down resistor	ROFF	Pulldown GHx to OUTx			150	kÿ
		Pulldown GLx to GND			150	
Propagation Delay	tpd	IN1, IN2 to GHx or GLx			500	ns
Output dead time	tDEAD	TDEAD = 2'b00			120	ns
		TDEAD = 2'b01			240	
		TDEAD = 2'b10			480	
		TDEAD = 2'b11			960	
Gate drive current driving between	tDRIVE				2.5	ÿs
Gate clamping voltage (GHx)	VC(GS)	Forward clamping voltage			16	V
		Negative clamping voltage			-0.7	
Current regulation parameters (SP, **SN, SO, VREF)**						
VREF Input Voltage	VVREF		0.3		3.6 V	
VREF Input Impedance	RVREF	VREF_SCL = 00 (100%)	1			Mÿ
		VREF_SCL = 2'b01, 2'b10 or 2'b11		180		kÿ
Sampling Gain	OF	GAIN_CS = 00; 10 < VSP < 450 mV; VSN = GND	9.75	10	10.25	V/V
		GAIN_CS = 01; 10 < VSP < 225 mV; VSN = GND	19.5	20	20.5	
		GAIN_CS = 10; 10 < VSP < 112 mV; VSN = GND	39	40	41	
		GAIN_CS = 11; 10 < VSP < 56 mV; VSN = GND	78	80	82	V/V
Input voltage bias	SAW	VSP = VSN = GND		5	10 mV	
Bias temperature drift	VIO(OPERATION)	VSP = VSN = GND		10		ÿV/°C

Electrical characteristics parameters (continued)

Unless otherwise specified, TA **= 25°C.**

parameter	symbol	condition	Min.	Typ.	Max.	Unit
SP input current	ISP	VSP = 100 mV; VSN = GND		-20		ÿA
SO output voltage	ALL		OFF x SAW		4.5	V
Sampling settling time ±1%	tS	VSP = VSN = GND to VSP = 240 mV, VSN = GND, OFF = 10; CSO = 200 pF			0.5	ÿs
		VSP = VSN = GND to VSP = 120 mV, VSN = GND, OFF = 20; CSO = 200 pF			1	
		VSP = VSN = GND to VSP = 60 mV, VSN = GND, OFF = 40; CSO = 200 pF			2	
		VSP = VSN = GND to VSP = 30 mV, VSN = GND, OFF = 80; CSO = 200 pF			4	
Fixed off time	toff	TOFF = 00		25		ÿs
		TOFF = 01		50		
		TOFF = 10		100		
		TOFF = 11		200		
Blanking time	tBLANK			2		ÿs
Protection function						
VM undervoltage threshold	VUVLO2	VM falling		5.25		V
		VM rising		5.4		
VM digital circuit undervoltage threshold	VUVLO1				4.5	V
VM undervoltage hysteresis	VUVLO_HYS	Rising to falling threshold		150		mV
Charge Pump Undervoltage Threshold	VCP_UVLO	VCP falling		EIA + 2.8		V
		VCP rising		EIA + 3.0		
Charge Pump Undervoltage Hysteresis	VCPUV_HYS	Rising to falling threshold		200		mV
VDS Threshold	VDS (OCP)	VDS_LEVEL = 3'b000		0.06		V
		VDS_LEVEL = 3'b001		0.145		
		VDS_LEVEL = 3'b010		0.17		
		VDS_LEVEL = 3'b011		0.2		
		VDS_LEVEL = 3'b100		0.12		
		VDS_LEVEL = 3'b101		0.24		
		VDS_LEVEL = 3'b110		0.48		

Electrical characteristics parameters (continued)

Unless otherwise specified, TA **= 25°C.**

parameter	symbol	condition	Min.	Typ.	Max.	Unit
VDS Threshold	VDS (OCP)	VDS_LEVEL = 3'b111		0.96		V
SP overcurrent protection threshold	VSP (OCP)	VSP with respect to GND	0.8	1	1.2	V
OCP de-peak time	tOCP		4	4.5	5	μs
OCP restart time	tRETRY		2.8	3	3.2	ms
Watchdog timer period	tWD	WD_DLY = 2'b00		10		ms
		WD_DLY = 2'b01		20		
		WD_DLY = 2'b10		50		
		WD_DLY = 2'b11		100		
Watchdog reset time	peat			64		μs
Over temperature shutdown temperature	TSD			160		°C
Over temperature shutdown hysteresis	THYS			25		°C

SPI Timing Requirements

symbol	describe	Min.	Typ.	Max.	Unit
tSCLK	SCLK minimum period	100			ns
tSCLKH	CLK minimum high level time	50			ns
tSCLKL	CLK minimum low level time	50			ns
tSU_SDI	SDI input data setup time	20			ns
tHD_SDI	SDI input data hold time	30			ns
tD_SDO	SDO output delay time			30	ns
tSU_nSCS	nSCS setup time	50			ns
tHD_nSCS	nSCS hold time nSCS	50			ns
tHI_nSCS	minimum high level time before pulling low	400			ns
tDIS_nSCS	Shutdown delay time, nSCS pulled high to SDO Hi-Z		10		ns

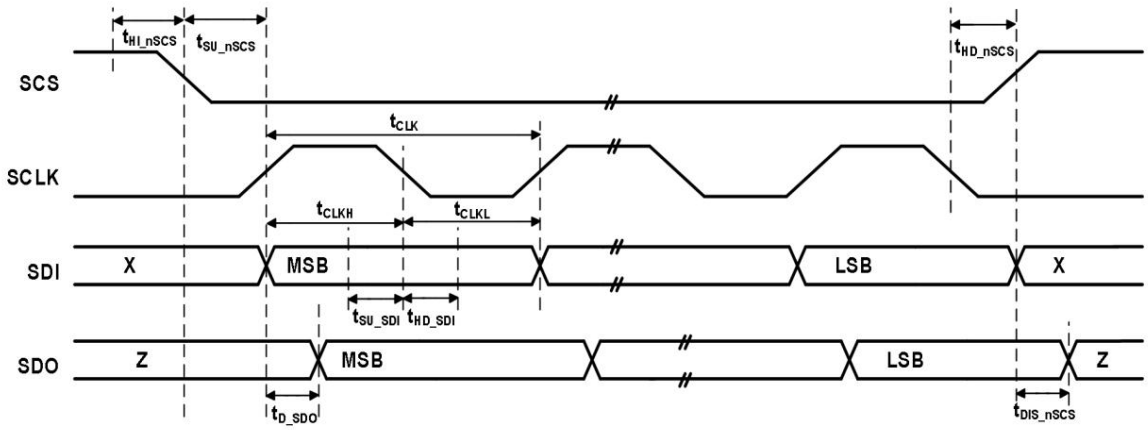


Figure **2 SPI** timing diagram

Functional Description

Overview

The TMI8721-Q1 is an H-bridge gate driver that drives brushed DC motors through four external N-MOSFETs; it operates in independent half-bridges

The TMI8721-Q1 operates with a power supply voltage of 5.5V to 38V and can be switched on and off via the nSLEEP pin.

The control mode can be configured as: PWM, PH/EN or independent half-bridge.

The TMI8721-Q1 uses smart gate drive technology that combines protection features with gate drive configurability. The gate drive current can be controlled by the device

The high-side and low-side

The side gate voltage (VGS) is about 10.5 V. At lower VM voltages, VGS decreases.

The TMI8721-Q1 integrates internal current chopper regulation to effectively limit inrush or startup current and operating current. The device contains a shunt

Amplifier, used to provide accurate current measurement for the system controller, SO pin outputs the voltage of the sampling amplifier, and the sampling amplifier gain is adjustable

The device provides a range of protection features, including VM undervoltage protection, charge pump undervoltage protection, VDS overvoltage protection for external MOSFET

Overcurrent protection and VGS gate fault protection, as well as internal thermal shutdown, etc.

Control method

The TMI8721-Q1 uses a configurable input interface for control and provides three control modes to suit different control schemes.

The mode is selected by the MODE pin as shown in Table 1. The MODE pin is latched when the VM is powered on or exits sleep mode.

Table **1 MODE** pin configuration

MODE status	Control method
H	Independent Half-Bridge Mode
L	H-bridge PH/EN
Hi-Z	H-bridge PWM

The truth tables of the logic control method are shown in Table 2, Table 3, and Table 4.

Table **2 PH/EN** control mode **(MODE = L)**

nSLEEP PH	**EN GH1 GL1 OUT1 GH2 GL2 OUT2 AVDD/DVDD** Motor Status									
0	XXXX Hi-Z XX Hi-Z Not working									Sleep
1	X 0		0	1	L	0	1	L	Work	brake
1	0	1	0	1	L	1	0	H	Work	Reversal
1	1	1	1	0	H	0	1	L	Work	Forward

Table **3** Half-bridge control mode **(MODE = H)**

nSLEEP IN1	**IN2 GH1 GL1 OUT1 GH2 GL2 OUT2 AVDD/DVDD** working status								
0	XXXX Hi-Z XX Hi-Z Not working								Sleep
1	X	0	X X X			0	1	L Working HB2 Low side open	
1	X	1	X X X			1	0	H Operation HB2 High side open	
1	0	X	0	1	L	XXX Working HB1 Low side on			
1	1	X	1	0	HXXX Operation HB1 High side open				

Table **4 PWM** control mode **(MODE = Hi-Z)**

nSLEEP IN1	IN2	GH1	GL1	OUT1	GH2	GL2	OUT2	AVDD/DVDD working status		
0	XXXX	Hi-Z	XX	Hi-Z	Not working					Sleep
1	0	0	0	0	Hi-Z	0	0	Hi-Z	Work	slide
1	1	0	1	0	H	0	1	L	Work	Forward
1	0	1	0	1	L	1	0	H	Work	Reversal
1	1	1	0	1	L	0	1	L	Work	brake

Current Regulation

The maximum current through the motor winding can be adjusted by current PWM chopping with a fixed off time.

The motor current depends on the winding DC voltage and inductance to rise at a certain rate. When the current reaches the chopping threshold, the H-bridge enters the braking mode (low-side slow

During the sampling process, the voltage on the SP pin will be blanked for a period of time (tBLANK), and then the current is enabled.

Sampling circuit.

The maximum current limit is set by selecting the sampling resistor and the VREF pin voltage. The sampling gain AV is adjustable to 10, 20, 40, 80V/V.

Use the following formula to calculate the chopping current (ICHOP).

$$I_{CHOP} = \frac{V_{VREF}}{A_V \times R_{SENSE}} - V_{IO}$$

For example, if the sampling resistance is 50mÿ, VREF voltage is 3.3V, sampling ratio is 20V/V, and bias voltage VIO is 5mV, then the maximum current limit value ICHOP is

for

3.2A. Sampling amplifier output (SO)

The voltage at the SO pin of the TMI8721-Q1 is equal to the voltage across the SP and SN pins multiplied by the sampling gain Av.

The following formula can be used to approximately calculate the H-bridge current.

$$I_{SENSE} = \frac{V_{SO} - V_{IO}}{A_V \times R_{SENSE}}$$

When the SP and SN voltages are 0V, the SO pin outputs the amplifier bias voltage multiplied by the amplifier gain VIO x Av.

When the voltage is greater than 0V, the SO pin output is the sum of the amplifier bias voltage and the voltage across the sense resistor multiplied by the amplifier gain (VIO + VRSENSE) × Av.

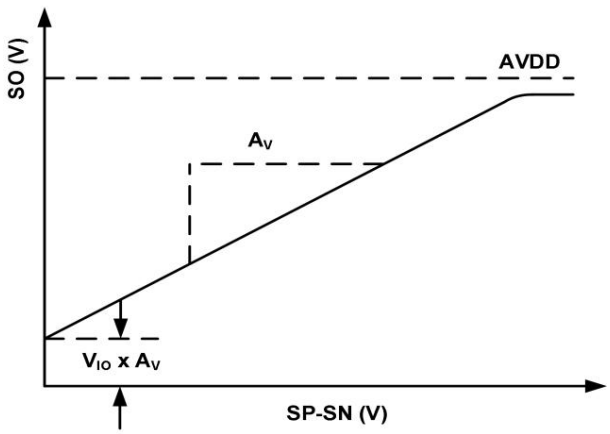


Figure **3** Current sampling amplifier output

The SO pin can provide 5mA of current. If the pin is shorted to ground, or the pin drives a higher current load, the output acts as a constant current source. In this state, the output voltage cannot represent the H-bridge current. In the braking mode device, the current circulates through the low-side MOS, and no current flows through the sampling resistor, so the output voltage cannot represent the H-bridge current.

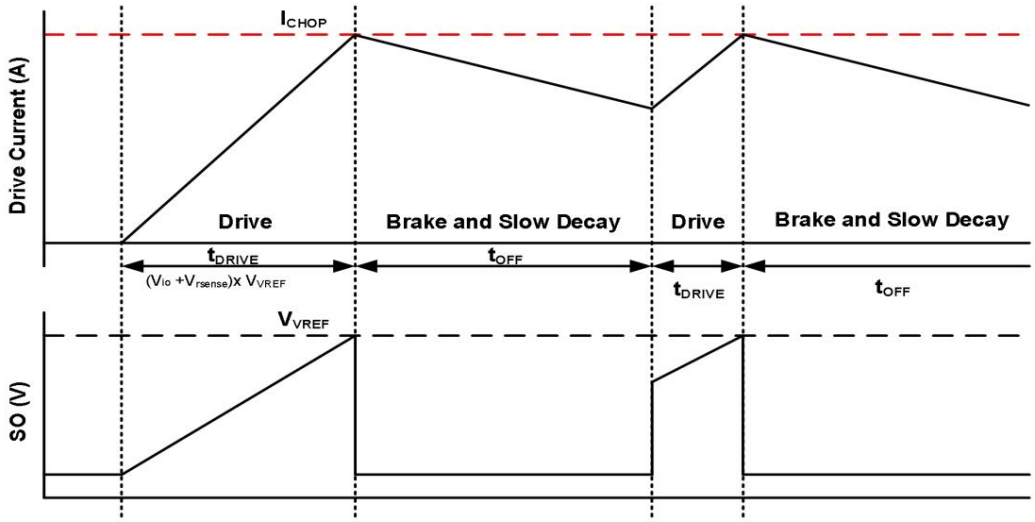


Figure **4** Current sampling amplifier and current chopping working state

TMI8721-Q1 allows the amplifier to operate in sample-and-hold mode. To enable this mode, set the SH_EN bit to 1 via SPI.
In mode, when the driver is in braking mode, the amplifier output is disabled and in Hi-Z.

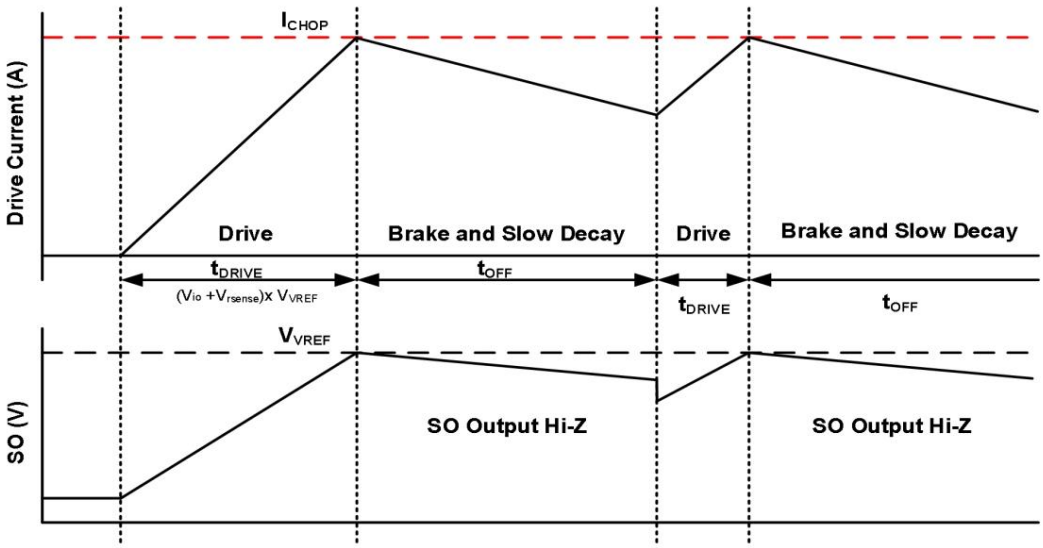


Figure **5** Sample and hold working mode

Gate drive structure

The TMI8721-Q1 is a single-channel H-bridge gate driver, and Figure 6 shows the block diagram of the pre-driver.

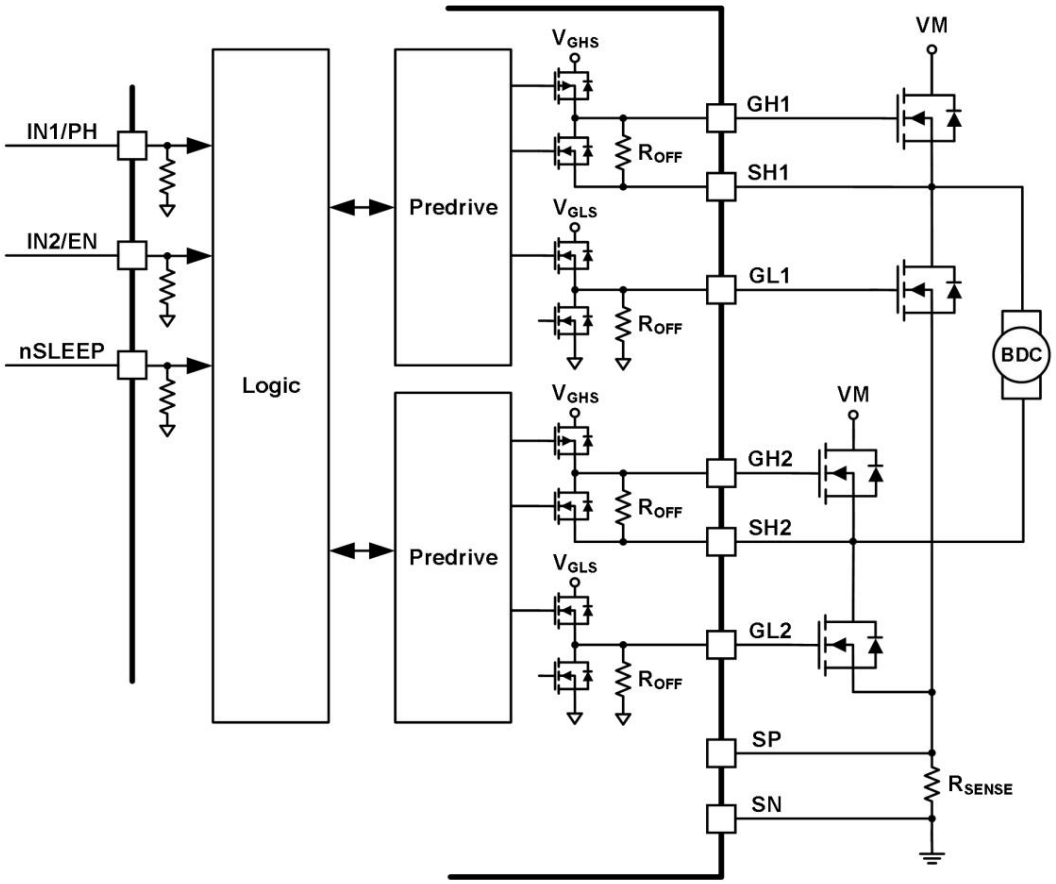


Figure **6** Pre-driver block diagram

The gate driver inside the TMI8721-Q1 device directly drives the N-channel MOSFET to drive the motor. Provided by a charge pump, an internal regulator generates the low-side gate drive voltage.

The peak drive current of the gate driver can be configured through the IDRIVE register of the TMI8721-Q1. The peak SOURCE current can be set to the values listed in the Gate Drive Parameters section of the Electrical Parameters. The peak value of the SINK current is approximately twice the peak value of the SOURCE current. Adjusting the peak current changes the output slew rate, which also depends on the input capacitance and gate charge of the MOSFET.

Higher switching frequencies cause additional noise on the VM and GND pins. This additional noise is likely to occur due to the relatively slow reverse recovery of the low-side body diode when the body diode turns on momentarily due to reverse bias voltage (similar to breakdown). Lower switching frequencies result in additional power dissipation because the external MOSFET is turned on and off for longer periods of time. When changing

the output state, a peak current (IDRIVE) is applied for a short time (tDRIVE) to charge the gate capacitance. After this time, a weak current source (IHOLD) is used to hold the gate in the desired state. When selecting the gate drive current for a given external MOSFET, the selected current must be large enough to fully charge or discharge the gate during tDRIVE, otherwise excessive power will be dissipated.

During high-side turn-on, the low-side gate is pulled low by a strong pull-down (ISTRONG). This pull-down prevents the low-side MOSFET QGS from charging and Keeps the MOSFET off even when fast switching occurs at the output. The gate

drive circuit includes dead time in the analog circuit to prevent both the high-side and low-side MOS from turning on at the same time.

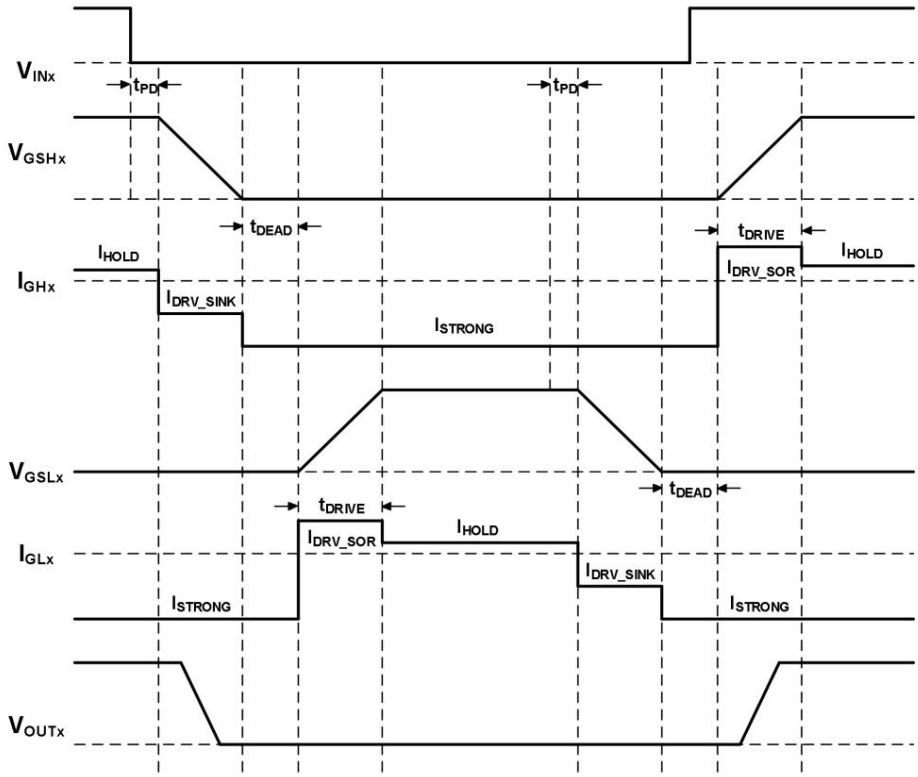


Figure **7** Gate drive control external **MOS**

Overcurrent protection

The TMI8721-Q1 monitors the VDS voltage of each external MOSFET during operation. The OCP state is detected when the VDS voltage is greater than the VDS threshold for longer than the OCP de-spike time (tOCP) . After detection, all GATEs in the H-bridge are disabled for the tretry duration. Afterwards, the H-bridge is re-enabled based on the state of the INx pins. If the overcurrent fault persists, the cycle repeats; otherwise the device resumes normal operation. The VDS threshold voltage of the TMI8721-Q1 device is adjustable. The block diagram of VDS detection is shown in Figure 8.

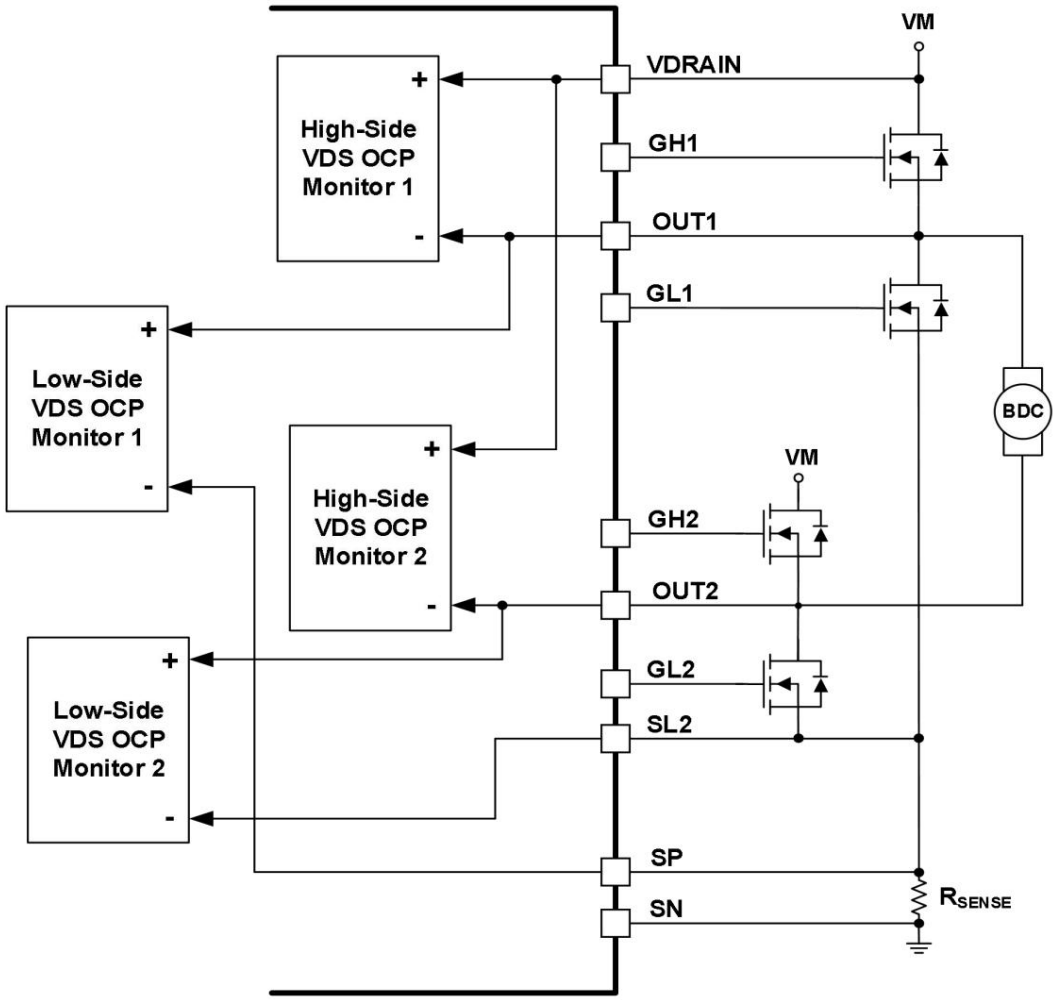


Figure **8 VDS** block diagram

VM undervoltage protection

When the VM voltage is less than the VM undervoltage threshold (UVLO2), all MOSFETs in the H-bridge are turned off, the charge pump is turned off, nFAULT is pulled low, and VM_UVFL is set to 1. After the VM voltage is higher than the undervoltage threshold (UVLO2), the operation resumes, nFAULT is pulled high, and VM_UVFL remains until CLR_FLT is written. Even if the output driver is disabled, the SPI settings on the

TMI8721-Q1 device are not reset by this fault, and the SPI maintains the settings and corresponding internal activities until the VM voltage is lower than the digital block undervoltage threshold (UVLO1).

Digital module undervoltage

When the VM voltage is lower than the digital block undervoltage threshold (UVLO1), the internal SPI is reset and nFAULT is pulled low.

VCP undervoltage protection

When the voltage on the VCP pin is lower than the charge pump undervoltage threshold, all MOS in the H-bridge are disabled, nFAULT is pulled low, and VCP_UVFL is set to 1. When the VCP voltage is higher than the CPUV threshold, the working state is restored. After recovery, nFAULT is pulled high and VCP_UVFL remains until CLR_FLT is written.

Gate Fault Protection (GDF)

The TMI8721-Q1 detects gate driver faults by monitoring the GHx and GLx pins.

A gate fault is detected if there is no increase or decrease after a certain period of time. A gate fault can also occur when GHx or GLx is shorted to GND, OUTx, or VM pins.

In addition, a gate driver fault can occur when the selected drive current is insufficient to turn on the external MOSFET.

After that, all MOSFETs are disabled, nFAULT is pulled low, and the GDF register bit is set to 1. After the OCP restart time tretry, the driver

When the driver is re-enabled, nFLULT is restored. The GDF bit remains until CLR_FLT is written.

Over temperature protection (TSD)

If the device temperature exceeds the overtemperature shutdown temperature, all MOSFETs in the H-bridge are turned off, the charge pump is turned off, and the AVDD regulator is turned off.

The nFAULT pin is pulled low and the OTSD register is set to 1. When the device temperature is lower than the TSD-THYS temperature, the device automatically recovers.

OTSD remains set until CLR_FLT is written. **Watchdog**

(WDFLT)

The TMI8721-Q1 device supports the MCU-enabled watchdog function, ensuring that the external controller that indicates the device is in a known working state.

SPI sets the WD_EN bit to 1 to enable the watchdog function (disabled by default). After the watchdog is enabled, the internal timer will be set according to the time set by the WD_DLY bit.

Register address 0x00 must be read by the MCU within the time interval set by the WD_DLY bit to reset the watchdog.

If the timer expires, the nWDFLT pin is enabled. When the nWDFLT pin is enabled:

1. nWDFLT pin is pulled low for 64us;
2. The nFAULT pin is pulled low;
3. Clear the WD_EN bit;
4. The driver is disabled;

Fault Response

The response of the device under fault conditions is shown in Table 5.

Table **5** Fault Response

FAULT	CONDITION	H-BRIDGE	CHARGE PUMP	DEPARTMENT	DVDD	RECOVERY
UVLO	VVM ÿ V(UVLOx)	Disabled	Disabled	Disabled	Operating	VVM ÿ V(UVLOx)
CPUV	VVCP ÿ V(CP_UV)	Disabled	Operating	Operating	Operating	VVCP ÿ V(CP_UV)
OCP	VDS ÿ VDS(OCP) VSP – VSN > 1 V	Disabled	Operating	Operating	Operating	t(RETRY)
GDF	Gate voltage unchanged after t(DRIVE)	Disabled	Operating	Operating	Operating	t(RETRY)
WDFLT	Watchdog timer expires	Disabled	Operating	Operating	Operating	CLR_FLT bit
TSD	TJ ÿ TSD	Disabled	Disabled	Disabled	Operating	TJ ÿ TSD – Thys

programming

SPI

TMI8721-Q1 implements functions such as device configuration, operating parameter setting, and diagnostic information reading through SPI.

The SPI input data (SDI) word consists of 5-bit command bits, 3-bit don't care bits and 8-bit data bits.

The SPI output data (SDO) word consists of 8-bit don't care bits and 8-bit data bits.

For a write command (W0=0), the value fed back by the SDO pin is the data in the register currently being written.

For a read command (W0=1), the value fed back by the SDO pin is the data in the register currently being read.

Table **6 SDI** input data format

R/W	ADDRESS					DON'T CARE			DATA							
b15	b14	b13	b12	b11	b10	b9			b8	b7	b6	b5	b4	b3	b2	b1	b0
W0	A3	A2	A1	A0	XXX		D7	D6	D5	D4	D3	D2	D1				D0

Table **7 SDO** output data format

DON'T CARE									DATA							
b15	b14	b13	b12	b11	b10	b9			b8	b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X				XXX		D7	D6	D5	D4	D3	D2	D1	D0

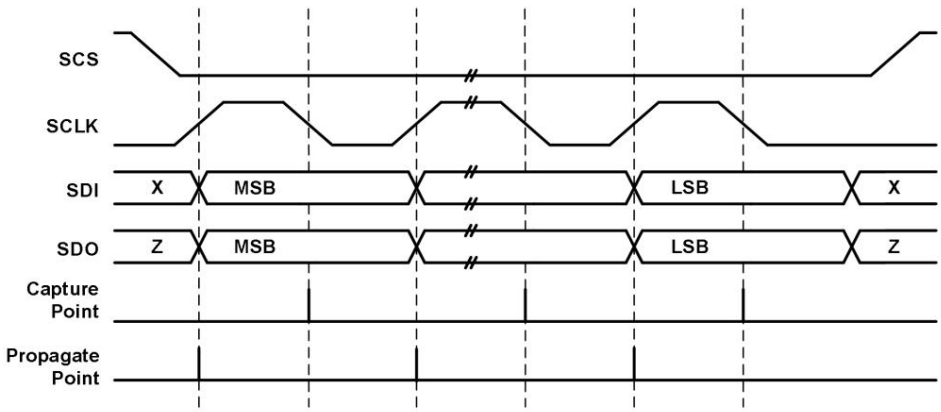


Figure **9 SPI** slave timing diagram

Table **8** Register Overview

Name Address		7	6	5	4	3	2	1	0
FAULT Status	0	FAULT	WDFLT	GDF	OCP VM_UVFL		VCP_ UVFL	OTSD	OTW
VDS and GDF	1	H2_GDF L2_GDF		H1_GDF L1_GDF H2_VDS			L2_VDS H1_VDS		L1_VDS
Main	2	RESERVED		LOCK			IN1/PH	IN2/EN	CLR_FLT
IDRIVE and WD	3	TDEAD		WD_EN	WD_DLY		IDRIVE		
VDS	4	SO_LIM	VDS			DIS_H2_ VDS	DIS_L2_ VDS	DIS_H1_ VDS	DIS_L1_ VDS
Config	5	TOFF		CHOP_IDS	VREF_SCL		SH_EN	GAIN_CS	

1. FAULT Status Register (address = 0x00h)

FAULT status is shown in Table 9 and described in Table 10.

Table 9. FAULT Status Register

b7	b6	b5	b4	b3	b2	b1	b0
FAULT	WDFLT	GDF	OCP	VM_UVFL VCP_UVFL		OTSD	OTW

Table 10. FAULT Status Field Descriptions

Bit	Field	Type	Default Description	
7	FAULT	R	0	Logic OR of the FAULT status register excluding the OTW bit
6	WDFLT	R	0	Watchdog time-out fault
5	GDF	R	0	Indicates gate drive fault condition
4	OCP	R	0	Indicates VDS monitor overcurrent fault condition
3	VM_UVFL	R	0	Indicates VM undervoltage lockout fault condition
2	VCP_UVFL	R	0	Indicates charge-pump undervoltage fault condition
1	OTSD	R	0	Indicates overtemperature shutdown
0	OTW	R	0	Indicates overtemperature warning

2. VDS and GDF Status Register (address = 0x01h)

VDS and GDF status is shown in Table 11 and described in Table 12.

Table 11. VDS and GDF Status Register

b7	b6	b5	b4	b3	b2	b1	b0
H2_GDF	L2_GDF	H1_GDF	L1_GDF	H2_VDS	L2_VDS	H1_VDS	L1_VDS

Table 12. VDS and GDF Status Field Descriptions

Bit	Field	Type	Default	Description
7	H2_GDF	R	0	Indicates gate drive fault on the high-side FET of half-bridge 2
6	L2_GDF	R	0	Indicates gate drive fault on the low-side FET of half-bridge 2
5	H1_GDF	R	0	Indicates gate drive fault on the high-side FET of half-bridge 1
4	L1_GDF	R	0	Indicates gate drive fault on the low-side FET of half-bridge 1
3	H2_VDS	R	0	Indicates VDS monitor overcurrent fault on the high-side FET of half-bridge 2
2	L2_VDS	R	0	Indicates VDS monitor overcurrent fault on the low-side FET of half-bridge 2
1	H1_VDS	R	0	Indicates VDS monitor overcurrent fault on the high-side FET of half-bridge 1
0	L1_VDS	R	0	Indicates VDS monitor overcurrent fault on the low-side FET of half-bridge 1

3. Main Control Register (address = 0x02h)

Main control is shown in Table 13 and described in Table 14.

Table 13. Main Control Register

b7	b6	b5	b4	b3	b2	b1	b0
RESERVED		LOCK			IN1/PH	IN2/EN	CLR_FLT

Table 14. Main Control Field Descriptions

Bit	Field	Type	Default	Description
7-6	RESERVED	R/W	00	Reserved
5-3	LOCK	R/W	011	Write 110b to lock the settings by ignoring further register changes except to address 0x02h. Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
2	IN1/PH	R/W	0	This bit is ORed with the IN1/PH pin
1	IN2/EN	R/W	0	This bit is ORed with the IN2/EN pin
0	CLR_FLT	R/W	0	Write a 1 to this bit to clear the fault bits

4. IDRIVE and WD Control Register (address = 0x03h)

IDRIVE and WD control is shown in Table 15 and described in Table 16.

Table 15. IDRIVE and WD Control Register

b7	b6	b5	b4	b3	b2	b1	b0
RESERVED		LOCK			IN1/PH	IN2/EN	CLR_FLT

Table 16. IDRIVE and WD Control Field Descriptions

Bit	Field	Type	Default	Description
7-6	TDEAD	R/W	00	Dead time 00b = 120 ns 01b = 240 ns 10b = 480 ns 11b = 960 ns
5	WD_EN	R/W	0	Enables or disables the watchdog time (disabled by default)
4-3	WD_DLY	R/W	00	Watchdog timeout delay (if WD_EN = 1) 00b = 10 ms 01b = 20 ms 10b = 50 ms 11b = 100 ms
2-0	IDRIVE	R/W	111	Sets the peak source current and peak sink current of the gate drive. Table lists the bit settings.

Table 17. IDRIVE Bit Settings

Bit Value	Source Current		Sink Current	
	VVM = 5.5 V	VVM = 13.5 V	VVM = 5.5 V	VVM = 13.5 V
000	High-side: 10 mA Low-side: 10 mA	High-side: 10 mA Low-side: 10 mA	High-side: 20 mA Low-side: 20 mA	High-side: 20 mA Low-side: 20 mA
010	High-side: 20 mA Low-side: 20 mA	High-side: 20 mA Low-side: 20 mA	High-side: 40 mA Low-side: 40 mA	High-side: 40 mA Low-side: 40 mA
010	High-side: 50 mA Low-side: 40 mA	High-side: 50 mA Low-side: 45 mA	High-side: 90 mA Low-side: 85 mA	High-side: 95 mA Low-side: 95 mA
011	High-side: 70 mA Low-side: 55 mA	High-side: 70 mA Low-side: 60 mA	High-side: 120 mA Low-side: 115 mA	High-side: 130 mA Low-side: 125 mA
100	High-side: 100 mA Low-side: 75 mA	High-side: 105 mA Low-side: 90 mA	High-side: 170 mA Low-side: 160 mA	High-side: 185 mA Low-side: 180 mA
101	High-side: 145 mA Low-side: 115 mA	High-side: 155 mA Low-side: 130 mA	High-side: 250 mA Low-side: 235 mA	High-side: 265 mA Low-side: 260 mA
110	High-side: 190 mA Low-side: 145 mA	High-side: 210 mA Low-side: 180 mA	High-side: 330 mA Low-side: 300 mA	High-side: 350 mA Low-side: 350 mA
111	High-side: 240 mA Low-side: 190 mA	High-side: 260 mA Low-side: 225 mA	High-side: 420 mA Low-side: 360 mA	High-side: 440 mA Low-side: 430 mA

5. VDS Control Register (address = 0x04h)

VDS control is shown in Table 18 and described in Table 19.

Table 18. VDS Control Register

b7	b6	b5	b4	b3	b2	b1	b0
SO_LIM	VDS			DIS_H2_VDS	DIS_L2_VDS	DIS_H1_VDS	DIS_L1_VDS

Table 19. VDS Control Field Descriptions

Bit	Field	Type	Default	Description
7	SO_LIM	R/W	0	0b = Default operation 1b = SO output is voltage-limited to 3.6 V
6-4	VDS	R/W	111	Sets the VDS(OCP) monitor for each FET 000b = 0.06V 001b = 0.145V 010b = 0.17 V 011b = 0.2 V 100b = 0.12V 101b = 0.24 V 110b = 0.48V 111b = 0.96 V
3	DIS_H2_VDS	R/W	0	Disables the VDS monitor on the high-side FET of half-bridge 2 (enabled by default)
2	DIS_L2_VDS	R/W	0	Disables the VDS monitor on the low-side FET of half-bridge 2 (enabled by default)
1	DIS_H1_VDS	R/W	0	Disables the VDS monitor on the high-side FET of half-bridge 1 (enabled by default)
0	DIS_L1_VDS	R/W	0	Disables the VDS monitor on the low-side FET of half-bridge 1 (enabled by default)

6. Config Control Register (address = 0x05h)

Config control is shown in Table 20 and described in Table 21.

Table 20. Config Control Register

b7	b6	b5	b4	b3	b2	b1	b0
TOFF		CHOP_IDS	VREF_SCL		SH_EN	GAIN_CS	

Table 21. Config Control Field Descriptions

Bit	Field	Type	Default	Description
7-6	TOFF	R/W	00	Off time for PWM current chopping 00b = 25 µs 01b = 50 µs 10b = 100 µs 11b = 200 µs
5	CHOP_IDS	R/W	0	Disables current regulation (enabled by default)
4-3	VREF_SCL	R/W	00	Scale factor for the VREF input 00b = 100% 01b = 75% 10b = 50% 11b = 25%
2	SH_EN	R/W	0	Enables sample and hold operation of the shunt amplifier (disabled by default)
1-0	GAIN_CS	R/W	01	Shunt amplifier gain setting 00b = 10V/V 01b = 19.8 V/V 10b = 39.4 V/V 11b = 78 V/V

Application Schematic

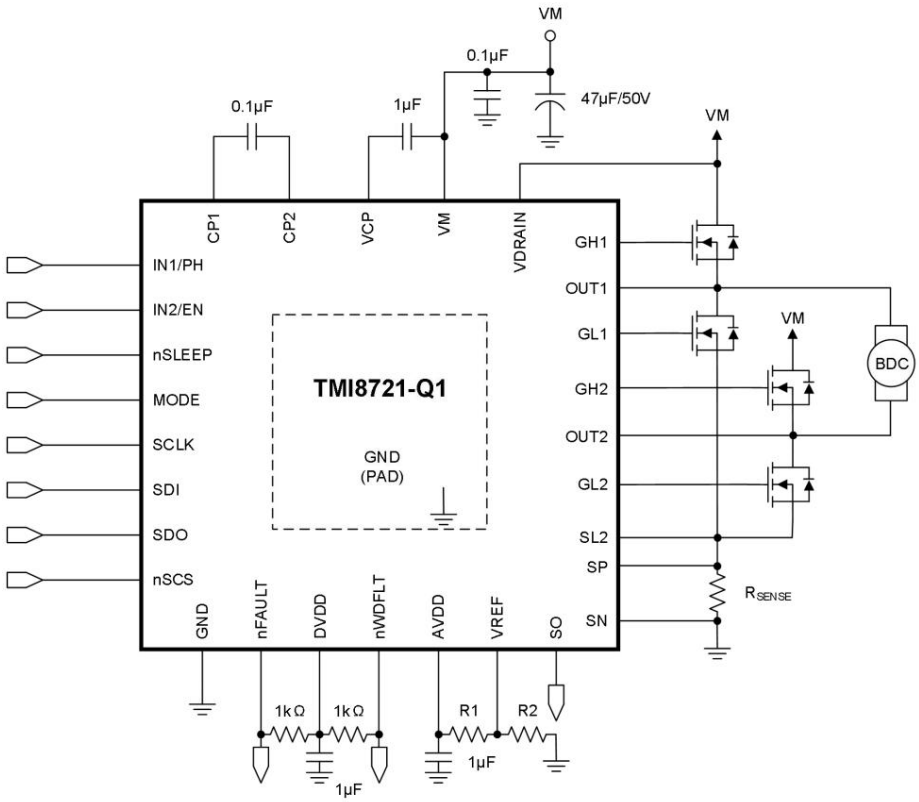


Figure **10 TMI8721-Q1** application schematic

block diagram

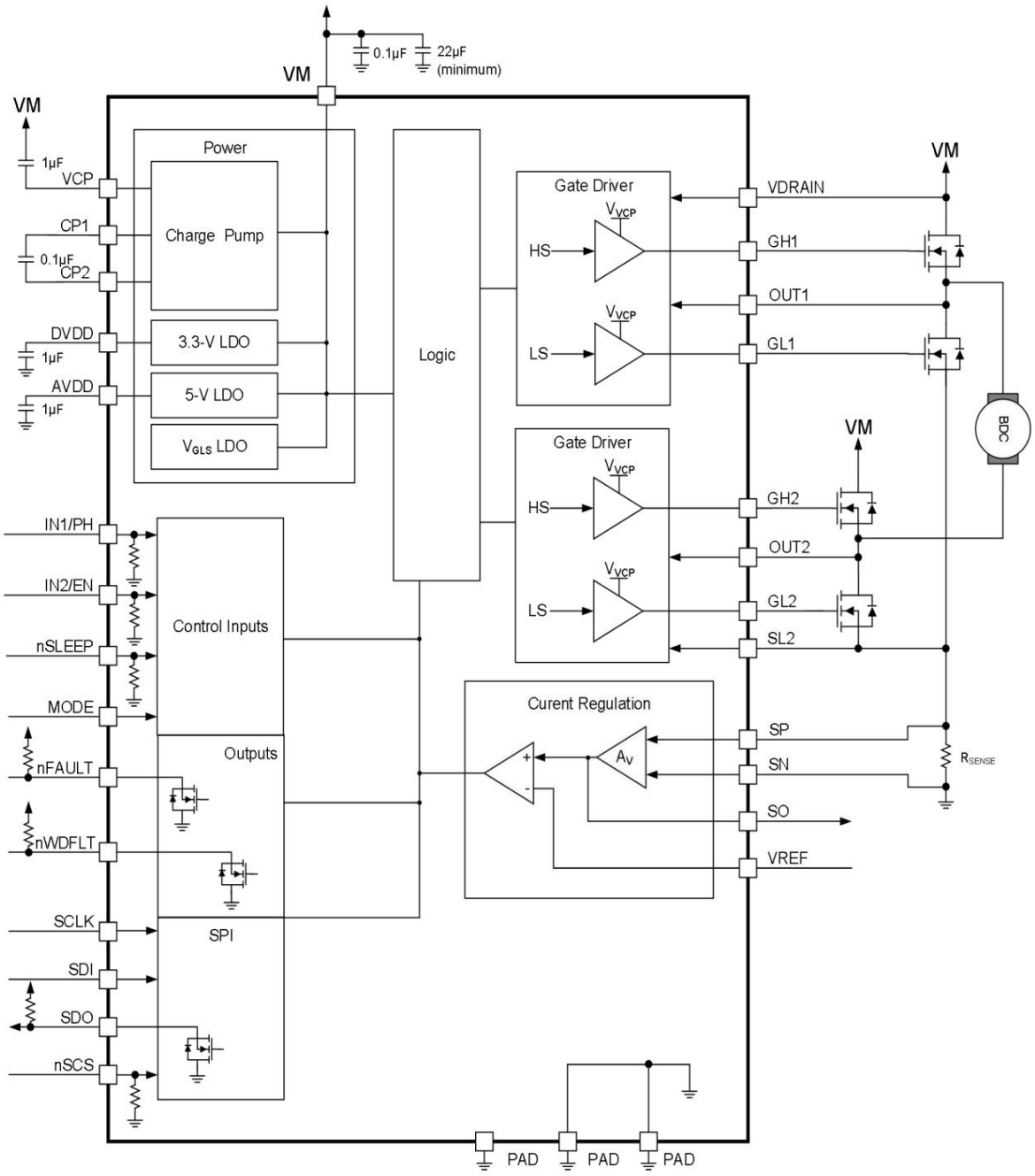
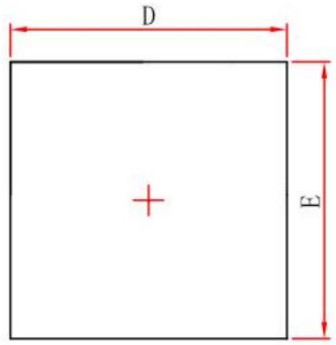


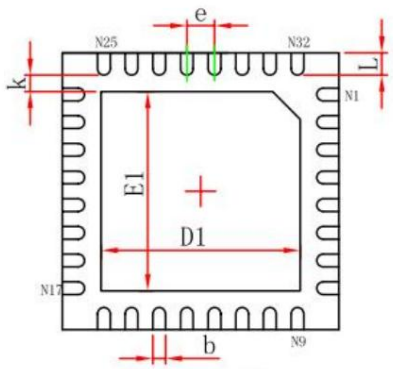
Figure **11 TMI8721-Q1** block diagram

Packaging information

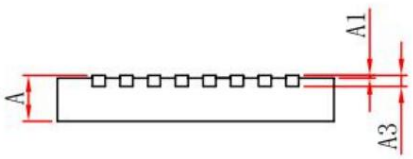
QFN5x5-32



Top View



Bottom View

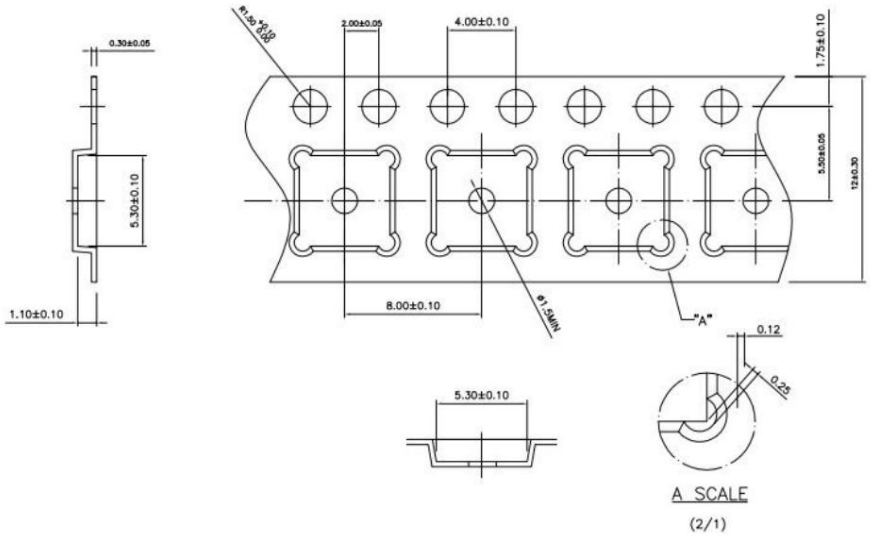


Side View

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	0.700	0.800	E1	3.300	3.500
A1	0.000	0.050	k	0.200MIN	
A3	0.203REF		and	0.500TYP	
D	4.924	5.076	b	0.200	0.300
AND	4.924	5.076	L	0.324	0.476
D1	3.300	3.500			

Packing size

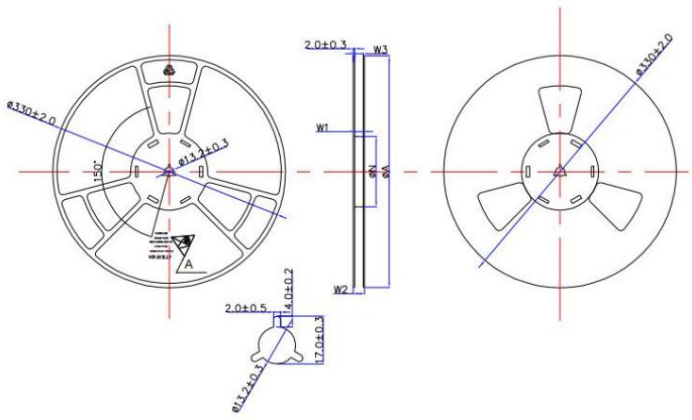
Tape size: QFN5x5-32



Unit: mm

Symbol	Dimensions	Symbol	Dimensions	Symbol	Dimensions		
A0	6.70±0.10	i	5° TYPE	AND	1.75±0.10	D1	1.55 MIN
B0	10.05±0.10	t	0.30±0.05	F	7.50±0.10	P0	0.30±0.10
K0	1.50±0.10	At	16.00±0.30	P2	2.00±0.10	10P0	40.00±0.20
Q1	1.35±0.10	P	8.00±0.10	D	1.50±0.10		

Reel size: QFN5x5-32



Unit: mm

Ø A	Ø N	W1(+2/0)	W2(Max)	W2(Max)
330±2.0	100±1.0	12.4	18.4	11.9/15.4

Notes:

1) All dimensions are in millimeters.

2) The unit quantity per roll is 5000.

3) The MSL level is 3.

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