TOSHIBA MOS MEMORY PRODUCT

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2088P-35, TMM2088P-45
TMM2088P-55

DESCRIPTION

The TMM2088P is a 65,536 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 8 bits and operates from a single 5-volt supply. The TMM2088P is features an automatic stand-by mode when deselect by $\overline{CS1}$ signal. Thus the TMM2088P is suitable for use in cache memory and high speed storage. The TMM2088P is offered in a 28 pin standard plastic dual in-line package with 0.3 inch width for high density assembly.

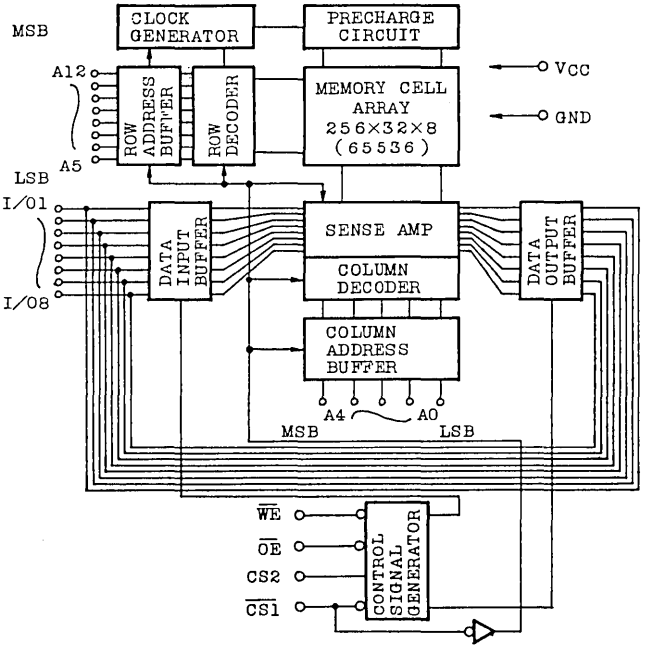
FEATURES

- Access Time and Current

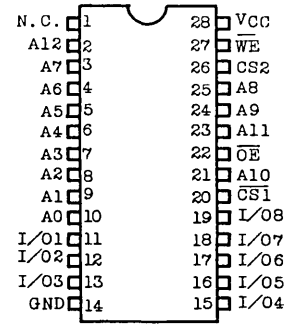
Parameter / Part Number	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2088P-35	35ns	135mA	15mA
TMM2088P-45	45ns	135mA	15mA
TMM2088P-55	55ns	135mA	15mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: ($\overline{CS1}$)
- Output Buffer Control: ($\overline{OE}$)
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Compatible)
- Inputs Protected: (All inputs have Protection against static charge.)

BLOCK DIAGRAM



PIN CONNECTION



PIN NAMES

A0 ∿ A12	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
I/O1 ∿ I/O8	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground
N.C.	No Connection

OPERATION MODE

MODE	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O1 ∿ 8	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	-3.5 ∿ 7.0	V
$T_{opr.}$	Operating Temperature	0 ∿ 70	°C
$T_{stg.}$	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature • Time	260 • 10	°C•sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V (Min.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V ∿ 5.5V	-1.0	1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	-4.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	8.0	-	mA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V∿5.5V	-1.0	1.0	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	-	30	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH}, I_{OUT}=0mA	-	15	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, I_{OUT}=0mA	-	135	mA

CAPACITANCE* (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		TMM2088P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	-	45	-	55	-	ns
t_{ACC}	Address Access Time	-	35	-	45	-	55	
t_{CO1}	$\overline{CS1}$ Access Time	-	35	-	45	-	45	
t_{CO2}	CS2 Access Time	-	25	-	25	-	30	
t_{OE}	$\overline{OE}$ Access Time	-	20	-	20	-	25	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	
t_{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	0	-	5	-	5	-	
t_{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2	-	20	-	20	-	20	
t_{OLZ}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	
t_{OHZ}	Output Disable Time from $\overline{OE}$	-	15	-	15	-	20	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to POwer Down Time	-	30	-	30	-	30	

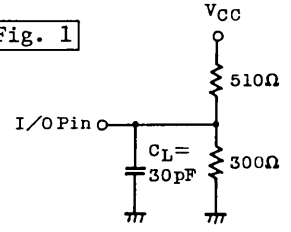
WRITE CYCLE

SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		TMM2088P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	-	45	-	55	-	ns
t_{CW}	Chip Selection to End of Write	30	-	40	-	50	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	25	-	35	-	45	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	15	-	20	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	
t_{WLZ}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	
t_{WHZ}	Output Disable Time from $\overline{WE}$	-	15	-	15	-	20	

A.C. TEST CONDITIONS

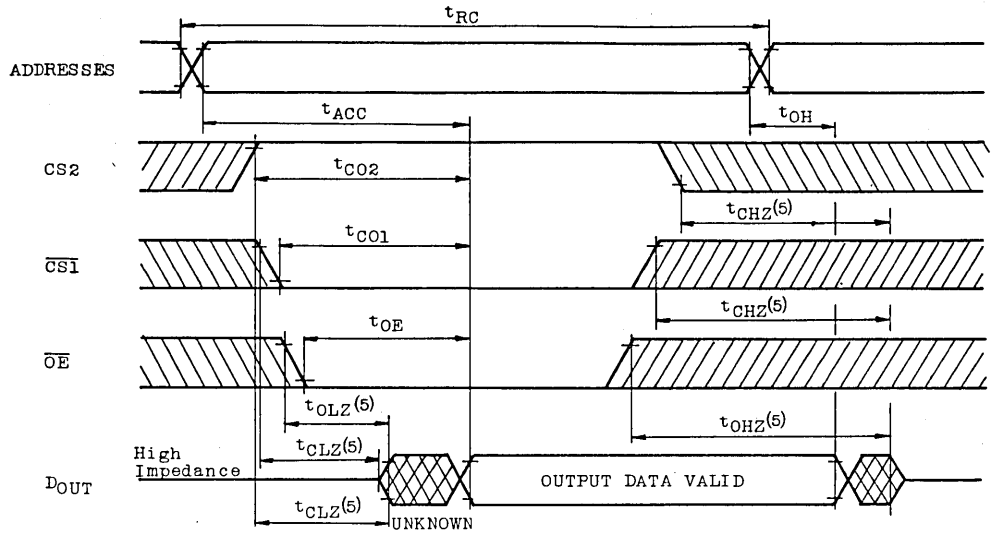
Input Pulse Levels	0.0 ∿ 3.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig. 1

Fig. 1

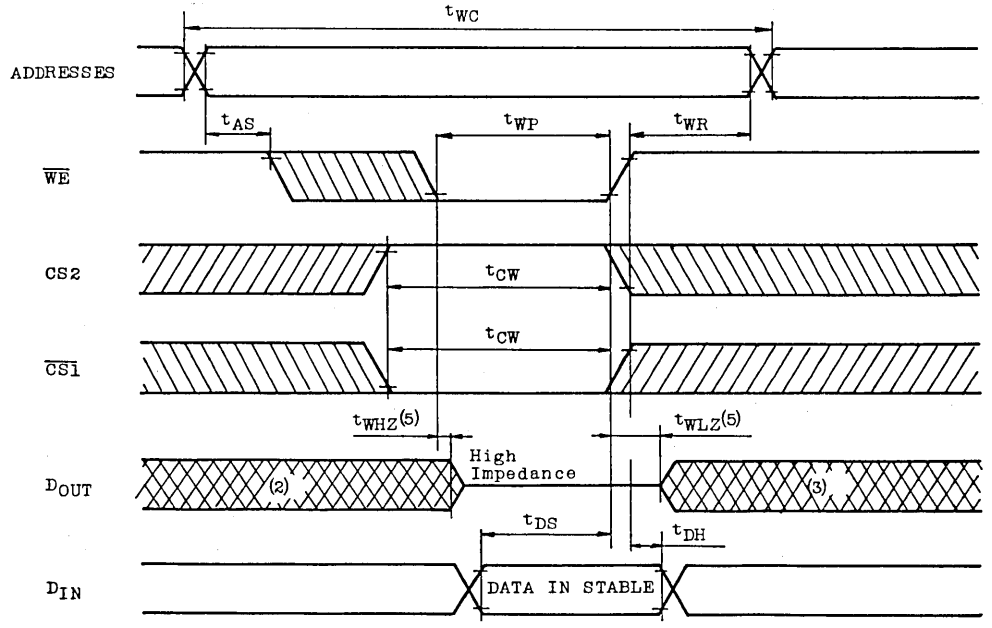


TIMING WAVEFORMS

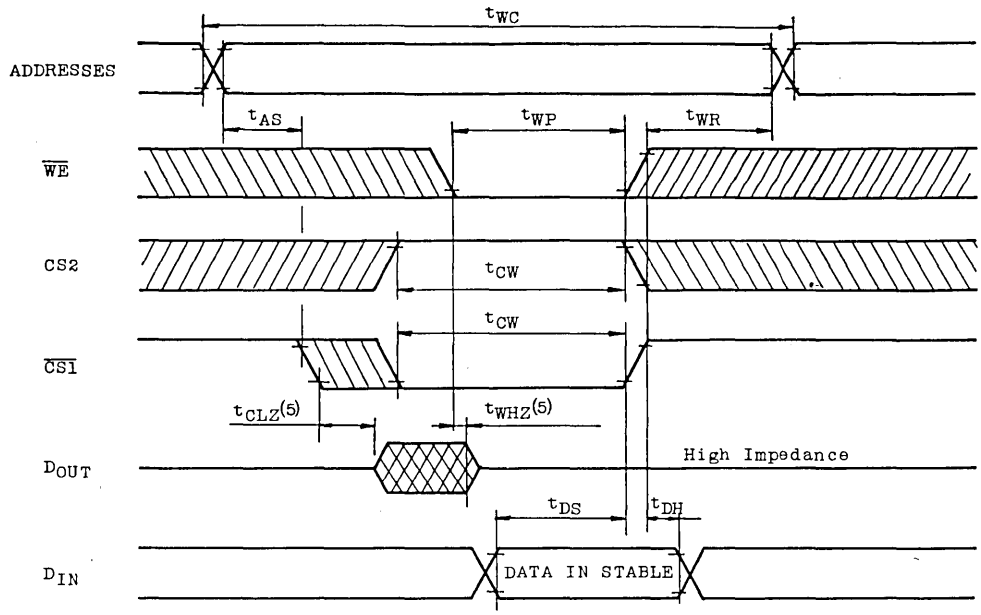
READ CYCLE (1)



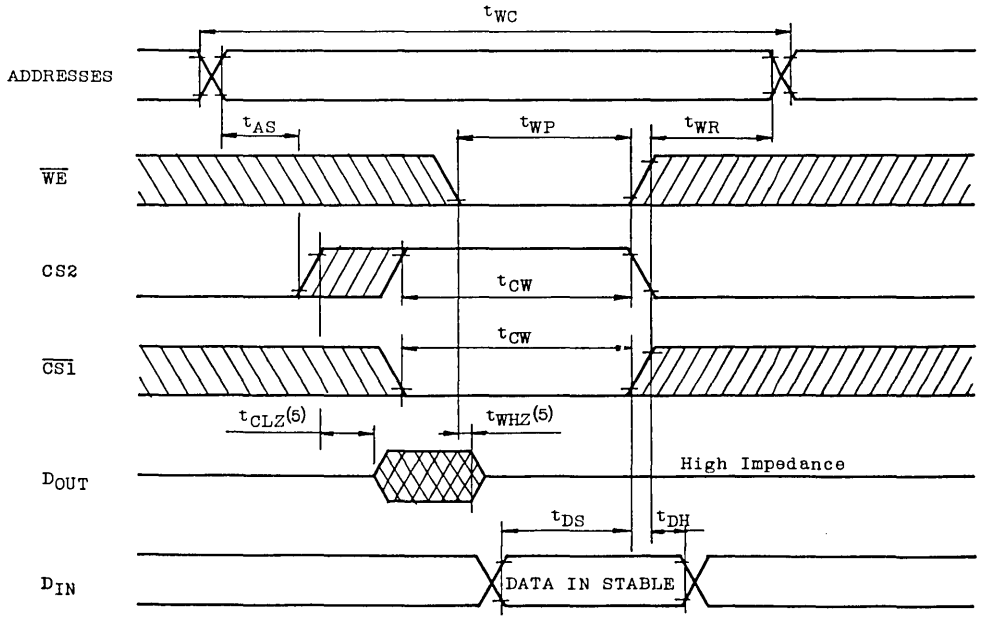
WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

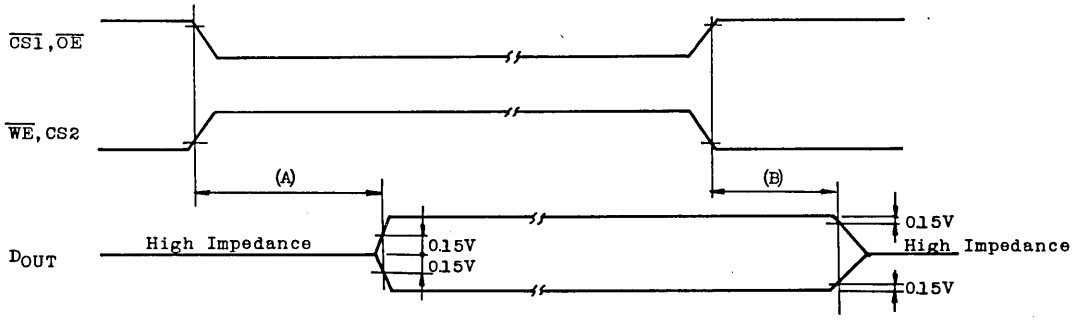
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

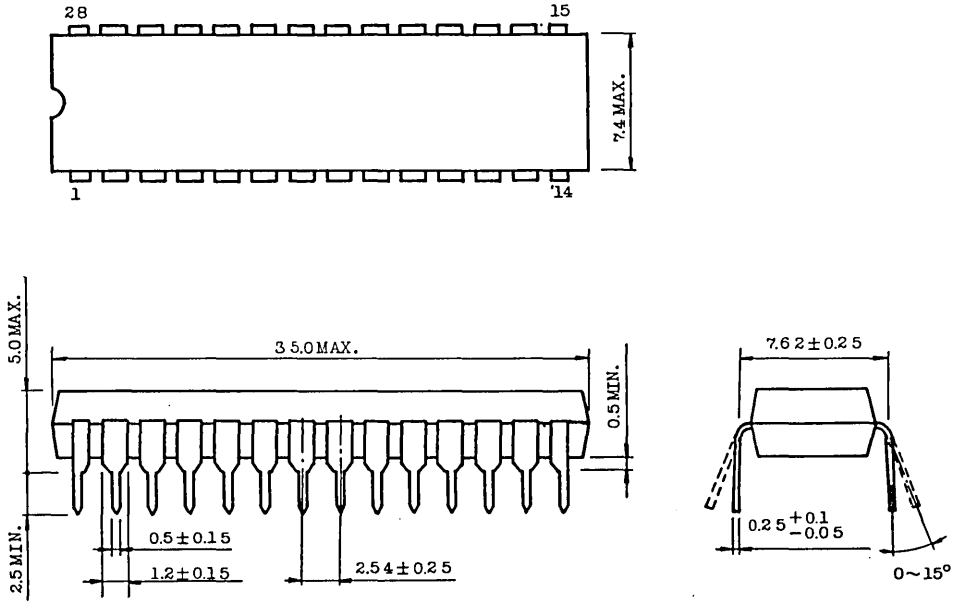
(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time



DIP 28 PIN OUTLINE DRAWING

Unit in mm



Note: Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.