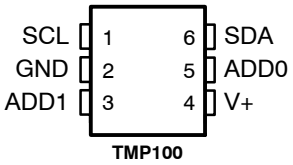
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Digital Output: I²C Serial 2-Wire**
- **Resolution: 9- to 12-Bits, User Selectable**
- **Accuracy: ±2°C from –25°C to +85°C (MAX), ±3°C from –55°C to +125°C (MAX)**
- **Low Quiescent Current: 45 μA, 0.1-μA Standby**
- **Wide Supply Range: 2.7 V to 5.5 V**
- **Small SOT23-6 Package**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## applications

- **Power-Supply Temperature Monitoring**
- **Computer Peripheral Thermal Protection**
- **Notebook Computers**
- **Battery Management**
- **Thermostat Controls**
- **Environmental Monitoring**
- **Electromechanical Device Temperature**

**DBV PACKAGE**
**(TOP VIEW)**




**TMP100**

## description/ordering information

The TMP100 and TMP101 are 2-wire, serial output temperature sensors available in SOT23–6 packages. Requiring no external components, the TMP100 and TMP101 are capable of reading temperatures with a resolution of 0.0625°C.

The TMP100 and TMP101 feature SMBus and I²C™ interface compatibility, with the TMP100 allowing up to eight devices on one bus.

The TMP100 and TMP101 are ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

The TMP100M and TMP101M are specified for operation over a temperature range of –55°C to +125°C.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –55°C to 125°C | SOT23-6 (DBV) | Reel of 3000 | TMP100MDBVREP | 100E |

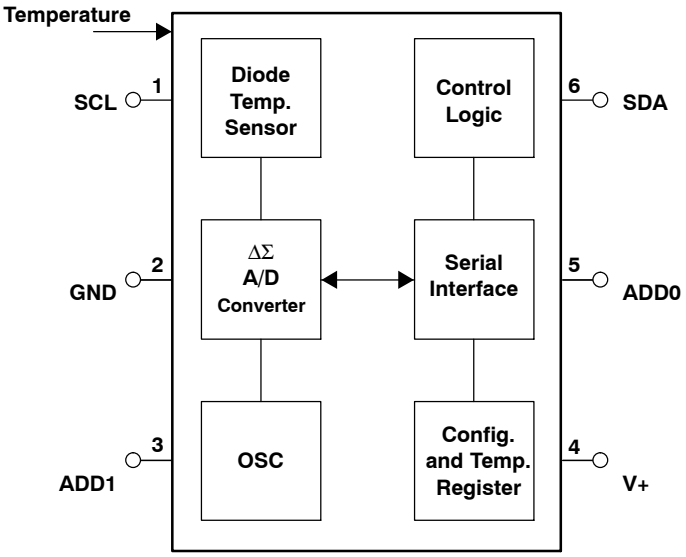
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ Product Preview

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

I²C is a registered trademark of Philips Incorporated.

## functional block diagram




TMP100

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage, V+ | 7.5 V |
| Input voltage range | –0.5 V to 7.5 V |
| Operating free-air temperature range, $T_A$ | –55°C to 125°C |
| Storage temperature range, $T_{stg}$ | –60°C to 150°C |
| Maximum Junction temperature, $T_J$ | 150°C |
| Thermal impedance, $\theta_{JA}$ (See Note 1) | 165°C/W |
| Lead temperature soldering | 300°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The thermal impedance, $\theta_{JA}$, for the DBV package is determined for JEDEC high–K PCB (JESD 51–7).

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, V+ | 2.7 | | 5.5 | V |
| Operating free-air temperature, $T_A$ | –55 | | 125 | °C |

## electrical characteristics over recommended operating free-air temperature range, $V_{DD}$ = 2.7 V to 5.5 V (unless otherwise noted)

### temperature input

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Range | | –55 | | 125 | °C |
| Accuracy (temperature error) | –25°C to 85°C | | ±0.5 | ±2 | °C |
| | –55°C to 125°C | | ±1 | ±3 | |
| Resolution | Selectable | | ±0.0625 | | °C |

### digital input/output

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 0.7(V+) | | (V+) + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | | –0.5 | | 0.3(V+) | V |
| $I_{IN}$ | Input current | $V_{IN}$ = 0 V to 6 V | | | | 1 | µA |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 3 mA | SDA | 0 | 0.15 | 0.4 | V |
| | | $I_{OL}$ = 4 mA | ALERT | 0 | 0.15 | 0.4 | |
| | Resolution | Selectable | | | 9 to 12 | | bits |
| | Conversion time | 9-bit | | | 40 | 75 | ms |
| | | 10-bit | | | 80 | 150 | |
| | | 11-bit | | | 160 | 300 | |
| | | 12-bit | | | 320 | 600 | |
| | Conversion rate | 9-bit | | | 25 | | s/s |
| | | 10-bit | | | 12 | | |
| | | 11-bit | | | 6 | | |
| | | 12-bit | | | 3 | | |

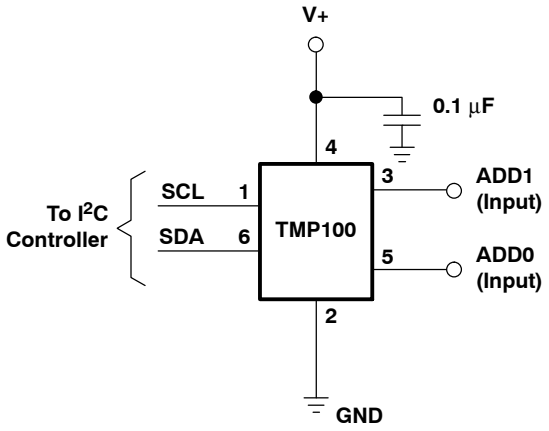
### power supply

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_Q$ | Quiescent current | Serial bus inactive | | | 45 | 75 | µA |
| | | Serial bus active | SCL = 400 kHz | | 70 | | |
| | | | SCL = 3.4 MHz | | 150 | | |
| $I_{SD}$ | Shutdown current | Serial bus inactive | | | 0.1 | 1 | µA |
| | | Serial bus active | SCL = 400 kHz | | 20 | | |
| | | | SCL = 3.4 MHz | | 100 | | |

## APPLICATION INFORMATION

The TMP100 and TMP101 are digital temperature sensors optimal for thermal management and thermal protection applications. The TMP100 and TMP101 are I²C and SMBus interface compatible and are specified over a temperature range of −55°C to +125°C.

The TMP100 and TMP101 require no external components for operation except for pullup resistors on SCL, SDA, and ALERT although a 0.1-μF bypass capacitor is recommended, as shown in Figure 1.




NOTE 2: SCL and SDA require pullup resistors for I²C bus applications.

**Figure 1. Typical Connections of the TMP100**

The die flag of the lead frame is connected to pin 2. The sensing device of the TMP100 and TMP101 is the chip itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path. The GND pin of the TMP100 or TMP101 is directly connected to the metal lead frame and is the best choice for thermal input.

To maintain the accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature. A thermally conductive adhesive assists in achieving accurate surface temperature measurement.

### pointer register

Figure 2 shows the internal register structure of the TMP100 and TMP101. The 8-bit pointer register of the TMP100 and TMP101 is used to address a given data register. The pointer register uses the two LSBs to identify which of the data registers should respond to a read or write command. Table 1 identifies the bits of the pointer register byte. Table 2 describes the pointer address of the registers available in the TMP100 and TMP101. Power-up reset value of P1/P0 is 00.

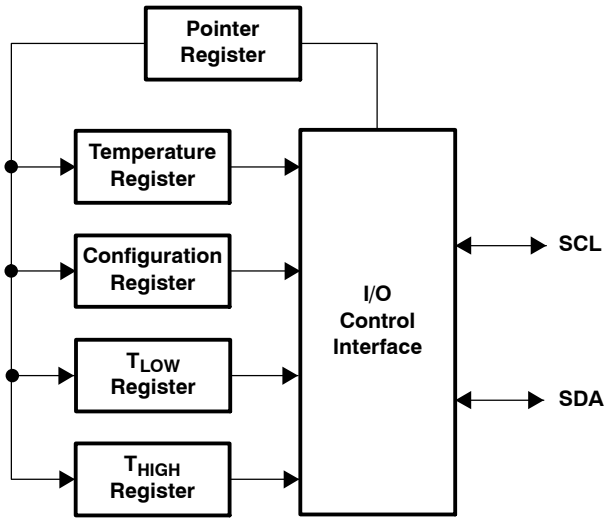



**Figure 2. Internal Register Structure of TMP100 and TMP101**

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Register Bits | |

**Table 1. Pointer Register Byte**

| P1 | P0 | REGISTER |
|---|---|---|
| 0 | 0 | Temperature Register (READ Only) |
| 0 | 1 | Configuration Register (READ/WRITE) |
| 1 | 0 | $T_{LOW}$ Register (READ/WRITE) |
| 1 | 1 | $T_{HIGH}$ Register (READ/WRITE) |

**Table 2. Pointer Addresses of the TMP100 Registers**

## APPLICATION INFORMATION

### temperature register

The temperature register of the TMP100 or TMP101 is a 12-bit read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data and are described in Table 3 and Table 4. The first 12 bits are used to indicate temperature with all remaining bits equal to zero. Data format for temperature is summarized in Table 5. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 |

**Table 3. Byte 1 of the Temperature Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| T3 | T2 | T1 | T0 | 0 | 0 | 0 | 0 |

**Table 4. Byte 2 of the Temperature Register**

| TEMPERATURE (°C) | DIGITAL OUTPUT (BINARY) | HEX |
|---|---|---|
| 128 | 0111 1111 1111 | 7FF |
| 127.9375 | 0111 1111 1111 | 7FF |
| 100 | 0110 0100 0000 | 640 |
| 80 | 0101 0000 0000 | 500 |
| 75 | 0100 1011 0000 | 4B0 |
| 50 | 0011 0010 0000 | 320 |
| 25 | 0001 1001 0000 | 190 |
| 0.25 | 0000 0000 0100 | 004 |
| 0.0 | 0000 0000 0000 | 000 |
| –0.25 | 1111 1111 1100 | FFC |
| –25 | 1110 0111 0000 | E70 |
| –55 | 1100 1001 0000 | C90 |
| –128 | 1000 0000 0000 | 800 |

**Table 5. Temperature Data Format**

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the configuration register and setting the resolution bits accordingly. For 9, 10, or 11 bit resolution, the most significant bits in the temperature register are used with the unused LSBs set to zero.

## APPLICATION INFORMATION

### configuration register

The configuration register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the configuration register for the TMP100 and TMP101 is shown in Table 6, followed by a breakdown of the register bits. The power-up/reset value of the configuration register is all bits equal to 0. The OS/ALERT bit will read as 1 after power-up/reset.

| Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 1 | OS/ALERT | R1 | R0 | F1 | F0 | POL | TM | SD |

**Table 6. Configuration Register Format**

### shutdown mode (SD)

The shutdown mode of the TMP100 and TMP101 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to less than 1 μA. For the TMP100 and TMP101, shutdown mode is enabled when the SD bit is 1. The device shutdowns once the current conversion is completed. For SD equal to 0, the device maintains continuous conversion.

### thermostat mode (TM)

The thermostat mode bit of the TMP101 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *high and low limit registers* and *SMBus alert function* sections.

### polarity (POL)

The polarity bit of the TMP101 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin will be active low as shown in Figure 3. For POL = 1, the ALERT pin will be active high and the state of the ALERT pin is inverted.

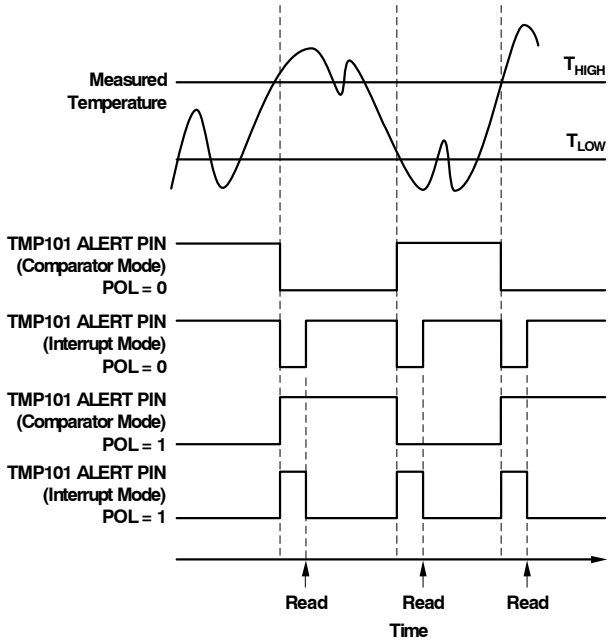



**Figure 3. Output Transfer Function Diagrams**

## APPLICATION INFORMATION

### fault queue (F1/F0)

A fault condition occurs when the measured temperature exceeds the limits set in the $T_{HIGH}$ and $T_{LOW}$ registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert due to environmental noise and requires consecutive fault measurements to trigger the alert function. Table 7 defines the number of measured faults that may be programmed to trigger an alert condition.

| F1 | F0 | CONSECUTIVE FAULTS |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |

**Table 7. Fault Settings of the TMP100 and TMP101**

### converter resolution (R1/R0)

The converter resolution bits control the resolution of the internal analog-to-digital (A/D) converter. This allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 8 identifies the resolution bits and relationship between resolution and conversion time.

| R1 | R0 | RESOLUTION | CONVERSION TIME (Typical) |
|---|---|---|---|
| 0 | 0 | 9 Bits (0.5°C) | 40 ms |
| 0 | 1 | 10 Bits (0.25°C) | 80 ms |
| 1 | 0 | 11 Bits (0.125°C) | 160 ms |
| 1 | 1 | 12 Bits (0.0625°C) | 320 ms |

**Table 8. Resolution of the TMP100**

### os/alert (OS)

The TMP100 and TMP101 feature a one-shot temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS/ALERT bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This is useful to reduce power consumption in the TMP100 and TMP101 when continuous monitoring of temperature is not required.

Reading the OS/ALERT bit provides information about the comparator mode status. The state of the POL bit will invert the polarity of data returned from the OS/ALERT bit. For POL = 0, the OS/ALERT reads as 1 until the temperature equals or exceeds $T_{HIGH}$ for the programmed number of consecutive faults, causing the OS/ALERT bit to read as 0. The OS/ALERT bit continues to read as 0 until the temperature falls below $T_{LOW}$ for the programmed number of consecutive faults when it again reads as 1. The status of the TM bit does not affect the status of the OS/ALERT bit.

## APPLICATION INFORMATION

### high and low limit registers

In comparator mode (TM = 0), the ALERT pin of the TMP101 becomes active when the temperature equals or exceeds the value in $T_{HIGH}$ and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated $T_{LOW}$ value for the same number of faults.

In Interrupt Mode (TM = 1) the ALERT Pin becomes active when the temperature equals or exceeds $T_{HIGH}$ for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs or the device successfully responds to the SMBus Alert Response Address. The ALERT pin will also be cleared if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below $T_{LOW}$. When the temperature falls below $T_{LOW}$, the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert Response Address. Once the ALERT pin is cleared, the above cycle repeats with the ALERT pin becoming active when the temperature equals or exceeds $T_{HIGH}$. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This also clears the state of the internal registers in the device returning the device to Comparator Mode (TM = 0).

The ALERT pin function for both operational modes is represented in Figure 3. Table 9 and Table 10 describe the format for the $T_{HIGH}$ and $T_{LOW}$ registers. Power-up reset values for $T_{HIGH}$ and $T_{LOW}$ are: $T_{HIGH}$ = 80°C and $T_{LOW}$ = 75°C. The format of the data for $T_{HIGH}$ and $T_{LOW}$ is the same as for the temperature register.

All 12 bits for the temperature, $T_{HIGH}$, and $T_{LOW}$ registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in $T_{HIGH}$ and $T_{LOW}$ can affect the ALERT output even if the converter is configured for 9-bit resolution.

| Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 1 | H11 | H10 | H9 | H8 | H7 | H6 | H5 | H4 |

| Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 2 | H3 | H2 | H1 | H0 | 0 | 0 | 0 | 0 |

**Table 9. Bytes 1 and 2 of $T_{HIGH}$ Register**

| Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 1 | L11 | L10 | L9 | L8 | L7 | L6 | L5 | L4 |

| Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 2 | L3 | L2 | L1 | L0 | 0 | 0 | 0 | 0 |

**Table 10. Bytes 1 and 2 of $T_{LOW}$ Register**

## APPLICATION INFORMATION

### serial interface

The TMP100 and TMP101 operate only as slave devices on the I²C bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The TMP100 and TMP101 support the transmission protocol for fast (up to 400 kHz) and high-speed (up to 3.4 MHz) modes. All data bytes are transmitted most significant bit first.

### serial bus address

To program the TMP100 and TMP101, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP100 features two address pins to allow up to eight devices to be addressed on a single I²C interface. Table 11 describes the pin logic levels used to properly connect up to eight devices. *Float* indicates the pin is left unconnected. The state of pins ADD0 and ADD1 is sampled on the first I²C bus communication and should be set prior to any activity on the interface.

| ADD1 | ADD0 | SLAVE ADDRESS |
|---|---|---|
| 0 | 0 | 1001000 |
| 0 | Float | 1001001 |
| 0 | 1 | 1001010 |
| 1 | 0 | 1001100 |
| 1 | Float | 1001101 |
| 1 | 1 | 1001110 |
| Float | 0 | 1001011 |
| Float | 1 | 1001111 |

**Table 11. Address Pins and Slave Addresses for TMP100**

The address pins of the TMP100 and TMP101 are read after reset or in response to an I²C address acquire request. Following a read, the state of the address pins is latched to minimize power dissipation associated with detection.

## APPLICATION INFORMATION

### bus overview

The device that initiates the transfer is called a *master* and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a high-to-low logic level while SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high, as any change in SDA while SCL is high will be interpreted as a control signal. Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from low-to-high, while SCL is high.

### writing/reading to the TMP100 and TMP101

Accessing a particular register on the TMP100 and TMP101 is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the I²C slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP100 and TMP101 requires a value for the pointer register. (See Figure 5.)

When reading from the TMP100 and TMP101, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This is accomplished by issuing an I²C slave address byte with the R/$\overline{W}$ bit low, followed by the pointer register byte. No additional data is required. The master can then generate a START condition and send the I²C slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 6 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the pointer register bytes as the TMP100 and TMP101 remembers the pointer register value until it is changed by the next write operation.

### slave mode operations

The TMP100 and TMP101 can operate as slave receivers or slave transmitters.

#### *slave receiver mode*

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP100 or TMP101 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP100 or TMP101 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP100 and TMP101 acknowledge reception of each data byte. The master may terminate data transfer by generating a START or STOP condition.

#### *slave transmitter mode*

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master may terminate data transfer by generating a not-acknowledge on reception of any data byte, or generating a START or STOP condition.

## APPLICATION INFORMATION

### SMBus alert function

The TMP101 supports the SMBus Alert function. When the TMP101 is operating in Interrupt Mode (TM = 1), the ALERT pin of the TMP101 may be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP101 is active, the TMP101 acknowledges the SMBus Alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding $T_{HIGH}$ or falling below $T_{LOW}$ caused the ALERT condition. For POL = 0, this bit will be LOW if the temperature is greater than or equal to $T_{HIGH}$. This bit will be HIGH if the temperature is less than $T_{LOW}$. The polarity of this bit will be inverted if POL = 1. See Figure 7 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus alert command determines which device clears its ALERT status. If the TMP101 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP101 loses the arbitration, its ALERT pin remains active.

The TMP100 also responds to the SMBus ALERT command if its TM bit is set to 1. Since it does not have an ALERT pin, the master needs to periodically poll the device by issuing an SMBus Alert command. If the TMP100 has generated an ALERT, it acknowledges the SMBus Alert command and returns its slave address in the next byte.

### general call

The TMP100 and TMP101 respond to the I²C General Call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000100, the TMP100 and TMP101 latch the status of their address pins, but will not reset. If the second byte is 00000110, the TMP100 and TMP101 latch the status of their address pins and reset their internal registers.

### high-speed mode

In order for the I²C bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP100 and TMP101 will not acknowledge this byte as required by the I²C specification, but switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4 MHz. After the Hs-mode master code has been issued, the master transmits an I²C slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP100 and TMP101 switch their input and output filters back to fast-mode operation.

### timing diagrams

The TMP100 and TMP101 are I²C and SMBus compatible. Figure 4 through Figure 7 describe the various operations on the TMP100 and TMP101. Bus definitions are given below. Parameters for Figure 4 are defined in Table 12.

**Bus Idle:** Both SDA and SCL lines remain high.

**Start Data Transfer:** A change in the state of the SDA line, from high-to-low, while the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from low-to-high while the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

**Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

## APPLICATION INFORMATION

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a not-acknowledge on the last byte that has been transmitted by the slave.

| PARAMETER | | FAST MODE | | HIGH-SPEED MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $f_{(SCLK)}$ | SLCK operating frequency | | 0.4 | | 3.4 | MHz |
| $t_{(BUF)}$ | Bus free time between STOP and START condition | 600 | | 160 | | ns |
| $t_{h(STA)}$ | Hold time after repeated START condition. After this period, the first clock is generated. | 600 | | 160 | | ns |
| $t_{su(STA)}$ | Repeated START condition setup time | 600 | | 160 | | ns |
| $t_{su(STO)}$ | STOP condition setup time | 600 | | 160 | | ns |
| $t_{h(DAT)}$ | Data hold time | 0 | | 0 | | ns |
| $t_{su(DAT)}$ | Data setup time | 100 | | 10 | | ns |
| $t_{(LOW)}$ | SCLK clock low period | 1300 | | 160 | | ns |
| $t_{(HIGH)}$ | SCLK clock high period | 600 | | 60 | | ns |
| $t_f$ | Clock/data fall time | | 300 | | 160 | ns |
| $t_r$ | Clock/data rise time | | 300 | | 160 | ns |

**Table 12. Timing Diagram Definitions**

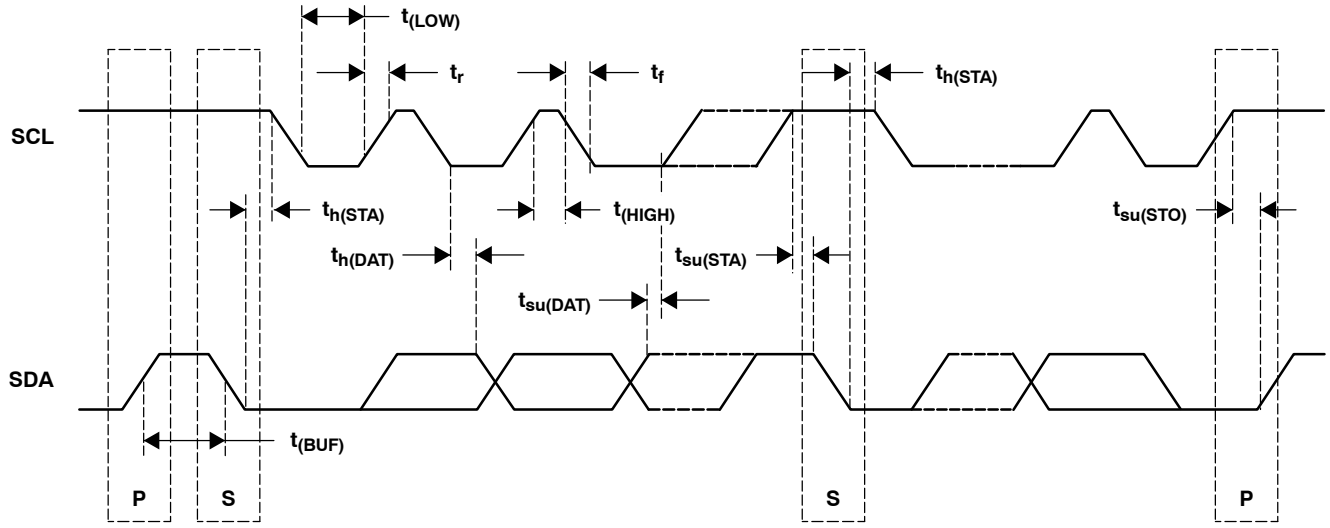



**Figure 4. I²C Timing Diagram**

## APPLICATION INFORMATION

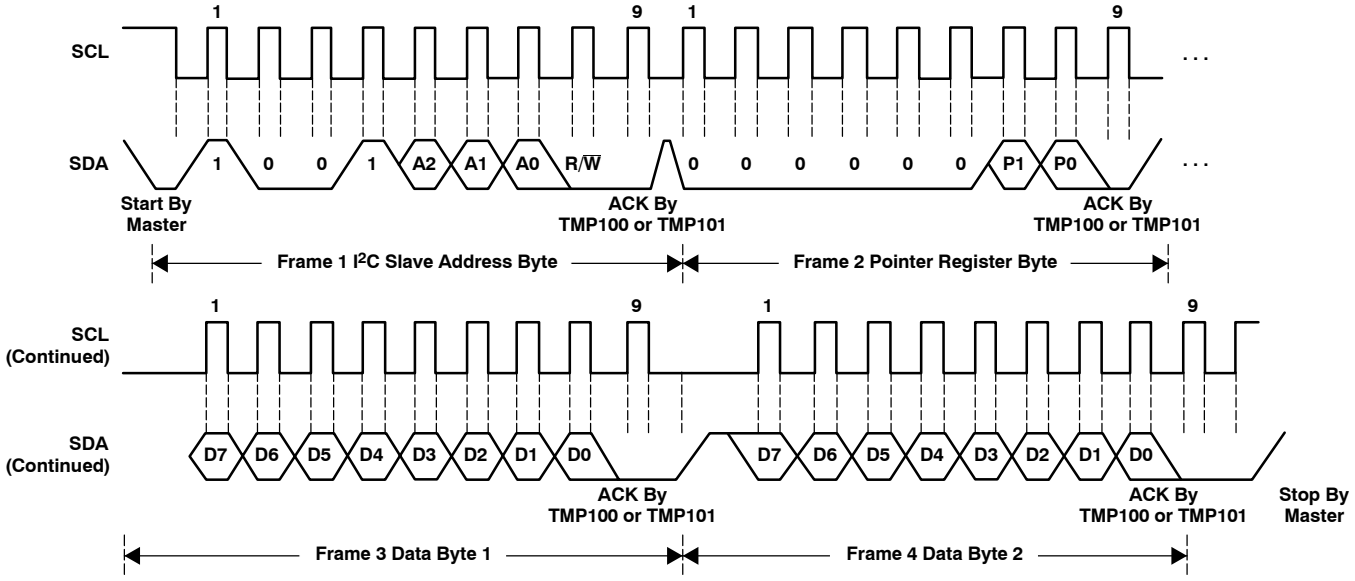



**Figure 5. I²C Timing Diagram for Write Word Format**

## APPLICATION INFORMATION

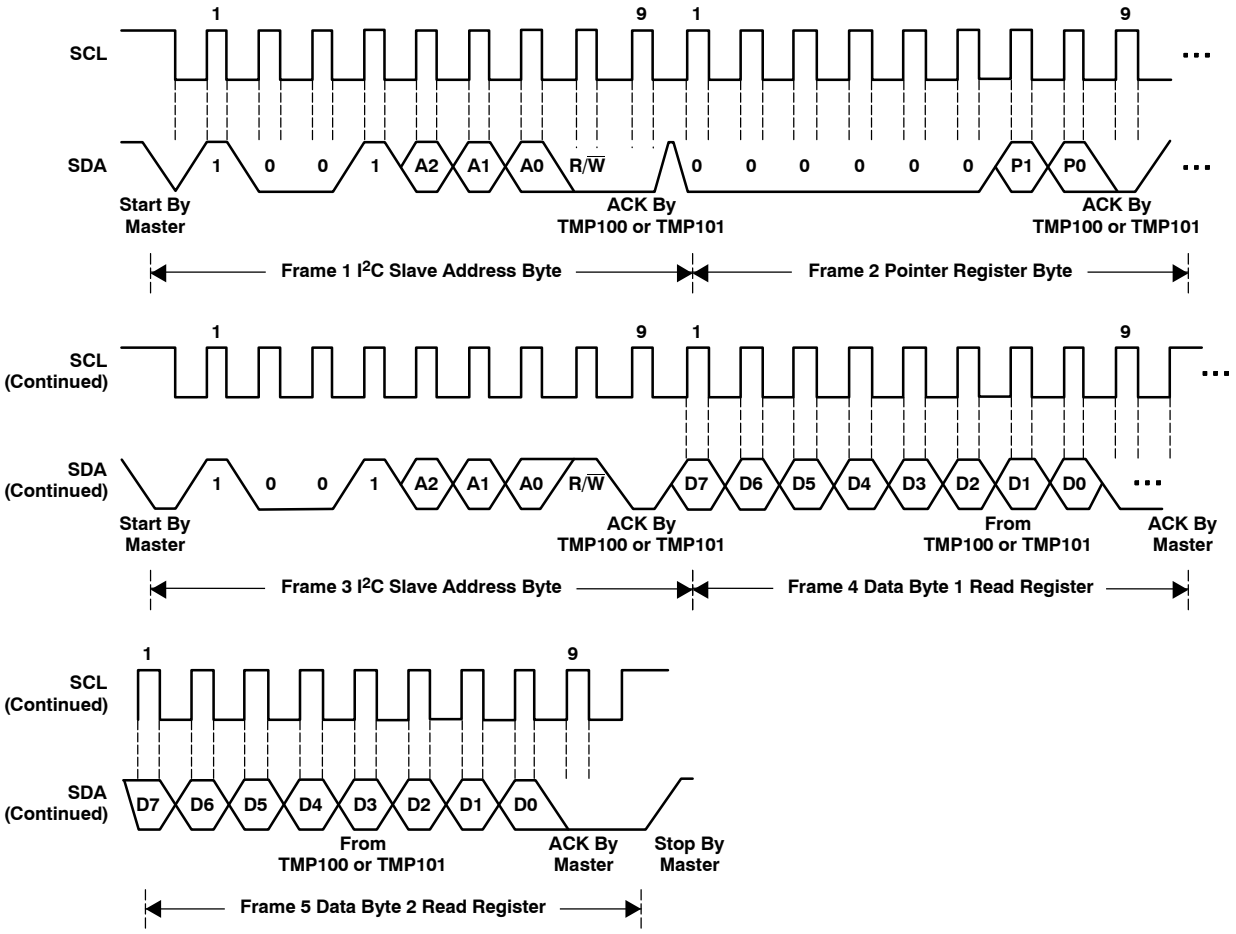



**Figure 6. I²C Timing Diagram for Read Word Format**

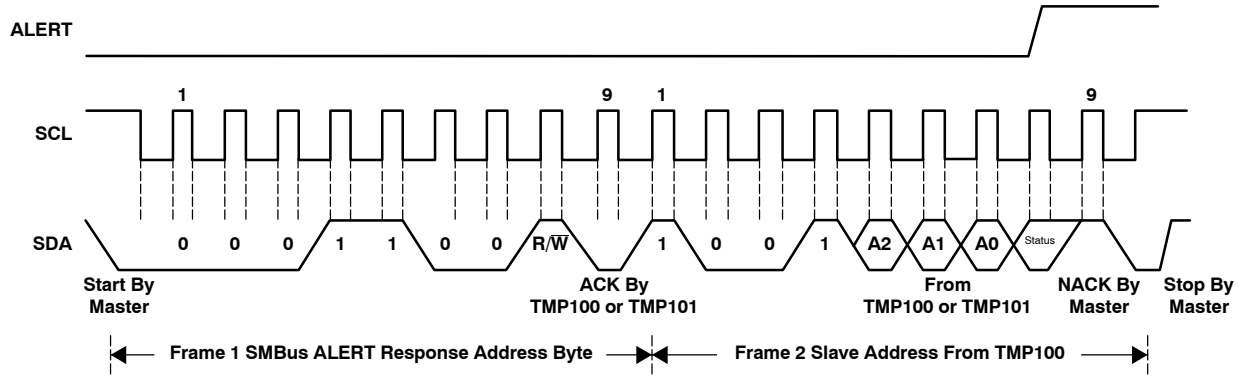



**Figure 7. Timing Diagram for SMBus ALERT**

## TYPICAL CHARACTERISTICS, at $T_A$ = 25°C, V+ = 5 V, UNLESS OTHERWISE NOTED

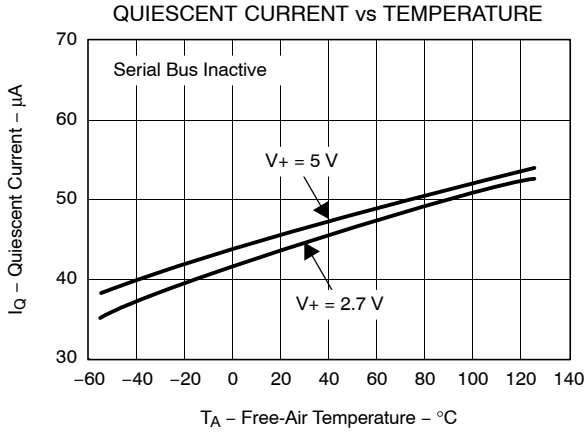



**Figure 8**

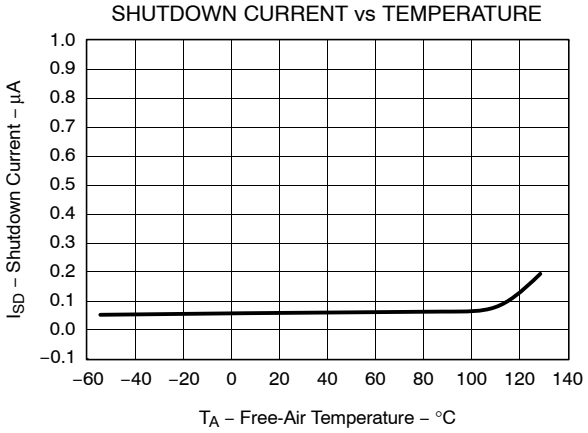



**Figure 9**

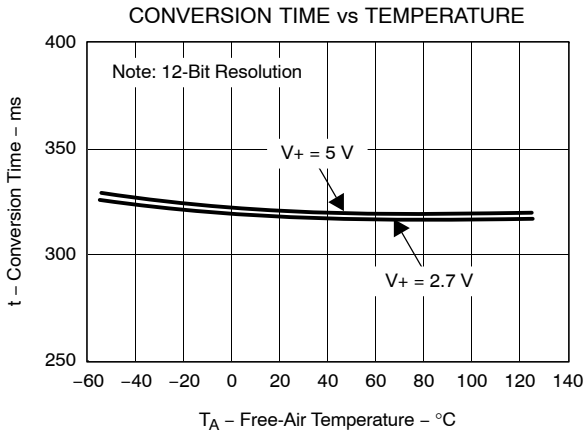



**Figure 10**

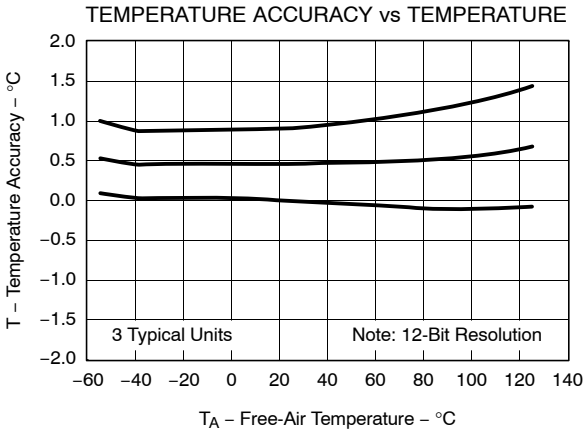



**Figure 11**

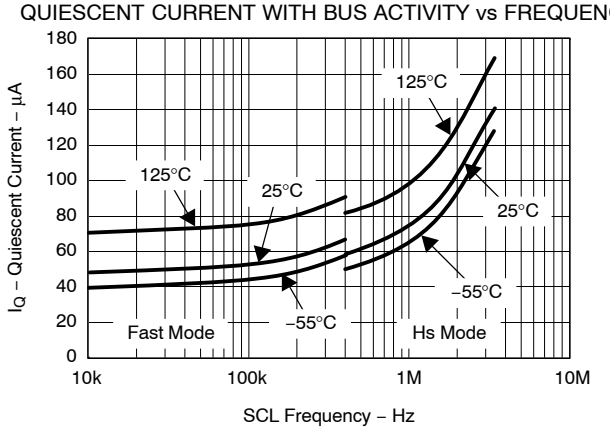



**Figure 12**

## Revision History

| DATE | REV | PAGE | SECTION | DESCRIPTION |
|---|---|---|---|---|
| 10–04–13 | B | 10 | serial bus address | deleted Table 12 and first 2 sentences in paragraph above the table |
| 09–30–13 | B | Document | Multiple sections throughout document | Changed to Rev B October 2013.<br>Corrected only what was marked in red. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP100MDBVREP | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 100E | Samples |
| V62/05618-01XE | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -55 to 125 | 100E | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF TMP100-EP :**

- Catalog: TMP100
- Automotive: TMP100-Q1

NOTE: Qualified Version Definitions:

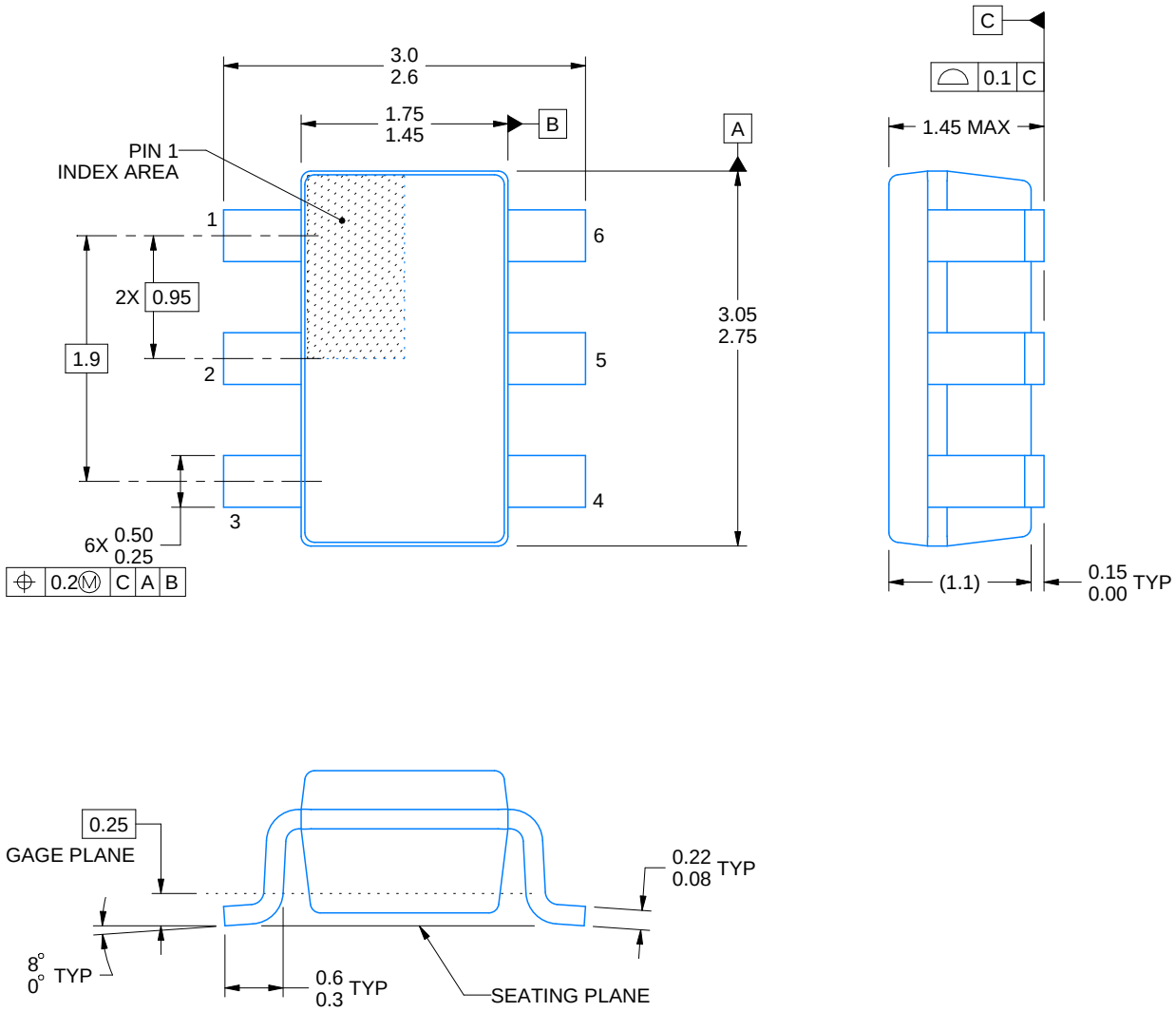
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

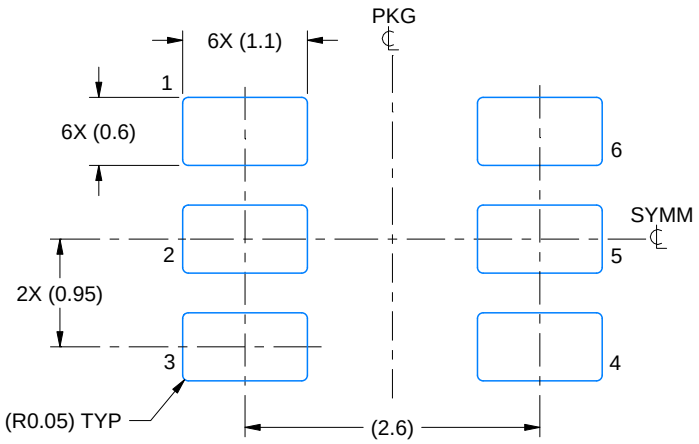
SMALL OUTLINE TRANSISTOR



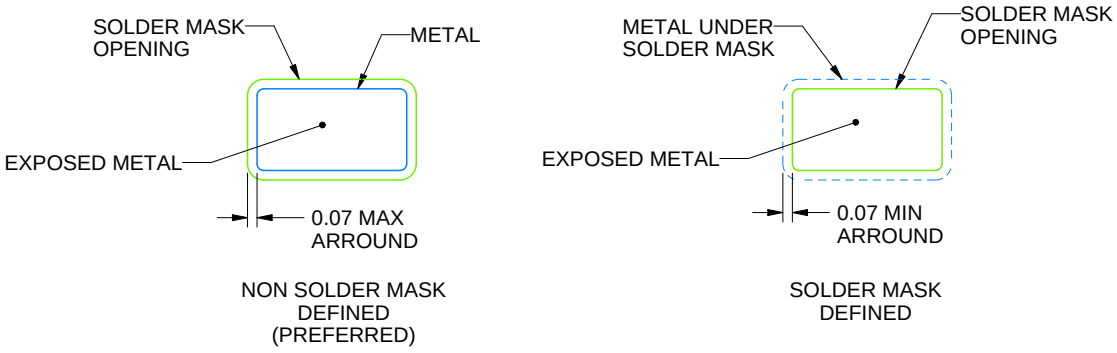

4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

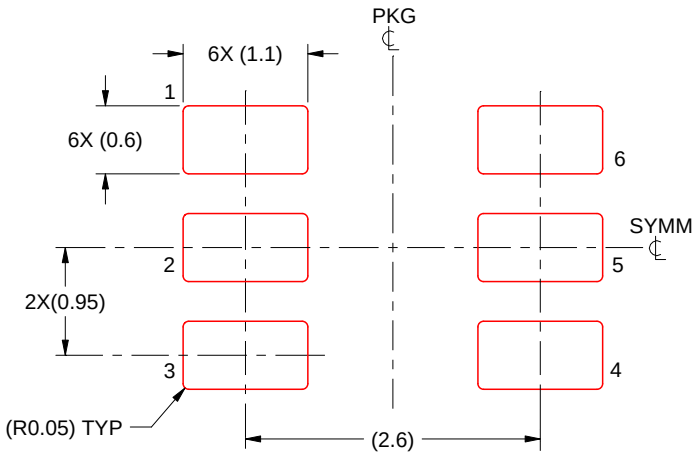



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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