TMP1820 1-Wire®, 1.7-V to 5.5-V Bus Powered Supply, ±0.3°C Accurate Digital Temperature Sensor

ADVANCE INFORMATION

1 Features

- Multi-drop shared bus for data communication features
  - 1-Wire interface
  - Standard and overdrive data rates modes (up to 90 kbps)
  - Legacy and short addressing
  - Cyclic redundancy check (CRC)
- Flexible power supply option: V_{DD} (supply) powered or bus powered
  - 1.7 V to 5.5 V (OVD mode or bus powered)
  - 2.5 V to 5.5V (STD mode)
- High accuracy temperature sensor:
  - ±0.1°C (typical) from –20°C to +85°C
  - ±0.3°C (maximum) from –20°C to +85°C
  - ±0.4°C (maximum) from –55°C to +125°C
- 12-bit temperature resolution: 62.5 m°C (1 LSB)
- Low power
  - Active current: 85 µA (typical)
  - Shutdown current: 1.6 µA (typical)
  - Average current: 3.85 µA at 1Hz duty cycle
  - Fast conversion time: 27 ms (maximum)
- Safety and compliance
  - NIST traceable
  - Factory programmed non erasable 64-bit identification number for device addressing
  - IEC 61000-4-2 ESD: 8kV contact discharge

2 Applications

- Factory Automation and control
  - Temperature Transmitter
  - PLC, DCS & PAC
- Medical
  - CPAP machine
  - Electronic hospital bed & bed control
- Grid Infrastructure
  - EV charging infrastructure
  - Wired communication modules
- Appliances
  - Refrigerator & freezer
  - Air conditioner outdoor unit
  - Merchant battery charger
- Building Automation
  - HVAC motor control

3 Description

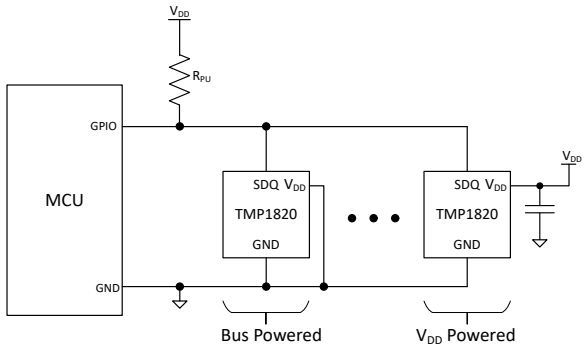
The TMP1820 is 1-Wire®, high-accuracy, digital-output temperature sensor. The accuracy is as high as ±0.1°C across the –20°C to +85°C or ±0.4°C across the –55°C to +125°C temperature range. Each device incorporates a factory-programmed 64-bit unique identification number used for addressing and allows NIST traceability. The 1-Wire® interface supports both a standard communication mode for legacy applications and an overdrive mode (with up to 90 kbps data rate) for faster communication present in modern applications. Overdrive mode also allows the user to lower the bus power to as low as 1.7V over the entire temperature range.

For the simplest mode of operation, the TMP1820 1-Wire® interface only requires a single connection and a ground return for bus-powered mode. The combination of unique ID and bus-powered operation can lead to cabling simplifications, which can reduce solution complexity and cost. In applications that require the absolute lowest power consumption, a VDD power pin also available if a dedicated power supply is available. Additionally, the low-noise and precision of the TMP1820 can reduce the power consumption of one-sample applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMP1820	LPG (TO-92, 3)	4.00 mm × 1.52 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2023	*	Initial release.

5 Pin Configuration and Functions

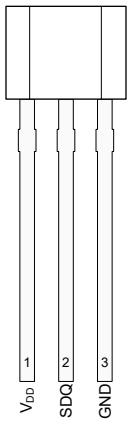

Figure 5-1. LPG 3-Pin TO-92 — Front View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	TO-92		
GND	3	—	Ground
SDQ	2	I/O	Serial bidirectional data. In bus-powered mode the pin is used to power the internal capacitor
V_{DD}	1	I	Supply voltage in V_{DD} powered mode. In bus-powered mode, this pin must be connected to ground.

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6 Specifications

6.1 Absolute Maximum Ratings

Over free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD}		6.5	V
I/O voltage	SDQ, Bus-powered mode	–0.3	6.5	V
	SDQ, Supply-powered mode	–0.3	V_{DD} + 0.3	
Operating junction temperature, T_J		-55	150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	V
		IEC 61000-4-2 Contact Discharge	SDQ pin	±8000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage V_{DD} powered mode		1.70		5.5	V
V_{PUR}	Pullup Resistor (PUR) voltage on SDQ in bus-powered mode (V_{DD} = GND)	Standard mode	2.5		5.5	V
		Overdrive mode	1.7		5.5	V
$V_{I/O}$	SDQ pin in V_{DD} powered mode		0		5.5	V
T_A	Operating ambient temperature(1)		-55		150	°C

(1) In bus-powered mode, overdrive speed supports the maximum operating temperature up to 150°C, while standard speed supports up to 125°C for full V_{PUR} range and 150°C for V_{PUR} > 2.5V. In practice the temperature is limited to 125°C due to the 12-bit resolution

6.4 Thermal Information

THERMAL METRIC(1)		TMP1820 LPG (TO-92) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	99.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	99.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	NA	°C/W
M_T	Thermal Mass	34.2	mJ/°C

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over free-air temperature range and V_{DD} = 1.7 V to 5.5 V (unless otherwise noted); Typical specifications are at T_A = 25 °C and V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR							
T_{ERR}	Temperature accuracy	-20°C to 85°C			±0.1	±0.3	°C
		-55°C to 125°C				±0.4	
PSR	DC power supply sensitivity					±0.03	°C/V
T_{RES}	Temperature resolution	Including sign bit			12		Bits
		LSB			62.5		m°C
T_{REPEAT}	Repeatability(1)	V_{DD} = 3.3 V 1-Hz conversion interval, 300 acquisition			±1		LSB
T_{LTD}	Long-term stability and drift	1000 hours at 125°C(2)			0.0625		°C
T_{HYST}	Temperature cycling and hysteresis	T_{START} = -40°C T_{FINISH} = 125°C T_{TEST} = 25°C 3 cycles			4		LSB
t_{RESP_L}	Response time (Stirred Liquid)	τ = 63 % 25°C to 75°C			TBD		s
t_{ACT}	Active Conversion time			TBD		27	ms
t_{DELAY}	Start-up delay for temperature conversion			100		300	µs
SDQ DIGITAL INPUT/OUTPUT							
C_{IN}	SDQ pin capacitance				40		pF
V_{IL}	Input logic low level(3)			–0.3		0.2 × V_{DD}	V
V_{IH}	Input logic high level(3)			0.8 × V_{DD}		V_{DD} + 0.3	V
V_{HYST}	Hysteresis				0.3		V
I_{IN}	Input leakage current				±0.5	TBD	µA
V_{OL}	Output low level	I_{OL} = –4 mA				0.4	V
POWER SUPPLY							
I_{DD_ACTIVE}	Supply current during temperature conversion	Temperature Conversion, serial bus inactive			85	TBD	µA
I_{DD_SD}	Shutdown current	Serial bus inactive, one shot conversion mode	T_A = -40°C to 85°C		1.6	TBD	µA
			T_A = -40°C to 125°C			TBD	
V_{POR}	Power-on reset threshold voltage	Supply rising		1.5			V
V_{POR}	Brownout detect	Supply falling				1.3	V
t_{INIT}	Reset Initialization Time	Time required by device to reset after power up				2	ms

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) Long term stability is determined using accelerated operational life testing at a junction temperature of 150 °C.
(3) In bus powered mode, the supply voltage is V_{PUR}. In supply powered mode, the supply voltage is V_{DD}.

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6.6 1-Wire Interface Timing

Over free-air temperature range and V_{DD} = 1.7 V to 5.5 V in overdrive mode or V_{DD} = 2.5 V to 5.5 V in standard mode (unless otherwise noted)

		STANDARD MODE		OVERDRIVE MODE		UNIT
		MIN	MAX	MIN	MAX	
BUS RESET AND BIT SLOT TIMING						
t_{RSTL}	Host to device bus reset pulse width (1)	480	560	48	80	µs
t_{RSTH}	Device to host response time(2)	480		48		µs
t_{PDH}	Device turnaround time for bus reset response	15	60	2	8	µs
t_{PDL}	Device to host response pulse width	60	240	8	24	µs
t_{SLOT}	Bit slot time	t_{WR0L} + t_{RC}		t_{WR0L} + t_{RC}		µs
t_{REC}	Recovery time	2		2		µs
t_{GF}	Glitch filter width (3)	0.48		0.025		µs
t_F	Fall time		100		100	ns
BIT WRITE TIMING						
t_{WR0L}	Host write 0 width	60	120	9	10	µs
t_{WR1L}	Host write 1 width	2	15	1	2	µs
t_{RDV}	Device read data valid time	15		2		µs
t_{DSW}	Device read data window	15	45	2	7	µs
BIT READ TIMING						
t_{RL}	Host drive read bit slot time (4)	2	5	2	3	µs
t_{RWAIT}	Host wait time before read data sampling window(5)		t_{RL}+t_{RC}		t_{RL}+t_{RC}	µs
t_{MSW}	Host read data sampling window	t_{RL}+t_{RC}	30	t_{RL}+t_{RC}	3	µs

(1) In bus-powered mode, extending the t_{RSTL} above 600 µs may cause the device to power-on reset
(2) The t_{RSTH} is the maximum time the host must wait to receive a response from the furthest device, taking into account the propagation delay and recovery time for all the devices.
(3) The glitch filter timing applies only on the rising edge of the SDQ signal
(4) t_{RL} minimum time includes the glitch filter timing.
(5) The t_{RC} time is defined as the time taken for the bus voltage to rise from 0V to minimum V_{IH} of the host. This is a function of the bus pullup resistor, devices and parasitic capacitance of the trace or cable. The parameter must be characterized for the application.

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6.7 Timing Diagrams

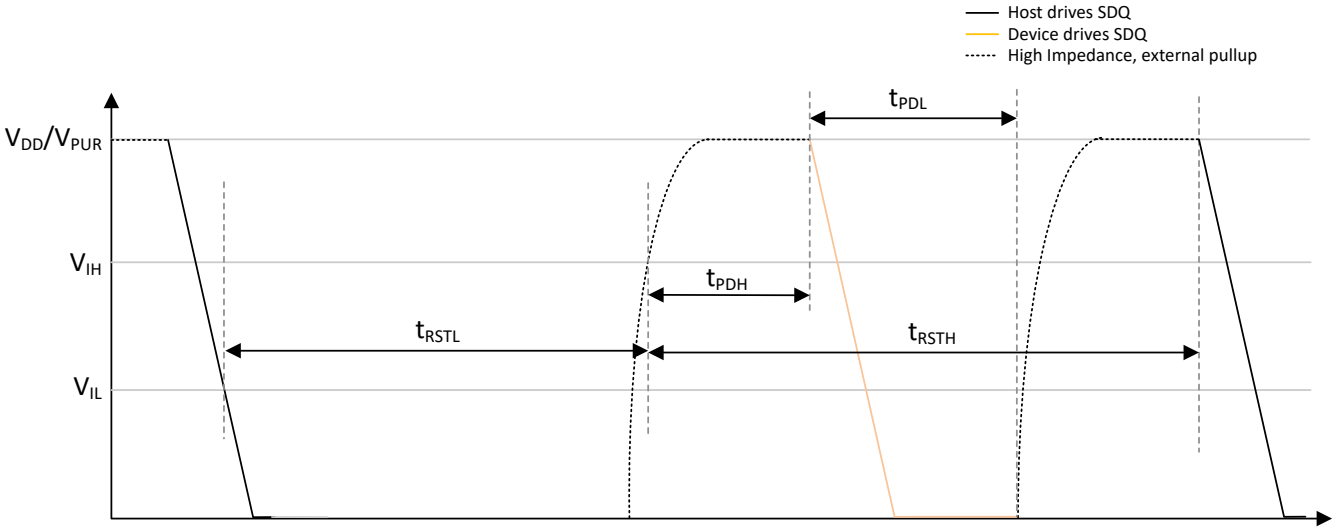

Figure 6-1. Bus Reset Timing Diagram

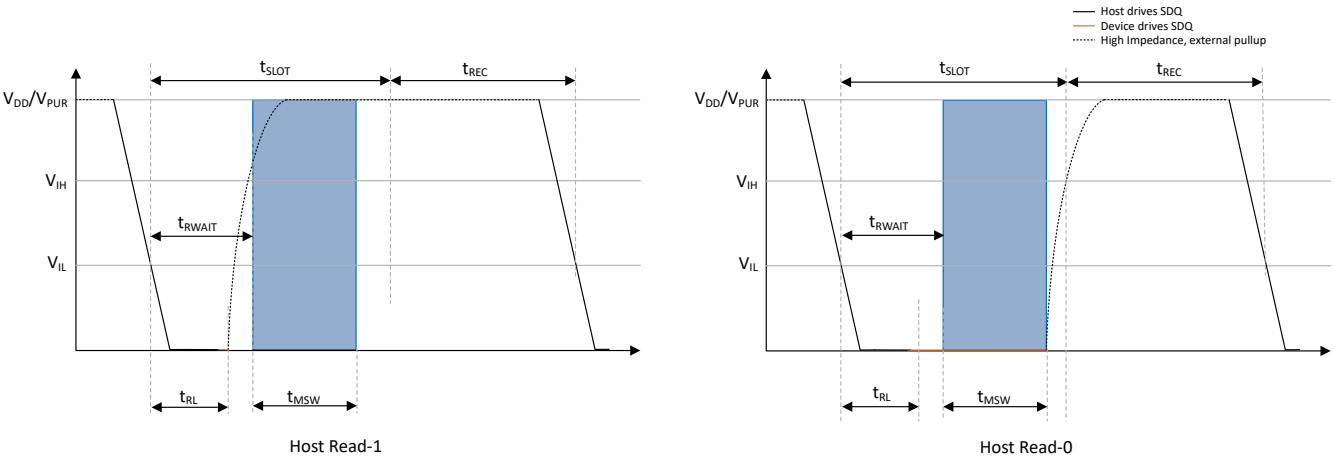

Figure 6-2. Read Timing Diagram

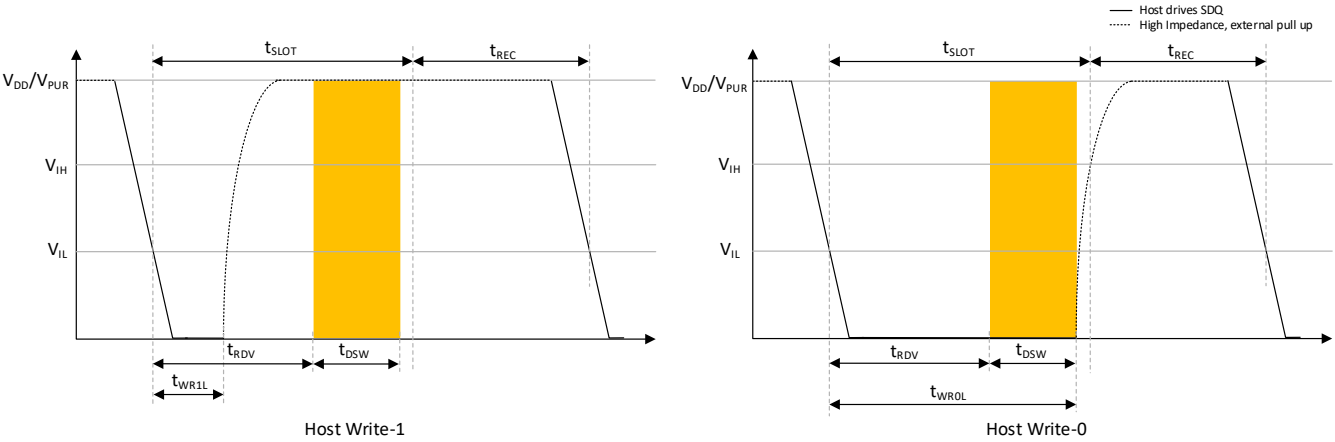

Figure 6-3. Write Timing Diagram

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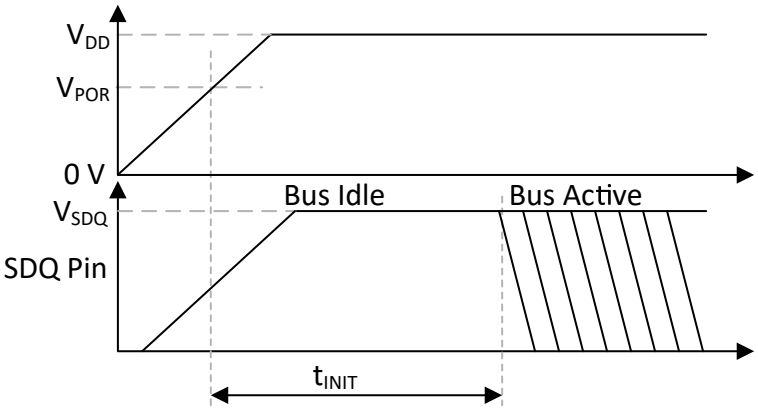

Figure 6-4. V_{DD} Powered Initialization Timing Diagram

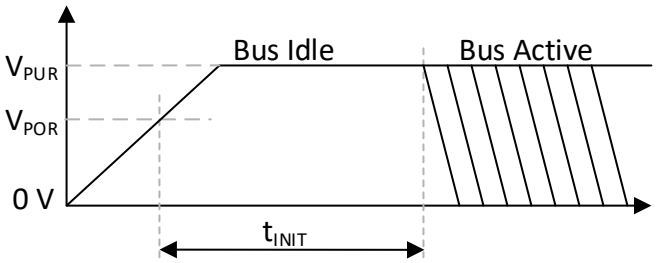

Figure 6-5. Bus Powered Initialization Timing Diagram

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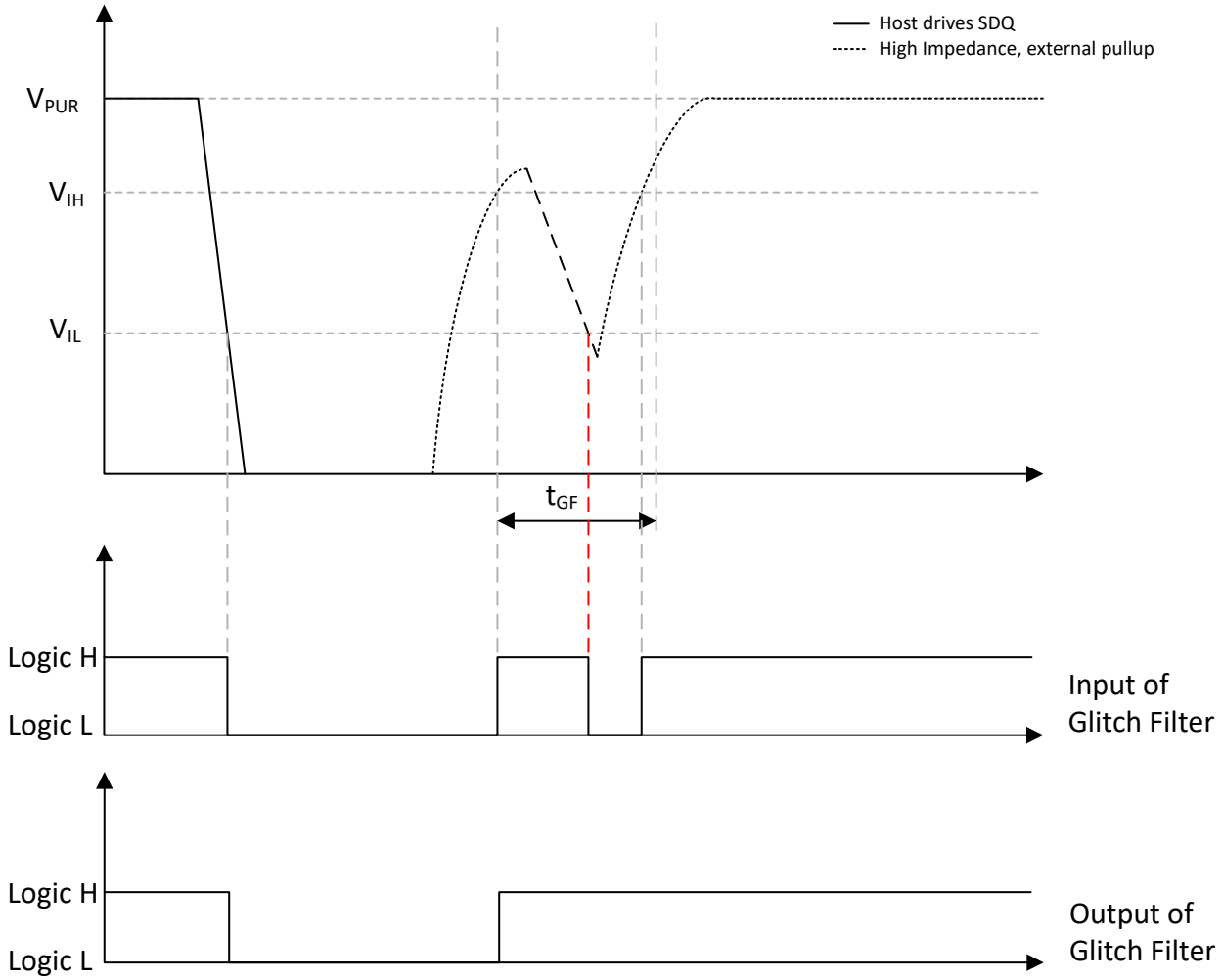

Figure 6-6. Glitch Filter Timing Diagram

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7 Detailed Description

7.1 Overview

The TMP1820 is a digital-output temperature sensor designed for thermal-management and thermal-protection applications. This temperature sensor implements a 1-Wire interface capable of operating powered either from the supply (referred to as supply-powered) or from the bus (referred to as bus-powered or parasitic powered). Figure 7-1 shows the block diagram.

7.2 Functional Block Diagram

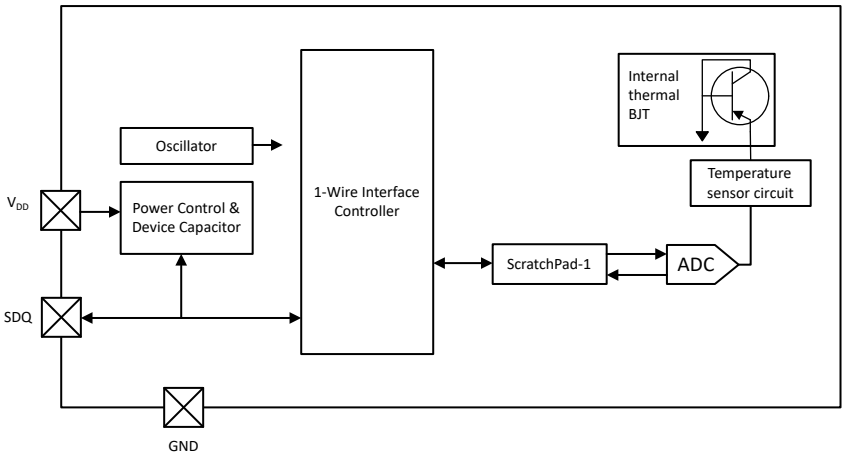

Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Power Up

The device operates in either supply-powered or bus-powered mode. A steady power supply is required during the initialization time (t_{INIT}). Irrespective of the powering mode, when the supply voltage reaches the POR voltage, the initialization time of t_{INIT} is required to allow the initialization reset to complete. After the initialization period, the host MCU can begin accessing the device. Note that after initialization, the bus is ready to operate in overdrive mode.

During initialization, the device may not respond to any bus activity. In this phase, ringing or bouncing on SDQ pin can be considered as a standard mode reset pulse and move device out from the OVD mode, and as such should be avoided. After the initialization is complete, the device waits for the bus reset that is initiated by the host. If the host issues a standard speed reset, the TMP1820 automatically switches to standard mode.

7.3.2 Power Mode Switch

The device is designed to operate in both supply-powered and bus-powered mode. The dual mode implementation provides a unique method of redundancy. In case the power supply pin is disconnected, the device can draw power from the SDQ pin, given the proper pullup resistor value. See *Bus Pullup Resistor* for additional information.

In bus-powered mode, observed behavior will be the same as those of the supply-powered mode. The only limitation is the internal capacitor discharge and recharge cycle as operating current is drawn during active communication and recharged through the external pullup resistor during bus up time. If the internal voltage on the capacitor drops below the brownout threshold, the device resets itself and enters bus-powered mode on subsequent power up. The device will not complete any previously started communication during this initialization. After the device completes the POR and initialization sequence, the device will respond to the first bus communication starting with the reset sequence.

7.3.3 Bus Pullup Resistor

Carefully consider the selection of the bus pullup resistor to minimize:

1. Power consumption at the system level
2. EMI generated by SDQ pin current
3. Increase in temperature due to self-heating

Operating with a low impedance pullup resistor is possible, however this choice can negate the benefits of having a low quiescent current device (for example: 2 µA), can generate EMI due to the combination of high current (for example: 4 mA on the SDQ pin) with high logic transition-speed and smaller return lines (or GND traces), and create self-heating in the device (for example: 4 mA × 0.25 V × 180°C/W = 0.18°C junction temperature rise - this temperature rise happens only when the device pulls the SDQ pin down during host read/device write bit communication) affecting accuracy.

7.3.3.1 Bus-Powered Mode Versus Supply-Powered Mode

The pullup resistor value in V_{DD} supply mode can be much higher than value used in bus supply mode because the conversion current flows into the sensor through the V_{DD} pin but not through the SDQ. From a power saving point, the supply-powered mode is better than bus-powered mode.

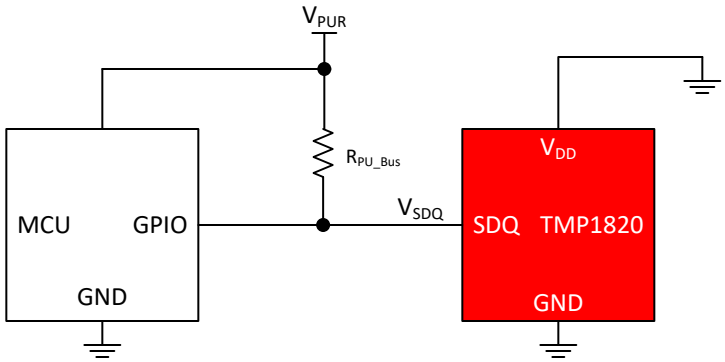

Figure 7-2. Bus-Powered Mode

Consider the total bus capacitance (SDQ pin(s) & line parasitic) along with the bus leakage current when selecting the pullup resistor. Select the pullup resistance value with the timing requirement in mind and allow V_{IH} signal level to be reached for either standard or overdrive mode. Note that the SDQ digital level high is set for voltages greater than 0.8x V_{DD} and that the SDQ pin digital level low is set for voltages lower than 0.2x V_{DD}.

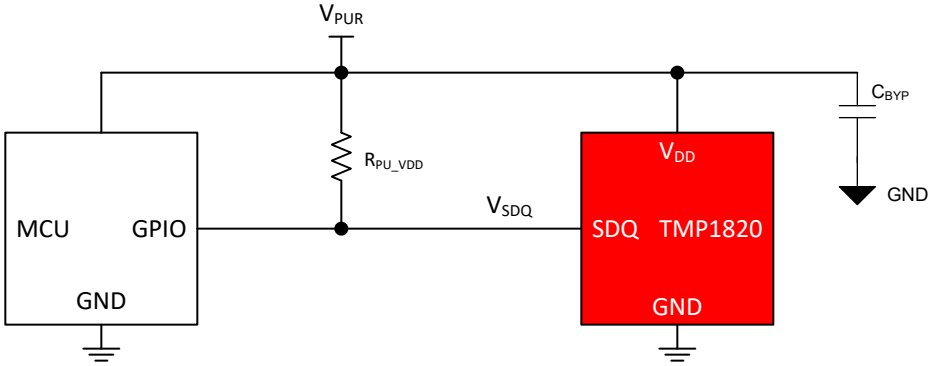

Figure 7-3. Supply-Powered Mode

When powering the TMP1820 using the supply-power mode, voltage variations on the SDQ pin to detect the logic level are only dependent on the V_{DD} supply variations. Take proper care to the power supply selection. Refer to *Power Supply Recommendations* for additional information.

7.3.3.2 Design Constraints for Bus-Powered Mode With Single Device Present on Bus

In bus-powered mode of operation, the device charges an internal capacitor through the SDQ pin and the pullup resistor to supply the power to the IC. This charge on the capacitor is used during bus communication when the SDQ pin is low. The SDQ pin is also used to communicate with the device and acquire the temperature. During

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temperature conversion, the bus must be held high to allow sufficient current through the pullup resistor. The SDQ pin voltage during the high current operation must be maintained to allow sufficient operating margins. Use Equation 1 to calculate the pullup resistor value.

$$V_{PUR} - I_{R_{PU\_Bus}} \times R_{PU\_Bus} > 1.6\ V \quad (1)$$

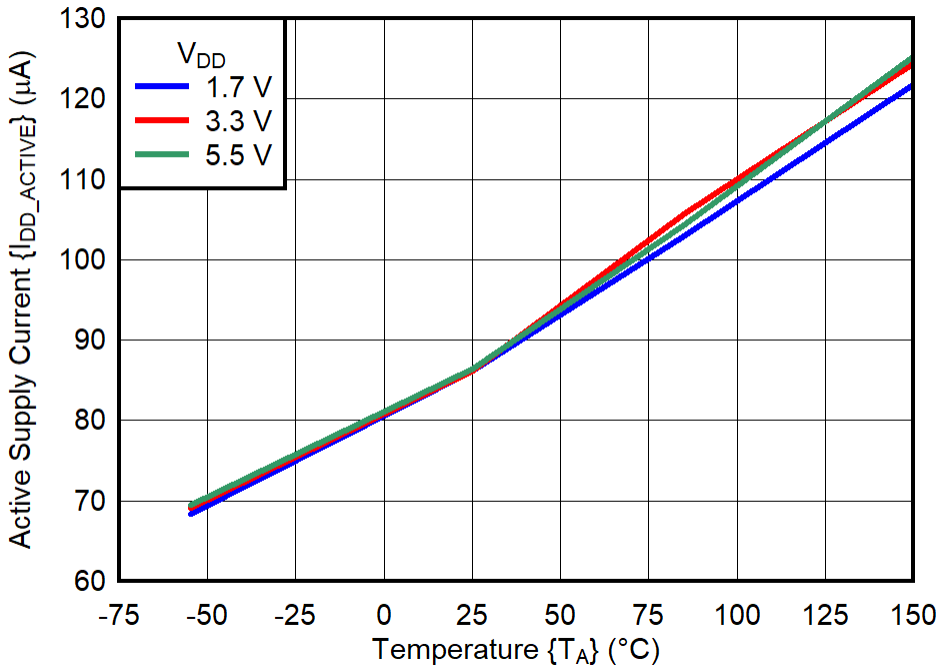

Figure 7-4. Supply Current During Temperature Conversion

7.3.3.3 Design Constraints for Bus-Powered Mode With Multiple Devices Present on Bus

If multiple devices are on the bus during bus-powered mode, another constraint is added to the example due to the threshold level. As mentioned in the previous section, the device charges an internal capacitor through the SDQ pin and the pullup resistor to supply the power to the IC. This charge on the capacitor is used during bus communication when the SDQ pin is low. During temperature conversion, the bus must be held idle to allow sufficient current through the pullup resistor. However, because there are other devices present on the bus, the SDQ pin voltage must not go below 0.8x V_{DD}. Otherwise, the bus can be reset by one of the other devices. The SDQ pin voltage during the high current operation must be maintained to allow sufficient operating margins. This behavior is describe in *Bus Pullup Resistor*. The pullup resistor must now also satisfy Equation 2.

$$V_S - N \times I_{R_{PU\_Bus}} \times R_{PU\_Bus} > 0.8\ \times V_{PUR} \quad (2)$$

where N: number of devices present on bus

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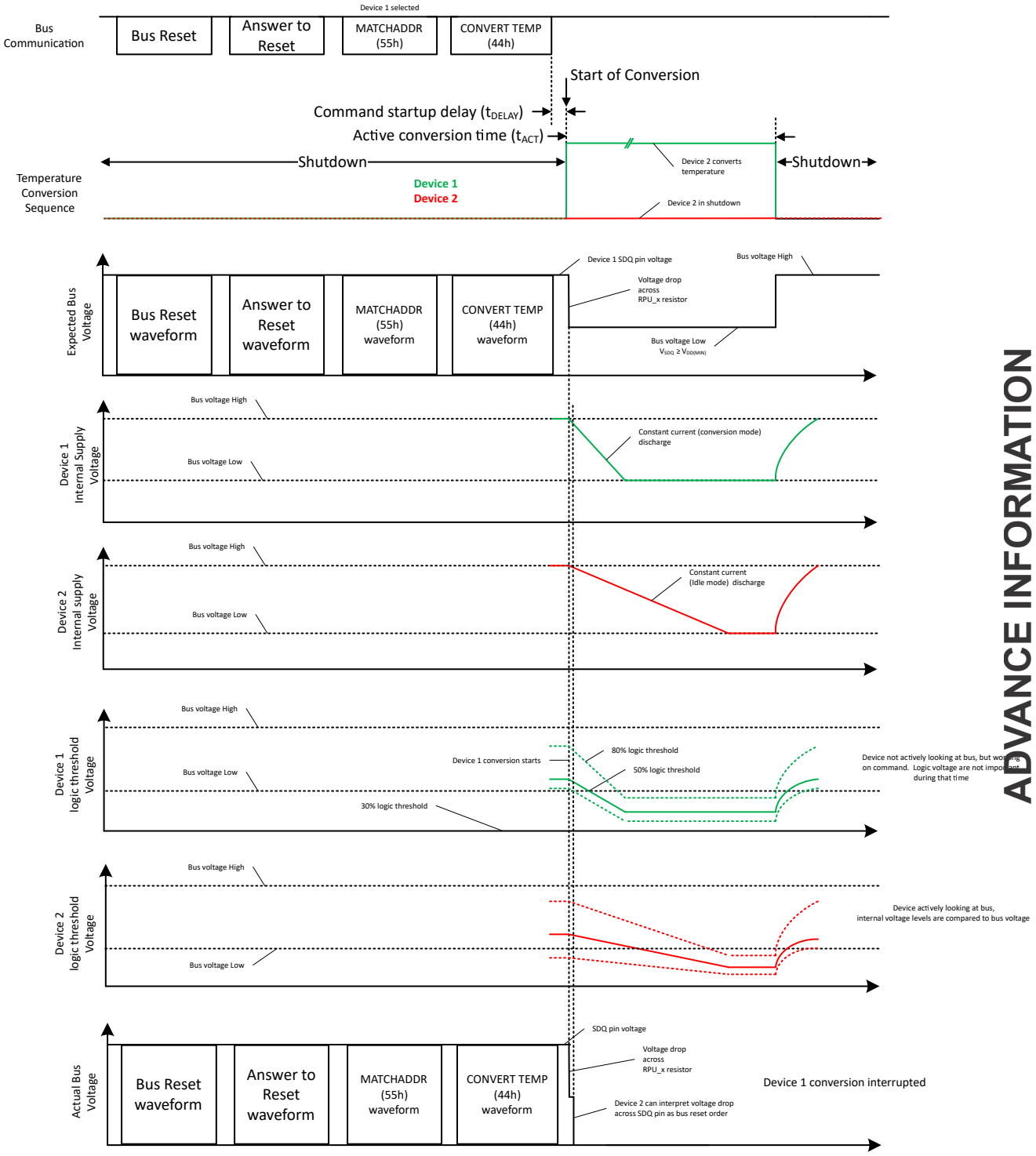

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Supply-powered mode constraints

When the device is supplied through the V_{DD} power pin, a larger pullup resistor value can be used to minimize the overall power consumption, as the SDQ pin is used only for communication. Select the pullup resistor value to support the required bus speed of operation timing. A first order model, below, is considering only the bus capacitor, C_{BUS} and the number of time constant, n, required to satisfy V_{IH} ≥0.8 .V_{DD} . T_{RC} is the bus recovery time needed to go from 0V to $V_{IH(MIN)}$.

$$t_{RC} = t_{WAIT} - t_{RL} = n \times \tau = n \times R_{PU\_VDD} \times C_{BUS} \quad (3)$$

Select the number n of time constants to satisfy the minimum V_{IH} threshold required for the bus to be considered high. The model can be improved by considering bus leakage due to SDQ pins present, resistor and capacitance variations, etc...

Minimum pullup resistor constraint

The minimum resistor constraints are due to:

1. Logic voltage threshold and maximum allowable pulldown current
2. Self-heating and temperature accuracy system specification
3. Power consumption

As mentioned above, the first constraint is set by the logic voltage threshold, $V_{OL(MAX)}$, and the maximum current allowed in the pulldown transistor, Equation 4. Again, as previously mentioned, this equation is valid for both the bus-powered and the supply-powered modes.

$$\frac{(V_{PU\_X} - V_{OL(MAX)})}{4 \times 10^{-3}} < R_{PU\_X} \quad (4)$$

with R_{PU_X}, V_{PU_X} following the nomenclature for either Bus-Powered Mode or Supply-Powered Mode.

The second constraint affects the temperature accuracy. Equation 5 show the self heating constraint due to the bus current. T_{SH} is the allowable self-heating temperature rise, or error, that affects the temperature measurement accuracy.

$$\frac{(V_S - V_{SDQ})}{T_{SH}} \times V_{SDQ} \times \theta_{JA} < R_{PU\_X} \quad (5)$$

The last constraint is system level. Unless the implementation is powered by a battery with a high duty cycle or long battery life requirement, this constraint can be ignored. The TMP1820 is a low quiescent current device, 85 µA typical during conversion and 1.6 µA otherwise.

Supplying the bus-powered implementation during temperature conversion

A simple solution is available to supply the bus-powered implementation, and eliminate the need for careful pullup resistor value for minimal voltage drop, consists in powering the TMP1820 directly from the bus during the conversion time. This solution is shown in Figure 7-6.

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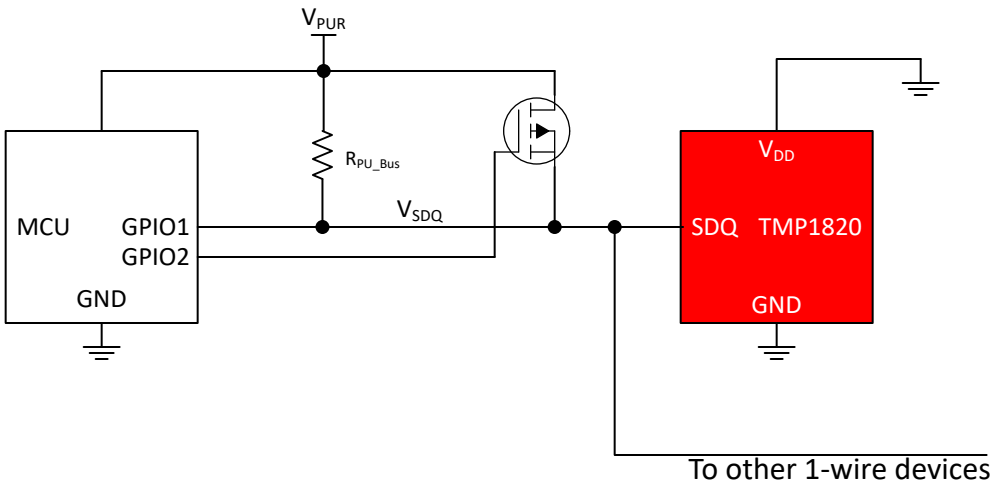

Figure 7-6. Supplying the Bus-Powered Implementation During Temperature Conversion

7.3.4 Temperature Results

The conversion is initiated by the host MCU by sending the temperature conversion command. At the end of every conversion, the device updates the temperature result registers. As shown in Figure 7-7, the device has a 12-bit legacy format, where the 12-bits are aligned to the right side.

Temperature Result MSB Register								Temperature Result LSB Register								Unit
12-bit Format																
Sign	Sign	Sign	Sign	Sign	64	32	16	8	4	2	1	0.5	0.25	0.125	0.0625	m°C
-2048	1024	512	256	128	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	fraction
-2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	power

Figure 7-7. Temperature Format

The temperature register reads as 0°C before the first conversion. Table 7-1 shows examples of possible binary data that can be read from the temperature result registers and the corresponding hexadecimal and temperature equivalents. Note that any temperature above 127.9375°C will be reported with the maximum code 07FFh.

Table 7-1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEXADECIMAL
>127.9375	0000 0111 1111 1111	07FF
127.9375	0000 0111 1111 1111	07FF
100	0000 0110 0100 0000	0640
25	0000 0001 1001 0000	0190
1	0000 0000 0001 0000	0010
0.125	0000 0000 0000 0010	0002
0	0000 0000 0000 0000	0000
–0.125	1111 1111 1111 1110	FFFE
–1	1111 1111 1111 0000	FFF0
–25	1111 1110 0111 0000	FE70
–40	1111 1101 1000 0000	FD80
–55	1111 1100 1001 0000	FC90

7.3.5 Standard Device Address

Every device comes with a unique 64-bit address that is factory programmed.

7.3.5.1 Unique 64-Bit Device Address

The device has a hard coded 64-bit factory programmed address that cannot be altered by the customer application. The unique 64-bit device address can be used for device addressing or for NIST traceability. Figure 7-8 shows the format. When the host accesses the device or when the device sends its address, this unique address is sent least significant bit (LSb) first. The unique 64-bit address consists of three fields:

1. the device family code is represented in the lower eight bits
2. the 48-bit unique number is found next
3. the 8-bit CRC checksum is calculated from the preceding 56-bit.

The device family code for TMP1820 will read as 28h.

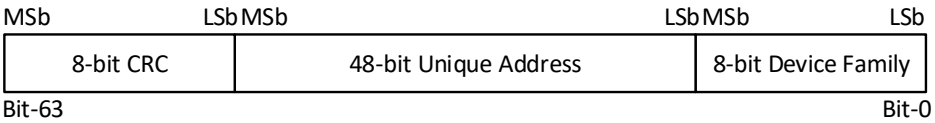

Figure 7-8. 64-Bit Device Address

7.3.6 Flexible Device Address

Depending on the user application case, the TMP1820 provides for some user and application configurable address modes, called flexible address mode. These modes exist alongside the standard device address, and is extremely useful for applications that require a combination of faster access.

7.3.7 CRC Generation

A cyclic redundancy check (CRC) mechanism for data integrity check and communication robustness is implemented. Table 7-2 lists the CRC 8-bit properties.

Table 7-2. CRC-8 Rule

CRC-8 Rule	Attributes
CRC width	8 bits
CRC polynomial	$x^8 + x^5 + x^4 + 1$ (31h)
Initial seed value	00h
Input data reflected	Yes
Output data reflected	Yes
XOR value	00h

When a new transaction is started, the CRC shift register is initialized with 00h for seed value. A C-code implementation is shown in Section 7.5.4.2. The CRC result is always part of the 64-bit unique address and is computed on the first 56 bits. When the host reads scratchpad-1 to access the temperature registers, the device appends the CRC after the eight bytes of scratchpad are sent.

To ensure that the communication occurred without any issue, the host can recalculate the CRC and compare the CRC against the received CRC from the device. This is achieved by shifting the read data from the device along with CRC bits. If there is no bus error, the shift register at the end of the bit shift will result in 00h.

The CRC from 8 bytes devise address is copied into the device Short address register and can be used for faster 2 bytes device flex addressing.

7.3.8 1-Wire Communication

The 1-Wire interface communication does not have a reference clock. As such, all communication are performed asynchronously with fixed time slot (t_{SLOT}) and variable pulse width to indicate logic '0' and '1'. In idle state, the external pull up resistor holds the line high. All communications are initiated by the host by driving the data line low and the bit value is decoded as the time for which the data line is held low.

Once the bus has been reset, see *Initializing Communication (Reset Pulse)*, a command is sent and the address phase is initiated. Depending on the command sent, see *Address Phase*, the host transmit either 8 bytes or move into the function phase, see *Function Phase*. The device being addressed either starts the temperature conversion process or communicates back to the host 8 bytes and the CRC. Considering that only 5 registers, see *Register Maps*, are implemented in the TMP1820, and the CRC is not desired in the application, the bus can be reset by the host once the desired amount of information is reached.

To accelerate the communication speed, the TMP1820 provide several command not seen in legacy devices. The most obvious improvement to the communication speed is the OVD mode, see *OVD SKIPADDR (3Ch)* and *OVD MATCHADDR (69h)*. Optimized address arbitration algorithms are also available in STD (or legacy) mode to speed communication once proper device initialization has been completed, see *SEARCHADDR (F0h)*. As in prior generation devices, a SKIPADDR command is available to address all the devices present on the communication, SDQ pin, bus. In this case, sizing of the pullup resistor is critical to ensure optimum performance, see *Bus Pullup Resistor*.

7.3.8.1 Initializing Communication (Reset Pulse)

As indicated in Section 7.4.2.2, the 1-Wire interface communication is initiated by a reset pulse. In the case of the TMP1820, the length of the reset pulse determine whether the device is operating in standard (STD or legacy) mode or in overdrive (OVD) mode allowing up to 90 kbps data rate.

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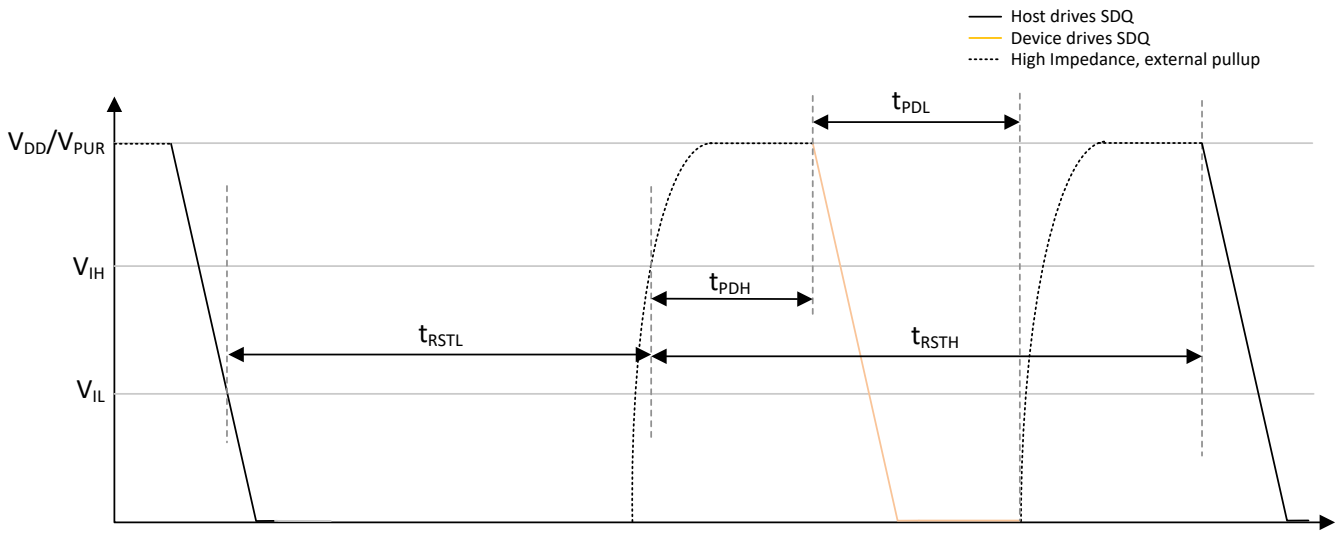

Figure 7-9. Bus Reset Timing Diagram

As indicated in Figure 7-9 and Section 6.6, all bus reset operations require a minimum of t_{RSTL} + t_{RSTH} (960 µs typical in STD mode and 96 µs typical in OVD mode).

7.3.8.2 Bit Communication

This section describes the communication and timing of a single bit, whether it is in read or write mode.

7.3.8.2.1 Host Write and Device Read

A host write is the means by which the host sends the command, function and data to the device(s). A host write starts by the host driving the data line low as shown in Figure 7-10.

If the host intends to transmit a logic '1', the host releases the line after t_{WR1L} time. If the host intends to transmit a logic '0', the host releases the line after t_{WR0L}.

After releasing the data line, the pullup causes the line to become high until the beginning of the next time slot. The device samples the line after t_{RDV} has elapsed from the falling edge, starting at V_{IL}, for the time frame indicated by t_{DSW}.

The application must factor the pullup resistor time constant created by the pullup resistor value and the bus capacitance and determine the release of the data line sampled (by the device) or driving the next write bit time slot (by the host). See Figure 7-10 "Host Write-0".

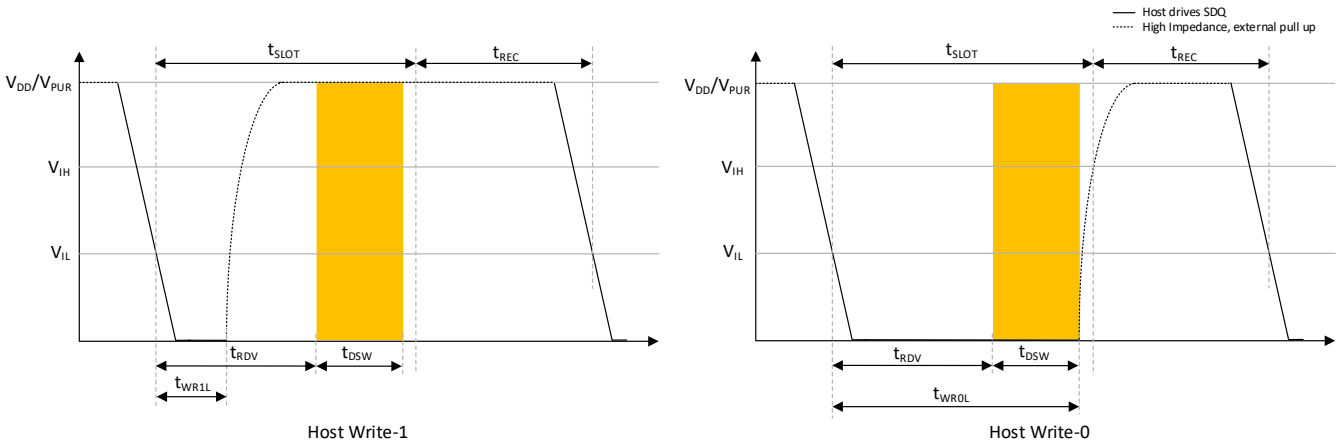

Figure 7-10. Host Write and Device Read

After the "Host Write/Device Read" operation is complete, t_{SLOT} time has elapsed, and the host releases the communication bus, resulting in:

1. closing the communication for this bit
2. if the device is operated in bus-powered mode, enabling the recharge of the internal capacitor and thus preparing the device for the next communication step, whether a bus reset or another bit being communicated between the host and the device.

Note that a minimum recovery time, t_{REC}, is necessary to ensure the internal capacitor is fully recharged. t_{REC} is measured from V_{IH} to V_{IL}.

7.3.8.2.2 Host Read and Device Write

A host read is the means by which the hosts acquire the data from the device or the CRC bit for data-integrity check. A host read starts by the host driving the data line low as shown in Figure 7-11.

Once the device detects the falling edge, the device may drive the line low before the bit-read slot time, t_{RL}. The device may release the bus from its side after the time $t_{RL(MIN)}$ elapses.

If the device intends to transmit a logic '1', then the device will release the bus before $t_{RL(MAX)}$ elapses. If the device intends to transmit a logic '0', then the device releases the bus after $t_{SLOT(MIN)}$.

The application must factor the pullup resistor time constant created by the pullup resistor value and the bus capacitance and determine the release of the data line sampled (by the host) or driving the next write bit time slot (by the device). See Figure 7-11 "Host Read-0".

The host must sample the line after the time t_{RWAIT}, for a time frame indicated by t_{MSW}. The application must factor the rise time due to pullup resistor and bus capacitance, to determine the sampling window for the bit level sent by the device or driving the next read bit time slot.

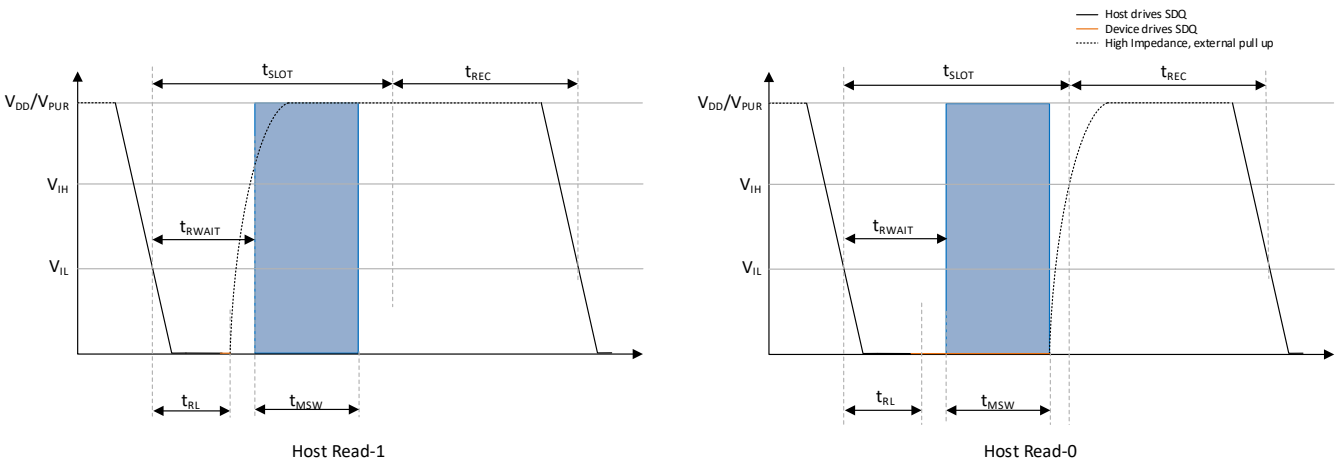

Figure 7-11. Host Read and Device Write

After the Host Read/Device Write operation is completed, t_{SLOT} time has elapsed, and the device releases the communication bus, resulting in:

1. closing the communication for this bit
2. if the device is operated in bus-powered mode, enabling the recharge of the internal capacitor and thus preparing the device for the next communication step, whether a bus reset or another bit being communicated between the host and the device.

Note that a minimum recovery time, t_{REC}, is necessary to ensure the internal capacitor is fully recharged. t_{REC} is measured from V_{IH} to V_{IL}.

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7.3.8.3 Byte Communication

Even though the communication is done one bit at a time, the data exchanged between the host and device is performed at byte boundary. Every byte is sent least significant bit (LSB) first. The device behavior is not predictable when incomplete bytes are sent.

As mentioned in *1-Wire Communication*, the communications is handled byte-by-byte by either the host or the device.

7.3.8.3.1 Byte Communication Example

Figure Figure 7-12 shows an example of how the command 33h (READADDR) develops.

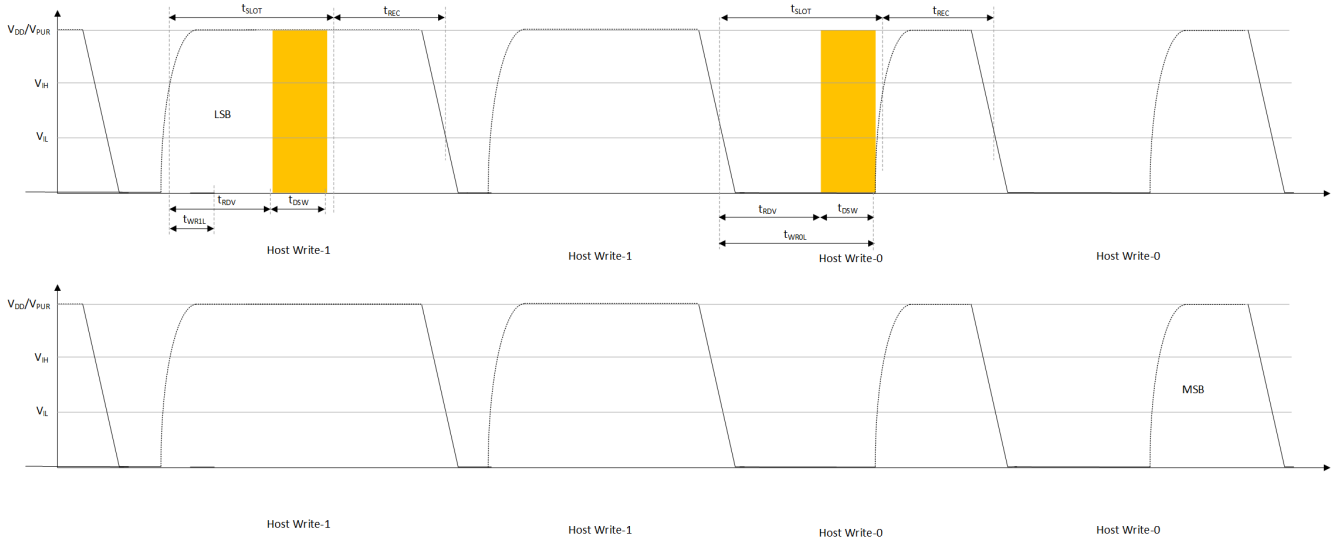

Figure 7-12. 33h (00110011b), READADDR Byte communication

As a reminder of the bit communication protocol used, Host Write-0 and host Write-1 timing are shown. For additional information on bit communication, see *Bit Communication*.

7.3.9 Resolution and Temperature Conversion Time

Unlike most legacy devices, the TMP1820 temperature conversion time does not vary and the full 12-bit resolution is always achieved in less than 27 ms.

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7.4 Device Functional Modes

7.4.1 Conversion Modes

The TMP1820 supports one shot conversion in both bus-powered and supply-powered mode.

7.4.1.1 Basic One-Shot Conversion Mode

During the one-shot conversion, the device goes through a bus reset, and the address and function phases to initiate the temperature conversion. During the communication, the device is in shutdown mode. After the

conversion request is registered by the device, the device starts the conversion and then returns to low power shutdown mode as shown in Figure 7-13.

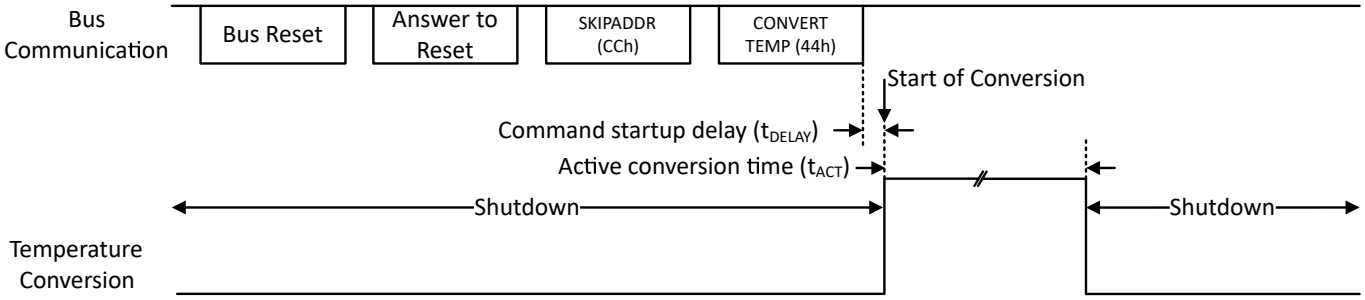

Figure 7-13. Single Device One-Shot Conversion Mode

In case multiple devices are present on the bus, see Figure 7-14, there is no change in how any one-shot conversion is performed by each device. However, when multiple devices are present, the combined current drain in bus-powered mode may cause the SDQ pin voltage to drop too low. In such use cases, it is required that the host implement a low impedance current path using an external FET/transistor switch. This low impedance path is switched on to satisfy the bus current requirement during active conversion and should be disabled after the active conversion duration is reached.

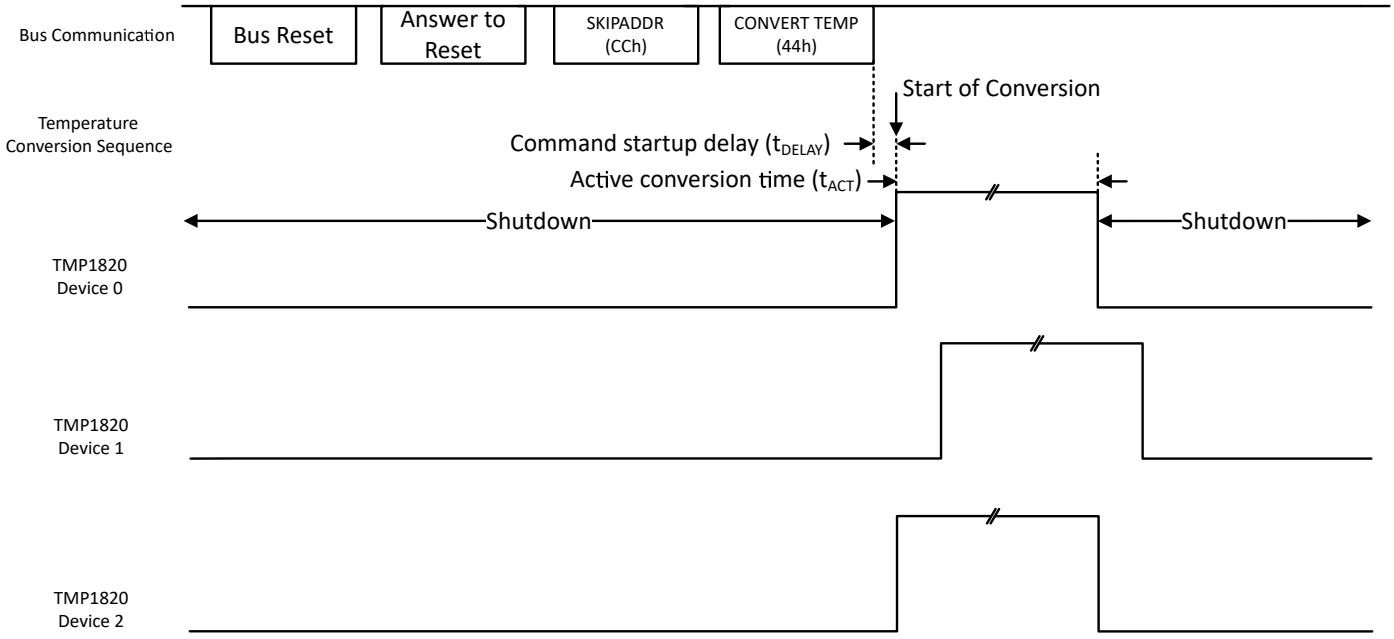

Figure 7-14. Multiple Device One-Shot Conversion Mode

7.4.2 1-Wire Interface Communication

To leverage the features effectively, the device access consists of three distinct phases. As shown in Figure 7-15, any bus communication starts with a bus reset condition to which every device on the bus must respond.

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This is followed by a highly configurable address phase, where the host selects which device to access. Finally there is a function phase, where the host assigns actions the selected device(s) must complete.

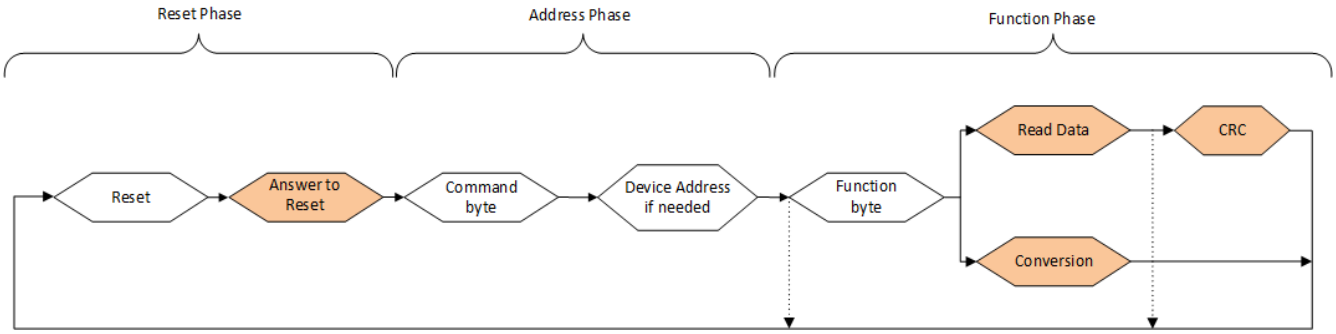

Figure 7-15. 1-Wire Bus Communication

In 1-Wire bus all write and reads are initiated by the host.

7.4.2.1 Reset Phase

The reset phase is beginning the communication. The phase is initiated by the host by holding the 1-Wire data line low for a period t_{RSTL}. All devices on the bus, irrespective of their current state will respond to the reset phase, will reinitialize their internal states and respond to the host-initiated reset. The devices respond after a minimum of t_{PDH}, by holding the 1-Wire low for a time period of t_{RSTH} as shown in Figure 6-1.

After power on, the 1-Wire interface is configured in the overdrive mode. If the host sends a reset pulse between 48 µs to 80 µs, then only devices operating in overdrive mode will respond to the reset pulse, while all other devices operating in standard mode will continue to wait for the standard mode reset pulse.

If the host sends a reset pulse of minimum t_{RSTL} for standard mode, the device will respond to the reset and automatically switch to standard mode. If the bus consists of mixed standard and overdrive speed devices, then sending a reset pulse in standard mode will reset all devices to standard mode speed of communication.

It is illegal for the host to send the reset for a particular speed of operation and then communicate in the alternate speed mode. Note also that if a reset pulse is sent which is greater than 80 µs, but less than 480 µs, then device will be reset but proper the device operation may not be achieved.

7.4.2.2 Address Phase

The address phase follows the reset phase as shown in Figure 7-16 and Figure 7-17. During this phase, the host presents one byte commands which may be followed either the host sending a 64-bit device address, a FLEX address or by skipping the address. Some of the commands are used to discover the device address, while others are used to select the device. The FLEX address has also been implemented whose code in stored in the short register address by the manufacturer. The CRC code of the 8-byte device address is used as the short address and stored in the short address register. This allows the devices to be addressed using 2 bytes instead of 9 bytes.

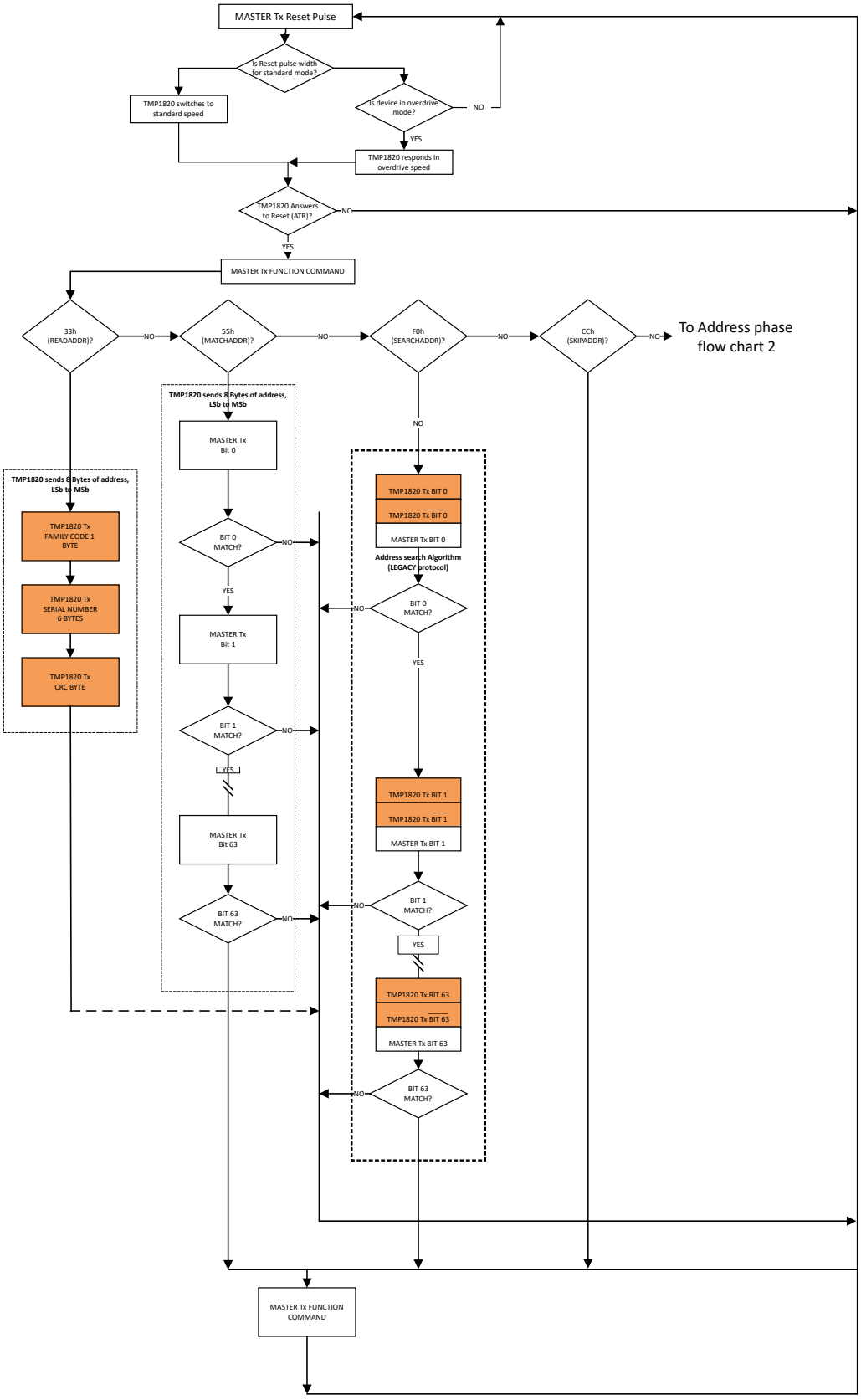

Figure 7-16. Address Phase Flowchart (a)

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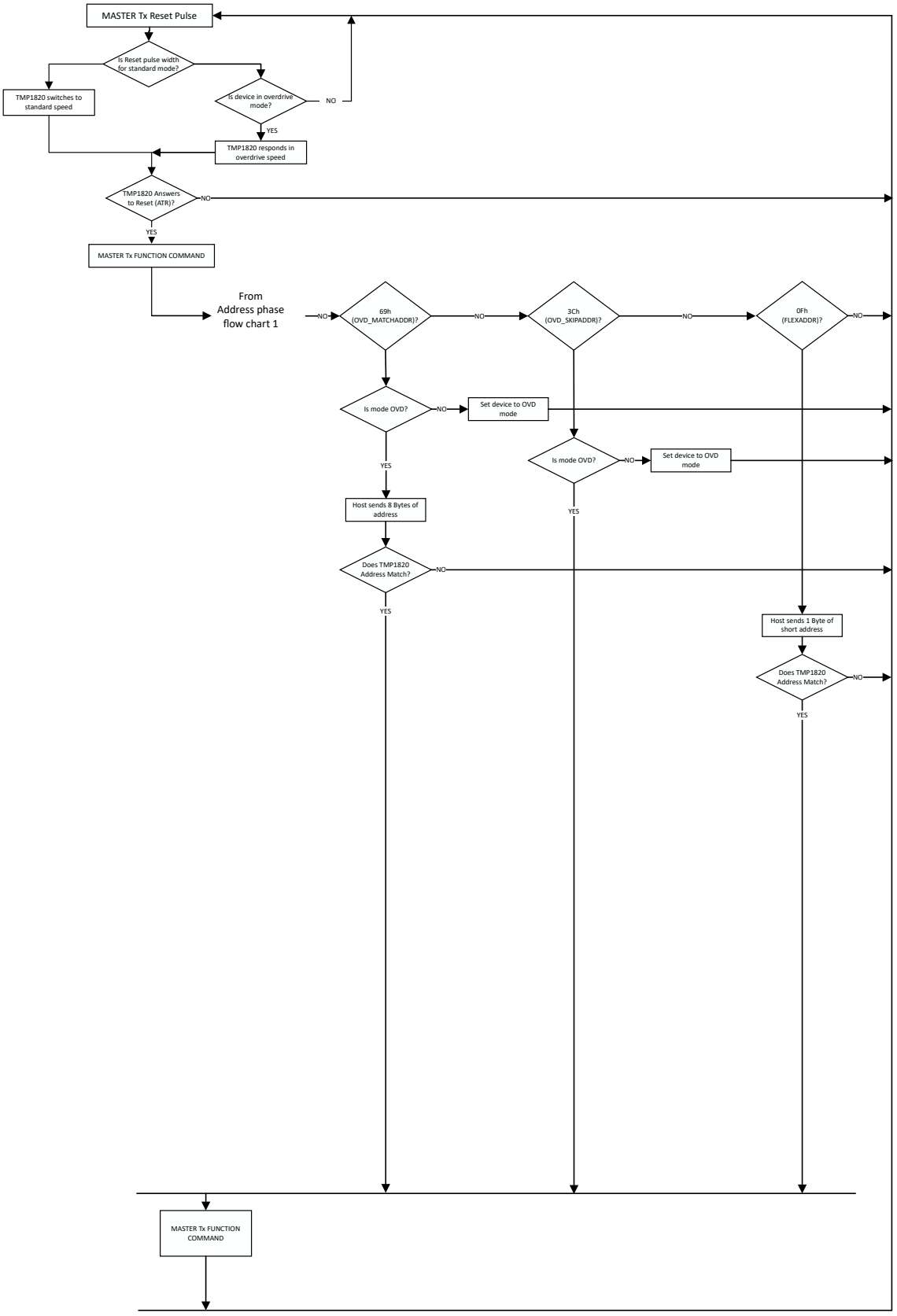

Figure 7-17. Address Phase Flowchart (b)

7.4.2.2.1 READADDR (33h)

The command is used by the host to read the 64-bit address of the device. This command must be used only when there is one device on the bus, because this command will result in a collision if multiple devices are present on the bus.

7.4.2.2.2 MATCHADDR (55h)

The command is used by the host and is followed by the 64-bit address of a single device on the bus. The address for each device is unique, therefore only one device can be selected by the command.

7.4.2.2.3 SEARCHADDR (F0h)

The command is used by the host to search the 64-bit address of all devices present on the bus after the system is powered up the first time. When there is a single device bus, the host can skip this command and instead use the SKIPADDR command to access the device.

7.4.2.2.4 SKIPADDR (CCh)

The host can issue this command to select all the devices on the bus simultaneously. This is useful for the host to trigger the temperature conversion for all the devices on the bus. Additionally, the host can use the command to increase the overall bus data throughput, when there is a single device on the bus.

The host must consider that when there are multiple devices on the bus, then the command must not issued, if it intends to read the devices, as it would be lead to collision on the bus.

7.4.2.2.5 FLEXADDR (0Fh)

The host issues the command to access a device by its short address that is configured in the short address register.

Using the command does not affect the 64-bit unique address of the device. The flex address mode is factory programmed using the CRC code of the 8-byte address. It is thus possible to have devices with the same address.

7.4.2.2.6 OVD SKIPADDR (3Ch)

The host can issue this command to select all devices supporting overdrive mode when operating in a mixed speed bus environment. This is useful when the host wants to trigger the temperature conversion for all the devices on the bus that support overdrive mode. Additionally, the host can use the command to increase the overall bus data throughput, when there is a single device on the bus.

Do not use this command when you intend to read the device temperature as collision on the bus will occur when all devices will send their data back to the host. Instead, read each individual device sequentially.

If the host issues a standard mode reset at anytime, the communication speed reverts back to standard mode.

If this OVD SKIPADDR is accessed while in standard mode, the device switches to OVD mode and waits for OVD reset. It the command arrives in OVD mode, the device proceeds to the function stage.

7.4.2.2.7 OVD MATCHADDR (69h)

The command is used by the host and is followed by a 64-bit address that is used to select a single device on the bus.

The address for each device is unique, therefore only one device can be selected by the command. The selected device will start all further communication in overdrive mode.

If the host issues a standard mode reset at anytime then all devices will revert back to standard communication mode. When this command is sent in standard mode, the command switch the device in OVD mode and does not proceed to function stage. An OVD reset would follow. If the device is already in OVD mode, then the 69h command can be used in OVD mode in the same way as the 55h command match address.

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7.4.2.3 Function Phase

Figure Figure 7-18 shows the functional phase that follows the address phase. During this phase the host may present different functions which is followed by either the host, reading the device data, or by starting a temperature conversion. Some of the functions may be broadcast to all the devices on the bus using SKIPADDR or OVD SKIPADDR. Read functions must always be unicast with a device selected during the address phase using MATCHADDR, or OVD MATCHADDR. For cases where there is a single device on the bus, the device address selection may be skipped.

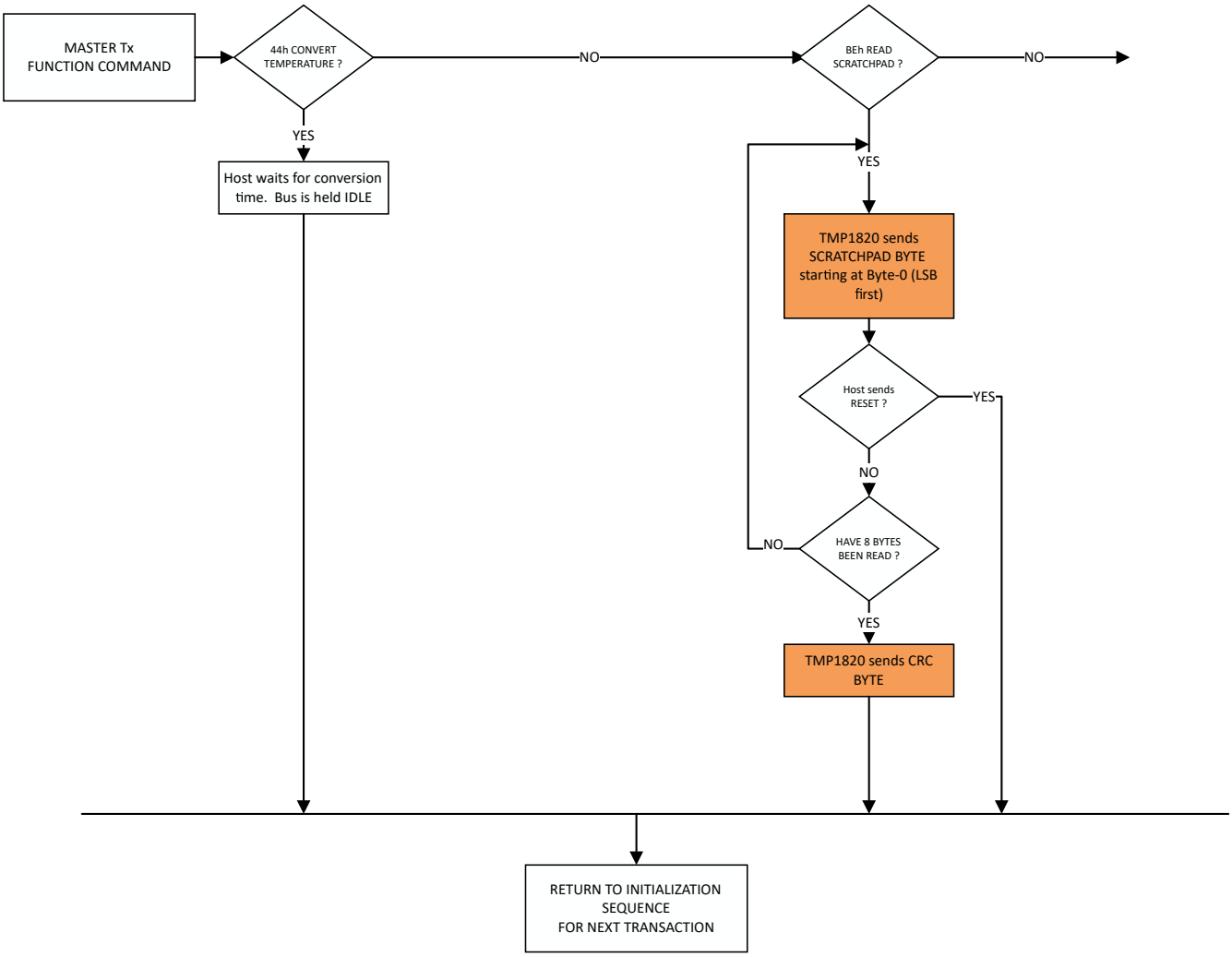

Figure 7-18. Function Phase Flowchart for Legacy Access

7.4.2.3.1 CONVERTTEMP (44h)

The function is issued by the host to perform the temperature conversion.

When the device is bus powered, the host must keep the bus idle for the duration of the active temperature conversion. After the temperature conversion is complete, the result is updated in the registers, temperature result LSB register and temperature result MSB register.

7.4.2.3.2 READ SCRATCHPAD-1 (BEh)

The function is issued by the host to read the temperature result. The selected device transmits the first eight bytes of the register scratchpad followed by CRC of the eight bytes. The host can terminate the function at any point by issuing a bus reset.

7.5 Programming

The sections below describe the sequences that must be followed to access the device functions properly.

7.5.1 Single Device Temperature Conversion and Read

Table 7-3 illustrates the communication flow that the host MCU must execute for temperature conversion and subsequent read of the temperature result. As the temperature results are the first two bytes of the register scratchpad, the host may optionally stop the read after the device transmits the first two bytes, by performing a reset on the bus.

Table 7-3. Single Device Temperature Conversion and Read Scratchpad-1 Sequence

HOST TO DEVICE	DEVICE TO HOST	COMMENTS
Reset		Host sends reset to initialize communication
	Answer to Reset	Device responds to initialization
SKIPADDR (CCh)		Host sends address command to select all device(s)
CONVERTTEMP (44h)		Host sends function command to start temperature conversion
Bus idle for t_{DELAY} + t_{CONV}		Bus is held in idle state (high) during temperature conversion
Reset		Host sends reset to initialize communication
	Answer to Reset	Device responds to initialization
SKIPADDR (CCh)		Host sends address command to select all device(s)
READ SCRATCHPAD-1 (BEh)		Host sends function command to read register scratchpad-1
	TEMP_RESULT_L	Device sends temperature result LSB register
	TEMP_RESULT_H	Device sends temperature result MSB register

7.5.2 Multiple Device Temperature Conversion and Read

Table 7-4 illustrates the program flow that the host MCU must execute for temperature conversion and subsequent read of the temperature result for multiple devices. The host must use the MATCHADDR command, because the devices do not arbitrate on a read function.

Table 7-4. Multiple Device Temperature Conversion and Read Scratchpad-1 Sequence

HOST TO DEVICE	DEVICE TO HOST	COMMENTS
Reset		Host sends reset to initialize communication
	Answer to Reset	Device responds to initialization
SKIPADDR (CCh)		Host sends address command to select all device(s)
CONVERTTEMP (44h)		Host sends function command to start temperature conversion. All devices on the bus convert simultaneously.
Bus idle for t_{DELAY} + t_{CONV}		Bus is held in idle state (high) during temperature conversion
Reset		Host sends reset to initialize communication
	Answer to Reset	Device responds to initialization
MATCHADDR (55h)		Host sends address command to select specific device
DEVICE-1 ADDRESS		Host sends 8 byte device address for selecting device-1
READ SCRATCHPAD-1 (BEh)		Host sends function command to read register scratchpad-1
	TEMP_RESULT_L	Device-1 sends temperature result LSB register
	TEMP_RESULT_H	Device-1 sends temperature result MSB register
Reset		Host sends reset to initialize communication
	Answer to Reset	Device responds to initialization
MATCHADDR (55h)		Host sends address command to select specific device
DEVICE-2 ADDRESS		Host sends 8 byte device address for selecting device-2
READ SCRATCHPAD-1 (BEh)		Host sends function command to read register scratchpad-1

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Table 7-4. Multiple Device Temperature Conversion and Read Scratchpad-1 Sequence (continued)

HOST TO DEVICE	DEVICE TO HOST	COMMENTS
	TEMP_RESULT_L	Device-2 sends temperature result LSB register
	TEMP_RESULT_H	Device-2 sends temperature result MSB register

7.5.3 Multiple Device Flexible Address Temperature Conversion and Read

Figure 7-19 illustrates the program flow that the host MCU must execute for temperature conversion and subsequent read of the temperature result for multiple devices using FLEXADDR command. The total number of bytes sent on the bus by the device or host for every temperature read is six bytes with FLEXADDR command, versus 12 bytes compared to Figure 7-19, thus allowing the host to read all the devices much faster compared to legacy method of access.

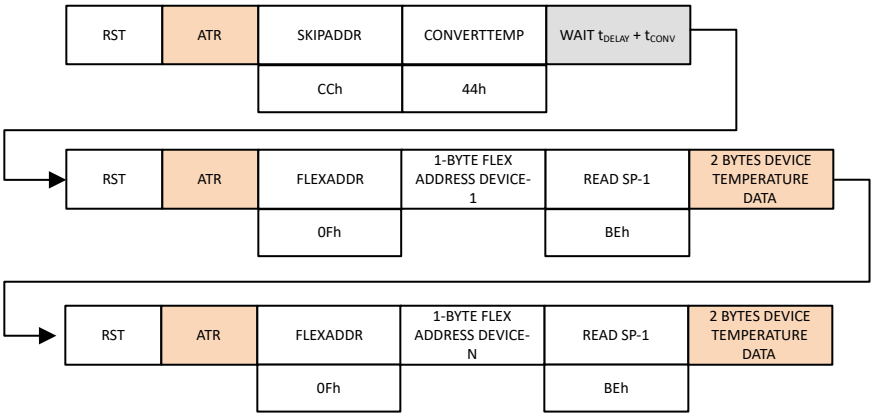

Figure 7-19. Multiple Device Flexible Address Temperature Conversion and Read Programming Flow

7.5.4 C-Code

These example are implemented using a Unix console.

7.5.4.1 Decoding Temperature Data

The TMP1820 temperature registers are using a 12-bit legacy format. Unlike other digital temperature sensors, the 12 bits are aligned to the right side, or least significant side, of the 16-bit word. The four unused bits are on the left side, or most significant side. For this reason, there is no shift needed to discard the extra bits, and it can be easier to think of the data as 16-bit when converting the data to degrees Celsius. 2's Complement is employed to describe negative temperatures. C code can easily convert the 2's Complement data when the data is typecast into the correct signed data type. Q notation describes the number of bits which represent a fractional result. 4 bits of fractional data, known as Q4, offers 0.0625°C resolution.

Figure 7-20. Encoding Parameters

PARAMETER	VALUE
Bits	16 (12 effective)
Q	4
Resolution	0.0625
Range (+)	127.9375
Range (–)	-128
25˚C	0x0190

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	Sign	Sign	Sign	Sign	64	32	16	8	4	2	1	0.5	0.25	0.125	0.0625
-2048	1024	512	256	128	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}

```
C Code Examples:
/* 16-bit format will have 0 bits discarded by right shift
   q4 is 0.062500 resolution
   the following bytes represent 24.5C */
uint8_t byte1 = 0x1;
uint8_t byte2 = 0x88;
float f = ((int8_t) byte1 << 8 | byte2) * 0.0625f;
int mC = ((int8_t) byte1 << 8 | byte2) * 1000 >> 4;
int C = ((int8_t) byte1 << 8 | byte2) >> 4;
```

7.5.4.2 CRC Generation

Two implementations of the CRC generation are shown below. The first example uses a lookup table while the second example uses a bit-wise comparison.

In the lookup table approach, the test program scans the arguments and print the resulting CRC to the console.

```
C Code Examples:
#include <stdio.h>

const uint8_t lut[256] = {
      0,  49,  98,  83, 196, 245, 166, 151, 185, 136, 219, 234, 125,  76,  31,  46,
     67, 114,  33,  16, 135, 182, 229, 212, 250, 203, 152, 169,  62,  15,  92, 109,
    134, 183, 228, 213,  66, 115,  32,  17,  63,  14,  93, 108, 251, 202, 153, 168,
    197, 244, 167, 150,   1,  48,  99,  82, 124,  77,  30,  47, 184, 137, 218, 235,
     61,  12,  95, 110, 249, 200, 155, 170, 132, 181, 230, 215,  64, 113,  34,  19,
    126,  79,  28,  45, 186, 139, 216, 233, 199, 246, 165, 148,   3,  50,  97,  80,
    187, 138, 217, 232, 127,  78,  29,  44,   2,  51,  96,  81, 198, 247, 164, 149,
    248, 201, 154, 171,  60,  13,  94, 111,  65, 112,  35,  18, 133, 180, 231, 214,
    122,  75,  24,  41, 190, 143, 220, 237, 195, 242, 161, 144,   7,  54, 101,  84,
     57,   8,  91, 106, 253, 204, 159, 174, 128, 177, 226, 211,  68, 117,  38,  23,
    252, 205, 158, 175,  56,   9,  90, 107,  69, 116,  39,  22, 129, 176, 227, 210,
    191, 142, 221, 236, 123,  74,  25,  40,   6,  55, 100,  85, 194, 243, 160, 145,
     71, 118,  37,  20, 131, 178, 225, 208, 254, 207, 156, 173,  58,  11,  88, 105,
      4,  53, 102,  87, 192, 241, 162, 147, 189, 140, 223, 238, 121,  72,  27,  42,
    193, 240, 163, 146,   5,  52, 103,  86, 120,  73,  26,  43, 188, 141, 222, 239,
    130, 179, 224, 209,  70, 119,  36,  21,  59,  10,  89, 104, 255, 206, 157, 172
};

const uint8_t rev[256] = {
      0, 128,  64, 192,  32, 160,  96, 224,  16, 144,  80, 208,  48, 176, 112, 240,
      8, 136,  72, 200,  40, 168, 104, 232,  24, 152,  88, 216,  56, 184, 120, 248,
      4, 132,  68, 196,  36, 164, 100, 228,  20, 148,  84, 212,  52, 180, 116, 244,
     12, 140,  76, 204,  44, 172, 108, 236,  28, 156,  92, 220,  60, 188, 124, 252,
      2, 130,  66, 194,  34, 162,  98, 226,  18, 146,  82, 210,  50, 178, 114, 242,
     10, 138,  74, 202,  42, 170, 106, 234,  26, 154,  90, 218,  58, 186, 122, 250,
      6, 134,  70, 198,  38, 166, 102, 230,  22, 150,  86, 214,  54, 182, 118, 246,
     14, 142,  78, 206,  46, 174, 110, 238,  30, 158,  94, 222,  62, 190, 126, 254,
      1, 129,  65, 193,  33, 161,  97, 225,  17, 145,  81, 209,  49, 177, 113, 241,
      9, 137,  73, 201,  41, 169, 105, 233,  25, 153,  89, 217,  57, 185, 121, 249,
      5, 133,  69, 197,  37, 165, 101, 229,  21, 149,  85, 213,  53, 181, 117, 245,
     13, 141,  77, 205,  45, 173, 109, 237,  29, 157,  93, 221,  61, 189, 125, 253,
      3, 131,  67, 195,  35, 163,  99, 227,  19, 147,  83, 211,  51, 179, 115, 243,
     11, 139,  75, 203,  43, 171, 107, 235,  27, 155,  91, 219,  59, 187, 123, 251,
      7, 135,  71, 199,  39, 167, 103, 231,  23, 151,  87, 215,  55, 183, 119, 247,
     15, 143,  79, 207,  47, 175, 111, 239,  31, 159,  95, 223,  63, 191, 127, 255
};

unsigned char crcT182(unsigned char msg[], int msglen){
 unsigned char crc = 0x00;
 for (int byte = 0; byte < msglen; byte++){
  printf("msgbyte: 0x%X\n", msg[byte]);
  crc ^= rev[msg[byte]];
  crc = lut[crc];
 }
 return rev[crc];
}

void main(int argc, char *argv[]){
```

```
 unsigned char crc = 0x00;
 unsigned char msg[80];
 int msglen = (argc > 1) ? (argc - 1) : 2;
 msg[0] = 0xAB;
 msg[1] = 0xCD;
 for (int i = 1; i < argc; i++){
  sscanf(argv[i], "%X", &msg[i-1]);
 }
 printf("crc: 0x%X\n",crcT182(msg, msglen));
}
```

The second example uses the bit-wise operator.

```
#include <stdio.h>

unsigned char crcBitReverse(unsigned char m) {
    unsigned char r = 0;
    for (unsigned char bit = 0; bit < 8; bit++) {
        r |= (m & 1 << bit) ? 1 << (7- bit) : 0;
    }
    return r;
}
unsigned char crcT182(unsigned char msg[], int msglen){
 unsigned char crc = 0x00;
 for (int byte = 0; byte < msglen; byte++){
  printf("msgbyte: 0x%x\n", msg[byte]);
  crc ^= crcBitReverse(msg[byte]);
  for (int bit = 0; bit < 8; bit++){
   if (crc & 0x80)
    crc = (crc << 1) ^ 0x31;
   else
    crc = (crc << 1);
  }
 }
 return crcBitReverse(crc);
}

void main(int argc, char *argv[]){
 unsigned char crc = 0x00;
 unsigned char msg[80];
 int msglen = (argc > 1) ? (argc - 1) : 2;
 msg[0] = 0xAB;
 msg[1] = 0xCD;
 for (int i = 1; i < argc; i++){
  sscanf(argv[i], "%X", &msg[i-1]);
 }
 printf("crc: 0x%X\n",crcT182(msg, msglen));
}
```

Both of these implementation return the following, after compilation.

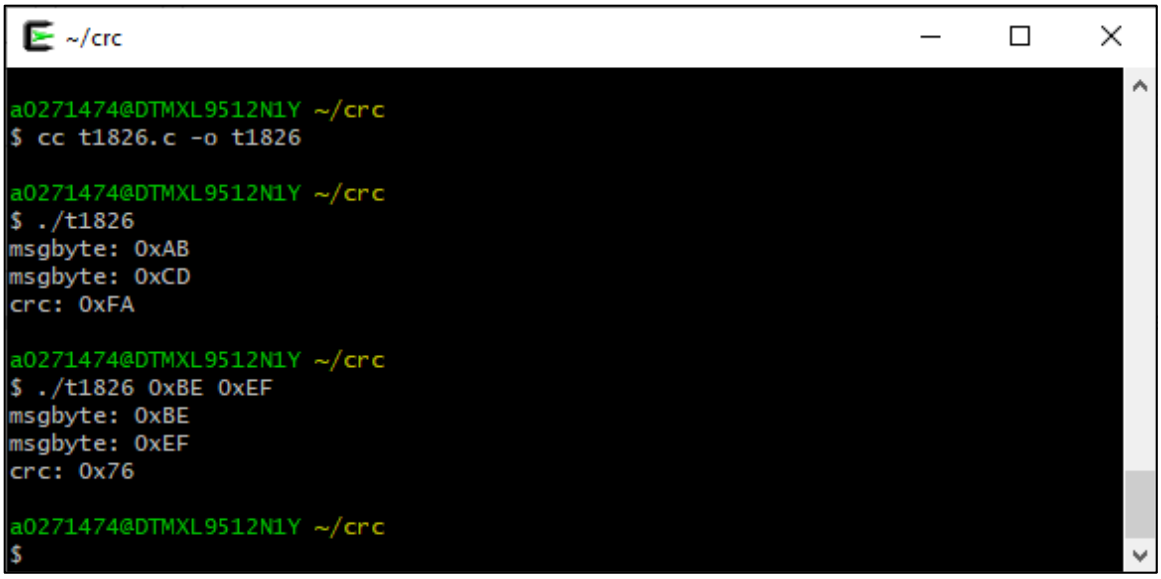

Figure 7-21. CRC Generation Console Results

7.6 Register Maps

Table 7-5. Register Map

SCRATCHPAD-1 BYTE	TYPE	RESET	REGISTER NAME	REGISTER DESCRIPTION	SECTION
00h	R	00h	TEMP_RESULT_L	Temperature Result LSB register	Go
01h	R	00h	TEMP_RESULT_H	Temperature Result MSB register	Go
02h	R	3Ch	STATUS_REG	Status register	Go
03h	R	FFh	Reserved	Reserved	
04h	R	70h	Reserved	Reserved	
05h	R	80h	Reserved	Reserved	
06h	R	XXh	SHORT_ADDR	Short Address register = CRC of device ID	Go
07h	R	FFh	Reserved	Reserved	
08h	R	00h	Reserved	Reserved	
09h	R	00h	Reserved	Reserved	
0Ah	R	F0h	Reserved	Reserved	
0Bh	R	07h	Reserved	Reserved	
0Ch	R	00h	Reserved	Reserved	
0Dh	R	00h	Reserved	Reserved	
0Eh	R	FFh	Reserved	Reserved	
0Fh	R	FFh	Reserved	Reserved	

Table 7-6. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Reset or Default Value		
-n		Value after reset or the default value

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7.6.1 Temperature Result LSB Register (Address offset = 00h) [reset = 00h]

The register is part of the 16-bit temperature result readout that stores the least significant byte of the output of the most recent conversion. The temperature format is in 2's complement format. Following a power-up, the register has the value 00h until the first conversion is complete. After the POR (power On Reset), the device immediately proceed to temperature conversion.

Return to Register Map.

Figure 7-22. Temperature Result LSB Register

7	6	5	4	3	2	1	0
TEMP_RESULT[7:0]							
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-7. Temperature Result LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_RESULT[7:0]	R	00h	Stores the LSB of the most recent temperature conversion results.

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7.6.2 Temperature Result MSB Register (Address = 01h) [reset = 00h]

The register is part of the 16-bit temperature result readout that stores the most significant byte of the output of the most recent conversion. Following a power-up, the register has the value 00h until the first conversion is complete.

Return to Register Map.

Figure 7-23. Temperature Result MSB Register

7	6	5	4	3	2	1	0
TEMP_RESULT[15:8]							
R-00h							

Table 7-8. Temperature Result MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEMP_RESULT[15:8]	R	00h	Stores the MSB of the most recent temperature conversion results.

7.6.3 Status Register (Address = 02h) [reset = 3Ch]

This register provides status of the data ready and power mode. The power mode status flag value is decided based on the powering technique used for the device detected at power up and updated during every bus reset. The data valid (DATA_VALD) flag is set after a conversion is completed. It is automatically cleared when the host reads the status register.

Figure 7-24. Status Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	DATA_VALD	POWER_MODE	Reserved	Reserved
R-1b	R-1b	R-1b	R-1b	RC-0b	R-0b	R-0b	R-0b

Table 7-9. Status Register Field Description

Bit	Field	Type	Reset	Description
7:4	Reserved	R	1111b	Reserved
3	DATA_VALD	RC	0b	Data valid status flag 0b = no update in temperature result register 1b = Temperature result register updated after conversion The data valid flag is automatically cleared when the host controller reads the status register
2	POWER_MODE	R	0b	Device power mode flag. 0b = VDD powered mode 1b = Bus powered mode
1	Reserved	R	0b	Reserved
0	Reserved	R	0b	Reserved

ADVANCE INFORMATION

7.6.4 Short Address Register (Address = 06h) [reset = XXh]

The register is used to program the short address for the device. This is a factory programmed address using the device address CRC byte.

Return to Register Map.

Figure 7-25. Short Address Register

7	6	5	4	3	2	1	0
SHORT_ADDRESS[7:0]							
R-XXh							

Table 7-10. Short Address Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SHORT_ADDRESS[7:0]	R	XXh	Stores the short address for the device which may be used to access the device without sending the 64-bit Unique Device Address. The address corresponds to the device address CRC byte.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMP1820 operates as a 1-Wire half duplex bus, either in supply or bus-powered mode. The device has an integrated capacitor to hold the charge required for communication.

The bus-powered mode is designed for applications working without a dedicated power supply pin and can reduce cabling costs. As the device current consumption during thermal conversion is low, the device may not require a low-impedance current path, thereby reducing the need for additional FET or load switch and current limiting resistor to bypass the bus pullup resistor. The pullup resistor used in bus-powered mode must be correctly sized to ensure that sufficient current can be supplied during a thermal conversion.

Additionally, if the host must reset the device when operating in bus-powered mode, the host must pull the communication line low for at least 35 ms allows the internal capacitor of the device to discharge and prepare the device for power-on reset.

8.2 Bus-Powered Application

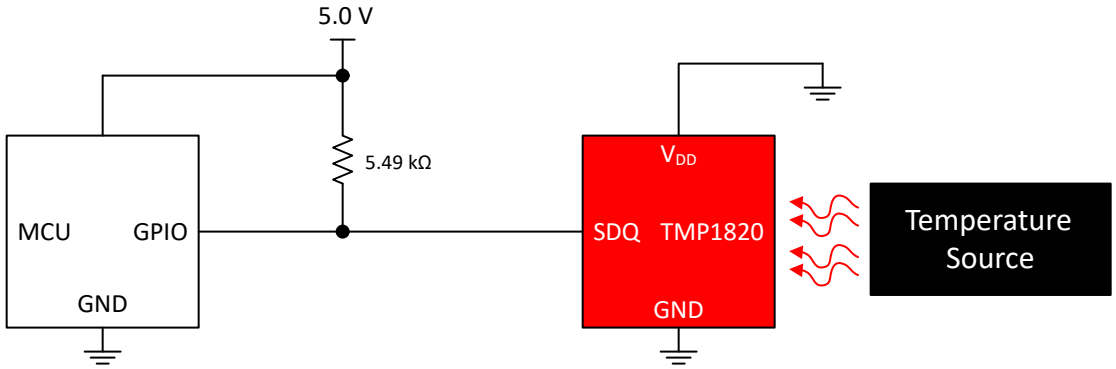

Figure 8-1. Bus-Powered Application

8.2.1 Design Requirements

For this design example, use the parameters listed below:

Table 8-1. Design Parameters

PARAMETER	VALUE
Power mode	Bus Powered
Supply (V_{DD})	5.0 V
Pullup resistor range (R_{PUR})	1.2 kΩ to 5.55 kΩ

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8.2.2 Detailed Design Procedure

This example uses the bus-powered mode as the primary mode of operation to reduce the wire count. The V_{DD} pin of the device must be connected to GND and the SDQ pin of the device must be connected to the host GPIO with a pullup resistor.

To calculate the pullup resistor range, substitute the value for V_{PUR}, $V_{OL(MAX)}$, $V_{IH(MIN)}$ and $I_{PU(MIN)}$ in Equation 7.

$$\frac{(5.0 - 0.0)}{4 \times 10^{-3}} < R_{PUR} < \frac{(5.0 - 4.0)}{180 \times 10^{-6}} \quad (6)$$

$$1.25\ k\Omega < R_{PUR} < 5.55\ k\Omega \quad (7)$$

The actual value of the pullup resistor can then be adjusted based on the speed of communication and bus or cable parasitic capacitance.

When the SDQ pin is activated, the TMP1820 is powered through the pullup resistor to charge its internal capacitors. When the internal capacitor is charged to the pullup voltage, the host can start communication. The bus idle state is high, which is maintained by the pullup resistor, when the host puts its GPIO in high impedance state.

The TMP1820 uses the stored charge to operate when the SDQ pin is low and evaluates the low period to decode bus reset and logic low sent by the host.

8.3 Supply-Powered Application

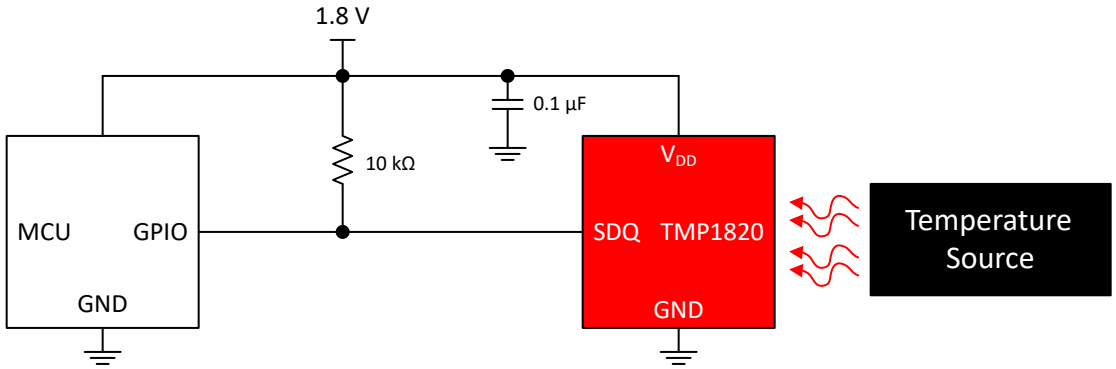

Figure 8-2. Supply-Powered Application

8.3.1 Design Requirements

For this design example use the parameters listed below:

Table 8-2. Design Parameters

PARAMETER	VALUE
Power mode	V_{DD} Powered
Supply (V_{DD})	1.8 V
Pullup resistor (R_{PUR})	10 kΩ

8.3.2 Detailed Design Procedure

The supply-powered mode uses the V_{DD} pin connected to the same supply rail as the host and pullup resistor. TI recommends to put a 0.1-µF bypass capacitor close to the V_{DD} pin of the TMP1820.

A standard pullup resistor value of 10 kΩ is large enough to provide proper communication with standard speed and avoid V_{OL} violation when the device is sending data to the host. Depending on the total bus load and application operating requirements, the pullup resistor value can be changed.

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8.4 UART Interface for Communication

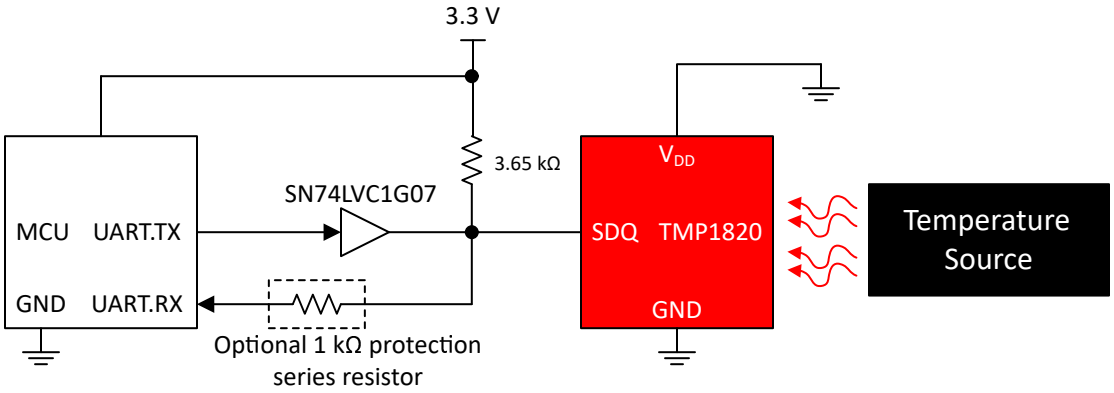

Figure 8-3. UART Interface for Communication

8.4.1 Design Requirements

For this design example, use the parameters listed below:

Table 8-3. Design Parameters

PARAMETER	VALUE
Power mode	Bus powered
Supply (V_{DD})	3.3 V
Pullup resistor range (R_{PUR})	750 Ω to 3.65 kΩ
Optional series resistor	1 kΩ

8.4.2 Detailed Design Procedure

If using GPIO for communication is not possible due to any reason, the UART peripheral available on most host controllers can be used to interface with the TMP1820. UART is a push-pull full duplex bus and to interface with TMP1820, a buffer with open-drain driver like the SN74LVC1G07 can be required.

The input of the buffer is connected to the UART transmit pin and the output of the buffer is connected to the SDQ pin on the TMP1820. The output of the buffer is also connected to the UART receive pin on the host. As the output is open-drain, a pullup resistor which can be calculated is required. See *Bus Pullup Resistor*. Substituting the value for V_{PUR} = 3.3 V, $V_{OL(MAX)}$ = 0.4 V, $V_{IH(MIN)}$ = 2.64 and $I_{PU(MIN)}$ = 180 µA, the R_{PUR} value selected must be greater than 725 Ω and less than 3.67 kΩ.

In software, the application must adjust the baud rate so that the bus can be reset, sending 00h. The start bit of the UART frame which is always 0, provides the required falling edge for data sent to the TMP1820. When sending a logic high to the device, the UART shall send FFh to the TMP1820 and, when sending a logic low to the device, the UART will send C0h. As UART is a full duplex bus, the host must flush the receive buffers during a transmit operation.

When receiving data from the TMP1820, the host shall send FFh and the device, by transmitting a logic high, detects and releases the bus. Transmitting a logic low detects and holds the bus. As a result, the host will receive a FFh for a logic high and F0h for a logic low depending on the baud rate configured.

In case there is a long trace, the optional series resistor can be used to protect the host GPIO and prevent line glitches on the bus.

8.5 Power Supply Recommendations

The TMP1820 operates with a power supply range of 1.7 V to 5.5 V in supply-powered mode. In bus-powered mode, the TMP1820 requires either 1.7 V to 5.5 V for bus communication in overdrive mode or 2.5 V to 5.5 V for bus communication in standard mode. When operating in supply-powered mode, a power-supply bypass capacitor is recommended for precision and stability. Place this power-supply bypass capacitor as close to

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the supply and ground pins of the device as possible. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies can require a bigger bypass capacitor to reject power-supply noise.

In bus-powered mode, the V_{DD} pin must be connected to ground. The internal capacitor in the device, is sufficient to provide power during bus communication. The internal capacitor is recharged through the external pullup resistor, during the recovery period. In cases where there is a long bus length or higher temperatures, it may be necessary for the host to provide additional time for bus recovery so as to allow enough time for the capacitor to recharge.

Note that bus communication are defaulted to overdrive mode. In OVD mode, ripple on the bus due to start-up may be interpreted by the device as a standard mode reset pulse, preventing further bus communication with the host in OVD mode.

8.6 Layout

8.6.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins when in supply powered mode. The recommended value of the capacitor is 0.1 µF. The open-drain SDQ pin requires an external pullup resistor which must not be higher than R_{PUR}.

When in bus-powered mode, only the external pullup resistor is required for the open-drain SDQ pin(s).

8.6.2 Layout Example

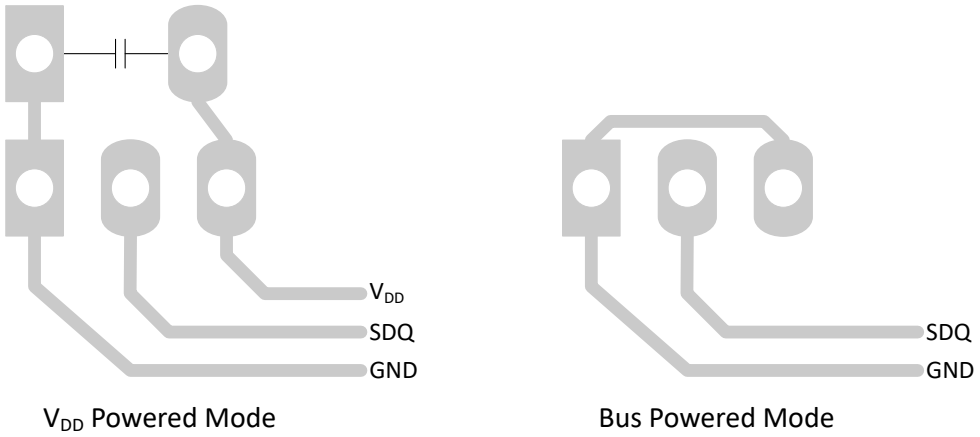

Figure 8-4. Layout Example

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

10.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PTMP1820LPGM	ACTIVE	LPG	TO-92	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	T1820

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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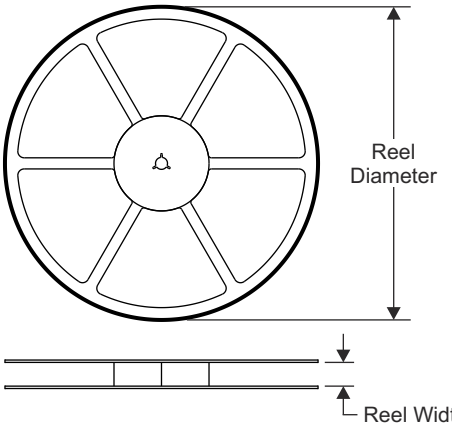
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

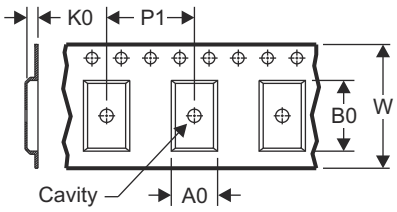
ADVANCE INFORMATION

10.2 Tape and Reel Information

REEL DIMENSIONS

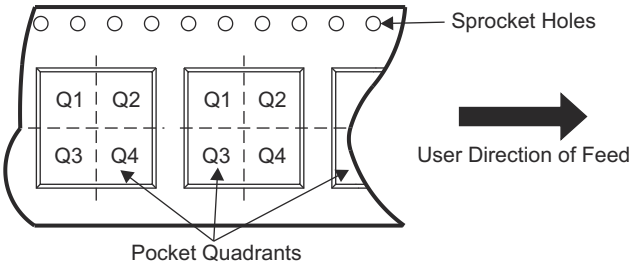


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

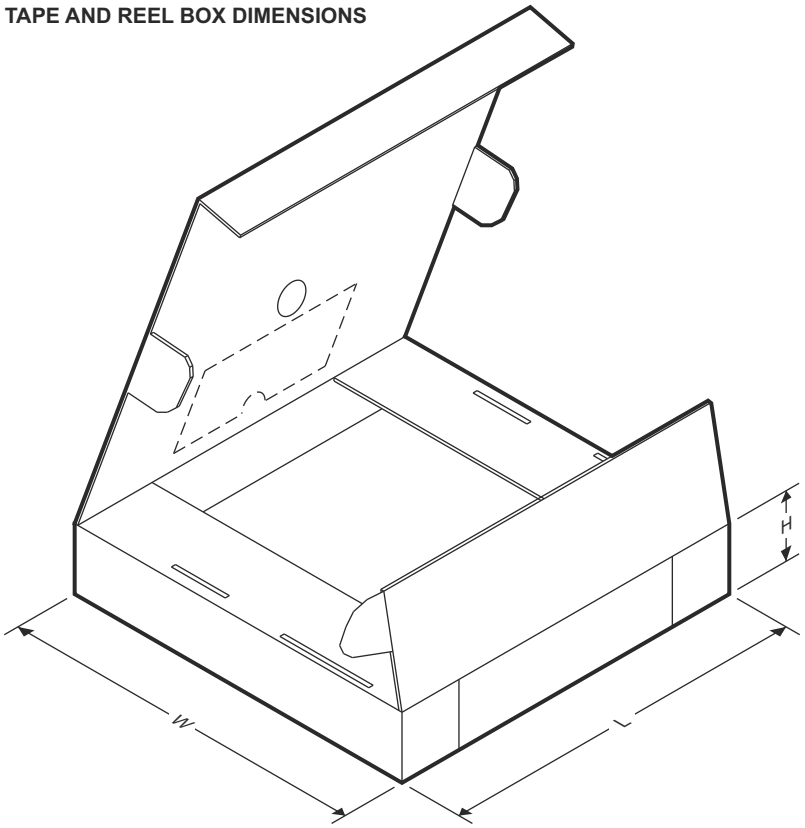
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTMP1820LPGM	LPG	TO-92	3	3000	360	18	Call TI	Call TI	Call TI	12.7	Call TI	Call TI

ADVANCE INFORMATION

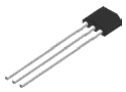
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTMP1820LPGM	LPG	TO-92	3	3000	330	184	40

ADVANCE INFORMATION

ADVANCE INFORMATION

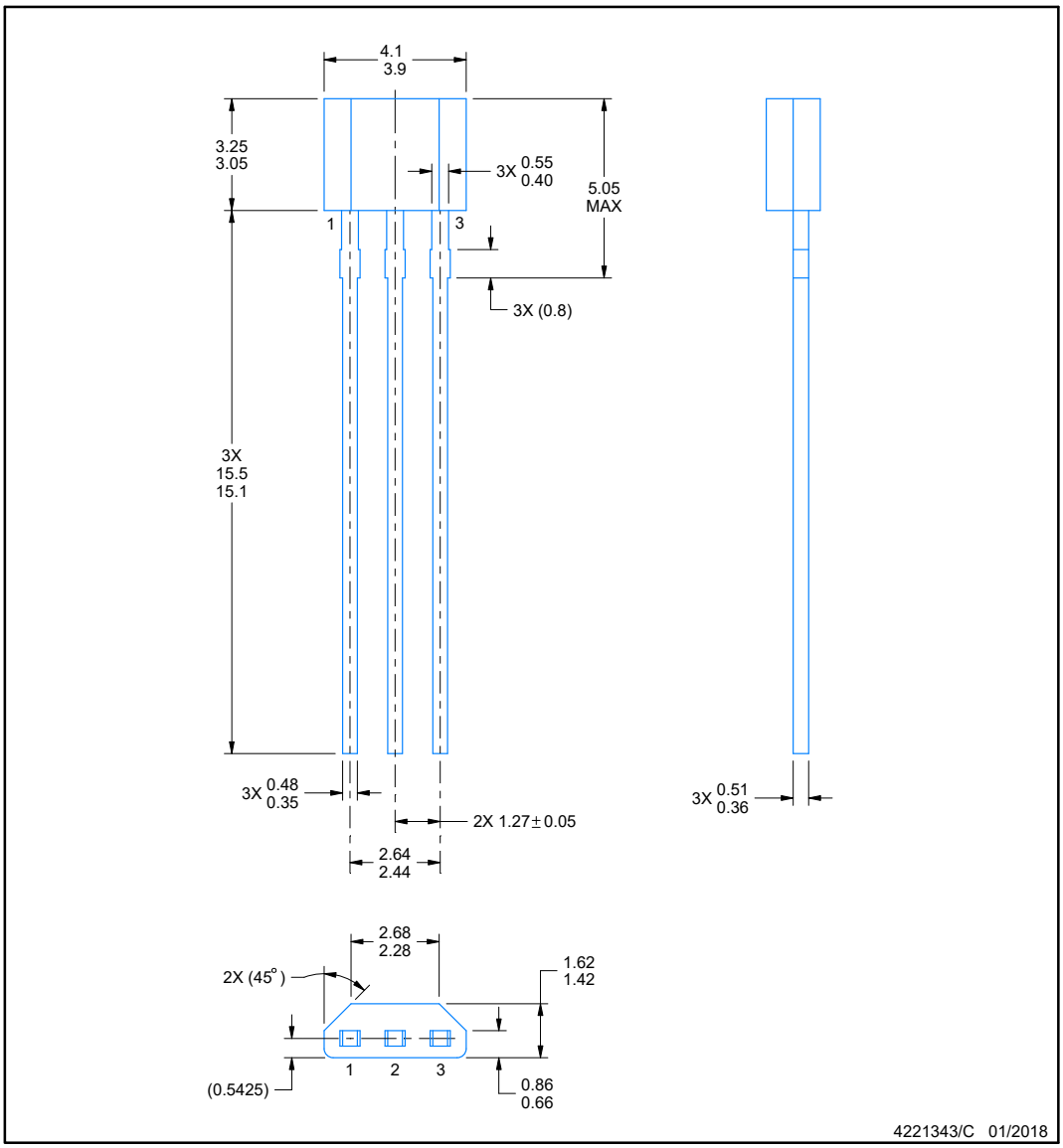


PACKAGE OUTLINE

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



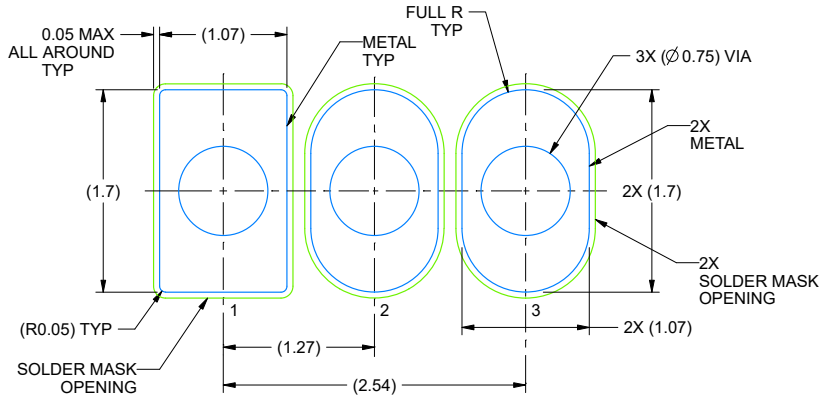
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

LPG0003A — **TO-92 - 5.05 mm max height**

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

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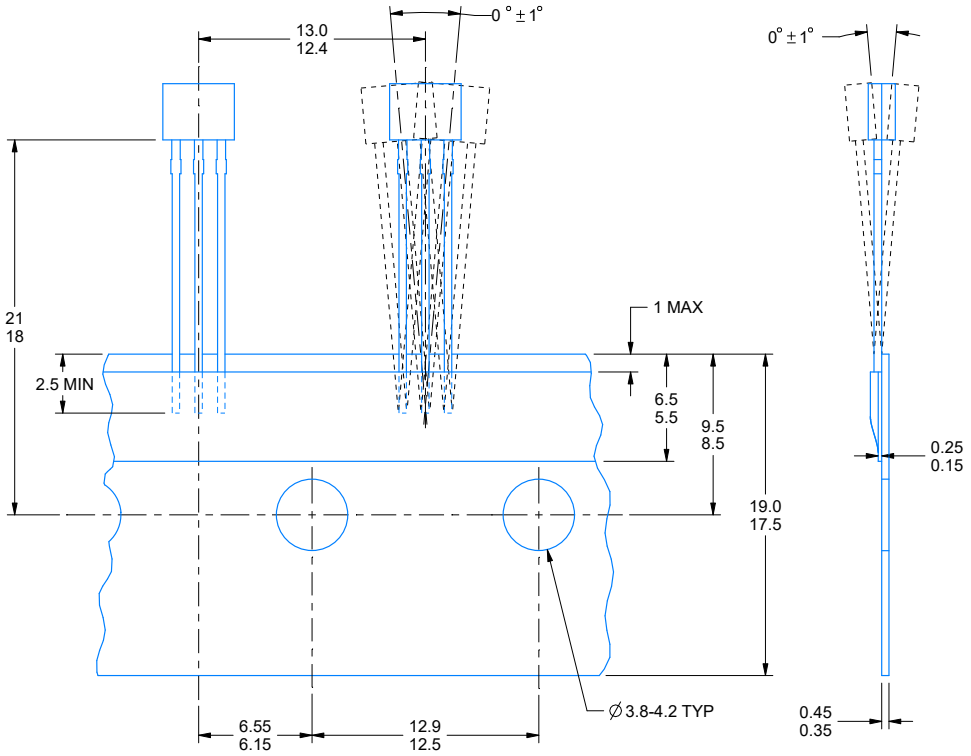
ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE SPECIFICATIONS

LPG0003A — **TO-92 - 5.05 mm max height**

TRANSISTOR OUTLINE



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMP1820LPGM	ACTIVE	TO-92	LPG	3	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

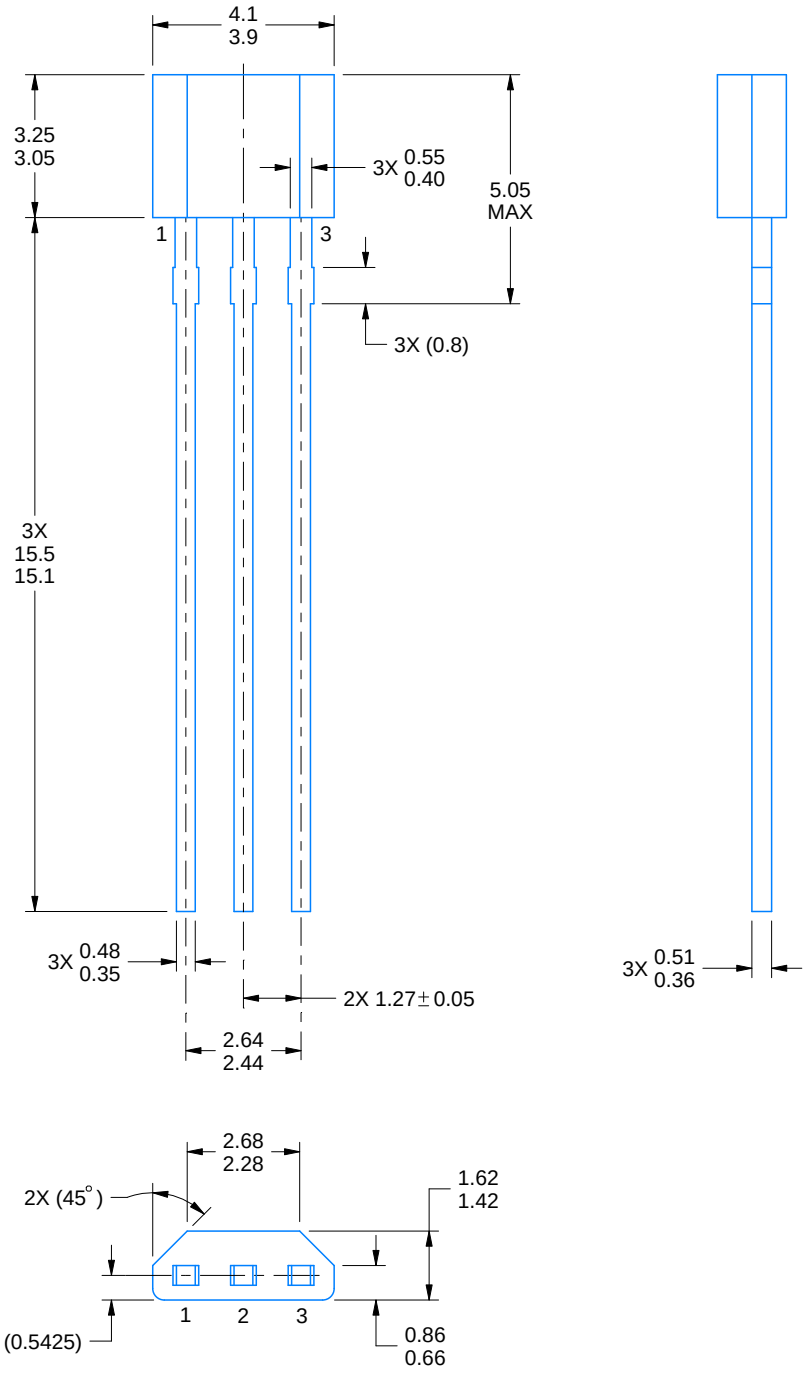
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



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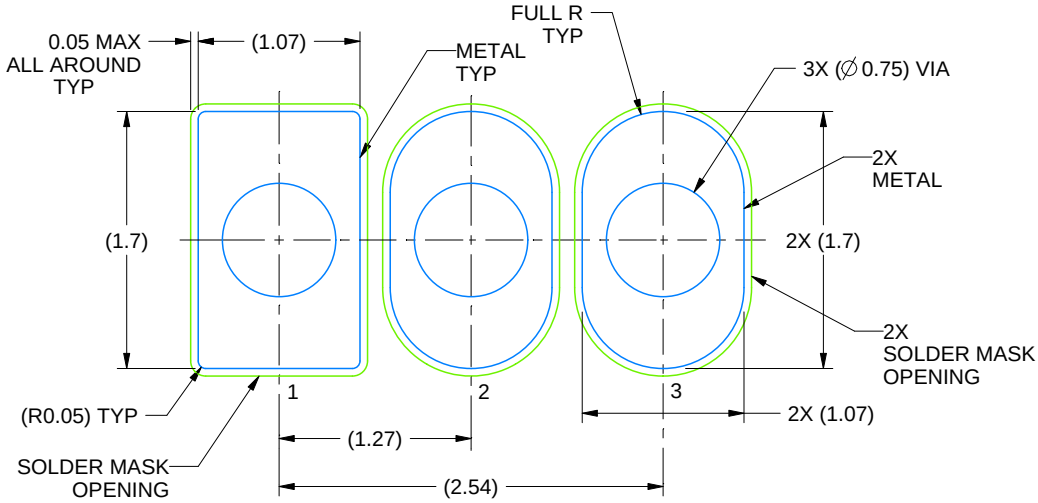
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

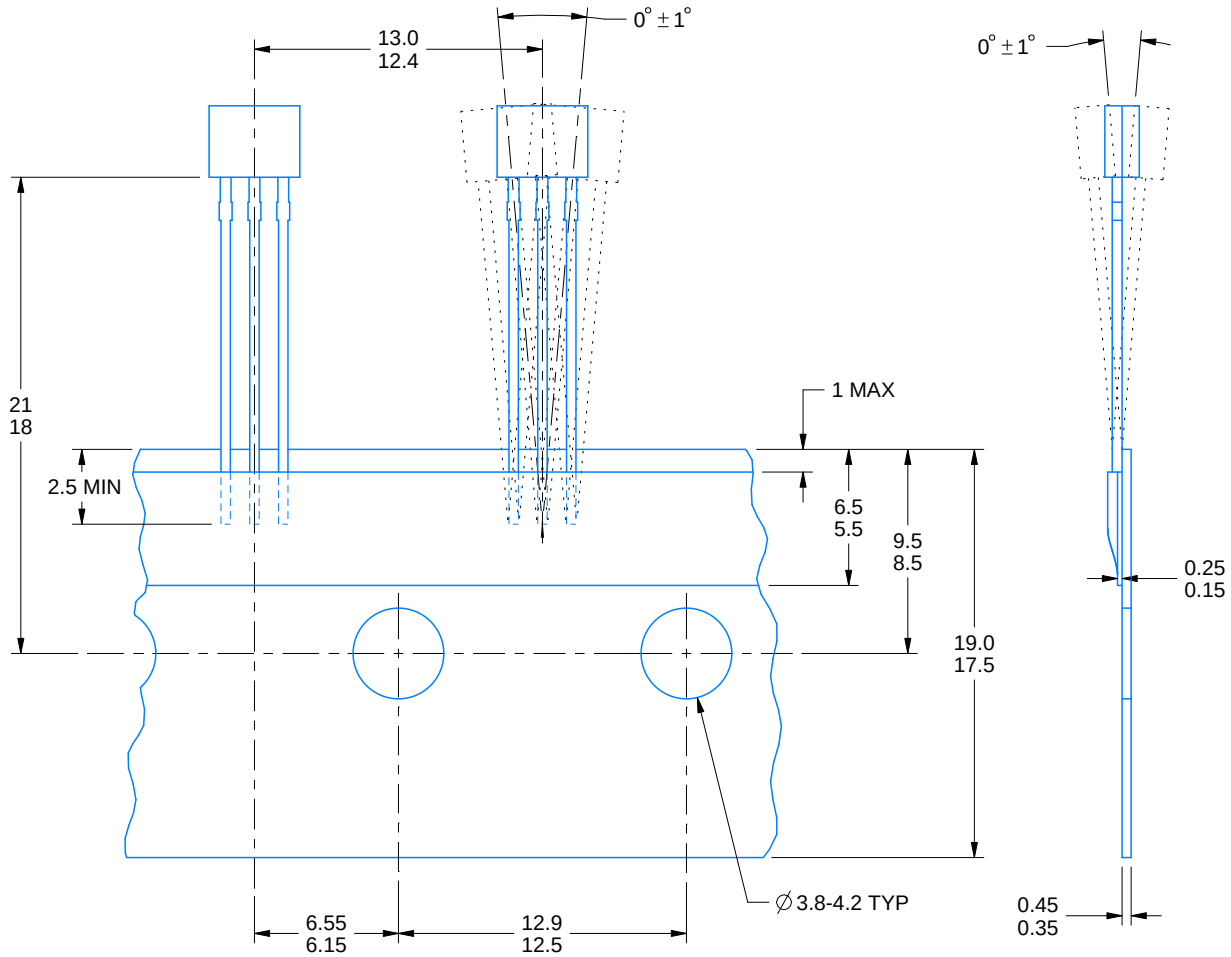
4221343/C 01/2018

TAPE SPECIFICATIONS

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



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