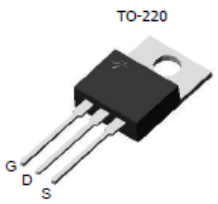
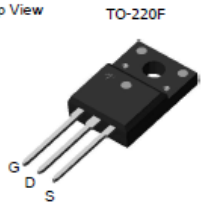
TMP20N50/TMPF20N50
TMP20N50G/TMPF20N50G

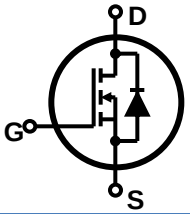
V_{DSS} = 550 V @T_{jmax}
I_D = 18A
$R_{DS(on)}$ = 0.3 Ω(max) @ V_{GS}= 10 V

Features

- Low gate charge
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant
- Halogen free package
- JEDEC Qualification







Device	Package	Marking	Remark
TMP20N50 / TMPF20N50	TO-220 / TO-220F	TMP20N50 / TMPF20N50	RoHS
TMP20N50G / TMPF20N50G	TO-220 / TO-220F	TMP20N50G / TMPF20N50G	Halogen Free

Absolute Maximum Ratings

Parameter		Symbol	TMP20N50(G)	TMPF20N50(G)	Unit
Drain-Source Voltage		V_{DS}	500		V
Gate-Source Voltage		V_{GS}	±30		V
Continuous Drain Current	T_C = 25 ℃	I_D	18	18*	A
	T_C = 100 ℃		13.1	13.1*	A
Pulsed Drain Current (Note 1)		I_{DM}	72	72*	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	954		mJ
Repetitive Avalanche Current (Note 1)		I_{AR}	18		A
Repetitive Avalanche Energy (Note 1)		E_{AR}	29		mJ
Power Dissipation	T_C = 25 ℃	P_D	290	48	W
	Derate above 25 ℃		2.32	0.38	W/℃
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5		V/ns
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150		℃
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		T_L	300		℃

* Limited only by maximum junction temperature

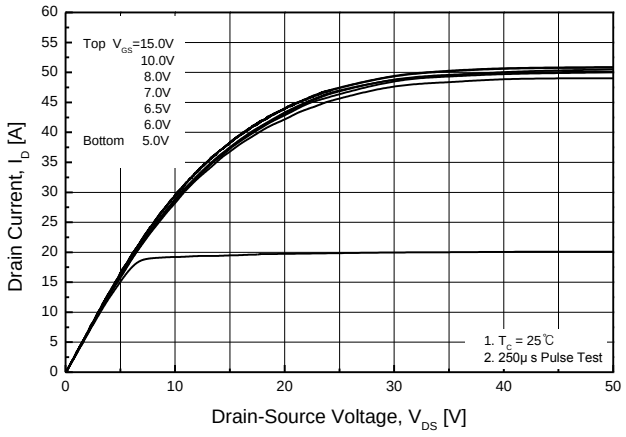
Thermal Characteristics

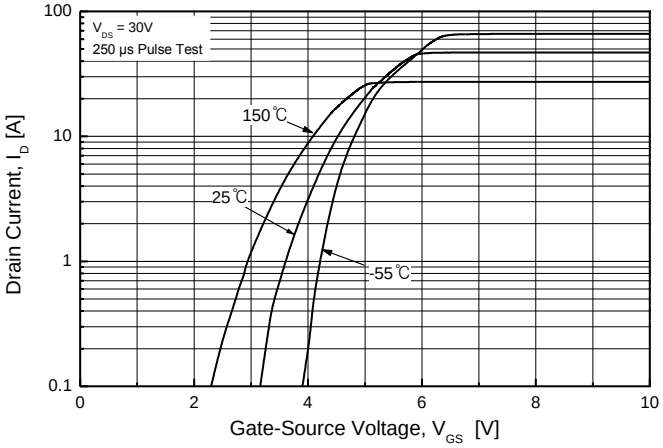
Parameter	Symbol	TMP20N50(G)	TMPF20N50(G)	Unit
Maximum Thermal resistance, Junction-to-Case	$R_{\theta JC}$	0.43	2.6	℃/W
Maximum Thermal resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	℃/W

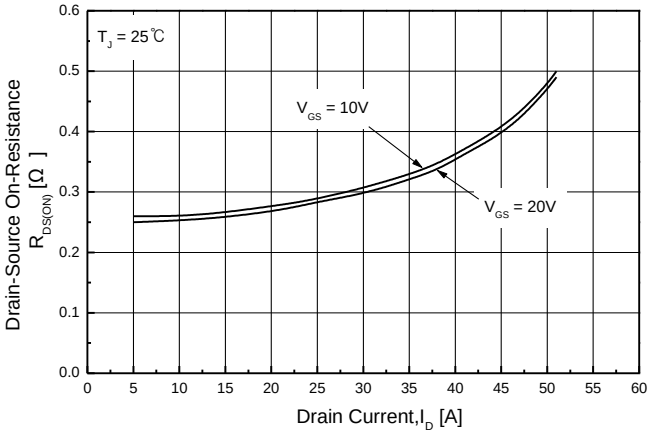
Electrical Characteristics : T_C=25℃, unless otherwise noted

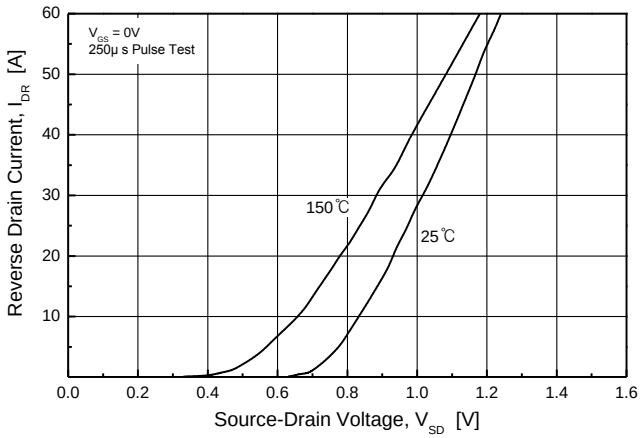
Parameter	Symbol	Test condition	Min	Typ	Max	Units
OFF						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 µA	500	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	µA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	µA
Forward Gate-Source Leakage Current	I_{GSSF}	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
Reverse Gate-Source Leakage Current	I_{GSSR}	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
ON						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2	--	4	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 9 A	--	0.25	0.3	Ω
Forward Transconductance (Note 4)	g_{FS}	V_{DS} = 30 V, I_D = 9 A	--	11	--	S
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	3094	--	pF
Output Capacitance	C_{oss}		--	296	--	pF
Reverse Transfer Capacitance	C_{rss}		--	9.2	--	pF
SWITCHING						
Turn-On Delay Time (Note 4,5)	$t_{d(on)}$	V_{DD} = 250 V, I_D = 18 A, R_G = 25 Ω	--	78	--	ns
Turn-On Rise Time (Note 4,5)	t_r		--	72	--	ns
Turn-Off Delay Time (Note 4,5)	$t_{d(off)}$		--	184	--	ns
Turn-Off Fall Time (Note 4,5)	t_f		--	68	--	ns
Total Gate Charge (Note 4,5)	Q_g	V_{DS} = 400V, I_D = 18 A, V_{GS} = 10 V	--	54	--	nC
Gate-Source Charge (Note 4,5)	Q_{gs}		--	15	--	nC
Gate-Drain Charge (Note 4,5)	Q_{gd}		--	12.5	--	nC
SOURCE DRAIN DIODE						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	--	--	18	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}	---	--	--	72	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 18 A	--	--	1.5	V
Reverse Recovery Time (Note 4)	t_{rr}	V_{GS} = 0 V, I_S = 18 A, dI_F / dt = 100 A/µs	--	426	--	ns
Reverse Recovery Charge (Note 4)	Q_{rr}		--	6	--	µC

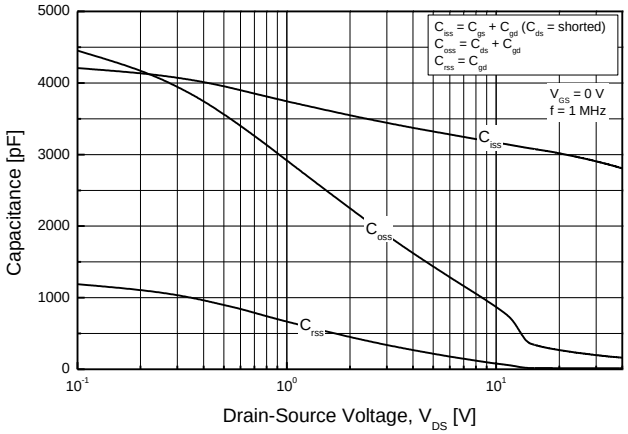
Note :
1. Repeated rating : Pulse width limited by safe operating area
2. L=5.3mH, I_{AS} = 18A, V_{DD} = 50V, R_G = 25Ω, Starting T_J= 25 ℃
3 I_{SD} ≤ 18A, di/dt ≤ 200A/µs , V_{DD} ≤ BV_{DS}, Starting T_J= 25 ℃
4. Pulse Test :Pulse width ≤ 300µs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

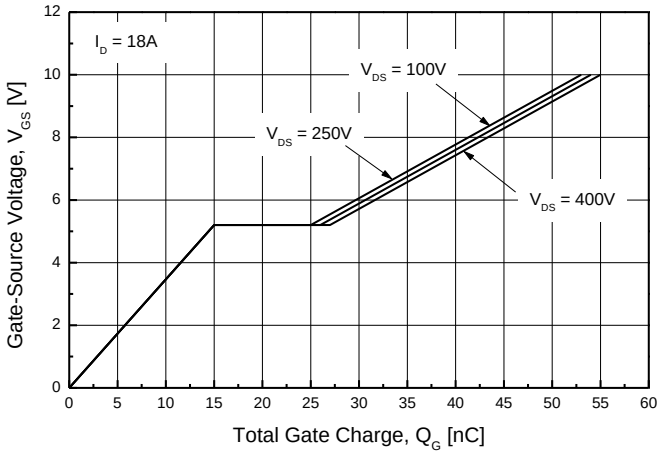

Top V_GS=15.0V
10.0V
8.0V
7.0V
6.5V
6.0V
Bottom 5.0V
1. T_c = 25℃
2. 250μ s Pulse Test
Drain Current, I_D [A]
Drain-Source Voltage, V_DS [V]

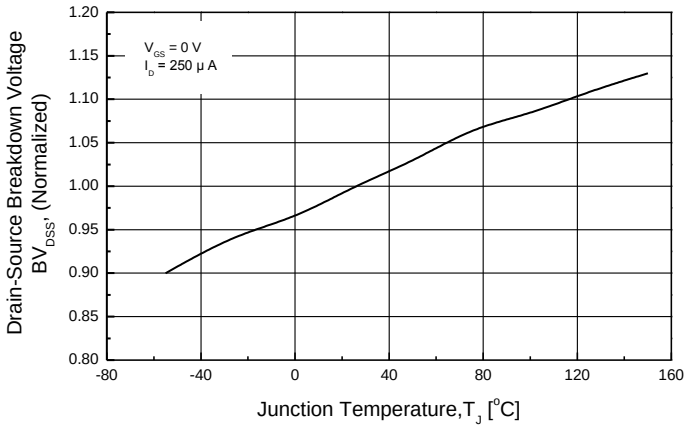

V_DS = 30V
250 μs Pulse Test
150℃
25℃
-55℃
Drain Current, I_D [A]
Gate-Source Voltage, V_GS [V]

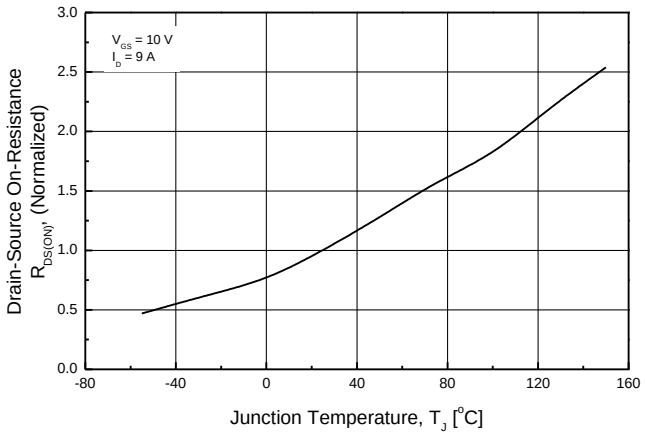

T_J = 25℃
V_GS = 10V
V_GS = 20V
Drain-Source On-Resistance
R_DS(ON) [Ω]
Drain Current,I_D [A]

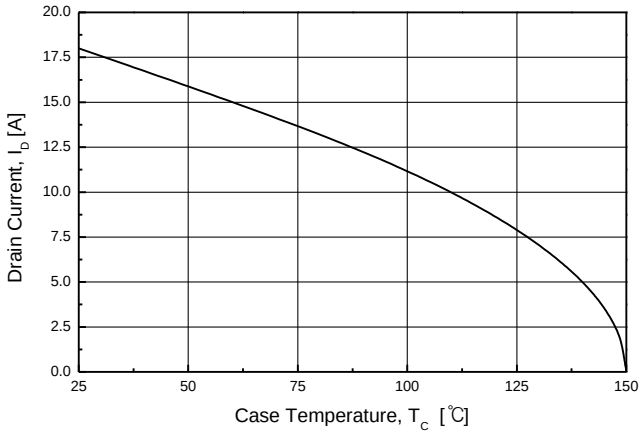

V_GS = 0V
250μ s Pulse Test
150℃
25℃
Reverse Drain Current, I_DR [A]
Source-Drain Voltage, V_SD [V]


C_iss = C_gs + C_gd (C_ds = shorted)
C_oss = C_ds + C_gd
C_rss = C_gd
V_GS = 0 V
f = 1 MHz
C_iss
C_oss
C_rss
Capacitance [pF]
Drain-Source Voltage, V_DS [V]

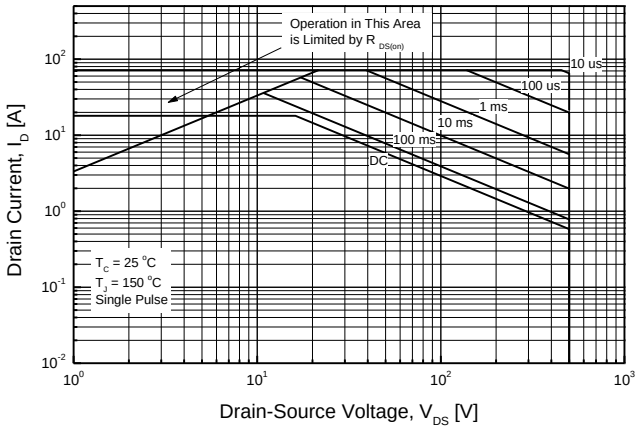

I_D = 18A
V_DS = 100V
V_DS = 250V
V_DS = 400V
Gate-Source Voltage, V_GS [V]
Total Gate Charge, Q_G [nC]



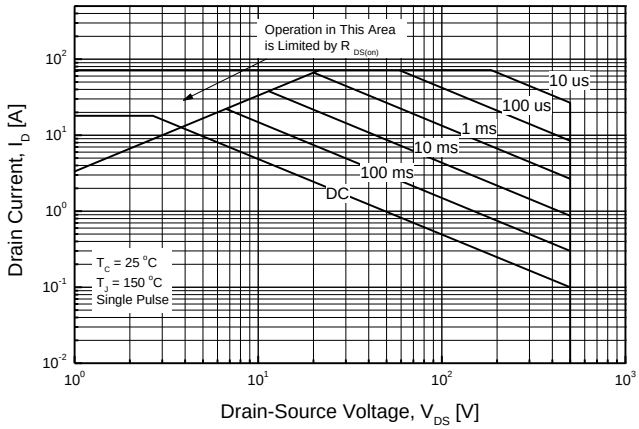




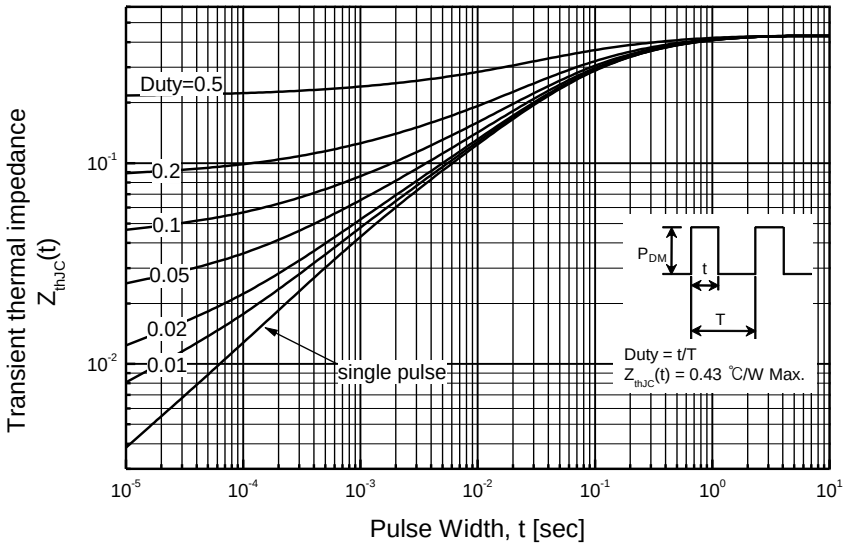
TMP20N50(G)



TMPF20N50(G)



TMP20N50(G)



TMPF20N50(G)