CMOS 4-BIT MICROCONTROLLER

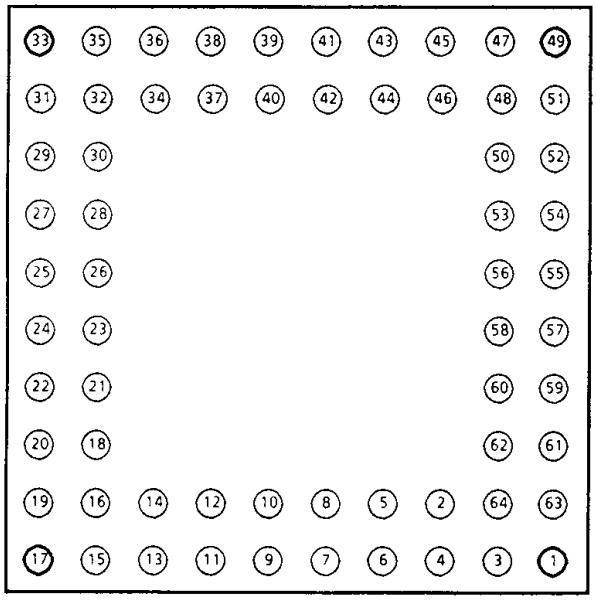
TMP42C00Y

The 42C00 is a system development evaluator chip used for development and operation confirmation of TLCS-42 systems. The electrical characteristics and some of the functions of TLCS-42 NMOS and TLCS-42 CMOS are different, but, functionally, various equivalent systems can be configured using the 42C00.

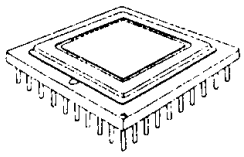
PART No.	ROM	RAM	PACKAGE
TMP42C00Y	1024 x 8-bit (external)	32 x 4-bit	PGA64

PIN ASSIGNMENTS (TOP VIEW)

PGA64



PGA64



TMP42C00Y

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
1	A8	14	$\overline{HALTA}$	27	$\overline{RESET}$	40	VSS	53	D3
2	A9	15	P40	28	P00	41	HR	54	D2
3	P30	16	P41	29	P01	42	P20	55	D1
4	P31	17	P42	30	P02	43	P21	56	D0
5	P32	18	P43	31	P03	44	P22 ($\overline{HOLD}$)	57	A0
6	P33	19	P50	32	$\overline{HOLDA}$	45	B0	58	A1
7	SPORT	20	P51	33	IHOLD	46	B1	59	A2
8	VSS	21	P52	34	SF	47	B2	60	A3
9	DPORT	22	P53	35	P10	48	B3	61	A4
10	DCY	23	CF	36	P11	49	D7	62	A5
11	$\overline{S3}$	24	VDD	37	P12	50	D6	63	A6
12	$\overline{S1}$	25	XOUT	38	P13	51	D5	64	A7
13	$\overline{HALTR}$	26	XIN	39	DACC	52	D4		

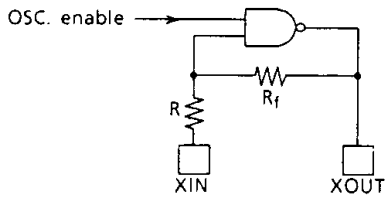
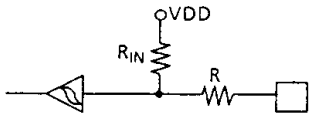
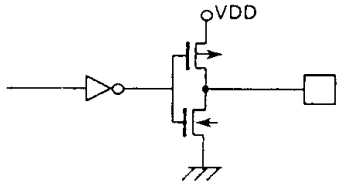
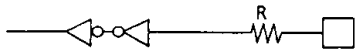
PIN FUNCTION

PIN NAME	INPUT/OUTPUT	FUNCTIONS
P03 - P00 P13 - P10	I/O	4-bit I/O port with latch, Same operations as NMOS product are performed after reset. Four types of input/output can be selected for CMOS products by executing the I/O control instruction [MOV A, P].
P22 ($\overline{HOLD}$)	I/O (INPUT)	3-bit I/O port with latch. Hold request / release signal input Same operations as NMOS product are performed after reset. Four types of input/output can be selected for CMOS products by executing the I/O control instruction [MOV A, P].
P21 P20	I/O	
P33 - P30 P43 - P40 P53 - P50	I/O	4-bit I/O port with latch. When using as input port, the latch must be set to "1".
A11 - A0	OUTPUT	Program memory address output
D7 - D0	INPUT	Program memory data input
$\overline{S1}$, $\overline{S3}$	OUTPUT	Internal clock output
B3 - B0		Internal bus data output
DCY		Internal operation state signal output. Indicates that the first of two instruction cycles is being executed.
DPORT		Port control signal output (Output latch pulse)
SPORT		Port control signal output (Input strove)
DACC		Control signal output which indicates the timing for loading data to accumulator
HR, SF, CF		Monitor outputs of H register, status flag and carry flag
$\overline{HALTR}$	INPUT	CPU halt request signal input. The CPU is set to the halt mode (actually, [NOP] instruction is executed) by inputting low level. Used in the address stop and single-step modes.
$\overline{HALTA}$	OUTPUT	Monitor output indicating when the CPU has entered the halt mode due to a halt request signal (HALTR).
$\overline{HOLDA}$		Monitor output indicating when the CPU has entered the hold operating mode due to a [HOLD] instruction (TLCS-42 CMOS only). Low level is output during the hold operating mode.
IHOLD	INPUT	Release signal input for hold operating mode.
XIN	INPUT	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.
XOUT	OUTPUT	
$\overline{RESET}$	INPUT	Reset signal input
VDD	Power Supply	+ 5V
VSS		0V (GND)

INPUT/OUTPUT CIRCUITRY

1. CONTROL PINS

The input/output circuits of 42C00 control pins are shown below. Only ceramic oscillators are supported.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	INPUT OUTPUT		Resonator connecting pins R = 1KΩ (typ.) R_f = 1MΩ (typ.)
$\overline{RESET}$	INPUT		Hysteresis input Pull-up resistor R_{IN} = 160KΩ (typ.) R = 1KΩ (typ.)
A11-A0 $\overline{S1}$, $\overline{S3}$ B3-B0 DCY DPORT SPORT DACC HR SF, CF $\overline{HALTA}$ $\overline{HOLDA}$	OUTPUT		Push-pull output
D7-D0 $\overline{HALTR}$ IHOLD	INPUT		R = 1KΩ (typ.)

2. I/O PORTS (NOTES FOR USE)

The 42C00Y is functionally different from CMOS and NMOS products with a pull-up resistor as follows.

(1) P0 (P03~P00), P1 (P13~P10), P2 (P22~P20) port

The 42C00Y P0~P2 port circuitries can be used the same as CMOS products by executing the I/O control instruction [MOV A, P]. (Refer to Figure 1.)

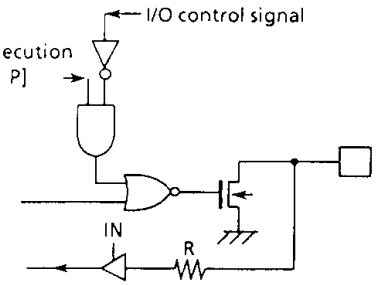
PORT	I/O	CIRCUITRY	INITIAL STATE	REMARKS
P0 P1 P2	I/O		Hi-Z (INPUT)	Same as CMOS products using the I/O control instruction [MOV A, P]. Always necessary after initializing and before port access when CMOS products are the target.

Figure 1. P0, P1, P2 port

In addition the I/O ports of CMOS products do not include a pull-down resistor in the input modes, so that external resistor is necessary when configuring input circuitries for CMOS products. In case of not executing the instruction, P0~P2 port circuitries are the same as NMOS products with a pull-up resistor.

(2) P3 (P33~P30), P4 (P43~P40), P5 (P53~P50) port

The P3~P5 port circuitries are configured as sink open drain I/O port. (Refer to Figure 2.)

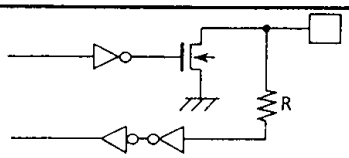
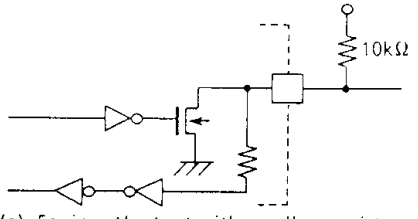
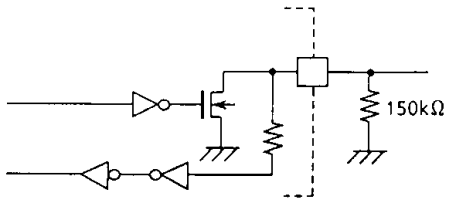
PORT	I/O	CIRCUITRY	INITIAL STATE	REMARKS
P3 P4 P5	I/O		Hi-Z (INPUT)	Sink open drain output (R = 1KΩ typ.)

Figure 2. P3, P4, P5 port

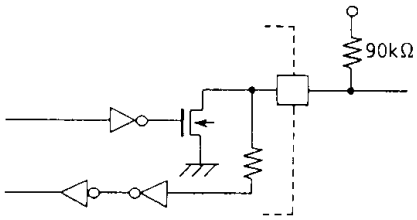
External resistor is necessary when configuring the same as I/O ports of NMOS products with a pull-up resistor and CMOS products. (Refer to Figure 3.)



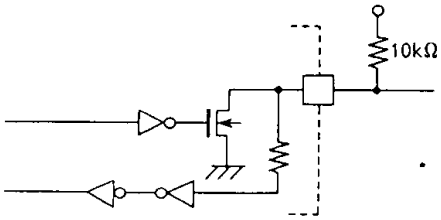
(a) For input/output with a pull-up resistor



(b) For input with a pull-down transistor



(c) For input with a pull-up resistor



(d) For push-pull output

Figure 3. Example of external circuitry

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
Input Voltage	V_{IN}		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	− 0.5 to 12	
Power Dissipation [T_{opr} = 85°C]	PD		300	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 40 to 85	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 40 to 85°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}			4.0	6.0	V
Input High Voltage	V_{IH1}	Except sink open drain pin		V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Sink open drain pin		V_{DD} × 0.8		
Input Low Voltage	V_{IL1}	Except sink open drain pin		0	V_{DD} × 0.3	V
	V_{IL2}	Sink open drain pin			V_{DD} × 0.2	
Clock Frequency	fc		V_{DD} = 4.0 to 6.0V	0.2	2.0	MHz
			V_{DD} = 4.5 to 6.0V		5.0	

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = −40 to 85°C)

PARAMETER	SYMBOL	PIN	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.3	−	V
Input Current	I_{IN}	Open drain pin	V_{DD} = 6V, V_{IN} = 0V	−	−	− 2.0	μA
Input Resistance	R_{IN}	$\overline{RESET}$		65	160	340	KΩ
Output Leakaged Current	I_{LO}	Open drain pin	V_{DD} = 6V, V_{OUT} = 6V	−	−	2.0	μA
Output Low Current	I_{OL}	Ports P0-P5	V_{DD} = 4.5V, V_{OL} = 0.4V	1.6	5.0	−	mA
Supply Current (In the Normal mode)	I_{DD}		V_{DD} = 6V, fc = 2MHz	−	1.5	5.0	mA
Supply Current (In the HOLD mode)	I_{DDH}		V_{DD} = 6V	−	5.0	20	μA

Note 1 : Typ. values shows those at VDD = 5V, Topr = 25°C.

Note 2 : Supply Current in the Normal operating mode : $\overline{RESET}$ pin is 0V, and XOUT pin and ports are opened in the external clock operation.

Note 3 : Supply Current in the Hold operating mode : All pins except the power supply pins (VDD, VSS) are opened.
sink open drain pin is fixed to OV.

A.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = −40 to 85°C)

PARAMETER	SYMBOL	CONDITIONS		Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	V_{DD} = 4.0 to 6.0V		2.5	−	25	μs
		V_{DD} = 4.5 to 6.0V		1.0	−	25	
High level Clock pulse Width	t_{WCH}	$V_{IN} = V_{IH}$	For external clock operation	100	−	−	ns
Low level Clock pulse Width	t_{WCL}	$V_{IN} = V_{IL}$					