SPECIFICATION OF TMP4310APL/TMP4310APLL

This specification is applied to TMP4310APL/TMP4310APLL, one of versions of TLCS-43.

TMP4310APL/TMP4310APLL is the low power version of TMP4310AP. There are some differences in electrical characteristics between TMP4310APL/TMP4310APLL and TMP4310AP; however, their functions, instructions and pin connections are compatible. When using and examining TMP4310APL/TMP4310APLL, therefore, it is recommended that this specification be used together with the technical data on TMP4310AP.

Main differences in electrical characteristics between AP and APL/APLL are as follows:

1. Basic clock

   Internal oscillation (with resistance externally installed between X_{IN} and $\overline{TEST}$) and external clock supply can be available.

 1.1 Frequency of external supply clock

   f=200kHz to 400kHz (APL) (V_{DD}=5.5V ± 20%, T_{opr}=0°C to 55°C)

   f=50kHz to 200kHz (APLL)

 1.2 Internal oscillation frequency

   f=200kHz to 400kHz (APL, R_X=56kΩ) (V_{DD}=5.5V ± 20%, T_{opr}=0°C to 55°C)

   f=110kHz to 200kHz (APLL, R_X=110kΩ)

2. Low input voltage and clock low input voltage (at time of external supply)

   V_{IL} MAX.=V_{CL} MAX.=0.55V (V_{DD}=5.5V ± 20%, T_{opr}=0°C to 55°C)

3. High output voltage

   V_{OH} MIN.=2.4V (V_{DD}=5.5V ± 20%, T_{opr}=0°C to 55°C, I_{OH}=-50μA)

4. Supply current

   I_{DD} TYP.=30mA, I_{DD} MAX.=45mA (APL) (V_{DD}=6.0V, T_{opr}=25°C)

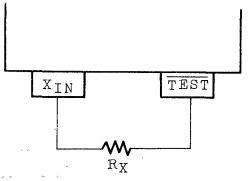
   I_{DD} TYP.=15mA, I_{DD} MAX.=27mA (APLL)

5. Pull up resistance of $\overline{RST}$ and $\overline{INT}$ terminals is not contained.

TMP4310APL/TMP4310APLL BASIC CLOCK

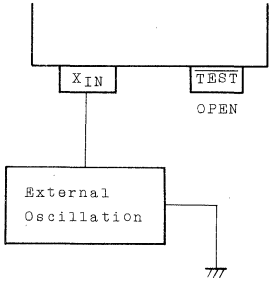
The methods of generating and supplying the basic clock of TMP4310APL/TMP4310APLL are as follows:

(1) Internal oscillation



The basic clock of TMP4310APL/TMP4310APLL can be obatined by connecting the resistance as shown in the left figure.
(f_{osc}=200kHz to 400kHz at R_X=56kΩ, APL)
(f_{osc}=110kHz to 200kHz at R_X=110kΩ, APLL)

(2) Supply of external clock



The basic clock of TMP4310APL/TMP4310APLL can be supplied from the external oscillation circuit as shown in the left figure.

TMP4310APL/TMP4310APLL ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING

SYMBOL	ITEM	RATING
V_{DD}	Supply Voltage	-0.5V to 7V
V_{IN}	Input Voltage	-0.5V to 7V
V_{OUT1}	Output Voltage (Except open drain terminal)	-0.5V to 7V
V_{OUT2}	Output Voltage (Open drain terminal)	-0.5V to 10V
Tstg	Storage Temperature	-55°C to 125°C
Topr	Operating Temperature	0°C to 55°C
Tsld	Soldering Temperature	260°C (10sec.)

D.C. CHARACTERISTICS (V_{DD}=5.5V±20%, Topr=0°C to 55°C) Unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IH1}	Input High Voltage	(INO, IOO, IO1, IO2, $\overline{RST}$)	-	2.2	-	V_{DD}	V
V_{IH2}		($\overline{INT}$)	-	3.5	-	V_{DD}	V
V_{IL}	Input Low Voltage		-	0	-	0.55	V
V_{CH}	Clock Input High Voltage (X_{IN})		External clock supply	3.8	-	V_{DD}	V
V_{CL}	Clock Input Low Voltage (X_{IN})			0	-	0.55	V
I_{IN1}	Input Current (INO, $\overline{RST}$, $\overline{INT}$)		V_{IN} = V_{DD}	-	-	20	μA
I_{IN2}	Input Current (IOO, IO1, IO2)	Open Drain	V_{IN} = V_{DD}	-	-	20	μA
		Pull Up	-	-	-	-	-
I_{IL1}	Input Low Current (IOO, IO1, IO2)	Open Drain	-	-	-	-	-
		Pull Up	V_{IN} = 0.55V	-	-	-1.6	mA
I_{LO}	Output Leak Current (OTO, OT1)	Open Drain	V_{OUT} = V_{DD}	-	-	20	μA
		Pull Up	-	-	-	-	-
V_{OH}	Output High Voltage	Open Drain	-	-	-	-	-
		Pull Up	I_{OH} = -50μA	2.4	-	-	V
V_{OL}	Output Low Voltage		I_{OL} = 1.6mA	-	-	0.4	V
I_{DD}	Supply Current	APL	V_{DD}=6.0V, Ta=25°C	-	30	45	mA
		APLL		-	15	27	mA

Pull-Up resistance of $\overline{RST}$ and $\overline{INT}$ terminals is not contained.

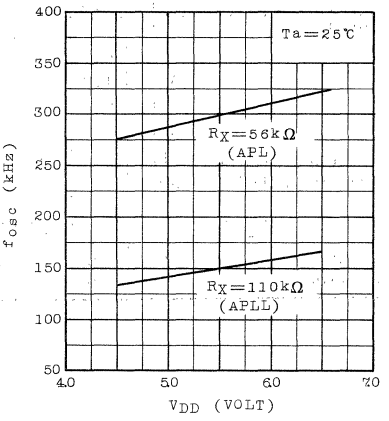
Low output voltage: It is possible that output port OT1 sinks large output current I_{OL} Typ.=20mA (V_{OL}=2V) for each pins. At the time when OT1 sinks large output current, low output voltage (V_{OL}) becomes V_{OL} Max.≈0.5V (I_{OL}=1.6mA).

A.C. CHARACTERISTICS (V_{DD}=5.5V±20%, T_{opr}=0°C to 55°C)

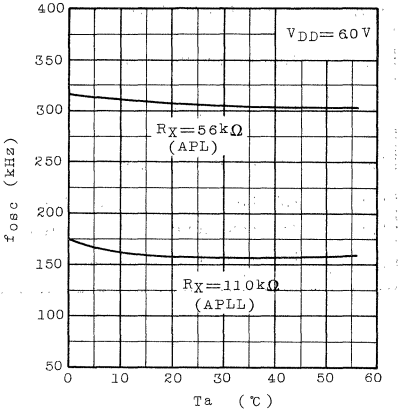
SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
$t_{\phi O}$	Clock Cycle Time	External clock supply	APL	2.5	-	5.0	μs
			APLL	5	-	20	μs
t_S	Input Set Up Time	-	APL	0.9	-	-	μs
			APLL	1.8	-	-	μs
t_H	Input Hold Time	-	APL	0.9	-	-	μs
			APLL	1.8	-	-	μs
t_D	Output Delay Time	C_L=50pF, R(Pull up)=50kΩ, 1TTL	APL	-	-	1.8	μs
			APLL	-	-	3.6	μs
t_{INT}	$\overline{INT}$ Low Level Pulse Width	-		4	-	-	Cycle
t_{RST}	$\overline{RST}$ Low Level Pulse Width	-		4	-	-	Cycle
f_{osc}	Internal Oscillation Frequency	R =56kΩ	APL	200	-	400	kHz
		R =110kΩ	APLL	110	-	200	kHz

TYPICAL CHARACTERISTICS

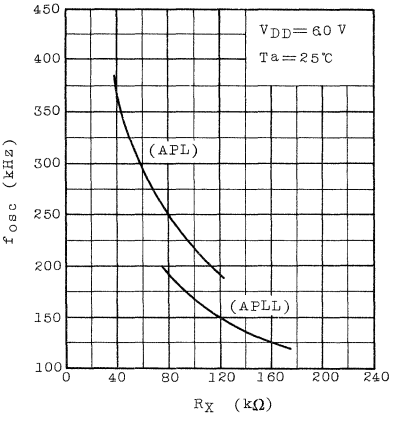
f_{osc} - V_{DD}

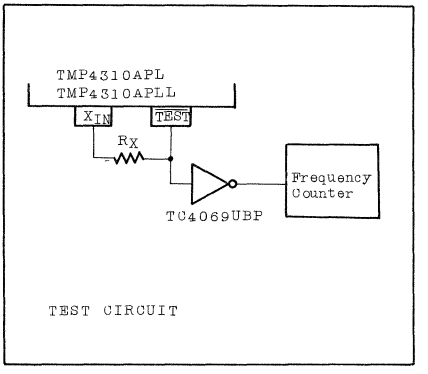


f_{osc} - Ta



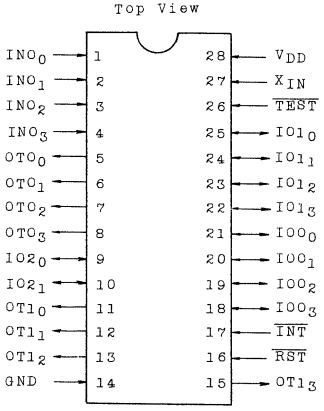
f_{osc} - R_X





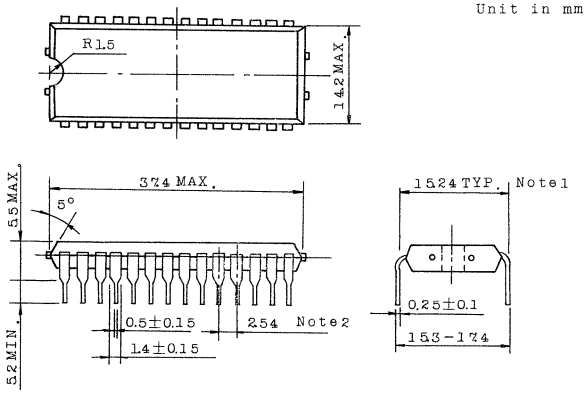
PIN CONNECTIONS

Top View



OUTLINE DRAWINGS

Unit in mm



Note 1. This dimension is measured at the center of bending point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical position with respect to No.1 and No.28 leads.