TMP4321AP

TOSHIBA MOS Digital Integrated Circuit
Silicon Monolithic
N-channel Silicon Gate Depression Load

GENERAL DESCRIPTION

TMP4321AP is one version of single-chip microcomputer TLCS43 series processed with NMOS.

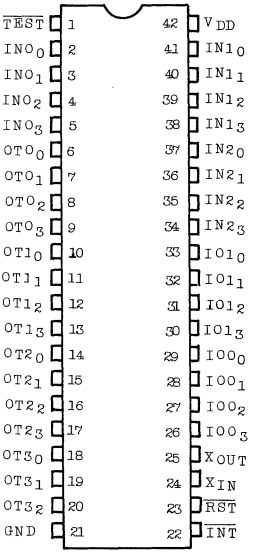
Since TMP4321AP can make periodic interrupt gained by dividing the CPU clock to 512 or 1024 using the built-in prescaler, it is most appropriate for computer control, such as sequence control.

Refer to the technical data of TLCS43 when using or considering TMP4321AP.

FEATURES

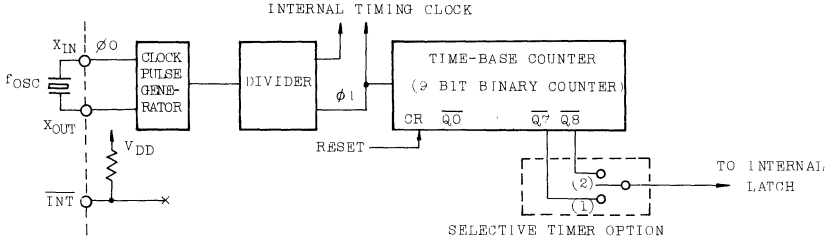
- o Software compatible with TLCS43 series
- o ROM capacity: 2048W x 8 Bits
- o RAM capacity: 128W x 4 Bits
- o Instruction executing rate: 4 μs
- o Input ports: 3 x 4 Bits
- o Input/output ports: 2 x 4 Bits
- o Output ports: 3 x 4 Bits
  1 x 3 Bits
- o Interrupt level: 1 level (Interrupt by timer)
- o Subroutine nesting: 4 levels (including interrupt level)
- o ROM data readout instructions
- o I/O level: TTL compatible
- o Ports available for large current output: 2 x 4 Bits
- o +5V single power operating (operating voltage margin: 5V ± 10%)
- o Operating temperature range: -10 ∿ 70°C

PIN CONNECTIONS



TIMER INTERRUPT

The following figure shows the configuration of timer interrupt circuit of TMP4321AP.



As shown in the above figure, interrupt is not caused by external source via $\overline{INT}$ pin, but it is only caused by the output divided by the built-in prescaler. The $\overline{INT}$ pin is usually set to "H" level (open) by the pull-up resistor, but it is not connected with the internal circuit.

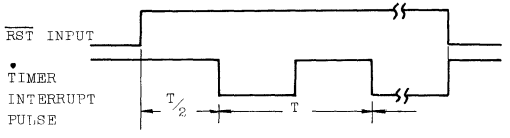
Assignment of selective timer option is as follows :

(1) Option INTDV7 is interrupted at $\frac{1}{fosc}$ x 512(S) cycle ($\overline{Q7}$).

(2) Option INTDV8 is interrupted at $\frac{1}{fosc}$ x 1024(S) cycle ($\overline{Q8}$).

(Refer to "Mask Option Assignment" in the technical data of TLCS43 for further details.)

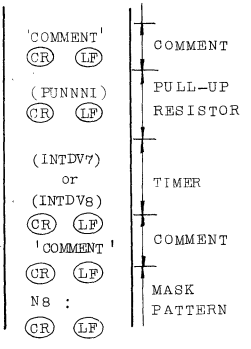
The relation between timer interrupt and reset is shown in the following figure.



T : INTERRUPT CYCLE BY OPTION ASSIGNMENT

Initial interrupt occurs at T/2 interval after the $\overline{RST}$ input is released, and then repeatedly occurs by every T cycle.

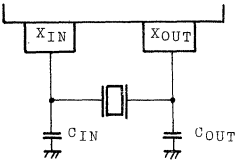
MASK ROM DATA TAPE FORMAT



BASIC CLOCK

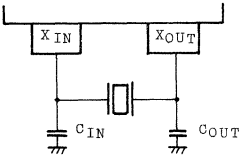
The following are four methods to generate and supply the basic clock pulse in the TMP4321AP.

(1) Direct connection of crystal oscillator



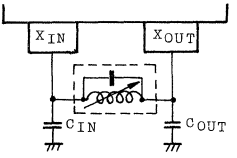
When a crystal oscillator has been connected to TMP4321AP as shown in the left figure, the basic clock pulse is generated at the frequency inherent in the crystal oscillator.
Recommendations for C_{IN} and C_{OUT}
$C_{IN}=C_{OUT}=60pF$ ($f_{OSC} \approx 500KHz$)

(2) Direct connection of ceramic oscillator



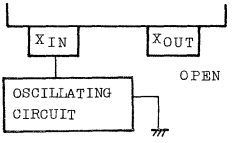
When a ceramic oscillator has been connected to TMP4321AP as shown in the left figure, the basic clock pulse is generated at the frequency inherent in the ceramic oscillator.
Recommendations for C_{IN} and C_{OUT}
$C_{IN}=C_{OUT}=100pF$ ($f_{OSC} \approx 500KHz$)

(3) Direct connection of IFT



When a IFT has been connected to TMP4321AP as shown in the left figure, the basic clock pulse is determined according to the circuit constant.
Recommendations for C_{IN} and C_{OUT}
$C_{IN}=C_{OUT}=100pF$ ($f_{OSC} \approx 500KHz$)

(4) Supply of external clock



The basic clock pulse of TMP4321AP can be supplied by an external oscillating circuit as shown in the left figure.

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply Voltage	-0.5 ∿ 7	V
V_{IN}	Input Voltage	-0.5 ∿ 7	V
V_{OUT1}	Output Voltage (except open drain terminal)	-0.5 ∿ 7	V
V_{OUT2}	Output Voltage (open drain terminal)	-0.5 ∿ 10	V
I_{OUT1}	Output Current (except OT1, OT2)	4	mA
I_{OUT2}	Output Current (OT1, OT2)	30	mA
Tstg	Storage Temperature	-55 ∿ 125	°C
Topr	Operating Temperature	-10 ∿ 70	°C
Tsld	Solder Temperature	260 (10 sec.)	°C
P_W	Power Dissipation (Ta = 70°C)	850	mW

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V±10%, Topr = -10 ∿ 70°C)

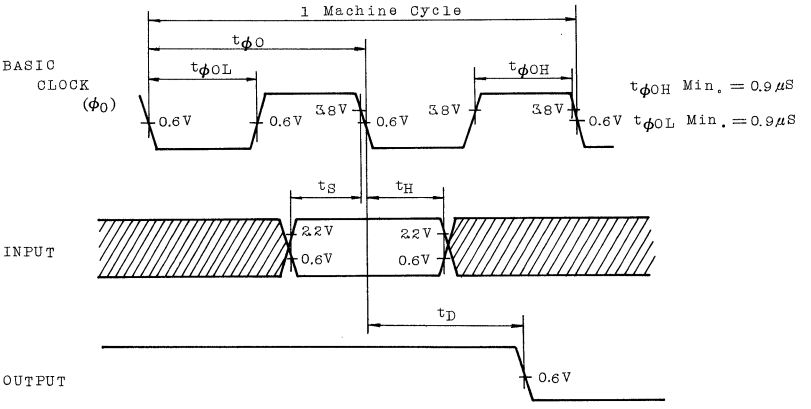
SYMBOL	PARAMETER		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IH1}	Input High Voltage (IN0, IN1, IN2, IO0, IO1, $\overline{RST}$)		-	2.2	-	V_{DD}	V
V_{IH2}	Input High Voltage ($\overline{INT}$)		-	3.5	-	V_{DD}	V
V_{IL}	Input Low Voltage		-	0	-	0.6	V
V_{CH}	Input High Clock Voltage (XIN)		-	3.8	-	V_{DD}	V
V_{CL}	Input Low Clock Voltage (XIN)		-	0	-	0.6	V
I_{IN1}	Input Current (INo, IN1, IN2)		V_{IN} = V_{DD}	-	-	20	µA
I_{IN2}	Input Current (IO0, IO1)	Open Drain	V_{IN} = V_{DD}	-	-	20	µA
		Pull Up	-	-	-	-	-
I_{IL1}	Input Low Current (IO0, IO1)	Open Drain	-	-	-	-	-
		Pull Up	V_{IN} = 0.6V	-	-	-1.6	mA
I_{IL2}	Input Low Current ($\overline{RST}$, $\overline{INT}$)		V_{IN} = 0.6V	-	-	-0.1	mA
I_{LO}	Output Leak Current (OT0, OT1, OT2, OT3)	Open Drain	V_{OUT} = V_{DD}	-	-	20	µA
		Pull Up	-	-	-	-	-
V_{OH}	Output High Voltage (except XOUT)	Open Drain	-	-	-	-	-
		Pull Up	I_{OH} =-100µA	2.4	-	-	V
V_{OL}	Output Low Voltage (except XOUT)		I_{OL} = 1.6 mA	-	-	0.4	V
I_{DD}	Supply Current		-	-	40	80	mA

Output Low Voltage : Output large current I_{OL} TYP.=20mA (V_{OL}=2V) is made possible by output ports OT1, OT2. When output large current sinks, output low voltage becomes V_{OL} MAX.≈0.5V(I_{OL}=1.6mA).

A.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V±10%, Topr = -10 ∿ 70°C) Refer to Timing Chart.

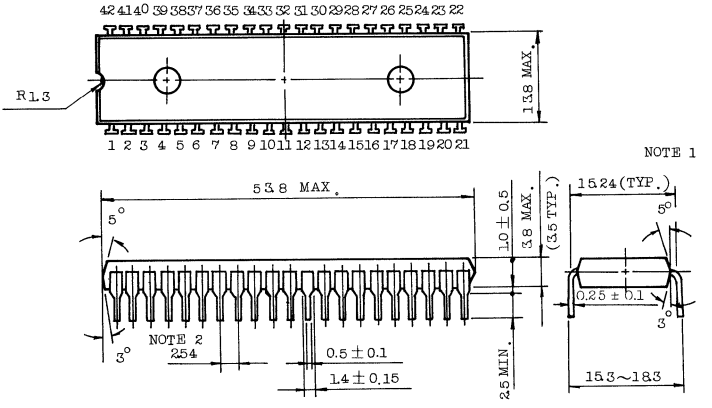
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$t_{\phi 0}$	Clock Cycle Time	-	2	-	5	µS
t_S	Input Setup Time	-	0.9	-	-	µS
t_H	Input Hold Time	-	0.9	-	-	µS
t_D	Output Delay Time	C_L=50pF, R(Pull Up)=50kΩ,1TTL	-	-	1.8	µS
t_{INT}	$\overline{INT}$ (Low Level Width)	-	4	-	-	Cycle
t_{RST}	$\overline{RST}$ (Low Level Width)	-	4	-	-	Cycle

TIMING CHART



EXTERNAL VIEW OF PACKAGE (Plastic Package)

Unit: mm



Note 1. The dimension of this external view indicates the lead bending center.

Note 2. Lead pitch is 2.54mm and tolerance is ± 0.25mm against theoretical center of each lead that is obtained on the basis of No.1 and No.42 leads.