Toshiba 東芝

INTEGRATED CIRCUIT

TECHNICAL DATA

TMP4399C

TOSHIBA MOS Digital Integrated Circuit

Silicon Monolithic

N-channel Silicon Gate Depletion Load

DESCRIPTION

TMP4399C is a single-chip microcomputer for evaluation, provided with the general purpose 16K EPROM (TMM323D) inserting socket, being capable of developing and checking hardware and software of TLCS-43 Application System by use of the EPROM.

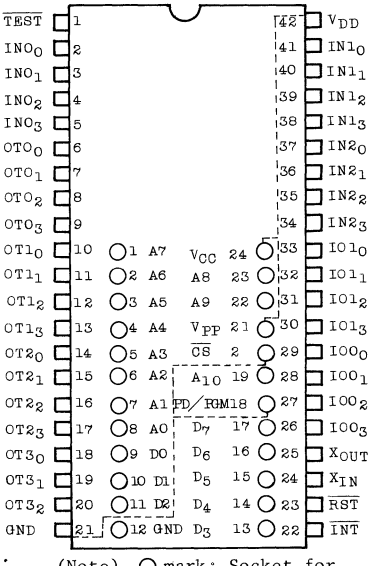
TMP4399C is equipped with a 24-pin socket which may directly mount the general purpose 16K EPROM (TMM323D) on the surface of the package. Therefore, when the fixed program written in the general purpose 16K EPROM is mounted on the package, TMP4399C becomes pin-compatible with TMP4315BP/TMP4320AP as the end product which the program has been written in the mask ROM. The former operates the same as the latter.

TMP4399C can be used within the range of a microcomputer for evaluating the TLCS-43 system as well as for mounting an equipment made on an experimental basis.

FEATURES

- o General purpose 16K EPROM TMM323D (equivalent to INTEL2716) can be used.
- o Compatible with TLCS-43 single-chip microcomputer family TMP4315BP/4320AP in pin.
- o Compatible with TLCS-43 Series in software.
- o ROM 2KW x 8 BIT RAM 128W x 4 BIT
- o Can be operated by +5V single power supply. Voltage margin is ±10% equal to that of mass-produced products.
- o Operating temperature range is -10 ∿ 70°C equal to that of mass-produced products.

PIN CONNECTIONS

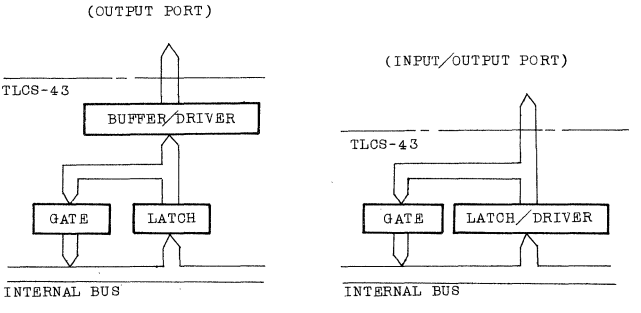


(Note) ○ mark: Socket for TMM323D

PRECAUTIONS FOR USING TMP4399C

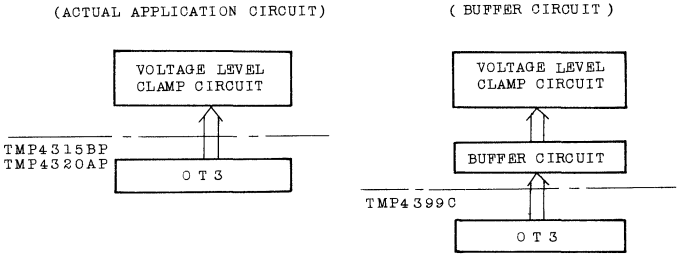
1. Precautions for using OT3 Output Port

The output port and input/output port of TLCS-43 are composed as shown in the following figures.



Therefore, when the circuit which clamps the output voltage level is connected directly to the outside of terminal, if the output data is referred to by the program, for the output port such data can be normally read, but for the input/output port erroneous data may be read unless the voltage level can be ensured as an input signal by the clamp circuit. For the purpose of reading correct data, it is necessary to separate the terminal from the clamp circuit by the buffer circuit.

The output port OT3 of TMP4399C serves as an input/output port owing to the configuration of the chip. In case of the system using TMP4315BP or TMP4320AP, therefore, if the output data of OT3 Port must be referred to by the program, care should be taken that the circuit which clamps the output level may not be connected directly to OT3 Port at the stage of development where TMP4399C is used.



2. Precautions for using large output current

In case of TMP4399C, each terminal of the output port OT1 and OT2 may sink large output current I_{OL} =20mA TYP. (V_{OL} =2V) when there ports sink large output current, a part of the DC electrical characteristics is changed. Attention should be paid to the main characteristics that the high input voltage of V_{IH1} and the low output voltage of V_{OL} at every terminal to be applied will become the valurs shown as follows:

V_{IH1} MIN. $\gtrsim$ 2.3 $\sim$ 2.4V

V_{OL} MAX. $\lesssim$ 0.5 $\sim$ 0.6V (I_{OL} = 1.6mA.)

The maximum rating of large output current is 30 mA.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Symbol	CHARACTERISTICS	RATING	UNIT
V_{DD}	Supply Voltage	-0.5 ∿ 7	V
V_{IN}	Input Voltage	-0.5 ∿ 7	V
V_{OUT1}	Output Voltage(excepting open drain terminal)	-0.5 ∿ 7	V
V_{OUT2}	Output Voltage(Open drain terminal)	-0.5 ∿ 10	V
I_{OUT1}	Output Current(Excepting OT1, OT2)	4	mA
I_{OUT2}	Output Current (OT1, OT2)	30	mA
T_{stg}	Storage Temperature	-55 ∿ 125	°C
T_{opr}	Operating Temperature	-10 ∿ 70	°C
T_{sld}	Soldering Temperature	260(10 sec.)	°C
P_W	Power Consumption (Ta = 70°C)	1	W

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, T_{opr} = -10 ∿ 70°C)

Symbol	CHARACTERISTICS	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IH1}	Input High V.(excepting $\overline{INT}$, X_{IN})	-	2.2	-	V_{DD}	V
V_{IH2}	Input High Voltage ($\overline{INT}$)	-	3.5	-	V_{DD}	V
V_{IL}	Input Low Voltage	-	0	-	0.6	V
V_{CH}	Clock Input High Voltage (X_{IN})	-	3.8	-	V_{DD}	V
V_{CL}	Clock Input Low Voltage (X_{IN})	-	0	-	0.6	V
I_{IN}	Input Current(excepting $\overline{RST}$, $\overline{INT}$)	V_{IN} = V_{DD}	-	-	20	μA
I_{IL2}	Input Low Current ($\overline{RST}$, $\overline{INT}$)	V_{IN} = 0.6V	-	-	-0.1	mA
I_{LO}	Output Leak Current(OTO,OT1,OT2)	V_{OUT} = V_{DD}	-	-	20	μA
V_{OH}	Output High Voltage (A0 ∿ A10)	I_{OH} = -100μA	24	-	-	V
V_{OL}	Output Low V. (excepting X_{OUT})	I_{OL} = 1.6 mA	-	-	0.4	V
I_{DD}	Supply Voltage	-	-	70	120	mA

[Operation of Evaluator Chip] Refer to the paragraph entitled "Precautions for Using Large Output Current".

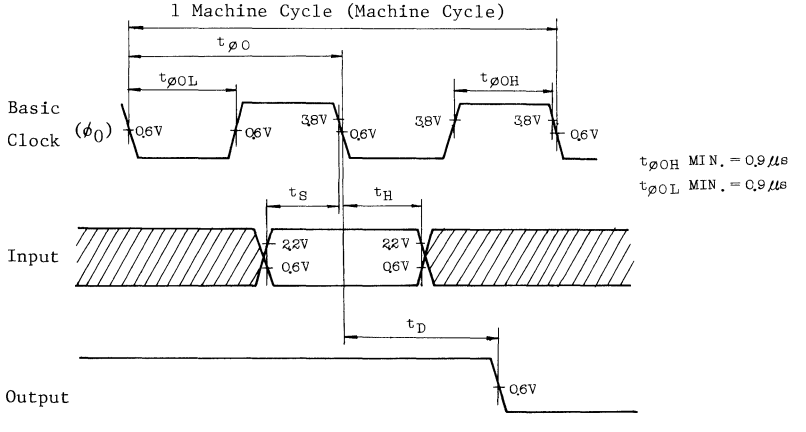
Refer to timing charts (1) and (2).

A.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, T_{opr} = -10 ∿ 70°C)

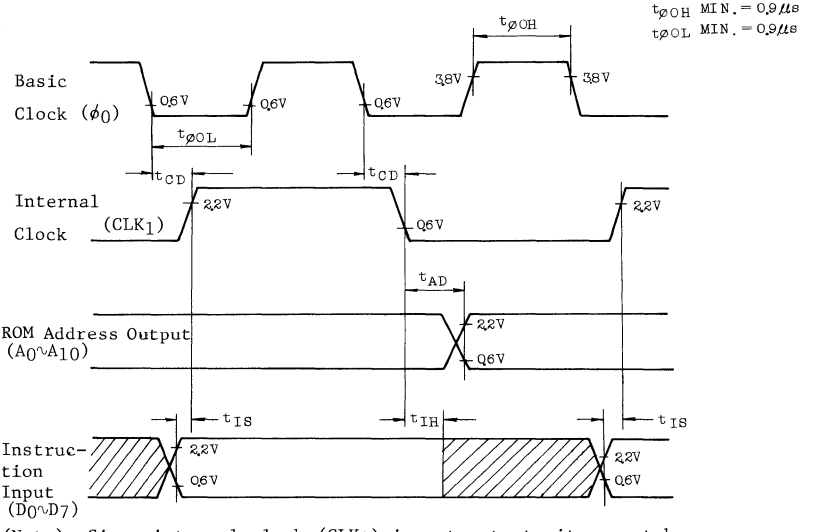
Symbol	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
$t_{\phi 0}$	Clock Cycle Time	-	2	-	5	μs
t_S	Input Setup Time	-	0.9	-	-	μs
t_H	Input Hold Time	-	0.9	-	-	μs
t_D	Output Delay Time	C_L=50PF R(Pull UP) =50kΩ,1TTL	-	-	1.8	μs
t_{INT}	$\overline{INT}$ Low Level Width	-	4	-	-	Cycle
t_{RST}	$\overline{RST}$ Low Level Width	-	4	-	-	Cycle
t_{CD}	Clock Output Delay Time	C_L = 50PF, 1TTL	-	-	0.4	μs
t_{AD}	Address Output Delay Time	C_L = 50PF, 1TTL	-	-	0.95	μs
t_{IS}	Instruction Input Setup Time	-	0.4	-	-	μs
t_{IH}	Instruction Input Hold Time	-	0	-	-	μs

TIMING CHART

(1)



(2)



(Note) Since internal clock (CLK_1) is not output, it cannot be seen from the outside.

EXTERNAL SHAPE OF PACKAGE