TOSHIBA MOS TYPE DIGITAL INTEGRATED CIRCUIT

TMP4700C

SILICON MONOLITHIC

N-CHANNEL SILICON GATE DEPRESSION LOAD

PRELIMINARY

NMOS 4-BIT SINGLE CHIP MICROCOMPUTER (TLCS-47N) TMP4700C

GENERAL DESCRIPTION

The TLCS-47 is the high speed and high performance, 4-bit single chip microcomputer series designed for general purpose use.

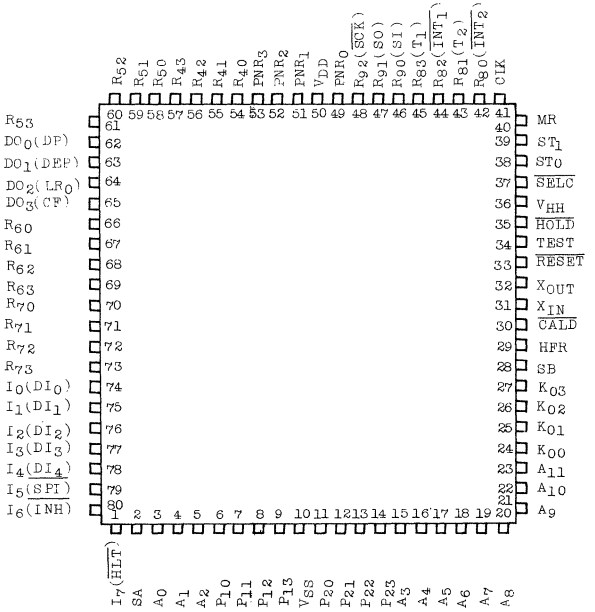
The TLCS-47 has variously powerful functions in order to meet with the advanced and complicated applications, which will be made in near future. In addition, software compatible NMOS family (TLCS-47N) and CMOS family (TLCS-47C) are also provided.

The TMP4700C is the system development evaluator chip used for developmental and operational check of the TLCS-47 application systems (programs).

Although the TLCS-47N and the TLCS-47C have different electric characteristics and some functions, the individual configuration of a functionally equivalent system is possible by using the TMP4700C.

Furhter, when the TMP4700C is used, the evaluation boards equivalent to respective versions of the TLCS-47 should be used.

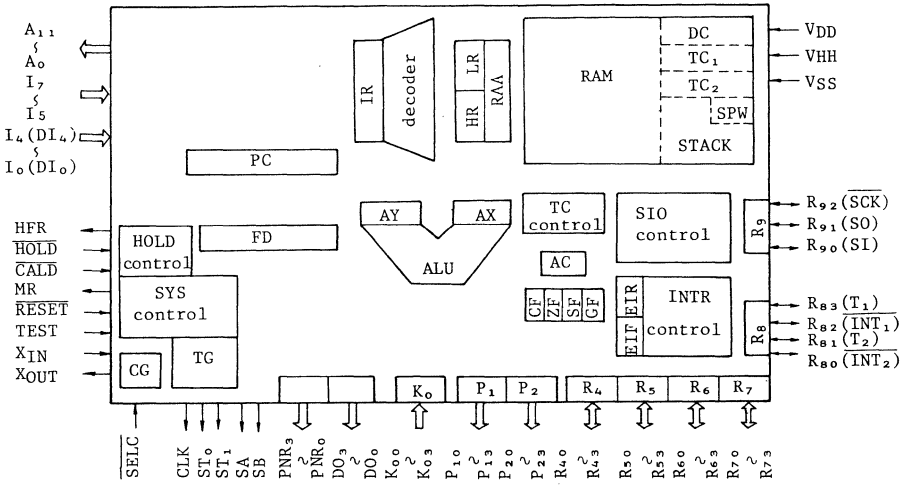
PIN CONNECTIONS (Top View)



PIN NAMES AND PIN DESCRIPTIONS

Pin Names	No.of Pins	I/O	Functions
$K_{03} \sim K_{00}$	4	Input	Input port
$P_{13} \sim P_{10}$	4	Output	Output port (corresponding to PLA)
$P_{23} \sim P_{20}$	4	Output	" (")
$R_{43} \sim R_{40}$	4	I/O	I/O port
$R_{53} \sim R_{50}$	4	I/O	"
$R_{63} \sim R_{60}$	4	I/O	"
$R_{73} \sim R_{70}$	4	I/O	"
R_{83} (T_1)	1	I/O	I/O port or timer/counter input
R_{82} ($\overline{INT_1}$)	1	I/O	" or interrupt input
R_{81} (T_2)	1	I/O	" or timer/counter input
R_{80} ($\overline{INT_2}$)	1	I/O	" or interrupt input
R_{92} ($\overline{SCK}$)	1	I/O	I/O port or shift clock for serial port
R_{91} (SO)	1	I/O	" or serial output
R_{90} (SI)	1	I/O	" or serial input
$A_{11} \sim A_0$	12	Output	Program memory address
I_7 ($\overline{HLT}$)	1	Input	Program data input (Holt request signal input)
I_6 ($\overline{INH}$)	1	Input	" (Inhibit control signal input)
I_5 ($\overline{SPI}$)	1	Input	" (Port control signal input)
$I_4(DI_4) \sim I_0(DI_0)$	5	Input	" (Data input)
DO_3 (CF)	1	Output	Data Output (Carry flag monitor)
DO_2 (LR_0)	1	Output	" (L register monitor)
DO_1 (DEP)	1	Output	" (Port control signal output)
DO_0 (DP)	1	Output	" (")
$PNR_3 \sim PNR_0$	4	Output	Port address output
CLK	1	Output	Strobe signal
ST_0, ST_1	2	Output	State signal
SA, SB	2	Output	Status signal
MR	1	Output	Master reset signal output
HFR	1	Output	Hold monitor output
$\overline{CALD}$	1	Input	Data fetch cycle request signal input
$\overline{SELC}$	1	Input	Clock select input
$\overline{HOLD}$	1	Input	Hold signal input
XIN, XOUT	2	Input, Output	Resonator connection terminal
$\overline{RESET}$	1	Input	Initialize signal input
TEST	1	Input	(Low level is input.)
V_{DD}	1	Power supply	+5V
V_{HH}	1	Power supply	+5V (Memory power supply)
V_{SS}	1	Power supply	0V

BLOCK DIAGRAM



BLOCK NAMES AND DESCRIPTIONS

Block Names	Functions
PC	Program counter (12 bits)
IR, decoder	Instruction register, Decoder
HR, LR	H register (page assignment of RAM), L register (address assignment in RAM page), (each 4-bit register)
RAA	RAM address buffer register (8 bits)
RAM	Deta memory
STACK	Save area of program counter and flags (RAM area)
SPW	Stack pointer word (RAM area)
DC	Data counter (12 bits, RAM area)
AX, AY	Temporary register of ALU input
ALU	Arithmetic and logic unit
AC	Accumulator
FLAG(CF,ZF,SF,GF)	Flags
K, P, R	Ports
INTR control	Interrupt control (EIF: Enable interrupt master F/F, EIR: Enable interrupt register)
FD	Frequency divider (4-stage prescaler + 18 stages)
TC_1, TC_2	12-bit timer/counter 2-channels (RAM area)
TC control	Timer/counter control
SIO control	Serial port control
HOLD control	Control of hold function
SYS control	Generation of various internal control signals
CG, TG,	Clock generator, timing generator

FUNCTIONAL DESCRIPTION

The TMP4700C is the system development evaluator chip for the TLCS-47. When a program memory (equivalent to TMM2732D, TMM323D-1) is externally mounted, it is possible to configurate a system equivalent to the TMP4740P or the TMP4720P (the input/output circuit format, however, must be equivalent to ($\overline{\text{IOCODE}}$ AA) and in the case of ($\overline{\text{IOCODE}}$ AE) and ($\overline{\text{IOCODE}}$ AF), externally mounted resistors are required).

In the case of other input/output circuit formats of the TMP4740P and TMP4720P, or in the case of other NMOS family or CMOS family, it is also possible to configurate an equivalent system by adding an external circuit using an evaluator chip dedicated terminal. Therefore, in application systems of these models, the evaluation boards equivalent to respective versions shall be used.

Further, when the TMP4700C is used, the technical descriptions for respective versions and the instruction manuals for equivalent evaluation boards, debugging tools and the like shall also be read.

The operation of the TMP4700C is described in the following on the basis of the terminal functions.

1. TLCS-47N standard chip equivalent terminals

   The terminals shown in Fig. 1.1 have the functions and characteristics equivalent to the input/output circuit format ($\overline{\text{IOCODE}}$ AA) of the standard chips (TMP4740P, TMP4720P) of the TLCS-47N. Therefore, in this case it is possible to configurate an equivalent system by externally mounting a program memory.

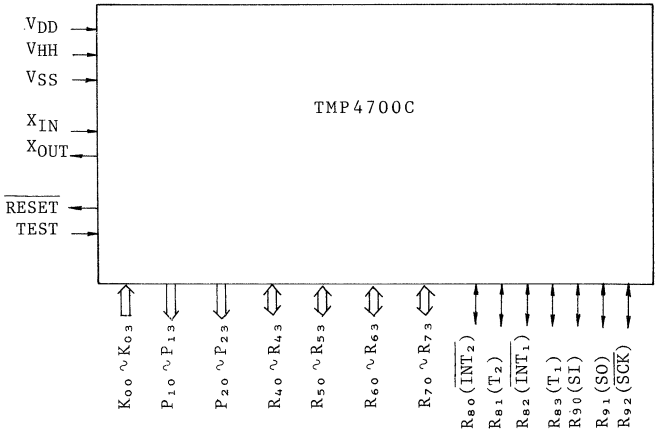
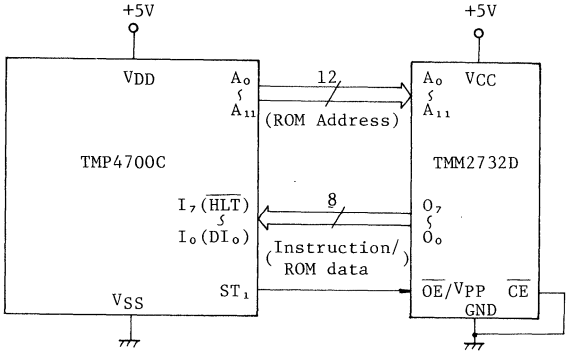


Fig.1.1 TLCS-47N Standard Chip ($\overline{\text{IOCODEAA}}$) Equivalent Terminals

2. Connection of Program Memory

As an externally mounted program memory, a programable ROM equivalent to the TMM2732D (4K x 8 bits) or TMM323D-1 (2K x 8 bits) is used.

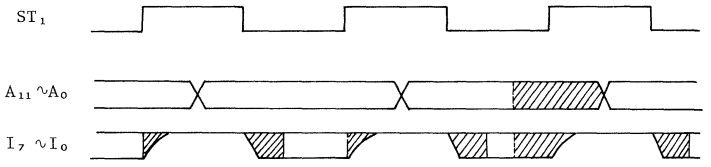
The connecting method of a program memory and the timing chart are shown in Fig. 2.1.
Further, A_{11} and I_7 ($\overline{\text{HLT}}$) terminals in the diagram are MSB, respectively.



Note 1. When the TMM323D-1 is used, the TMP4700C output terminal A_{11} should be opened.

Note 2. The instruction/ROM data input terminal has a built-in pull-up resistors.

(a) Connection of Program Memory



(b) Program Memory Access Timing Chart

Fig. 2.1 Connection of Program Memory

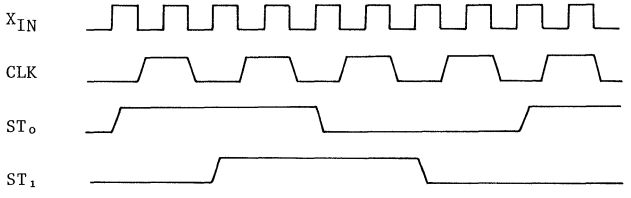
3. Control Terminals for External Circuits

(1) Timing signals (CLK, ST_0, ST_1, $\overline{SELC}$)

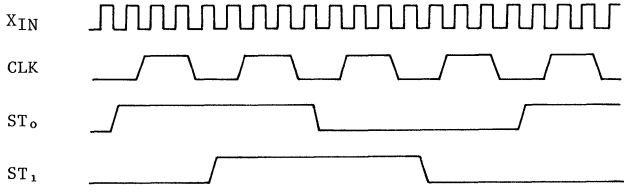
In order for the timing control of the external circuits, 3 types of signals are transmitted from the timing generator of the TMP4700C.

The TMP4700C is capable of supporting either system of the TLCS-47N and the TLCS-47C. For selecting these systems, the $\overline{SELC}$ signal input is used.

The timing chart of these signals is shown in Fig. 3.1. Further, the $\overline{SELC}$ terminal has a built-in pull-up resistor.



(a) TLCS-47N Support ($\overline{SELC}$ = 1)



Note: These are somewhat different from the operating timings of CMOS family.

(b) TLCS-47C Support ($\overline{SELC}$ = 0)

Fig. 3.1 Clock Timing Chart

(2) System control signal inputs

I_7 ($\overline{HLT}$)

$\overline{HLT}$ signal is the halt request signal input to the TMP4700C at time of the system debugging. $\overline{HLT}$ signal input is multiplexed with data input from the external ROM and a signal is input when ST_1 signal is at high level.

When a low level signal is input into $\overline{HLT}$ signal input and accepted, the TMP4700C starts the halt operation. At this time, CPU executes no operation cycle, but as long as HLT request is being accepted, it stops the divider to operate (therefore, the counting for the timer interruption of divider, the internal clock to the timer/counter and the internal shift clock for serial transfer are also stopped, accordingly), and furthermore, it inhibits the timer/counter operation and acceptance of interrupt requests.
However, a request for LCD data fetch cycle, which is used on LCD driver built-in version is accepted (one instruction cycle).
Further, the interrupt latch and the count latch for the timer/counter are set/reset independently of HLT operation and subsequent INH operations.

Further, I_7 ($\overline{HLT}$) terminal has a built-in pull-up resistor.

I_6 ($\overline{INH}$)

$\overline{INH}$ signal is the control signal input for temporarily inhibiting the divider operation, timer/counter operation and interrupt request acceptance at time of the system debugging. $\overline{INH}$ signal input is multiplexed with data input from the external ROM and a signal is input when ST_1 is at high level.

As long as a low level signal is input into $\overline{INH}$ input and is being accepted, the TMP4700C stops the divider to operate and inhibits the timer/counter operation and acceptance of interrupt requests. However, a request for LCD data fetch cycle, which is used on LCD driver built-in version is accepted (one instruction cycle).

Since this INH operation can be controlled independently of HLT operation, it can be used in normal system program operation. Furthermore, it also can be used for controlling the internal monitor at time of the system debugging.

Further, I_6 ($\overline{INH}$) terminal has a built-in pull-up resistor.

$\overline{HOLD}$

This input is equivalent to the $\overline{HOLD}$ terminal provided in the TLCS-47C.

As the system operation for the hold function, operation of this input is similar to that of each version of the TLCS-47C for $\overline{HOLD}$ terminal input except the followings:

(a) The oscillator is not stopped (normal oscillation is continued).

(b) Supply current don't decrease from the value of the TMP4700C operating current.

Further, this $\overline{HOLD}$ terminal has a built-in pull-up resistor.

$\overline{CALD}$

This is a request signal input for the data fetch cycle, which is used on LCD driver built-in version.

When a low level signal is input into the $\overline{CALD}$ input and accepted, the TMP4700C executes the LCD data fetch cycle (one instruction cycle).

Further, this $\overline{CALD}$ terminal has a built-in pull-up resistor.

(3) System control signal outputs

SA, SB

SA and SB signal outputs are signals for monitoring the internal operation of the TMP4700C (See Table 3.1). These signals are switched for every instruction cycle.

SA	SB	
0	0	Executes the first cycle of an instruction
0	1	Executes the LCD data fetch cycle by a CALD request
1	0	Executes the halt operation by a HLT request
1	1	Executes other operations

Table 3.1 SA, SB Signal Outputs

MR

This is a response signal to $\overline{\text{RESET}}$ signal input, and is the system reset signal.

HFR

This signal is a monitor signal relative to the hold operation and is also used for an external circuit control.

(4) Port control

In order to support the versions of TLCS-47 series commonly, the TMP4700C is able to input data from an external circuit or to output data to a register created in an external circuit.

(a) Control signals

$PNR_3 \sim PNR_0$

4 bit outputs indicating port addresses.

DO_0 (DP), DO_1 (DEP)

These signals (DP, DEP) control the port write/read by the external circuits. They are multiplexed with data output (DO) and are transmitted when ST_1 signal is at high level.

I_5 ($\overline{SPI}$)

$\overline{SPI}$ signal controls the port read by the external circuits. This signal is multiplexed with data input from an external ROM and is input when ST_1 signal is at high level.

(b) Data inputs

I_4 (DI_4) ∿ I_0 (DI_0)

These (DI_4 ∿ DI_0) are the data input terminals at time of the read operation from the external circuits. They are multiplexed with data inputs from the external ROM and are input when ST_1 signal is at high level.

(c) Data outputs

DO_3 (CF), DO_2 (LR_0), DO_1 (DEP), DO_0 (DP)

These (DO_3 ∿ DO_0) are the data output terminals at time of the write operation to the external circuits. These outputs are multiplexed with other outputs and are transmitted out when ST_1 signal is at low level.

Note: The port output timing on each versions of the TLCS-47 series and that on the TMP4700C external circuit somewhat differ each other.

DO_3 (CF)

Contents of the carry flag are transmitted. This CF output is multiplexed with the data output (DO) and is sent out when ST_1 signal is at high level.

DO_2 (LR_0)

Contents of LSB of L register is transmitted. This LR_0 output is multiplexed with the data output (DO) and is sent out when ST_1 signal is at high level.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING (V_{SS} = 0V)

SYMBOL	ITEM	RATING	UNIT
V_{DD} / V_{HH}	Supply Voltage	-0.5 ∿ 7	V
V_{IN}	Input Voltage	-0.5 ∿ 7	V
V_{OUT1}	Output Voltage (Except Open Drain Port)	-0.5 ∿ 7	V
V_{OUT2}	Output Voltage (Open Drain Port)	-0.5 ∿ 10	
I_{OUT}	Output Current (P_1, P_2)	30	mA
P_D	Power Dissipation (Topr = 70°C)	1	W
Tsol	Soldering Temperature · Time	260(10sec.)	°C
Tstg	Storage Temperature	-55 ∿ 125	
Topr	Operating Temperature	-30 ∿ 70	

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

SYMBOL	ITEM	CONDITION	MIN.	MAX.	UNIT
Topr	Operating Temperature		-30	70	°C
V_{DD} / V_{HH}	Supply Voltage		4.5	5.5	V
V_{HH1}	Supply Voltage (Memory Stand-by)		3.5	5.5	
V_{IH1}	High Level Input Voltage (Note 1)		2.2	VDD	V
V_{IH2}	High Level Input Voltage (Note 2)		3	VDD	
V_{IL1}	Low Level Input Voltage (Except K_0)		0	0.8	
V_{IL2}	Low Level Input Voltage (K_0)		0	1.2	
f_C	Clock Frequency		0.4	4.2	MHz
t_{WCH}	High Level Clock Pulse Width (Note 3)	VIN = VIH	80	-	nS
t_{WCL}	Low Level Clock Pulse Width (Note 3)	VIN = VIL	80	-	

(Note 1) Application terminals: R_4 ∿ R_7, $I_7(\overline{HLT})$ ∿ $I_0(DI_0)$

(Note 2) Application terminals: Inputs other than application termianl (Note 1)

(Note 3) For external clock operation

D.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = V_{HH} = 5V±10%, Topr = −30 ∿ 70°C)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. (*)	MAX.	UNIT
V_{HS}	Hysteresis Voltage (Schmitt Circuit Input)		−	0.5	−	V
I_{IN1}	Input Current (K_0, $\overline{RESET}$, TEST)	V_{DD}=V_{HH}=5.5V, V_{IN}=5.5V	−	−	20	μA
I_{IN2}	Input Current (R Port)	V_{DD}=5.5V, V_{IN}=5.5V	−	−	20	
I_{IL}	Current (**)	V_{DD}=5.5V, V_{IN}=0.4V	−	−	−2	mA
I_{LO}	Output Leakage Current (P, R Port)	V_{DD}=5.5V, V_{OUT}=5.5V	−	−	20	μA
V_{OH}	High Level Output Voltage (***)	V_{DD}=4.5V, I_{OH}=−400μA	2.4	−	−	V
V_{OL}	Low Level Output Voltage (Except $\overline{XOUT}$)	V_{DD}=4.5V, I_{OL}=1.6mA	−	−	0.4	
I_{OL}	Low Level Output Current (P_1, P_2)	V_{DD}=5V, VOL=1V	−	20	−	mA
I_{DD}+I_{HH}	Supply Current	V_{DD}=V_{HH}=5.5V	−	70	150	mA
I_{HH1}	Supply Current (Memory stand-by)	V_{DD}=V_{SS}, V_{HH}=3.5V	−	5	10	

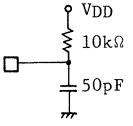
(*) TYP. values are at Topr=25°C, V_{DD}=V_{HH}=5V.
(**) Application terminals: $\overline{HOLD}$, $\overline{CALD}$, $\overline{SELC}$, I_7($\overline{HLT}$) ∿ I_0(DI_0).
(***) Application terminals: Control output terminal specific to evaluation.

A.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = V_{HH} = 5V±10%, Topr = −30 ∿ 70°C)

(1)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	Unit
tcy	Instruction Cycle Time		1.9	−	40	μS
t_{SDH}	Shift Data Holding Time	(Note 1)	0.5tcy − 300	−	−	nS

(Note 1) $\overline{SCK}$, SO Terminal External Circuit

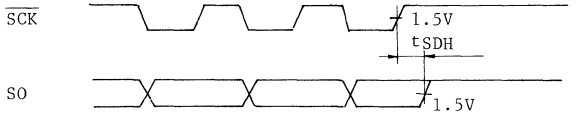


(2)

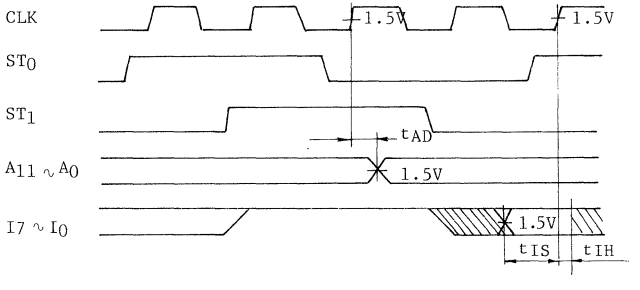
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
tAD	Address Delay Time	C_L = 100pF	−	−	270	nS
tIS	Data Set-up Time	"	150	−	−	
tIH	Data Hold Time	"	50	−	−	

A.C. Timing Chart

(1) Serial Port (Completion of transmission)

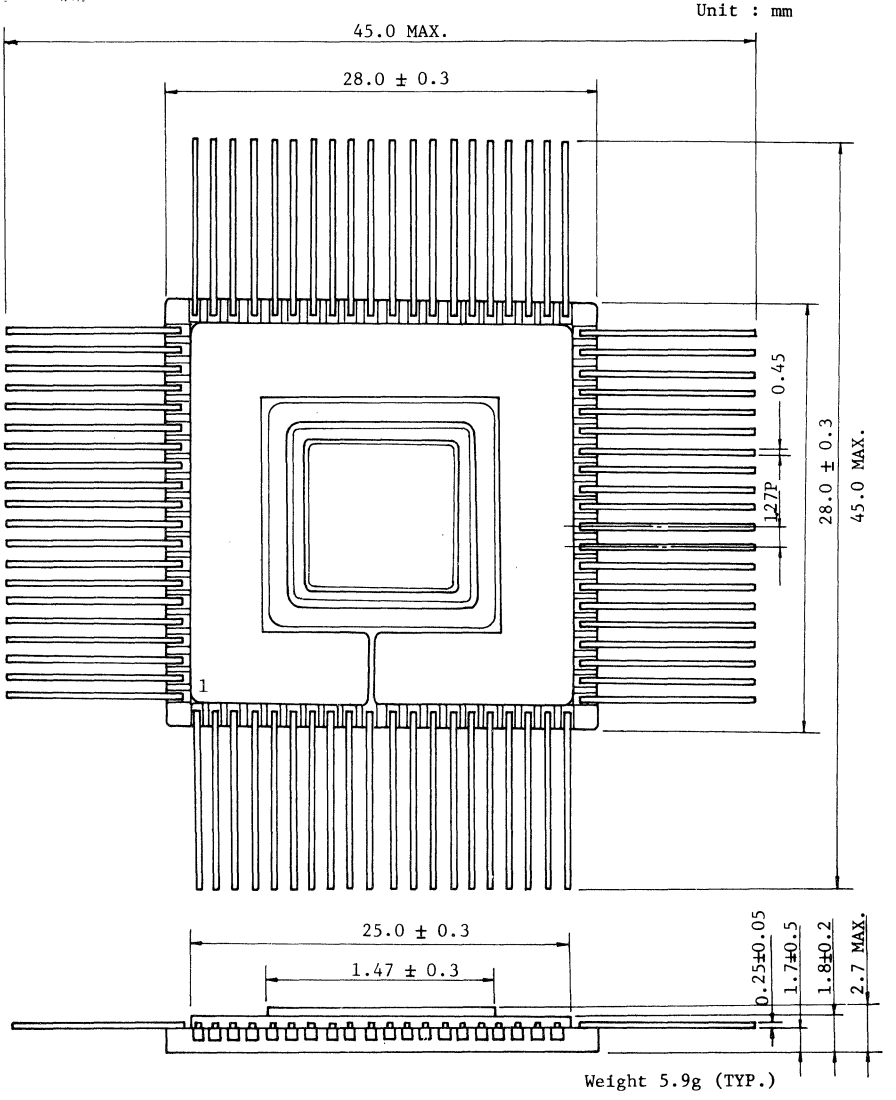


(2)



EXTERNAL DIMENSIONS

Unit : mm



Weight 5.9g (TYP.)