TOSHIBA MOS TYPE DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TMP4799C

SILICON MONOLITHIC

N-CHANNEL SILICON GATE DEPRESSION LOAD

# NMOS 4-BIT SINGLE CHIP MICROCOMPUTER (TLCS-47N) TMP4799C

## GENERAL DESCRIPTION

The TLCS-47 is the high speed and high performance, 4-bit single chip microcomputer series designed for the general purpose use.

The TLCS-47 has veriously powerful functions in order to meet with the advanced and complicated applications, which will be made in near future. In addition, software compatible NMOS family (TLCS-47N) and CMOS family (TLCS-47C) are also provided.

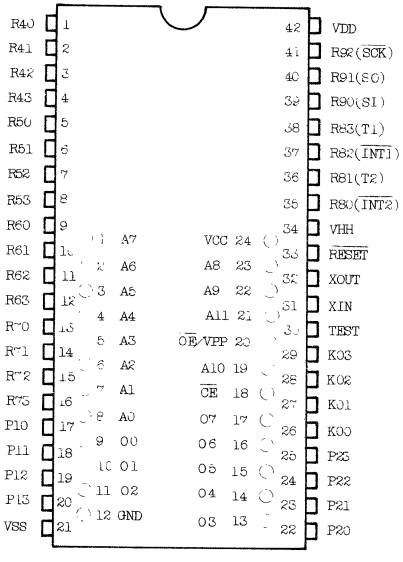
TMP4799C is the system development evaluator chip, which is equipped with a 24-pin socket which may directly mount the general purpose 32K EPROM (TMM2732D) on the top of the package. Therefore, when the program written in the 32K EPROM is mounted on the package, TMP4799C becomes pin compatible with TMP4740P, TMP4720P and can be used for developmental and operational check of the TLCS-47N application systems and programs. The former operates the same as the latter.

TMP4799C can be used within the range of a microcomputer for the TLCS-47N system as well as for mounting an equipment made on an experimental basis.

## FEATURES

- General purpose 32K EPROM TMM2732D (equivalent to INTEL 2732) can be used.
- Compatible with TLCS-47N single chip microcomputer family TMP4740P/TMP4720P in pin.
- Compatible with TLCS-47 series in software.
- ROM 4,096 × 8 BIT (external), RAM 256 × 4 BIT (internal)

## PIN CONNECTIONS (Top View)



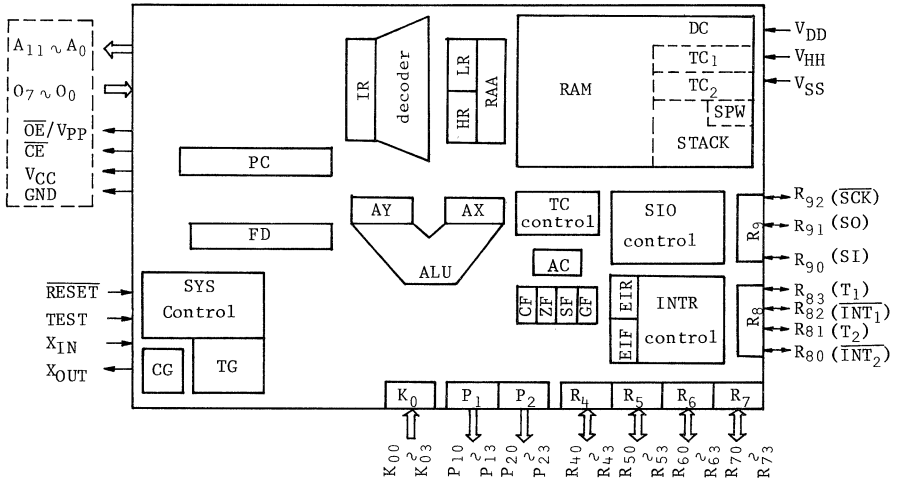

(NOTE) Mark : Socket for TMM2732D

PIN NAMES AND PIN DESCRIPTIONS

| Pin Names | No. of pins | Input/ Output | Functions | |
|---|---|---|---|---|
| $K_{03} \sim K_{00}$ | 4 | Input | Input port | |
| $P_{13} \sim P_{10}$ | 4 | Output | Output port (corresponding to PLA) | |
| $P_{23} \sim P_{20}$ | 4 | Output | " ( " ) | |
| $R_{43} \sim R_{40}$ | 4 | I/O | I/O port | |
| $R_{53} \sim R_{50}$ | 4 | I/O | " | |
| $R_{63} \sim R_{60}$ | 4 | I/O | " | |
| $R_{73} \sim R_{70}$ | 4 | I/O | " | |
| $R_{83}$ ($T_1$) | 1 | I/O | I/O port or timer/counter input | |
| $R_{82}$ ($\overline{INT_1}$) | 1 | I/O | " or interrupt input | |
| $R_{81}$ ($T_2$) | 1 | I/O | " or timer/counter input | |
| $R_{80}$ ($\overline{INT_2}$) | 1 | I/O | " or interrupt input | |
| $R_{92}$ ($\overline{SCK}$) | 1 | I/O | I/O port or shift clock for serial port | |
| $R_{91}$ (SO) | 1 | I/O | " or serial output | |
| $R_{90}$ (SI) | 1 | I/O | " or serial input | |
| $X_{IN}$, $X_{OUT}$ | 2 | Input, Output | Resonator connection terminals | |
| $\overline{RESET}$ | 1 | Input | Initialize signal input | |
| TEST | 1 | Input | (Low level is input.) | |
| $V_{DD}$ | 1 | Power supply | +5V | |
| $V_{HH}$ | 1 | Power supply | +5V (Memory power supply) | |
| $V_{SS}$ | 1 | Power supply | 0V | |
| $A_{11} \sim A_0$ | 12 | Output | Program memory address | Socket for TMM2732D |
| $O_7 \sim O_0$ | 8 | Input | Program data input | |
| $\overline{OE}/V_{PP}$ | 1 | Output | Output buffer control | |
| $\overline{CE}$ | 1 | Output | Chip Enable (connected with $V_{SS}$) | |
| $V_{CC}$ | 1 | Power supply | +5V (connected with $V_{DD}$) | |
| GND | 1 | Power supply | 0V (connected with $V_{SS}$) | |

Note : $\overline{RESET}$ terminal has no built-in pull-up resistor as well as TEST terminal has no built-in pull-down resistor.

## BLOCK DIAGRAM




## BLOCK NAMES AND DESCRIPTIONS

| Block Names | Functions |
|---|---|
| PC | Program counter (12 bits) |
| IR, decoder | Instruction register, Decoder |
| HR, LR | H register (page assignment of RAM), L register (address assignment in RAM page), (each 4-bit register) |
| RAA | RAM address buffer register (8 bits) |
| RAM | Deta memory |
| STACK | Save area of program counter and flags (RAM area) |
| SPW | Stack pointer word (RAM area) |
| DC | Data counter (12 bits, RAM area) |
| AX, AY | Temporary register of ALU input |
| ALU | Arithmetic and logic unit |
| AC | Accumulator |
| FLAG(CF,ZF,SF,GF) | Flags |
| K, P, R | Ports |
| INTR control | Interrupt control (EIF: Enable interrupt master F/F, EIR: Enable interrupt register) |
| FD | Frequency divider (4-stage prescaler + 18 stages) |
| $TC_1$, $TC_2$ | 12-bit timer/counter 2-channels (RAM area) |
| TC control | Timer/counter control |
| SIO control | Serial port control |
| SYS control | Generation of various internal control signals |
| CG, TG | Clock generator, timing generator |

## FUNCTIONAL DESCRIPTION

TMP4799C is the system development evaluator chip for the TLCS-47N. When the 32K EPROM (TMM2732D) in which the program is written is mounted on the package, it is possible to configurate a system equivalent to TMP4740P or TMP4720P.

The precautions for using TMP4799C are described.

1. Program Memory (ROM) and ROM address

The precautions for using TMP4799C as an evaluator chip for TMP4720P are described.

TMP4720P contains a program memory with 2,048 × 8-bit (addresses 000 - 7FF) capacity. In case of TMP4720P, the PLA data conversion table must be located in addresses 7E0 - 7FF, because the MSB in the program counter is not decoded and there is no physical ROM in addresses 800 - FFF.

When TMP4799C is used with 32K EPROM, the program counter with 12-bit length is decoded and there is a program memory with 4,096 × 8-bit (addresses 000 - FFF) capacity. In case of TMP4799C, the PLA data conversion table is, therefore, located in addresses FE0 - FFF.

No precaution is required, when TMP4799C is used as an evaluator chip for TMP4740P. It is because the former has the same address space as the latter.

Fig. 1.1 shows the ROM address space of TMP4740P, TMP4720P and TMP4799C.

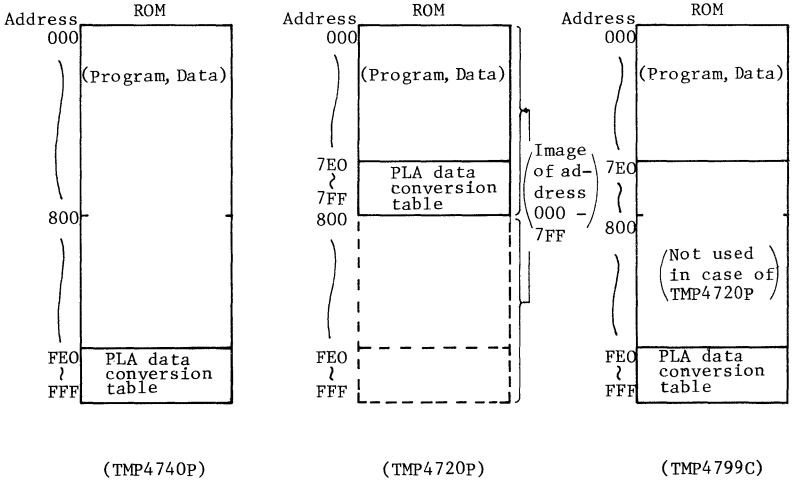



Fig. 1.1 ROM Capacity and Address

2. Data Memory (RAM) and RAM address

The precautions for using TMP4799C as an evaluator chip for TMP4720P are described.

Data memory contained in TMP4720P has a 128 × 4-bit (addresses 00 - 7F) capacity, and the specific RAM address, which is used for the stack area, the data counter, etc., is located in addresses 40 - 7F. It is because the MSB of RAM address buffer register is not decoded and there is no physical RAM in addresses 80 - FF in TMP4720P.

In case of TMP4799C, the RAM address buffer register with 8-bit length is decoded and there is data memory with 256 × 4-bit (addresses 00 - FF) capacity. Then the specific RAM address area is located in addresses C0 - FF in TMP4799C, while it located in addresses 40 - 7F in TMP4720P. Further, it is necessary to pay attention to the addresses of the data memory in case of accessing the data in the specific RAM address area.

Fig. 2.1 shows the RAM address space of TMP4740P, TMP4720P and TMP4799C.

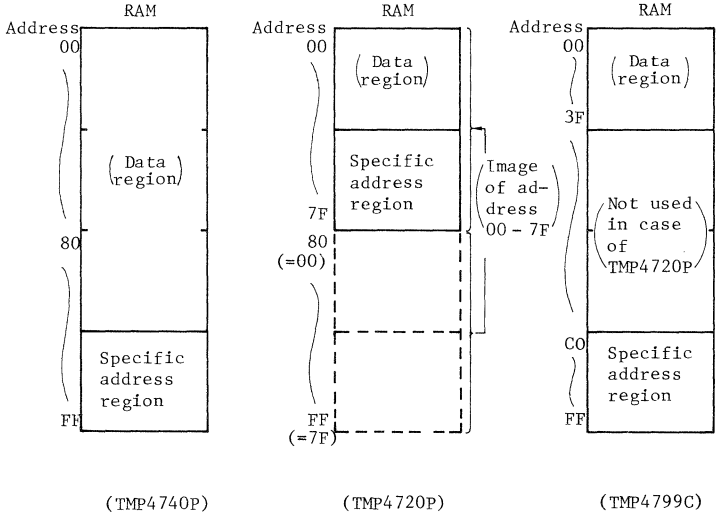
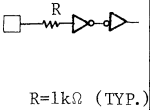
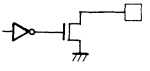
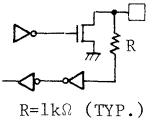
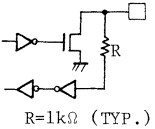
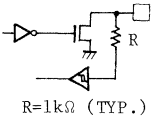



Fig. 2.1 RAM Capacity and Address

3. Input/Output circuit format

Fig. 3.1 shows the input/output circuit format of TMP4799C which is equivalent to "IOCODE AA" of TMP4740P and TMP4720P.

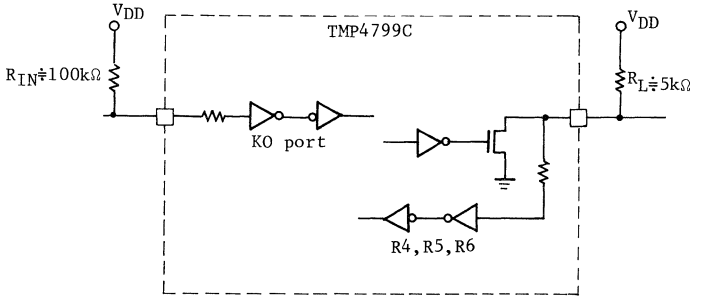
| port / Circuit | Input ($K_0$) | Output ($P_1$,$P_2$) | I/O ($R_4$,$R_5$,$R_6$) | I/O ($R_7$) | I/O ($R_8$,$R_9$) |
|---|---|---|---|---|---|
| I/O equivalent Circuit |   R=1kΩ (TYP.) |  |   R=1kΩ (TYP.) |   R=1kΩ (TYP.) |   R=1kΩ (TYP.) |
| Remark | ∘ High threshold input.<br>∘ No resistor is contained. | ∘ Sink open-drain output.<br>∘ High output current.<br>∘ Output latch is initialized to the high level. | ∘ Sink open-drain output.<br>∘ Output latch is initialized to the high level. | ∘ Sink open-drain output.<br>∘ Output latch is initialized to the high level. | ∘ Schmitt circuit input.<br>∘ Sink open-drain output.<br>∘ Output latch is initialized to the high level. |

Note : TMP4799C does not contain the pull-up resister with $\overline{\text{RESET}}$ pin and does not contain the pull-down resister with TEST pin. It is necessary to provide $\overline{\text{RESET}}$ pin with the pull-up resister (≈ 200kΩ TYP.) and to provide TEST pin with the pull-down resister (≈ 70kΩ TYP.), respectively.

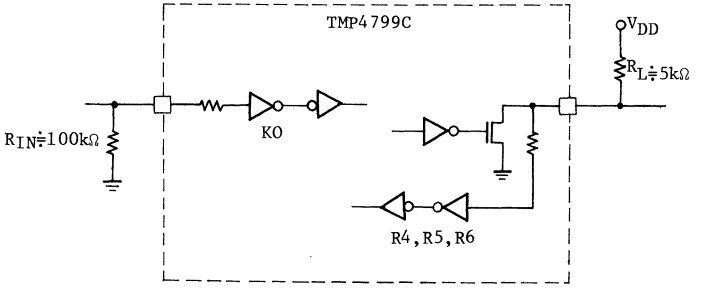
Fig. 3.1 Input/Output circuit format of TMP4799C

TMP4799C cannot be used as an evaluator chip for TMP4740P or TMP4720P which employs "IOCODE AH" or "IOCODE AI", because the output latches of R4, R5, R6 are initialized to the high level in the former and to the low level in the latter.

It is necessary to provide the pull-up or pull-down resisters with KO port and to provide the pull-up resisters with R4, R5, R6 ports when TMP4799C is used as an evaluator chip for TMP4740P or TMP4720P which employs "IOCODE AE" or "IOCODE AF", respectively. Fig. 3.2 shows the examples of the external circuitries.




(1) The external circuitry for TMP4799C
(equivalent to "IOCODE AE")




(2) The external circuitry for TMP4799C
(equivalent to "IOCODE AF")

Fig. 3.2 Example of external circuitry for TMP4799C

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS ($V_{SS}$=0V)

| SYMBOL | ITEM | RATING | UNITS |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | -0.5 ∿ 7 | V |
| $V_{HH}$ | | | |
| $V_{IN}$ | Input Voltage | -0.5 ∿ 7 | V |
| $V_{OUT1}$ | Output Voltage(Except Open Drain Port) | -0.5 ∿ 7 | V |
| $V_{OUT2}$ | Output Voltage (Open Drain Port) | -0.5 ∿ 10 | |
| $I_{OUT}$ | Output Current ($P_1$, $P_2$) | 30 | mA |
| $P_D$ | Power Dissipation ($T_{opr}$=70°C) | 1 | W |
| $T_{sol}$ | Soldering Temperature • Time | 260 (10 sec) | °C |
| $T_{stg}$ | Storage Temperature | -55 ∿ 125 | |
| $T_{opr}$ | Operating Temperature | -30 ∿ 70 | |

### RECOMMENDED OPERATING CONDITIONS ($V_{SS}$=0V)

| SYMBOL | ITEM | CONDITION | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|
| $T_{opr}$ | Operating Temperature | | -30 | 70 | °C |
| $V_{DD}$ | Supply Voltage | | 4.5 | 5.5 | V |
| $V_{HH}$ | | | | | |
| $V_{HH1}$ | Supply Voltage (Memory Stand-by) | | 3.5 | 5.5 | |
| $V_{IH1}$ | High Level Input Voltage ($R_4$ ∿ $R_7$) | | 2.2 | $V_{DD}$ | V |
| $V_{IH2}$ | High Level Input Voltage (Except $R_4$ ∿ $R_7$) | | 3 | $V_{DD}$ | |
| $V_{IL1}$ | Low Level Input Voltage (Except $K_0$) | | 0 | 0.8 | |
| $V_{IL2}$ | Low Level Input Voltage ($K_0$) | | 0 | 1.2 | |
| $f_C$ | Clock Frequency | | 0.4 | 4.2 | MHz |
| $t_{WCH}$ | High Level Clock Pulse Width (Note 1) | $V_{IN}$=$V_{IH}$ | 80 | - | nS |
| $t_{WCL}$ | Low Level Clock Pulse Width (Note 1) | $V_{IN}$=$V_{IL}$ | 80 | - | |

(Note 1) For external clock operation.

D.C. CHARACTERISTICS ($V_{SS}$=0V, $V_{DD}=V_{HH}$=5V±10%, $T_{opr}$=-30 ∿ 70°C)

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. (*) | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{HS}$ | Hysteresis Voltage (schmitt Circuit Input) | | - | 0.5 | - | V |
| $I_{IN1}$ | Input Current ($K_0$, $\overline{RESET}$, TEST) | $V_{DD}=V_{HH}$=5.5V, $V_{IN}$=5.5V | - | - | 20 | μA |
| $I_{IN2}$ | Input Current (R Port) | $V_{DD}$=5.5V, $V_{IN}$=5.5V | - | - | 20 | |
| $I_{IL}$ | Current (**) | $V_{DD}$=5.5V, $V_{IN}$=0.4V | - | - | -2 | mA |
| $I_{LO}$ | Output Leakage Current (P, R Port) | $V_{DD}$=5.5V, $V_{OUT}$=5.5V | - | - | 20 | μA |
| $V_{OH}$ | High Level Output Voltage (***) | $V_{DD}$=4.5V, $I_{OH}$=-400μA | 2.4 | - | - | V |
| $V_{OL}$ | Low Level Output Voltage (Except $X_{OUT}$) | $V_{DD}$=4.5V, $I_{OL}$=1.6mA | - | - | 0.4 | |
| $I_{OL}$ | Low Level Output Current ($P_1$, $P_2$) | $V_{DD}$=5V, $V_{OL}$=1V | - | 20 | - | mA |
| $I_{DD}+I_{HH}$ | Supply Current | $V_{DD}=V_{HH}$=5.5V | - | 70 | 150 | mA |
| $I_{HH1}$ | Supply Current (Memory stand-by) | $V_{DD}=V_{SS}$, $V_{HH}$=3.5V | - | 5 | 10 | |

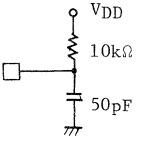
(*) TYP. values are at $T_{opr}$=25°C, $V_{DD}=V_{HH}$=5V.
(**) Application terminals : $O_7$ ∿ $O_0$
(***) Application terminals : $A_{11}$ ∿ $A_0$, $\overline{OE}/V_{PP}$

A.C. CHARACTERISTICS ($V_{SS}$=0V, $V_{DD}=V_{HH}$=5V±10%, $T_{opr}$=-30 ∿ 70°C)

(1)

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $t_{cy}$ | Instruction Cycle Time | | 1.9 | - | 20 | μS |
| $t_{SDH}$ | Shift Data Holding Time | (Note 1) | 0.5tcy-300 | - | - | nS |

(Note 1) $\overline{SCK}$, SO Terminal External Circuit

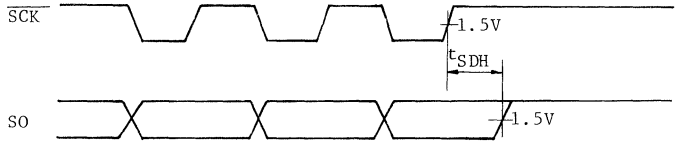



(2)

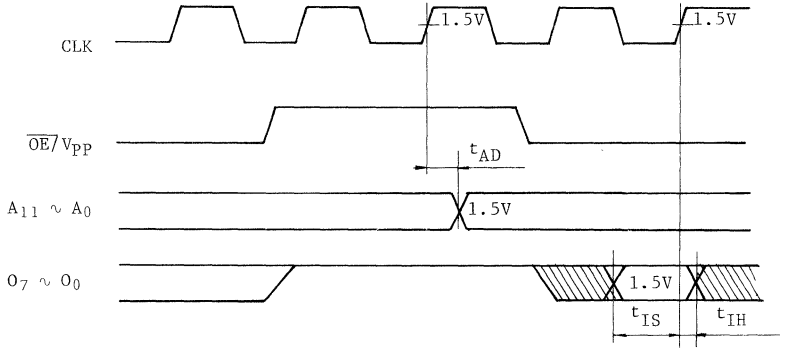
| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $t_{AD}$ | Address Delay Time | $C_L$=100pF | - | - | 270 | nS |
| $t_{IS}$ | Data Set-up Time | " | 150 | - | - | |
| $t_{IH}$ | Data Hold Time | " | 50 | - | - | |

A.C. Timing Chart

(1) Serial Port (Completion of transmission)

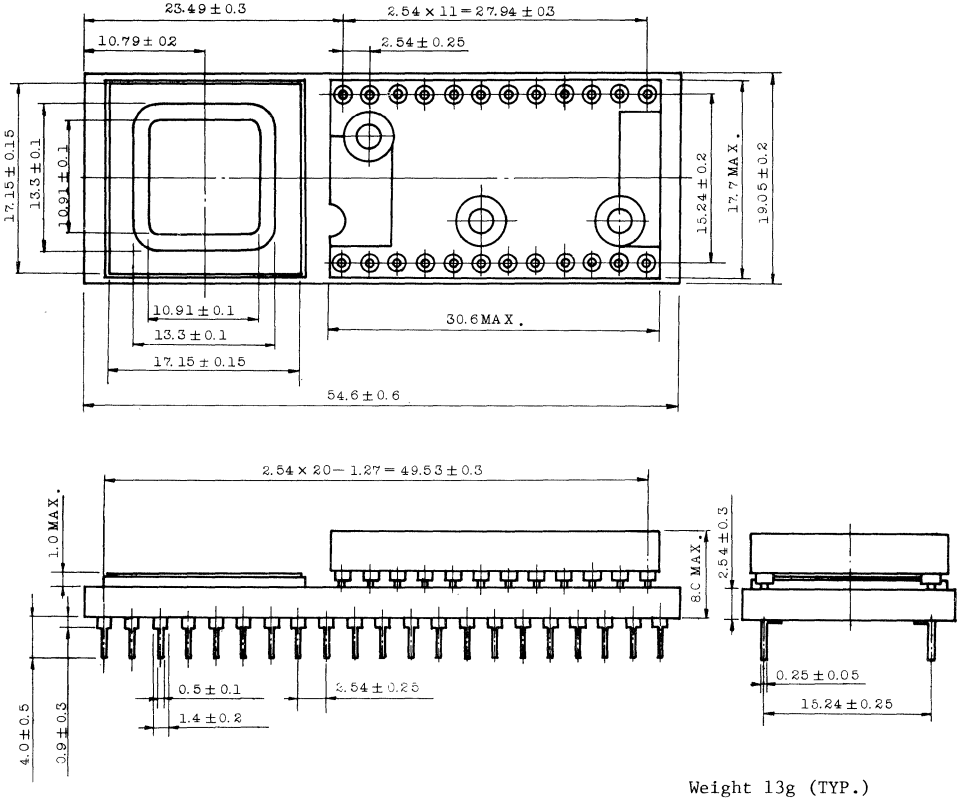



(2)



EXTERNAL DIMENSION VIEW

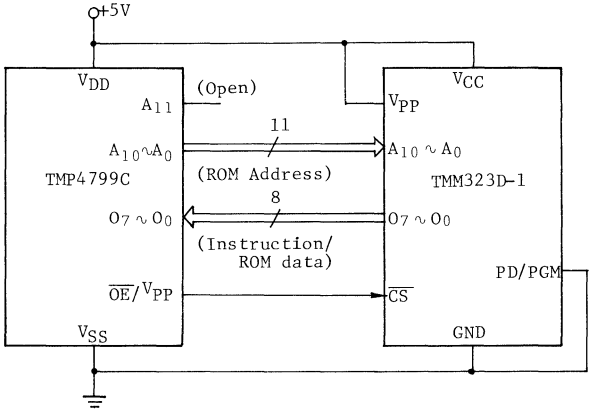
Unit in mm




Weight 13g (TYP.)

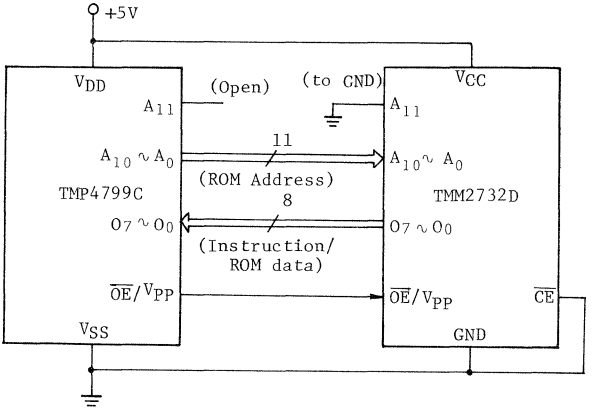
## CONNECTION OF PROGRAM MEMORY

When TMP4799C operates as the evaluator chip for TMP4720P, TMM323D-1 (2,048 × 8 bit) can be used as the program memory. The connecting method of a program memory is shown below.




| Pin Names of TMM323D-1 | Pin Names of TMM2732D | Connection |
|---|---|---|
| PD/PGM | $\overline{CE}$ | No change |
| $\overline{CS}$ | $\overline{OE}/V_{PP}$ | No change |
| $V_{PP}$ | $A_{11}$ | $A_{11}$ is open. $V_{PP}$ is connected to $V_{DD}$. |

TMP4799C used with TMM2732D, in which the program is written in the range of addresses 000 - 7FF, operates the same as TMP4720P when the connecting method shown below is adopted.




$A_{11}$ of TMP4799C is open.

$A_{11}$ of TMM2732D is connected to $V_{SS}$.