CMOS 4-BIT MICROCONTROLLER

TMP47C1238N, TMP47C1638N

The 47C1238/1638 are based on the TLCS-470A series. The 47C1238/1638 have on-screen display circuit (OSD) to display characters and marks which indicate channel or time on TV screen, A/D converter input, D/A converter output such as TV.

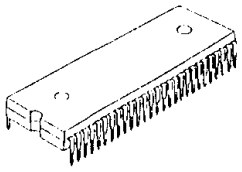
PART No.	ROM	RAM	PACKAGE	PIGGYBACK (adapter socket)
TMP47C1238N	12288 × 8-bit	512 × 4-bit	SDIP54	*TMP47C038E (BM1106)
TMP47C1638N	16384 × 8-bit			

* : Under Development

FEATURES

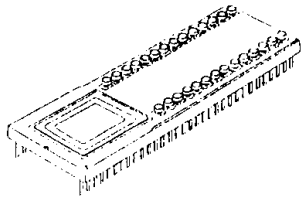
- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.3μs (at 6MHz), 244μs (at 32.8KHz)
- ◆105 basic instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available
- ◆I/O port (41 pins)
  - Input 3 ports 7 pins
  - I/O 7 ports 26 pins
  - Output 2 ports 8 pins
- ◆Two 12-bit Timer/Counters
- ◆Interval Timer
- ◆Watchdog Timer
- ◆Serial Interface with 8-bit buffer
- ◆On-screen display circuit
  - Character patterns : 128 Characters
  - Characters displayed : 20 columns × 4 lines
  - Composition : 14 × 18 dots (80 Characters)
    7 × 9 dots (48 Characters)
  - Size of character : 3 kinds (line by line)
  - Color of character : 7 kinds (character by character)
  - Variable display position : Horizontal / Vertical 128 steps
  - Fringing, Smoothing function
- ◆D/A converter (Pulse width modulation) outputs
  - 14-bit resolution 1 channel
  - 7-bit resolution 9 channels
- ◆4-bit A/D converter input (4 Channels)
- ◆Horizontal synchronous signal is detected by timer/counter
- ◆Pulse output (Clock for PLL IC)
- ◆Remote control signal preprocessing capability
- ◆High current outputs : LED direct drive (typ. 20mA × 8 bits)
- ◆Dual-clock operation
  High-speed/low-power consumption operating mode
- ◆Hold function : Battery/Capacitor back-up
- ◆Real Time Emulator : BM47C1638

SDIP54



TMP47C1238N
TMP47C1638N

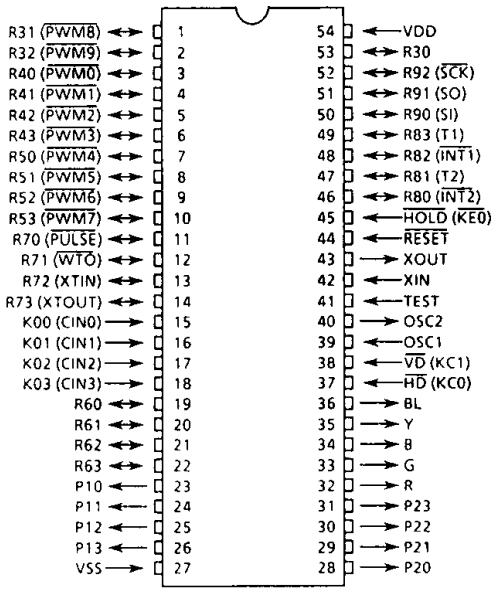
SDIC64



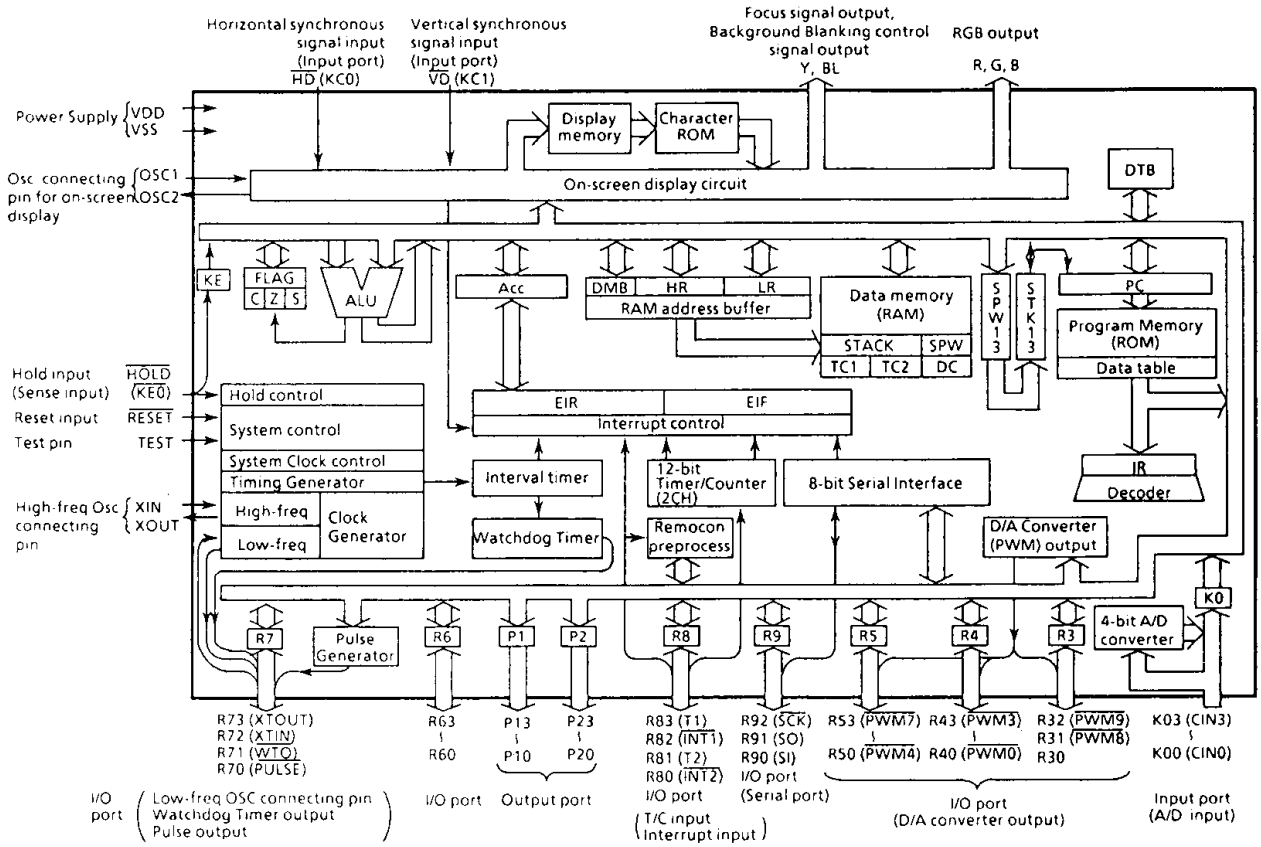
TMP47C038E

PIN ASSIGNMENT (TOP VIEW)

SDIP54



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (CIN3) -K00 (CIN0)	Input	4-bit input port.	A/D conversion (Comparator) input
P13 - P10	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
P23 - P20			
R32 ($\overline{PWM9}$), R31 ($\overline{PWM8}$)	I/O (Output)	3-bit I/O port with latch.	7-bit D/A converter (PWM) output
R30	I/O	When used as input port or D/A converter outputs pins, the latch must be set to "1".	
R43 ($\overline{PWM3}$) -R41 ($\overline{PWM1}$)	I/O (Output)	4-bit I/O port with latch. When used as input port or D/A converter outputs pins, the latch must be set to "1".	7-bit D/A converter (PWM) output
R40 ($\overline{PWM0}$)			14-bit D/A converter (PWM) output
R53 ($\overline{PWM7}$) -R50 ($\overline{PWM4}$)	I/O (Output)		7-bit D/A converter (PWM) output
R63 - R60	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R73 (XTOUT)	I/O (Output)	4-bit I/O port with latch. When used as input port watchdog output pin, or pulse output pin, the latch must be set to "1".	Resonator connecting pin (Low frequency)
R72 (XTIN)	I/O (Input)		
R71 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R70 ($\overline{PULSE}$)			Pulse output (Clock for PLL IC)
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 or REMO-CON input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
R, G, B	Output	RGB output	
Y	Output	Focus signal output	
BL		Background blanking control signal output	
$\overline{HD}$ (KC0)	Input	Horizontal synchronous signal input.	2-bit input port
$\overline{VD}$ (KC1)		Vertical synchronous signal input.	
OSC1, OSC2	Input, Output	Resonator connecting pin of on-screen display circuit.	
XIN, XOUT	Input, Output	Resonator connecting pin (High frequency). For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power Supply	+ 5V	
VSS		0V (GND)	

OPERATION

The following is a description of the 47C1238/1638 hardware configuration and operation. As the description is provided with priority on those parts differing from the 47C1260/1660, the technical data sheets for the 47C1260/1660 shall also be referred to.

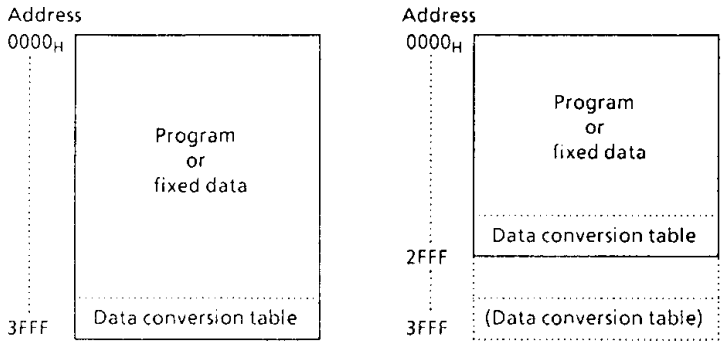
1. SYSTEM CONFIGURATION

(1) Program Memory (ROM)
(2) Data Memory (RAM)
(3) I/O Port
(4) On-screen display (OSD) control circuit
(5) A/D converter (Comparator) input
(6) D/A converter (Pulse width modulation) output
(7) Pulse output circuit

2. INTERNAL CPU FUNCTIONS

2.1 Program Memory

With the 47C1638, programs are stored at address 0000-3FFF$_H$ and, with the 47C1238, programs are stored at address 0000-2FFF$_H$. The 5-8 bit data conversion instruction [OUTB @HL] reads out the fixed data at address 3FE0-3FFF$_H$ and 2FE0-2FFF$_H$, respectively.
Also, with the 47C1238, "0" is read out when address 3000-3FFF$_H$ are accessed by a program.



(a) 47C1638 (b) 47C1238

Figure 2-1. Program Memory

Note. With the 47C1238, the 5-8 bit data conversion table is located at address 2FE0-2FFF$_H$ but, when evaluating the 47C1238 using a piggy-back chip, a conversion table is also required to place at address 3FE0-3FFF$_H$.

2.2 Data Memory (RAM)

The 47C1238 / 1638 have two built-in 256 × 4-bit banks (bank 0, bank 1) for a total of 512 × 4-bit data memory (RAM). The data memory bank selector (DMB) consists of 2 bits but DMB1 is not decoded when addressing the data memory. For example, when DMB is set to 2 or 3, bank 0 or 1 in data memory is accessed.

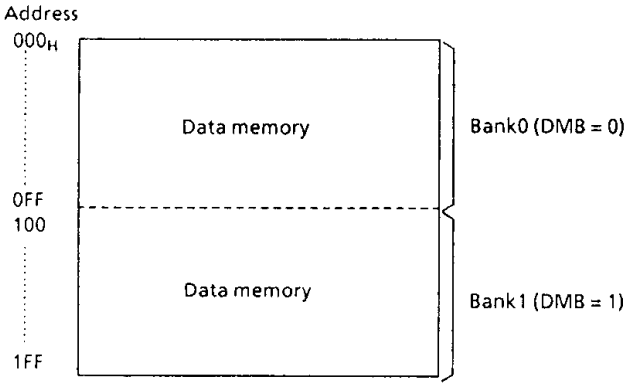


Figure 2-2. Data Memory (RAM)

3. PERIPHERAL HARDWARE FUNCTION

3.1 Input / Output Ports

The 47C1238 / 1638 have 12 built-in input/output ports as follows:

① K0	;	4-bit input	(also used for comparator input)
② P1, P2	;	4-bit output	
③ R3	;	3-bit input / output	(also used for pulse width modulation output)
④ R4, R5	;	4-bit input / output	(also used for pulse width modulation output)
⑤ R6	;	4-bit input / output	
⑥ R7	;	4-bit input / output	(also used for resonator connection, watchdog timer output, pulse output)
⑦ R8	;	4-bit input / output	(also used for external interrupt input, timer/counter input)
⑧ R9	;	3-bit input / output	(also used as a serial port)
⑨ KC	;	2-bit input	(also used for horizontal and vertical synchronous signal input)
⑩ KE	;	1-bit sense input	(also used for hold request / release signal input)

This section describes ports of ①, ③, ④, ⑥ and ⑨ which are changed from 47C1260/1660. Table 3-1 lists the port address assignments and the I/O 'instructions that can access the ports.

3.1.1 I/O Port

(1) Port K0 (K03-K00)

The 4-bit input port. Port K0 is shared digital input with the A/D converter (comparator) input. The K0 port input selector (OP13) determines whether this port is to be used for digital or comparator input. The most significant bit of the K0 port input selector is set to "1" for digital input and to "0" for comparator input.

The K0 port input selector is initialized to "0" during reset.

K0 port (Port address IP00)

3	2	1	0
K03 (CIN3)	K02 (CIN2)	K01 (CIN1)	K00 (CIN0)

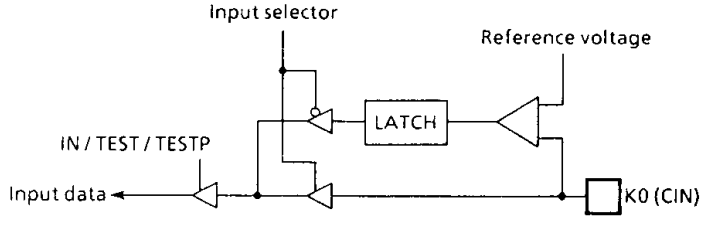


Figure 3-1. Port K0

(2) Port R3 (R32-R30)

This is a 3-bit input / output port with latch. Pins R32, R31 are also used for D/A converter (pulse width modulation) output. When this port is used for input, the latch should be set to "1". When R32, R31 are used for input, the $\overline{PWM}$ output should be also set to "H" level (all PWM data latches should be set to "0"). When using for $\overline{PWM}$ output, set the output latch to "1"; when using for R3 output, set the $\overline{PWM}$ output to "H" level. The output port latch is initialized to "1" and the $\overline{PWM}$ output level to "H" during reset. Also, there is no R33 port but "1" is read out when this bit is accessed.

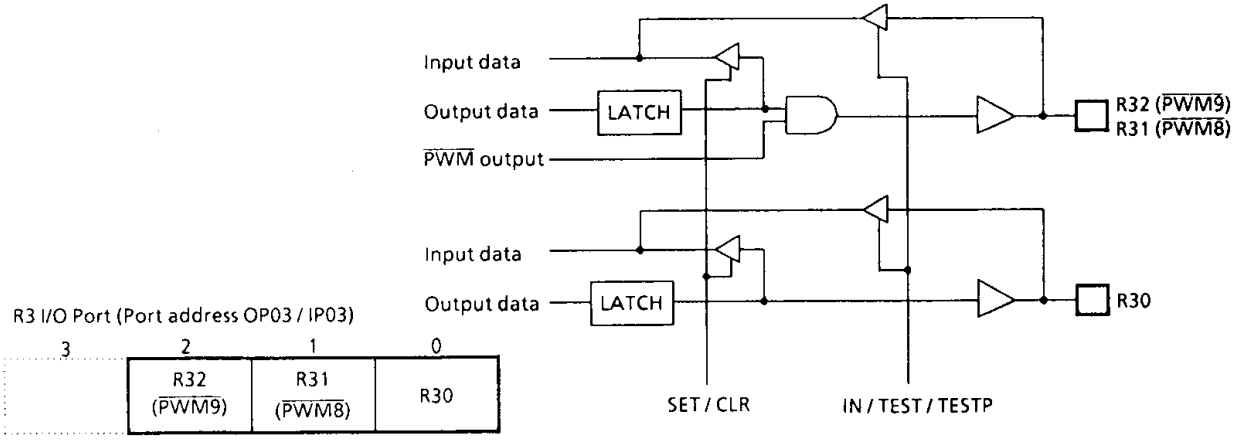


Figure 3-2. Port R3

(3) Port R4 (R43-R40), Port R5 (R53-R50)

These are 4-bit I/O port with latch. They are also used for D/A converter (PWM) output port. R4 port output buffers are Tri-state, and each bit of them can be controlled independently by the program. R5 port is also Tri-state port and they are controlled by the program. Controlling the Tri-state is performed by the command register accessed as port address OP00 and OP13. When some bit of the command register data is 0, the corresponding bit of the output buffers becomes high impedance state. The output latch should be set to "1" when the port is used as $\overline{PWM}$ output port, the $\overline{PWM}$ output should be to "H" level (PWM data is all "0") when the port is used as R4 and R5 port. The output buffers should be set to high impedance state, when the port is used as input port. And the output latch be set to "1", $\overline{PWM}$ output be set to "High" level, and the output buffer be set to High-Impedance state during reset.

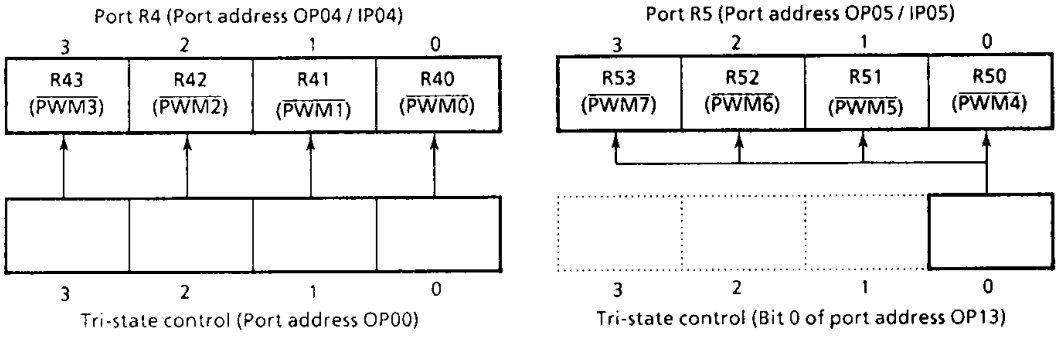


Figure 3-3. Port R4 ($\overline{PWM}$), R5 ($\overline{PWM}$) (1/2)

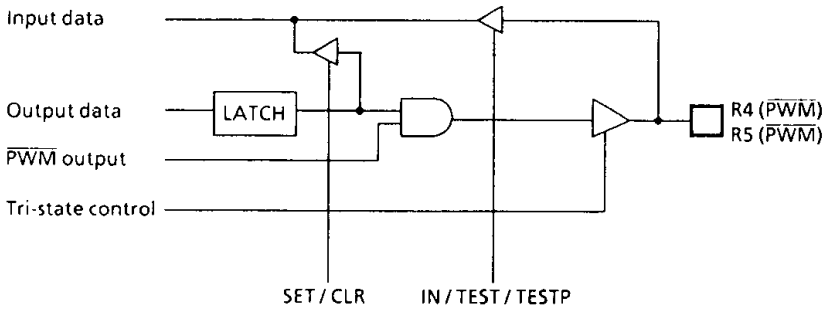
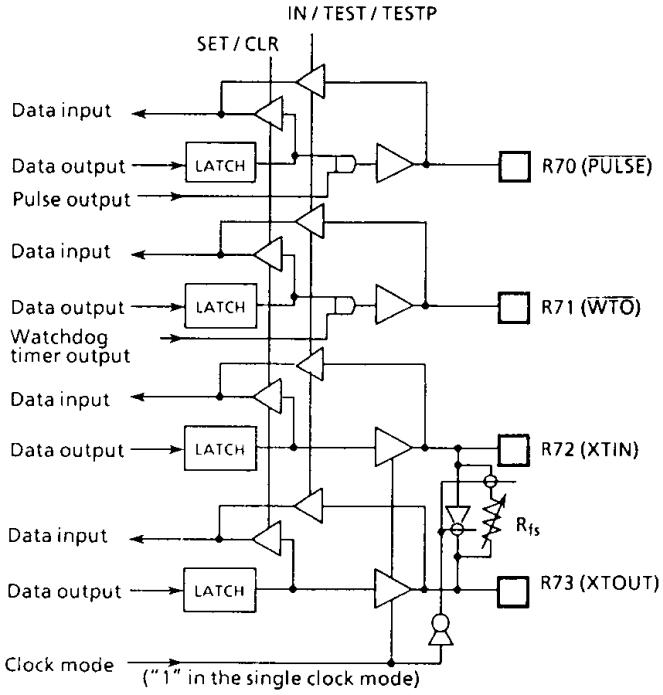


Figure 3-3. Port R4 ($\overline{PWM}$), R5 ($\overline{PWM}$) (2/2)

(4) Port R7 (R73-R70)

Port R7 is shared by the low-frequency resonator connection pins (XTIN, XTOUT), pulse output pin ($\overline{PULSE}$) and the watchdog timer output pin ($\overline{WTO}$). For the dual-clock mode operation, the low-frequency resonator (32.768 kHz), is connected to R72 (XTIN) and R73 (XTOUT) pins. For the single-clock mode operation, R72 and R73 pins are used for the ordinary I/O ports. When the watchdog timer is used, R71 ($\overline{WTO}$) becomes the watchdog timer output pin.

The watchdog timer output is the logical AND output with the port R71 output latch. To use the R71 pin for an ordinary I/O port, the watchdog timer must be disabled (with the watchdog timer output set to "1"). When the pulse output is used, R70 ($\overline{PULSE}$) becomes the pulse output pin. The pulse output is the logical AND output with the port R70 output latch. To use the R70 pin for an ordinary I/O port, the pulse output must be disabled (with the pulse output set to "1").



Port R7 (Port address OP07/IP07)

3	2	1	0
R73 (XTOUT)	R72 (XTIN)	R71 ($\overline{WTO}$)	R70 ($\overline{PULSE}$)

Figure 3-4. Port R7

(5) Port KC (KC1, KC0)

This is 2-bit input port. These port is also used as an input for vertical synchronous signal ($\overline{VD}$), horizontal synchronous signal ($\overline{HD}$). There are not bit 2, 3 of IP0C, however, "1" is read out when IP0C is accessed.

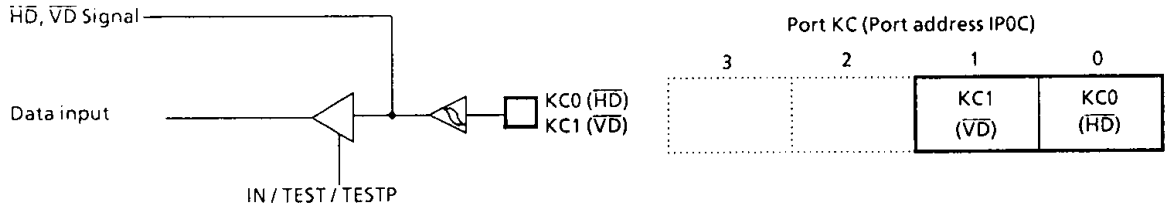


Figure 3-5. Port KC

Port Address (**)	Port		I/O instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	Tri-state(R4 port) Control	○	○	○	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note 3)	○	○	–
02	P2 output latch	P2 output port	○	○	○	○	○	○	–
03	R3 input port	R3 output port	○	○	○	–	○	○	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	KC ($\overline{HD}$, $\overline{VD}$) input port	OSD command selector	○	○	○	–	–	○	–
0D	REMO-CON count value	REMO-CON offset value	○	○	○	–	–	–	–
0E	Status input (Note 2)	Remote control signal preprocess circuit control	○	○	○	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	$\overline{HOLD}$ Pin Status	Hold operation mode	○	○	–	–	–	–	–
11	——	——	–	–	–	–	–	–	–
12	——	A / D converter input control	–	○	–	–	–	–	–
13	SK0, DTB, Status	Tri-state, DTB, comparator	○	○	–	–	–	–	–
14	——	——	–	–	–	–	–	–	–
15	——	Watchdog timer control	–	○	–	–	–	–	–
16	——	System clock control	–	○	–	–	–	–	–
17	Status input for PWM	PWM buffer selector	○	○	–	–	–	–	–
18	——	PWM data transfer buffer	–	○	–	–	–	–	–
19	——	interval timer interrupt control	–	○	–	–	–	–	–
1A	Display line counter	OSD control	○	○	–	–	–	–	–
1B	——	Pulse output control	–	○	–	–	–	–	–
1C	——	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	——	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	——	SIO control 1	–	○	–	–	–	–	–
1F	——	SIO control 2	–	○	–	–	–	–	–

Note 1 . "——" means the reserved state. Unavailable for the user programs.

Note 2 . The status input of serial interface, clock generator, and $\overline{HOLD}$ ($\overline{KE0}$) pin.

Note 3 . The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Table 3-1. Port Address Assignments and Available I/O Instructions

3.2 On-Screen Display (OSD) Circuit

A built-in display on-screen circuit enables TV on-screen displays of characters and symbols. Any 80 of a total of 128 character patterns can be displayed in 20 columns x 4 lines. It is possible to display more than 5 lines by using the OSD interrupt.

3.2.1 OSD Circuit Functions and Configuration

① Number of character patterns	128
② Number of display characters	80 (20 columns x 4 lines), more than 5 lines can be displayed by using the OSD interrupt.
③ Composition of a character	14 x 18 dots (80 characters), 7 x 9 dots (48 characters)
④ Character size	3 sizes (selectable line by line)
⑤ Display colors	Characters: 7 colors (selectable character by character), background color: 1 of 7 colors.
⑥ Fringing and smoothing function	
⑦ Display position:	horizontal: 128 steps; vertical: 128 steps

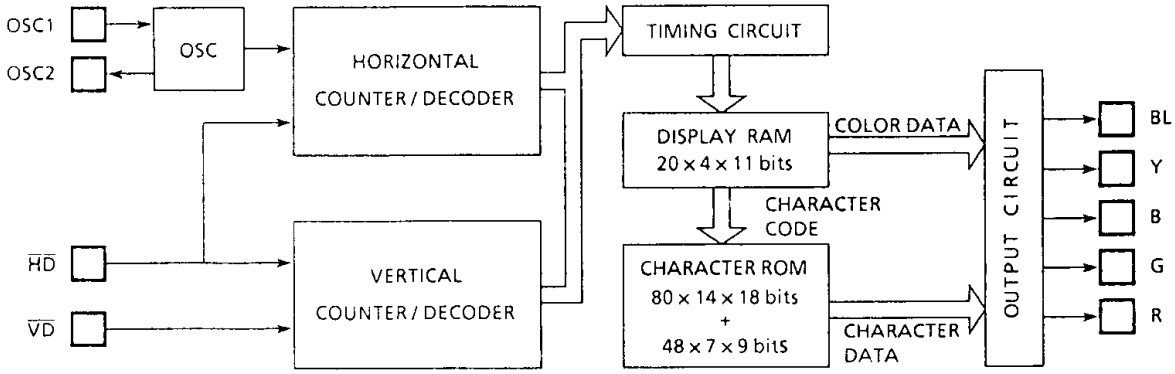


Figure 3-6. OSD Circuit

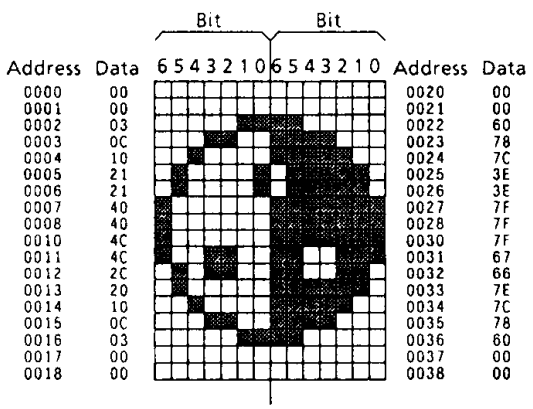
3.2.2 OSD Display Related Memory

(1) Character ROM

A total of 128 character patterns are built into the character ROM and the patterns can be freely designated by the user. The character ROM contains 80 characters with a 14 x 18 dot composition (character code 00_H - $4F_H$) and 48 characters with a 7 x 9 dot composition (character code 50_H - $7F_H$). Each dot corresponds to 1 bit of ROM. "1" turns on the dot and "0" turns off the dot.
The start address of character ROM can be calculated using the following expression.

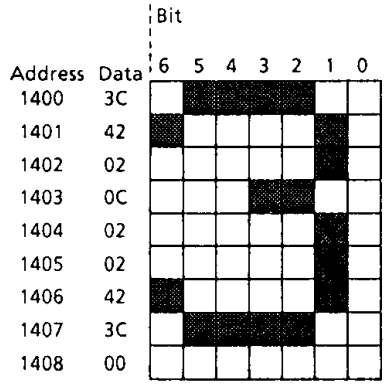
For character code 00_H - $4F_H$: Character ROM start address = CRA x 64
For character code 50_H - $7F_H$: Character ROM start address = 5120 + (CRA - 80) x 16
Note. CRA: Character code

As the character whose character code is $7E_H$ is fixed as a background and the character whose character code is $7F_H$ is fixed as a blank data, these two characters can not be designated by the user. Figure 3-7 shows the 14 x 18 dot composition character (Character code 00_H) and Figure 3-8 shows the 7 x 9 dot composition character (Character code 50_H), as an example. These figures also show the ROM address and the data of those patterns.
Figure 3-9 shows the ROM dump list for these 2 character patterns. When the piggy back is used or the ROM data is being submitted for manufacturing engineering samples, the address of character ROM should be placed to 4000_H to $56F8_H$.



(Character code 00_H)

Figure 3-7. 14 x 18 Dot Composition



(Character code 50_H)

Figure 3-8. 7 x 9 Dot Composition

```
0000/ 00 00 03 0C 10 21 21 40 40 00 00 00 00 00 00 00
0010/ 40 4C 2C 20 10 0C 03 00 00 00 00 00 00 00 00 00
0020/ 00 00 60 78 7C 3E 3E 7F 7F 00 00 00 00 00 00 00
0030/ 7F 67 66 7E 7C 78 60 00 00 00 00 00 00 00 00 00

1400/ 3C 42 02 0C 02 02 42 3C 00 00 00 00 00 00 00 00
```

Figure 3-9. Character ROM Dump List

(2) Display memory

The display memory has a 20-columns x 11-bit x 4 lines configuration with a one-to-one correspondence to the number of columns displayed on the screen. The character code, the color data and blinking flag for the display characters and symbols are stored to the display memory. When power on is performed, the contents of display memory becomes unpredictable.

There are two methods for writing data to the display memory. In the first method, the character code, color data and blinking flag are written at the same time. In the second method, only the color data and blinking flag are changed. The method for writing display data to the display memory is described in 3.2.3 (6).

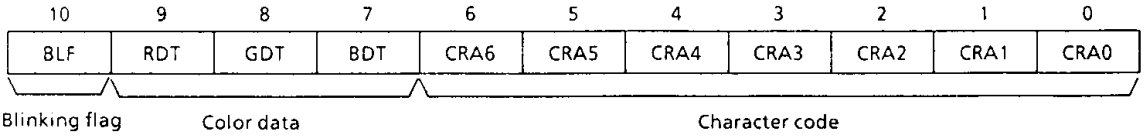


Figure 3-10. Bit Configuration of Display Memory

Line \ Column	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
2	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33
3	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
4	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73

Note. The numerals in the chart indicate display memory address (HEX).

Table 3-2. Display Memory Configuration

3.2.3 OSD Circuit Control

The OSD circuit is controlled by the command selector (OP0C) and control register (OP1A). Table 3-3 shows the relationship between OP0C and OP1A. The command selector selects the OSD control register. Writing data to the control register of all bits is performed by accessing OP1A two times. However, the second access is not required unless the second data are changed.

The OSD control register has a 28-word configuration and sets the display start position, display character ornamentation, display memory address and character codes.

After setting all control registers are completed and the command selector is set to F_H, display is enabled and the display starts. When the command selector is set to E_H, display is disabled.

(1) Display start position

Display start position of each display line on screen can be set in 128 steps both horizontally and vertically. The horizontal start position of the first line is set with OSD control register HS16 - HS10 while the vertical start position is set with VS16 - VS10. The display start positions of the 2nd - 4th lines are determined by setting HS26 - HS40 and VS26 - VS40 in the same way.

A double scan mode in which each vertical scan line is counted twice is provided to enable use with PAL and double scan mode TVs. It is possible to set the vertical display start position all over the screen area in this mode. Setting WSC (command selector is set to B_H) of the OSD control register to "1" enables the double scan mode and setting to "0" enables the normal mode.

The display start position can be calculated in following expressions.

Horizontal display start position of line "n"

$$HSn = \{(HSn6 \sim HSn4) \times 16^1 + (HSn3 \sim HSn0) \times 16^0\} \times 4T_{OSC} + \alpha T_{OSC}$$

α : 14 for a small size character, 28 for a middle and 56 for a large

Tosc : The period of OSD clock oscillation

Vertical display start position of line "n"

When WSC = 0 $VSn = \{(VSn6 \sim VSn4) \times 16^1 + (VSn3 \sim VSn0) \times 16^0\} \times 2T_{HD}$

When WSC = 1 $VSn = \{(VSn6 \sim VSn4) \times 16^1 + (VSn3 \sim VSn0) \times 16^0\} \times 4T_{HD}$

T_{HD} : The period of horizontal synchronous signal

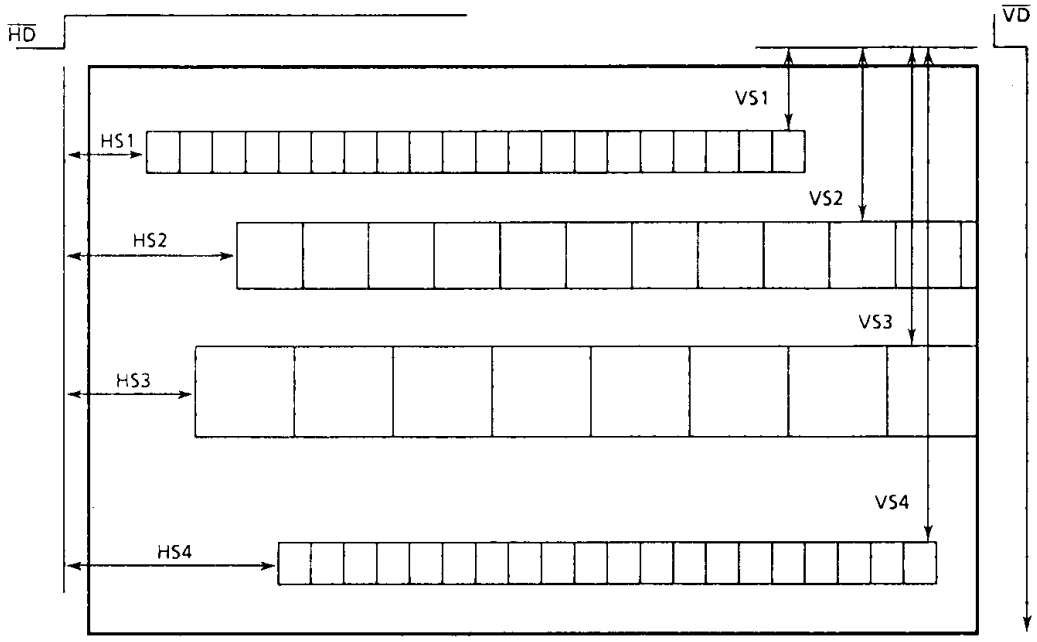


Figure 3-11. TV Screen Image

OSD Command selector (OP0C)	OSD control register to be accessed through OP1A	
	1st ACCESS	2nd ACCESS
0	Horizontal start position of 1st display line 3 2 1 0 HS13 HS12 HS11 HS10	3 2 1 0 HS16 HS15 HS14
1	Vertical start position of 1st display line 3 2 1 0 VS13 VS12 VS11 VS10	3 2 1 0 VS16 VS15 VS14
2	Horizontal start position of 2nd display line 3 2 1 0 HS23 HS22 HS21 HS20	3 2 1 0 HS26 HS25 HS24
3	Vertical start position of 2nd display line 3 2 1 0 VS23 VS22 VS21 VS20	3 2 1 0 VS26 VS25 VS24
4	Horizontal start position of 3rd display line 3 2 1 0 HS33 HS32 HS31 HS30	3 2 1 0 HS36 HS35 HS34
5	Vertical start position of 3rd display line 3 2 1 0 VS33 VS32 VS31 VS30	3 2 1 0 VS36 VS35 VS34
6	Horizontal start position of 4th display line 3 2 1 0 HS43 HS42 HS41 HS40	3 2 1 0 HS46 HS45 HS44
7	Vertical start position of 4th display line 3 2 1 0 VS43 VS42 VS41 VS40	3 2 1 0 VS46 VS45 VS44
8	Character size of 1st and 2nd line 3 2 1 0 CS21 CS20 CS11 CS10	Smoothing, OSD outputs polarities 3 2 1 0 ESMZ BLIV YIV RGBIV
9	Character size of 3rd and 4th line 3 2 1 0 CS41 CS40 CS31 CS30	OSD outputs tri-state control 3 2 1 0 EBFY EBFR EBFG EBFB
A	Blinking flag, Coloring (character) 3 2 1 0 BLF RDT GDT BDT	Fringing, Coloring (back ground) 3 2 1 0 EFRG RBDT GBDT BBDT
B	Blinking, Double scan mode 3 2 1 0 WSC BKMF SBS DSPF	OSD interrupt function 3 2 1 0 IOSD SVD ISDC1 ISDC0
C	Display memory address set, Display memory bank selector 3 2 1 0 DMA3 DMA2 DMA1 DMA0	3 2 1 0 MBK DMA6 DMA5 DMA4
D	Character code set 3 2 1 0 CRA3 CRA2 CRA1 CRA0	3 2 1 0 CRA6 CRA5 CRA4
E	OSD disable	
F	OSD enable	

Table 3-3. OSD Control Commands and Control Registers

(2) Display character sizes

Character size for screen display can be selected line by line from 3 sizes.

Small, middle and large character size can be set with OSD control register CS41 - CS10 (command selector is set to 9_H or A_H). It is also possible to display with mixing 7 x 9 dot and 14 x 18 dot composition characters. When the character size is set the same, both dot composition of characters are displayed in the same size.

Line / Character size	First display line		Second display line		Third display line		Fourth display line	
	CS11	CS10	CS21	CS20	CS31	CS30	CS41	CS40
Small character	1	1	1	1	1	1	1	1
Middle character	1	0	1	0	1	0	1	0
Large character	0	1	0	1	0	1	0	1
Display OFF	0	0	0	0	0	0	0	0

Table 3-4. Designation of Character Size

Size		Small character	Middle character	Large character
One dot size	14 x 18 dot composition	1 T_{OSC} x 1 T_{HD}	2 T_{OSC} x 2 T_{HD}	4 T_{OSC} x 4 T_{HD}
	7 x 9 dot composition	2 T_{OSC} x 2 T_{HD}	4 T_{OSC} x 4 T_{HD}	8 T_{OSC} x 8 T_{HD}
Character size		14 T_{OSC} x 18 T_{HD}	28 T_{OSC} x 36 T_{HD}	56 T_{OSC} x 72 T_{HD}

Note. T_{OSC} : *The period of OSD clock oscillation.*
T_{HD} : *The period of horizontal synchronous signal.*

Table 3-5. Character Size

(3) Smoothing and fringing functions

The smoothing function makes characters look smooth. When smoothing is enabled, additional dots (1/4 size) are displayed in the middle of the place where two dots contact each other only at a corner. However, this function is not available for 14 x 18 dot small character size.

Fringing displays the fringe of characters in a different color from rest of the color of the character. When fringing is enabled, a 1/2 dot width around the character periphery is displayed in a different color, as shown in Figure 3-12.

However, this function is not available for 14 x 18 dot small character size.

Smoothing is enabled by setting ESMZ (command selector is set to 8_H) of the OSD control register to "1". Fringing is enabled by setting EFRG (command selector is set to A_H) of the OSD control register to "1". When smoothing and fringing are enabled at the same time, smoothing has a priority, as shown in Figure 3-13.

The color of the fringe can be set by BBDT, GBDT, RBDT (command selector is set to A_H) of the OSD control register. Coloring for fringe is described in the next section.

(4) Display colors

One out of seven colors can be selected for each character to be displayed. Display character color is set by the color data in the display memory. The color data loaded to RDT, GDT, BDT (command selector is set to A_H) of the OSD control register are written to the display memory at the same time as the character code is written.

The entire background for the character area (14 x 18 or 8 x 9 dots) can be colored. The background color is set by RBDT, GBDT, BBDT of the OSD control register (command selector is set A_H).

When the fringing is enabled, the color of fringe is set by the background color data (RBDT, GBDT, BBDT). Thus, the entire background for the character area can not be colored at that time.

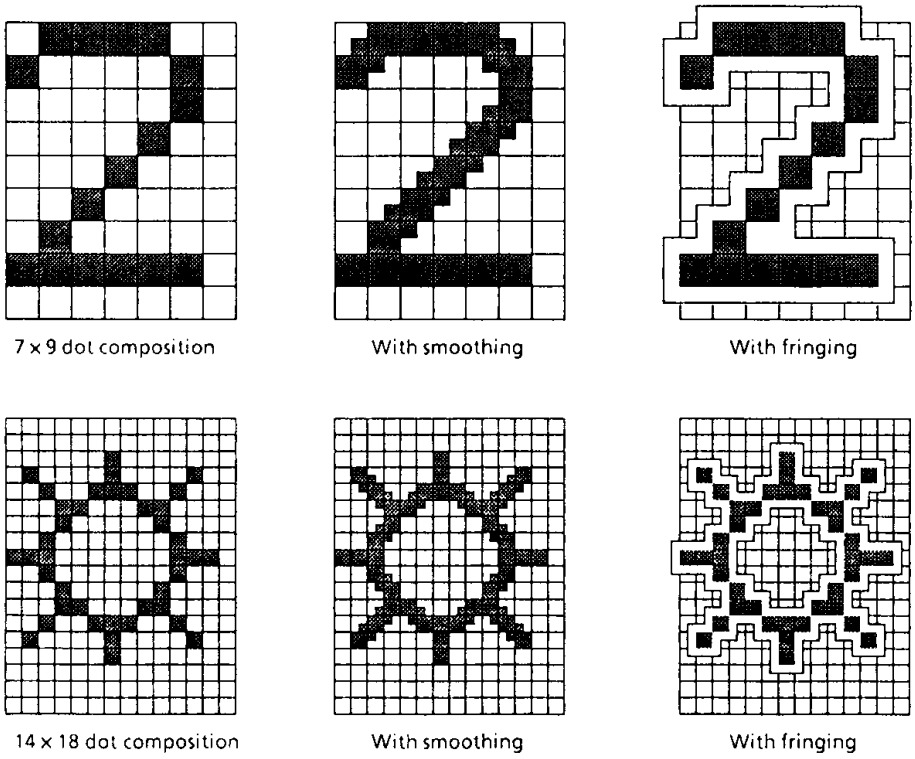


Figure 3-12. Example of Smoothing and Fringing Function

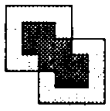


Figure 3-13. Priority of Smoothing and Fringing

(5) Blinking function

Any character displayed on the screen can be caused to blink. The blinking flag (BLF) of the display memory and DSPF, SBS, BKMF (command selector is set to B_H) of the OSD control register determine the blinking position and period. There are two kinds of setting blinking period; one is for the fixed period by the hardware and the other one is for the programmable period by the user.

To cause a character to blink, first set BLF of the display memory to "1".

The blinking flag BLF (command selector is set to A_H) of the OSD control register will then be written to the display memory at the same time as the character code is written.

Next, set BKMF to "1" to enable the blinking function. When SBS is "1", the character will blink at a period of fc/22. When SBS is "0", the value of DSPF itself determines whether or not the character is displayed. Thus, DSPF is alternately set and cleared with each cycle of the soft timer to produce the blinking .

OSD control register

3	2	1	0
(WSC)	BKMF	SBS	DSPF

BKMF	Blinking master flag

0 : Disable blinking.
1 : Enable blinking.

SBS	Blinking source select

0 : Blinking period is specified by DSPF.
1 : Blinking period is set to $fc/2^{22}$.

DSPF	Display enable control flag

0 : Erase the character which BLF is set to "1".
1 : Display the character which BLF is set to "1".

Figure 3-14. Control of Blinking Function

(6) Writing display data to the display memory

Display data, which consist of the character code, color data and blinking flag, are written to the display memory which corresponds to the one to one to the displayed position. Load the display memory address to DMA6 - DMA0 of the OSD control register and load the memory bank to MBK. When all of the display data is changed, clear MBK to "0". When only the color data and blinking flag are changed, set MBK to "1".

To change all of the display data, set the display memory address and clear MBK to "0"; then set the color data and blinking flag with BLF, BDT, GDT, RDT (command selector is set to A_H) of the OSD control register. Next, write the character code with CRA6 - CRA0 (command selector is set to D_H) of the OSD control register. When OP1A is accessed for the second time, the character code is written to the display memory with the color data and blinking flag which are set beforehand at the same time. Display memory address DMA6 - DMA0 are also automatically incremented at this time; therefore, it is not necessary to set the display memory address again when the display data is written continuously. However, this auto-increment function is only effective within one line of the display memory. Auto-increment does not operate when the line is changed (example: display memory address $13_H \rightarrow 20_H$).

When only the color data and blinking flag setting are changed, set the display memory address as above and set MBK to "1"; then set the color data and blinking flag with BLF, BDT, GDT, RDT of the OSD control register. The data are then sent to the display memory but the character code is not changed. Display memory address DMA6 - DMA0 are also automatically incremented at this time; therefore, it is not necessary to set the display memory address again when the color data and blinking flag is written continuously. However, this auto-increment function is only effective within one line of the display memory. Auto-increment does not operate when the line is changed (example: display memory address $13_H \rightarrow 20_H$).

(7) OSD output buffer

The OSD outputs for RGB and Y/BL use tri-state output buffers, which the respective polarities can be inverted. The polarity and the tri-state is controlled by accessing EBFY-EBFB, BLIV, YIV, RGBIV (command selector is set to 9_H or 8_H) of the OSD control register.

Symbol	Output pin	Data "0"	Data "1"
EBFY	Y, BL	Output Buffer OFF	Output Buffer ON
EBFB	B	Output Buffer OFF	Output Buffer ON
EBFG	G	Output Buffer OFF	Output Buffer ON
EBFR	R	Output Buffer OFF	Output Buffer ON

Table 3-6. Control of OSD Output

Symbol	Output port	Data "0"	Data "1"
BLIV	BL	Active High	Active Low
YIV	Y	Active High	Active Low
RGBIV	RGB	Active High	Active Low

Table 3-7. Control of OSD Output Polarity

(8) OSD output waveform

The OSD output pins comprise the R, G and B color signal outputs, the Y signal which is the logical OR of the R, G and B signals, and the BL signals output to all display character areas (excluding character code $7E_H$). Y and BL signal makes the display clearer by eliminating the video signal only where characters or background are displayed.

Figure 3-15 shows display example (1). The conditions for this example are as follows:

① Display data: 2, C, blank data (character code $7F_H$), background (character code $7E_H$).
② Color data: RDT = 1, BDT = 0, GDT = 0.
③ Background color data: BRDT = 0, BBDT = 1, BGDT = 0.
④ Fringing and smoothing disabled.
⑤ This screen display example is controlled by the R, B and BL signals.

Figure 3-16 shows display example (2). The conditions for this example are as follows:

① Display data: 2, C, blank data (character code $7F_H$), background (character code $7E_H$).
② Color data: RDT = 1, BDT = 0, GDT = 0.
③ Background color data: BRDT = 0, BBDT = 1, BGDT = 0.
④ Fringing enabled and smoothing disabled.
⑤ This screen display example is controlled by the R, B and Y signals.

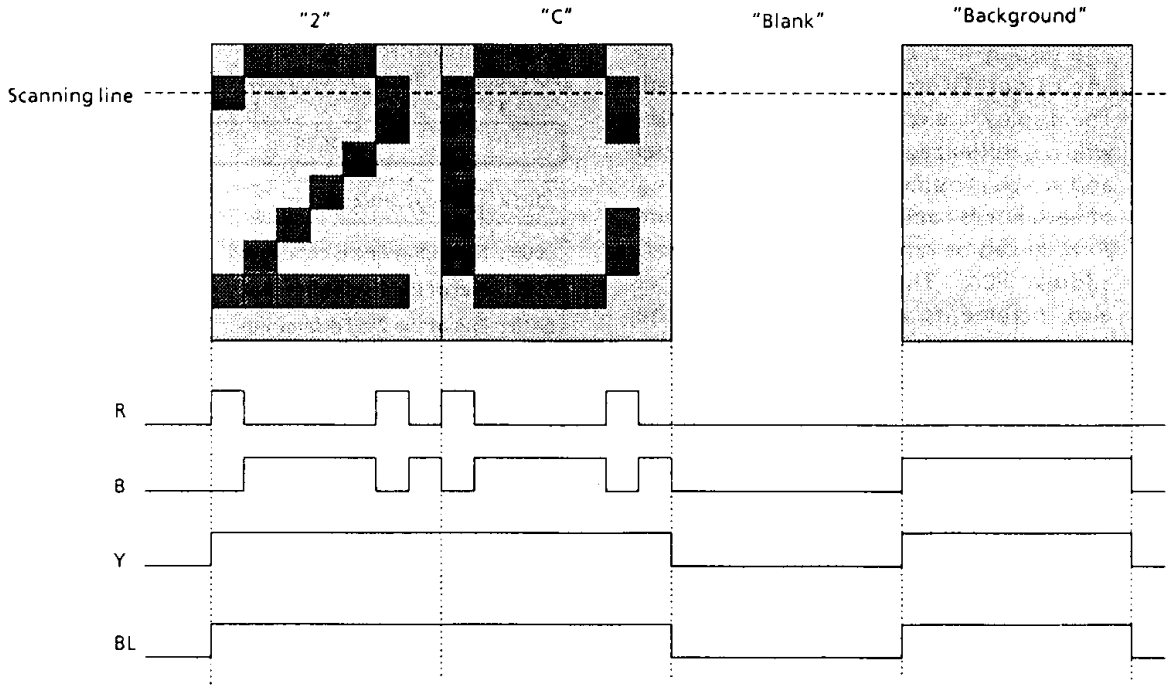


Figure 3-15. Example of OSD Display and Its Wave Form (1)

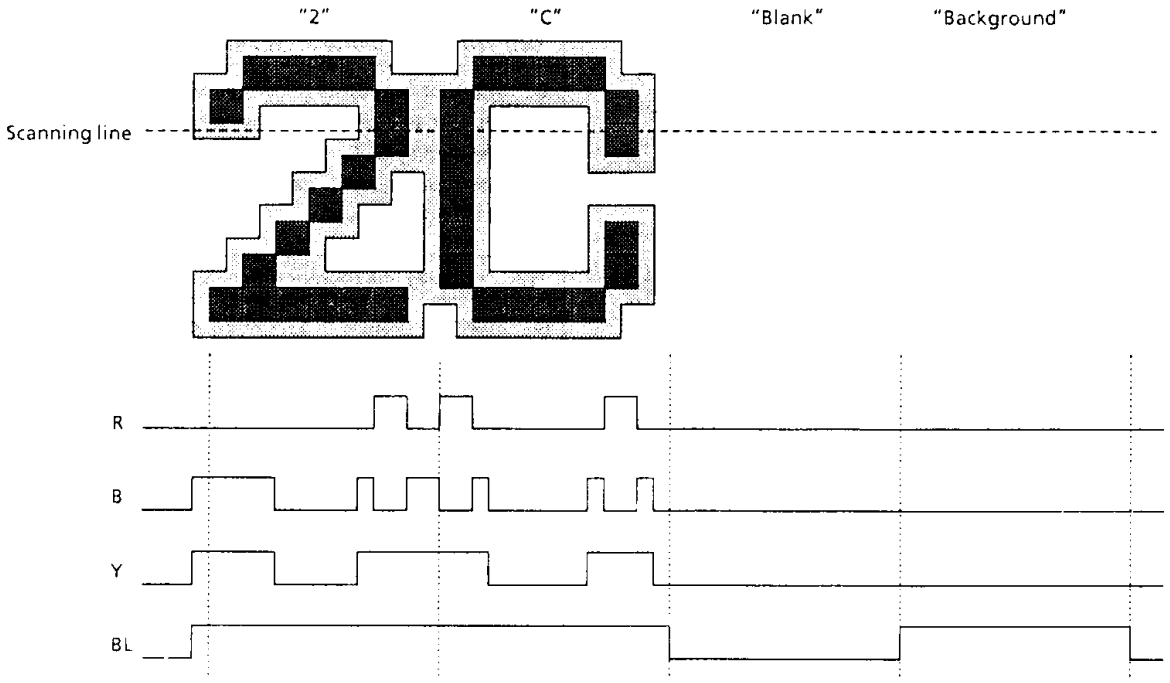


Figure 3-16. Example of OSD Display and Its Wave Form (2)

3.2.4 Multi-line Displays Using the OSD Interrupt

Up to 4 lines can be displayed on screen with the built-in hardware.

Multi-line displays of more than 5 lines are also available by using the OSD interrupt to rewrite the display start position and display data for the next display after the display of each line has been completed. The hardware related to the OSD interrupt comprises the display line counter, the interrupt generator circuit and its control circuit.

(1) Display line counter

The display line counter indicates which line of one TV screen is being displayed. The display line counter is a 4-bit counter which is initialized to "0" by the $\overline{VD}$ signal and which increments when last scanning of each line is completed. The display line counter can be read out by accessing port address IP0A. The display line counter also increments when the data of the display line are all blank data or the display line is disabled.

(2) Interrupt generator circuit

The interrupt generator circuit is controlled by OSD control registers IOSD, SVD, ISDC (command selector is set to B_H). One out of the two interrupt sources SIO or OSD can be selected by IOSD of OSD control register. A OSD interrupt request is generated when IOSD is set to "1" and an ISIO interrupt request is generated when IOSD is set to "0". The interrupt request is generated every falling edge of $\overline{VD}$ signal comes when SVD is set to "1". When the SVD is set to "0", interrupt request is generated at the start point of the first scanning line of the display line specified by ISDC.

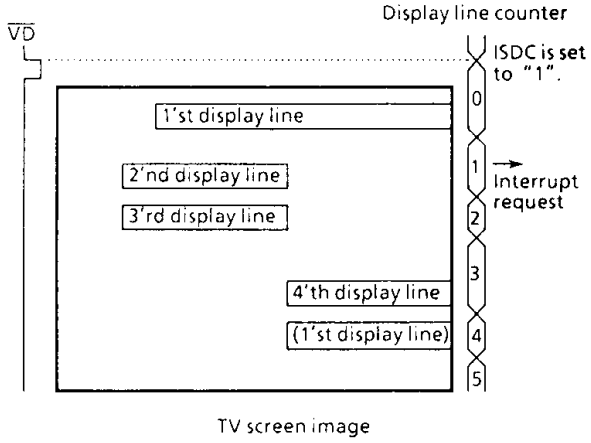


Figure 3-19. Multi Line Display Using OSD Interrupt

Display line counter
(Port address : IP0A Initialize to "0")

3	2	1	0
DCTR			

DCTR	Display line counter

0000 : No display line is completed.
0001 : End of the 1'st display line.
0010 : End of the 2'nd display line.
⋮
1111 : End of the 15'th display line.

Figure 3-17. Display Line Counter

3	2	1	0
IOSD	SVD	ISDC	

IOSD	Interrupt source

0 : ISIO interrupt request
1 : IOSD interrupt request

SVD	Interrupt source of OSD function

0 : Interrupt request is generated when the display line counter is counted to the certain value which is specified by ISDC.
1 : Interrupt request is generated when the falling edge of $\overline{VD}$ signal comes.

ISDC	Display line counter interrupt sources

00 : Interrupt request is generated at start points of the first scanning line of each display line.
01 : Interrupt request is generated at the start point of the first scanning line of the display line when the lower 2-bit of the display line counter is "01".
10 : Interrupt request is generated at the start point of the first scanning line of the display line when the lower 2-bit of the display line counter is "10".
11 : Interrupt request is generated at the start point of the first scanning line of the display line when the lower 2-bit of the display line counter is "11".

Figure 3-18. Control of OSD Interrupt

3.3 D/A Converter (Pulse Width Modulation) Output

The 47C1238 has 10 built-in pulse width modulation (PWM) channels. D/A converter output can easily be obtained by connecting an external low-pass filter.

$\overline{PWM}$ outputs are multiplexed with general purpose I/O ports as; R31, R32 ($\overline{PWM8}$, $\overline{PWM9}$), R4 ($\overline{PWM0}$ - $\overline{PWM3}$), R50 - R53 ($\overline{PWM4}$ - $\overline{PWM7}$). When these ports are used as $\overline{PWM}$ outputs, the corresponding bits of R3, R4 and R5 output latches should be set to "1". Resetting initializes the R3, R4 and R5 output latches to "1".

$\overline{PWM}$ output is controlled by the buffer selector (OP17) and data transfer register (OP18). Writing "C_H" to the buffer selector transfers the PWM data in the data transfer buffer to the PWM data latch, thus, the $\overline{PWM}$ output will be changed. The PWM data transferred to the PWM data latch are retained until overwritten.

Resetting and holding clear the buffer selector, data transfer buffer and PWM data latch to "0".

3.3.1 Pulse Width Modulation Circuit Output

(1) $\overline{PWM0}$ output

This is 14-bit resolution $\overline{PWM}$ output and one period is $T_M = 2^{15}/fc$ [sec].

The 8 high-order bits of the PWM data latch control the pulse width of the pulse output with a period of T_S ($T_S = T_M/64$), which is the sub-period of the $\overline{PWM0}$. When the 8-bit data are decimal n ($0 \leqq n \leqq 255$), this pulse width becomes $n \times t_0$, where $t_0 = 2/fc$.

The lower 6-bit of 14 bit data are used to control the generation of additional to wide pulse in each T_S period. When the 6-bit data are decimal m ($0 \leqq m \leqq 63$), the additional pulse is generated in each of m periods out of 64 periods contained in a T_M period. The relationship between the 6 bits data and the position of TS period where the additional pulse is generated is shown in Table 3-8.

(2) $\overline{PWM1}$ - $\overline{PWM9}$ outputs

These are 7-bit resolution $\overline{PWM}$ outputs and one period is $T_N = 2^8/fc$ [sec]. When the 7bit data are decimal k ($0 \leqq k \leqq 127$), the pulse width becomes $k \times t_0$. The wave form is illustrated in Figure 3-20.

3.3.2 Pulse Width Modulation Circuit Control (Data Transfer)

$\overline{PWM}$ output is controlled by writing the output data to data transfer buffers (OP18). For writing the output data are divided using the buffer selector (OP17). Buffer numbers are assigned to each of the data transfer buffers. Writing is performed in accordance with the corresponding tables shown in Table 3.9.

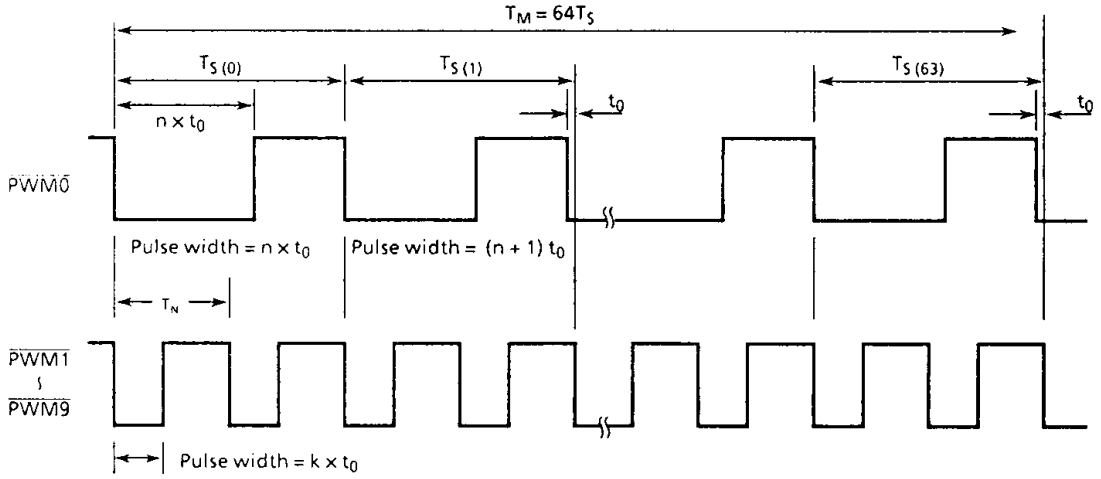
① Write the buffer number of the transfer buffer to which the data are to be written to the buffer selector (OP17).

② Write the 4 low-order bits of the corresponding PWM output data to the selected buffer (OP18).

③ Next, write the 4 high-order bits of $\overline{PWM}$ output data to the buffer.

④ When writing of the output data is completed, write "C_H" to the buffer selector.
When switching of the output data is completed, the PWM status input becomes "0", indicating that the next data can be written. Do not write PWM data when the PWM status is "1" because write errors can occur in this case. The PWM status can be read by accessing bit "0" of port address IP17.

While the output data are being written to the transfer buffer, the previously written data are being output. The maximum time from the point at which "C_H" is written to the buffer register until $\overline{PWM}$ output is switched is $2^{15}/fc$ (at 4MHz, 8192 μs) for $\overline{PWM0}$ output and $2^8/fc$ [sec] (at 4MHz, 128 μs) for $\overline{PWM1}$ - $\overline{PWM9}$ output.



Note. It is shown to the additional pulse $T_{S(1)}$ and $T_{S(63)}$ of the PWM0.

Figure 3-20. PWM Output Wave Form

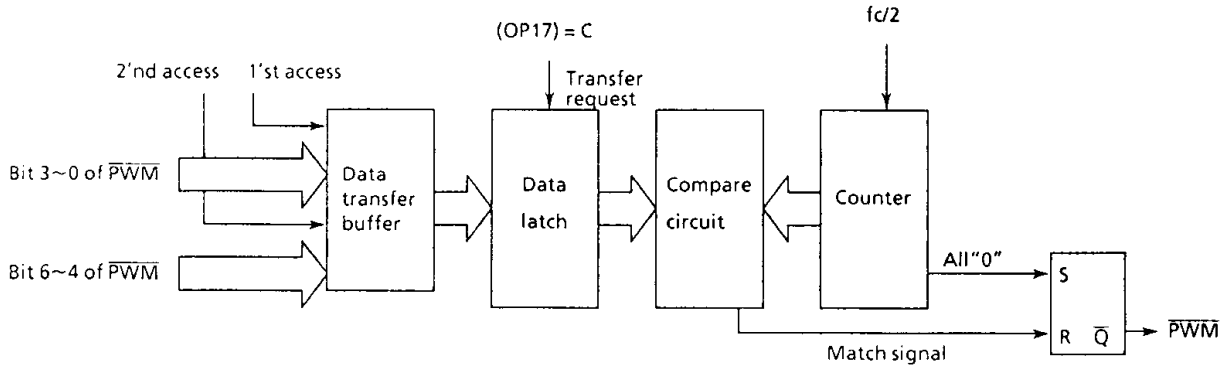


Figure 3-21. PWM Circuit Configuration (7bit Resolution)

Bit position of 6 bits data	Relative position of T_S where the output pulse is generated (No. i of $T_{S(i)}$ is listed)
Bit0	32
Bit1	16, 48
Bit2	8, 24, 40, 56
Bit3	4, 12, 20, 28, 36, 44, 52, 60
Bit4	2, 6, 10, 14, 18, 22, 26, 30, ·····, 58, 62
Bit5	1, 3, 5, 7, 9, 11, 13, 15, 17, ·····, 59, 61, 63

Note. When the corresponding bit is "1", it is output.

Table 3-8. Correspondence between 6 Bits Data and the Additional Pulse Generated T_S Periods

Buffer number (OP17)	Correspondence to bit (OP18)		Mode
	1'st access	2'nd access	
0	Bit 3~0 of $\overline{PWM0}$	Bit 5~4 of $\overline{PWM0}$	Writing
1	Bit 9~6 of $\overline{PWM0}$	Bit 13~10 of $\overline{PWM0}$	Writing
2	Bit 3~0 of $\overline{PWM1}$	Bit 6~4 of $\overline{PWM1}$	Writing
3	Bit 3~0 of $\overline{PWM2}$	Bit 6~4 of $\overline{PWM2}$	Writing
4	Bit 3~0 of $\overline{PWM3}$	Bit 6~4 of $\overline{PWM3}$	Writing
5	Bit 3~0 of $\overline{PWM4}$	Bit 6~4 of $\overline{PWM4}$	Writing
6	Bit 3~0 of $\overline{PWM5}$	Bit 6~4 of $\overline{PWM5}$	Writing
7	Bit 3~0 of $\overline{PWM6}$	Bit 6~4 of $\overline{PWM6}$	Writing
8	Bit 3~0 of $\overline{PWM7}$	Bit 6~4 of $\overline{PWM7}$	Writing
9	Bit 3~0 of $\overline{PWM8}$	Bit 6~4 of $\overline{PWM8}$	Writing
A	Bit 3~0 of $\overline{PWM9}$	Bit 6~4 of $\overline{PWM9}$	Writing
C	None	None	Transfer

Table 3-9. The Bit and Buffer Number of Data

3.4 4bit A/D Conversion (Comparator) Input

The comparator input is analog input to discriminate key input or AFC (Auto Frequency Control) signal. It's composed of 4-bit D/A converter, comparator and control circuit. Analog input level (CIN0-CIN3) can be detected as 16-stage by setting reference voltage.

The comparator input can also be used as K0 port (digital input). To use as K0 port, set the most significant bit of the port address OP13 to "1". Which port is selected digital (K0) or comparator (CIN) input can be monitored by accessing the port address IP13. DTB selector/status is also assigned to port address OP13/IP13.

Note. When the comparator input is selected, the comparator consumes typically 700μA current at VDD = 5V. To reduce the power consumption, K0 port should be set to digital input mode. In the HOLD mode, the comparator current is automatically cut off by hardware. Further, during the slow operating mode, A/D conversion input is automatically disabled by hardware to reduce the power consumption.

3.4.1 Circuit Configuration of Comparator Input

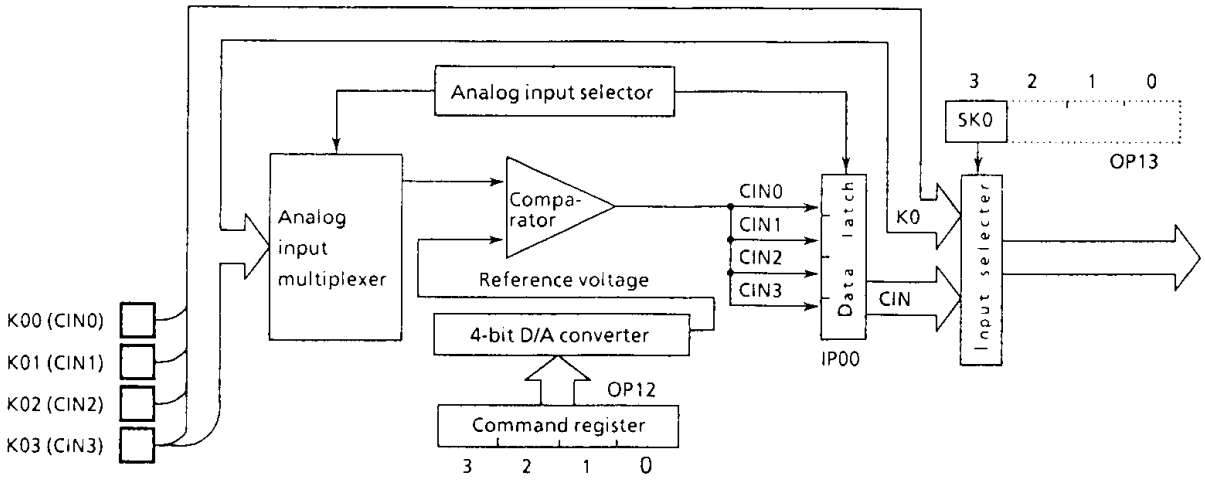


Figure 3-22. Circuit of Comparator Input

3.4.2 Control of Comparator Input

K0 port input selector command register
(Port address : OP13/IP13 Initial value 0110)

3	2	1	0
SK0	DTB		

SK0	Select K0 input mode
0 :	CIN comparator input
1 :	K0 digital input

Figure 3-23. Command Register, Status Register

Reference voltage (Vref) is set by command register (port address OP12), and it is determined by the following form.

$$V_{REF} = V_{DD} \times (n + 1) / 16 \text{ [V]} \quad (n = 0 \sim 15)$$

After initialization sequence, 4-channel comparator inputs continue comparison operation successively.
Since 2-instruction cycles are required to complete comparison of 1-channel, it is necessary to wait for 8-instruction cycles after setting a reference voltage to read data from the comparator. When analog input voltage is higher than reference voltage, comparator data latch is set to "1". At the initialization sequence, OP12 is set to "0". There is not latch when used to port K0.

OP12				Vref.
3	2	1	0	[V]
0	0	0	0	0.31
0	0	0	1	0.62
0	0	1	0	0.94
0	0	1	1	1.25
0	1	0	0	1.56
0	1	0	1	1.87
0	1	1	0	2.19
0	1	1	1	2.50
1	0	0	0	2.81
1	0	0	1	3.12
1	0	1	0	3.44
1	0	1	1	3.75
1	1	0	0	4.06
1	1	0	1	4.37
1	1	1	0	4.69
1	1	1	1	5.00

Table 3-10. Reference Voltage

3.5 Pulse Output Circuit

Pulse output circuit generates the pulse clock by dividing the clock frequency to R70 port. The pulse output is used for the basic clock for the PLL IC or peripheral ICs. The pulse output frequency can be set by accessing command register (OP1B). Command register is initialized to '11**' during reset. When R70 port is used as the pulse output, set R70 output latch to "1".

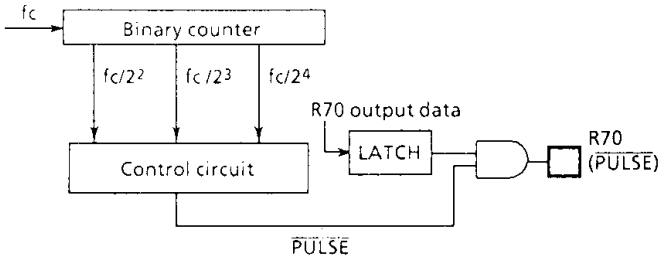


Figure 3-24. Pulse Output Circuit

Pulse output control command register
(Port address OP1B)

3	2	1	0
SPF			

SPF	Select pulse frequency
	at fc = 4MHz
00 :	Output pulse of fc/2⁴ [Hz] ... 250KHz
01 :	Output pulse of fc/2³ [Hz] ... 500KHz
10 :	Output pulse of fc/2² [Hz] 1MHz
11 :	Disable the pulse output

Figure 3-25. Pulse Output Command Register

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include port R7	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R7 port	− 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	30	mA
	I_{OUT2}	Ports R3, R6, R7, R8, R9	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	120	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	f_C	XIN, XOUT		0.4	6.0	MHz
	f_{OSD}	OSC1, OSC2		−	8.0	

Note . Input Voltage V_{IH3}, V_{IL3}: in the HOLD operating mode.

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Low Current	I_{IL}	Port R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	−	−	− 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Tri-state port Ports R3, R6, R8, R9 (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	± 2	μA
Output High Voltage	V_{OH1}	Port R (push-pull)	V_{DD} = 4.5V, I_{OH} = − 200μA	2.4	−	−	V
	V_{OH2}	Port R (tri-state), OSD outputs	V_{DD} = 4.5V, I_{OH} = − 0.7mA	4.1	−	−	
Output Low Voltage	V_{OL1}	Ports R3, R6-R9	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
	V_{OL2}	Port R (tri-state), OSD outputs	V_{DD} = 4.5V, I_{OL} = 0.7mA				
Output Low Current	I_{OL}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	−	20	−	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	−	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the pull-up / pull-down resistor is contained.
The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

A / D CONVERTER CHARACTERISTICS

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max.	UNIT
Analog input voltage	V_{AIN}	CIN		V_{SS}	-	V_{DD}	V
A / D conversion error	-			-	-	$\pm\frac{1}{2}$	LSB

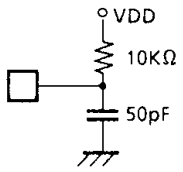
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = −30 to 70°C)

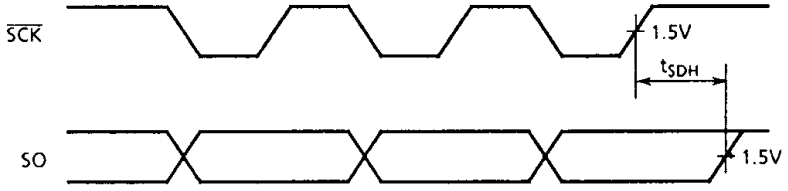
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.3	−	20	μs
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	−	−	ns
Low level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		0.5tcy − 300	−	−	ns

Note. Shift data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin.



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

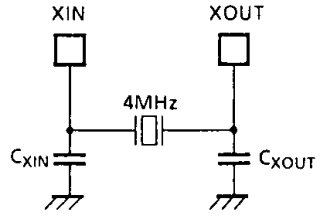
(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = −30 to 70°C)

(1) 4MHz
Ceramic Resonator

CSA4.00MG	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30pF

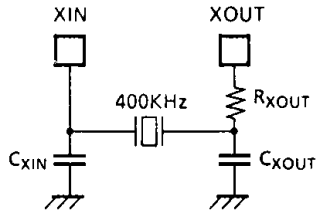
Crystal Oscillator

204B-6F 4.0000	(TOYOCOM)	$C_{XIN} = C_{XOUT}$ = 20pF

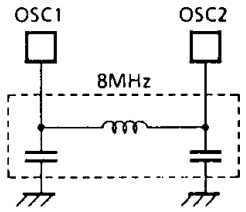


(2) 400KHz
Ceramic Resonator

CSB400B	(MURATA)	$C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ
KBR-400B	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

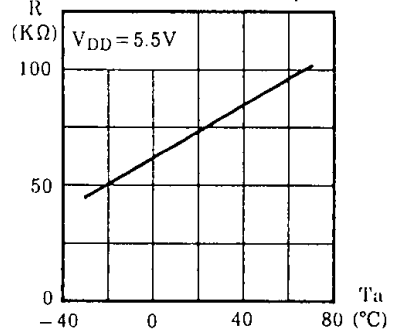


(3) 8MHz (for OSD)
LC Resonator

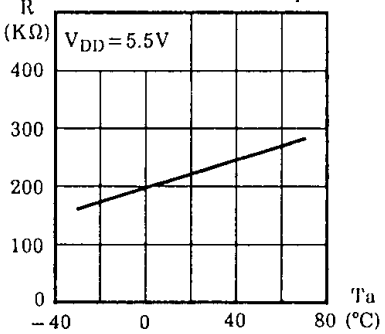


TYPICAL CHARACTERISTICS

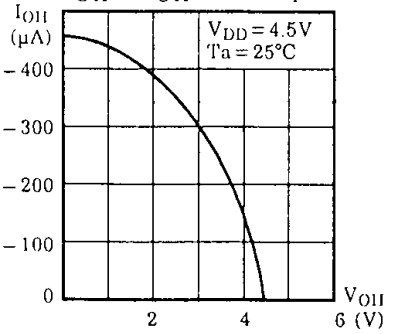
R – Ta K0 port



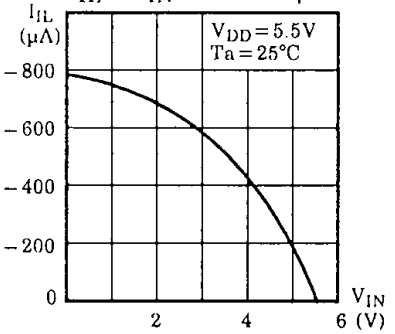
R – Ta $\overline{\text{RESET}}$ pin



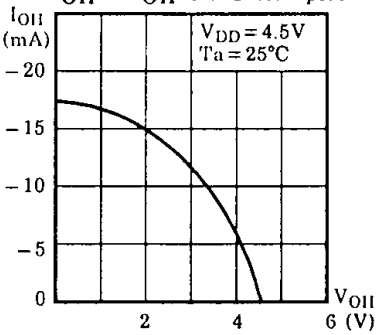
$I_{OH} - V_{OH}$ CMOS R port



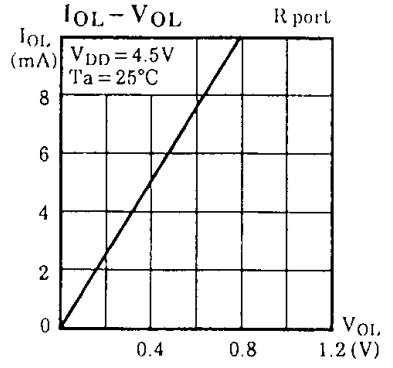
$I_{IL} - V_{IN}$ CMOS R port



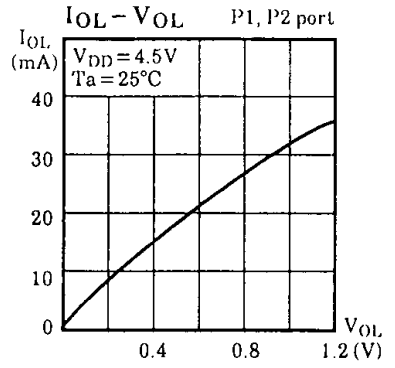
$I_{OH} - V_{OH}$ TRI-STATE port



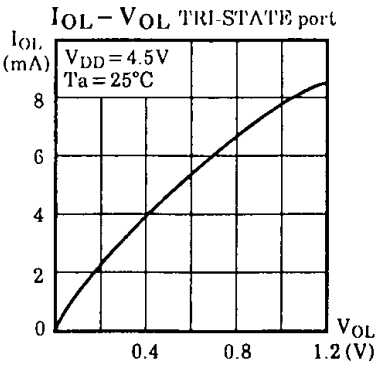
$I_{OL} - V_{OL}$ R port



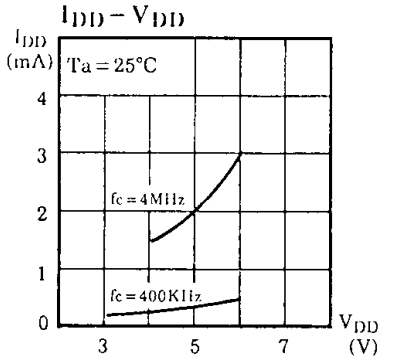
$I_{OL} - V_{OL}$ P1, P2 port



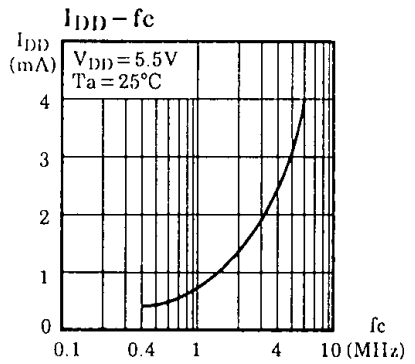
$I_{OL} - V_{OL}$ TRI-STATE port



$I_{DD} - V_{DD}$



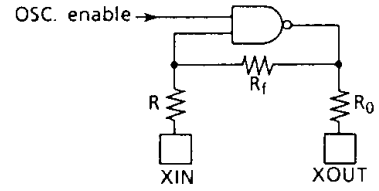
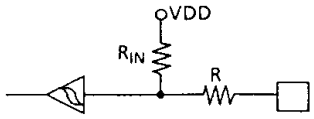
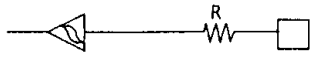
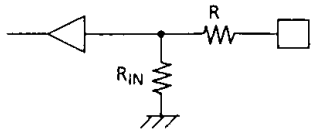
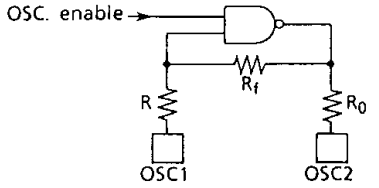
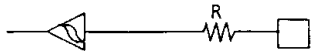
$I_{DD} - fc$



INPUT/OUTPUT CIRCUITRY

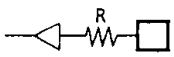
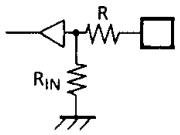
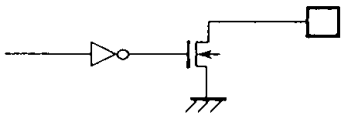
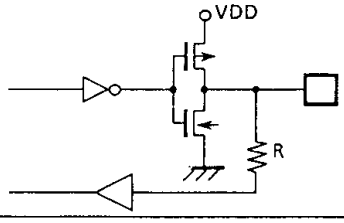
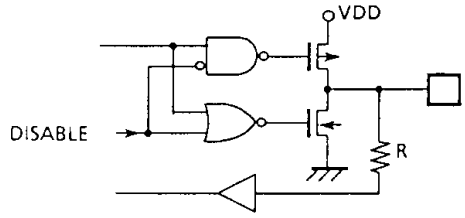
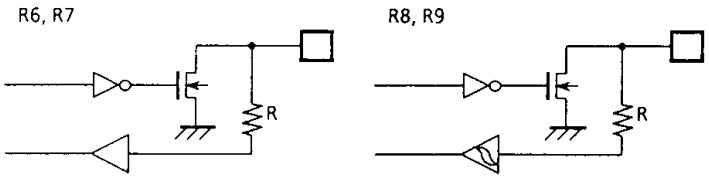
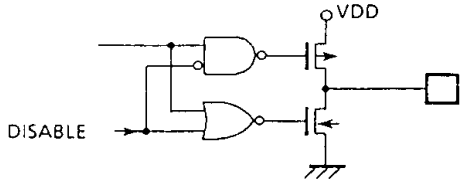
(1) Control pins

Input/output circuitries of the 47C1238/1638 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins R = 1KΩ (typ.) Rf = 1.5MΩ (typ.) RO = 2KΩ (typ.)
$\overline{RESET}$	Input		Hysteresis input Contained pull-up resistor RIN = 220KΩ (typ.) R = 1KΩ (typ.)
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)		Hysteresis input (Sense input) R = 1KΩ (typ.)
TEST	Input		Contained pull-down resistor RIN = 70KΩ (typ.) R = 1KΩ (typ.)
OSC1 OSC2	Input Output		Oscilation terminals for OSD R = 1KΩ (typ.) Rf = 1.5MΩ (typ.) RO = 2KΩ (typ.)
$\overline{HD}$ (KC0) $\overline{VD}$ (KC1)	Input		Synchronous signal input Hysteresis input R = 1KΩ (typ.)

(2) I/O ports

The input/output circuitries of the 47C1238/1638 I/O ports are shown below, designated by code.

PORT	I/O	INPUT/OUTPUT CIRCUITRY (code)	REMARKS
K0	Input	PA:  PC: 	Pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P1 P2	Output		Sink open drain Initial "Hi-Z" High drive current I_{OL} = 20mA (typ.)
R3	I/O		Push-pull output Initial "High" R = 1KΩ (typ.)
R4 R5	I/O		Tri-state I/O Initial "Hi-Z" R = 1KΩ (typ.)
R6 R7 R8 R9	I/O		Sink open drain Initial "Hi-Z" Hysteresis input (R8, R9) R = 1KΩ (typ.)
R G B Y BL	Output		Tri-state output Initial "Hi-z"

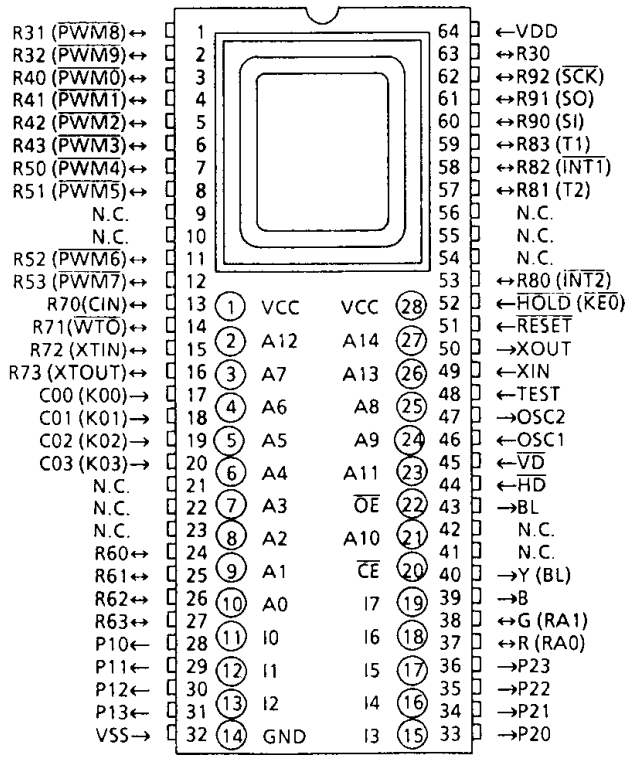
CMOS 4-BIT MICROCONTROLLER

TMP47C038E

The 47C038, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C1237/1637 and 47C1238/1638 application systems (programs). Conversion adapter socket BM1105 can be used to convert the 64-pin package of the 47C038 for pin compatibility with the 42-pin mask ROM 47C1237/1637. Conversion adapter socket BM1106 can be used to convert from 64 pins for pin compatibility with the 54-pin 47C1238/1638.

PIN ASSIGNMENT (TOP VIEW)

SDIC64



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A14 - A0	Output	Program memory address output
I7 - I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5~6.0V	–	–	150	ns
Data Setup Time	t_{IS}	C_L = 100pF	150	–	–	ns
Data Hold Time	t_{IH}	Topr = – 40~70°C	50	–	–	ns

NOTES FOR USE

(1) Program memory

The program storage areas are as shown in Figure 1. The 47C038 has a data table at addresses 4000-56FF$_H$ (128 characters) for display on-screen data so that characters and symbols can be displayed on TV screens. Thus, a 128K EPROM is not used.

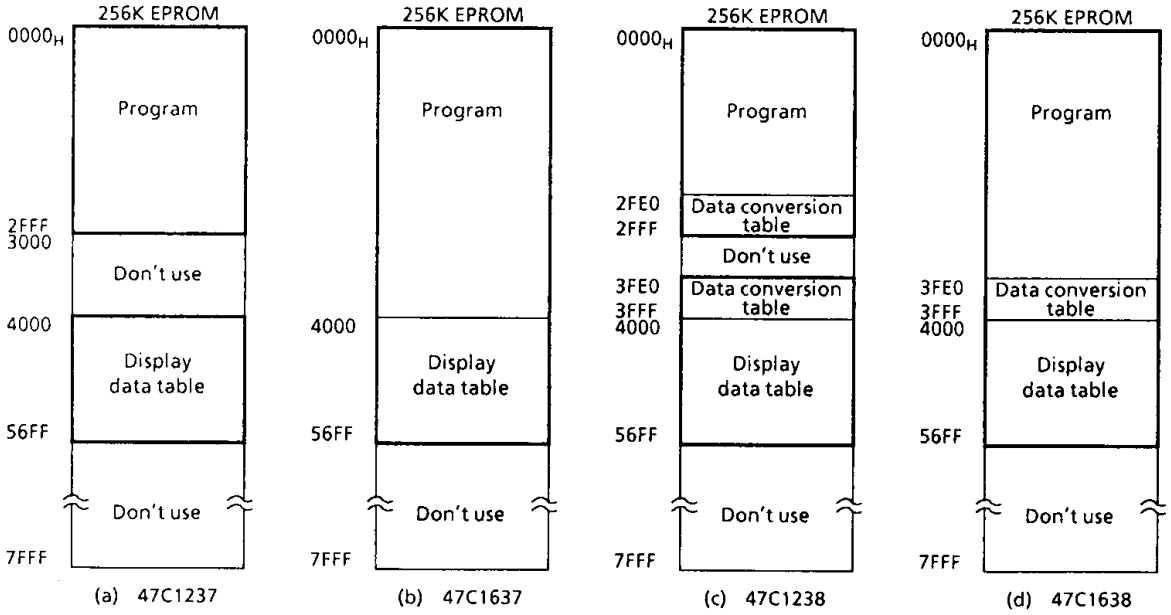


Figure1. Program Area

Note. When using the 47C038 to check 47C1238 operation, place data conversion tabels at two locations.

(2) Data memory

47C038 contains two 256 x 4-bit data memory banks (bank 0, bank 1).

(3) Input/outpu ports

The input/output circuit for the 47C038 input/output ports is the same as that of the 47C1237/1637 and 47C1238/1638 (code : PC), except that a pulldown resistor is not built into the K0 port.
When using as code PC evaluators, it is necessary to connect an external resistor.

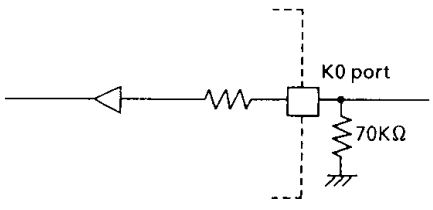


Figure 2. I/O Code and External Circuitry

Note. The 47C1237/1637 do not have built-in P1, P2 and R3 ports.