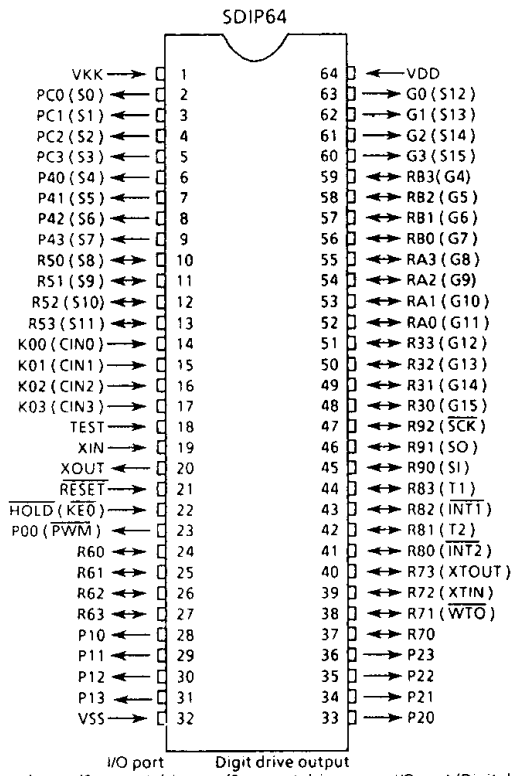
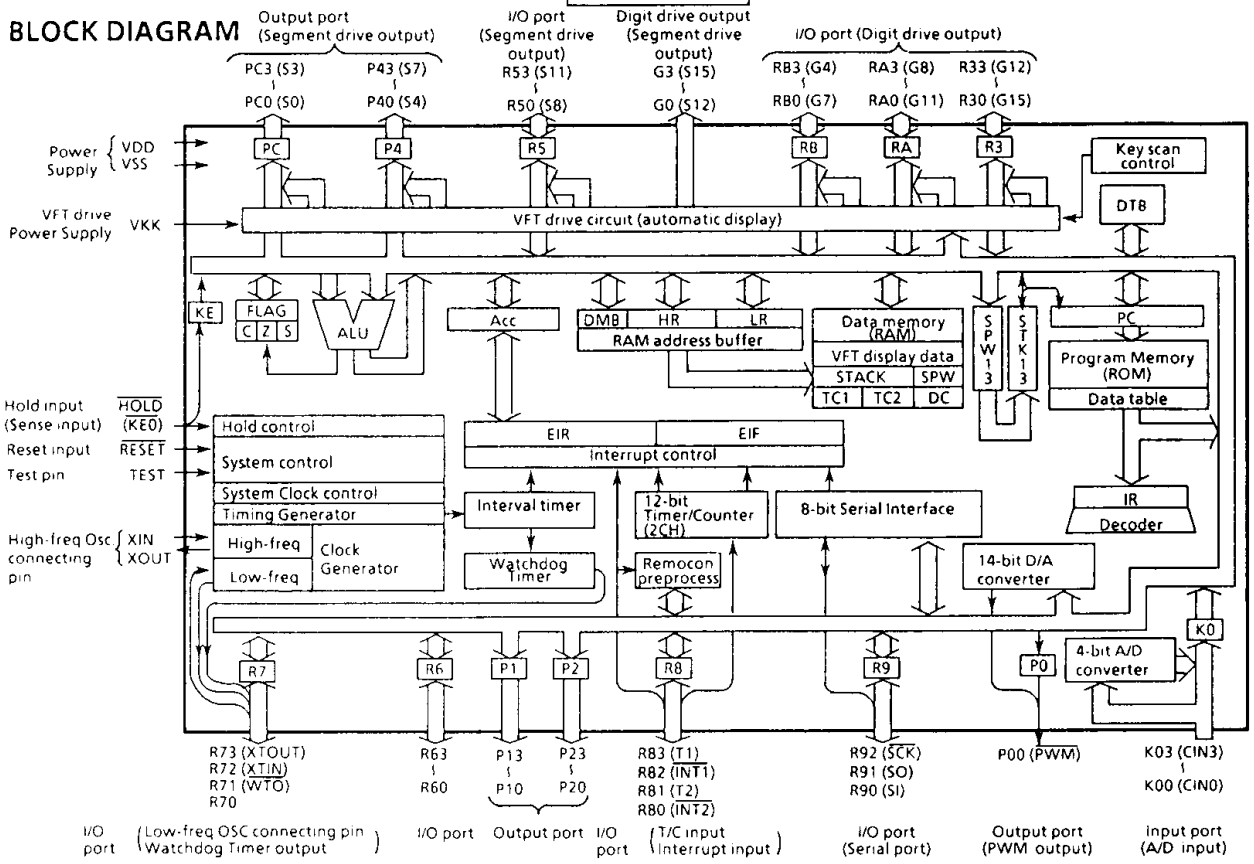
PIN ASSIGNMENT (TOP VIEW)

SDIP64



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (CIN3) - K00 (CIN0)	Input (Input)	4-bit input port	A / D conversion (Comparator) input
P00 ($\overline{PWM}$)	Output (Output)	1-bit output port with latch	D / A converter (PWM) output
P13 - P10 P23 - P20	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data coversion instruction [OUTB @HL].	
R63 - R60	I/O	4-bit I/O port with latch. When used as the input port, latch must be set to "1".	
R73 (XTOUT)	I/O (Output)	4-bit I/O port with latch. When used as the input port or watchdog timer output pin, the latch must be set to "1".	Resonator connecting pin (Low frequency)
R72 (XTIN)	I/O (Input)		
R71 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R70	I/O		
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as the input port, external interrupt input pin, or timer/counter input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as the input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
G3 (S15) - G0 (S12)	Output (Output)	VFT digit drive output	VFT Segment drive output
P43 (S7) - P40 (S4)		4-bit high breakdown voltage output port with latch	
PC3 (S3) - PC0 (S0)			
R53 (S11) - R50 (S8)	I/O (Output)	4-bit high breakdown voltage output port with latch	
R33 (G12) - R30 (G15)			VFT digit drive output
RA3 (G8) - RA0 (G11)			
RB3 (G4) - RB0 (G7)			
XIN	Input	Resonator connecting pin (High-frequency).	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input	HOLD request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power Supply	+ 5V	
VSS		0V (GND)	
VKK		VFT drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C1270/1670, the hardware configuration and operation are described.
As the description include mainly differences from the 47C1260/1660, the technical data sheets for the 47C1260/1660 shall also be referred to.

1. SYSTEM CONFIGURATION

(1) I/O Ports
(2) VFT drive circuit
(3) A/D Conversion (comparator) input circuit
(4) D/A Converter (pulse width modulation) output circuit

2. PERIPHERAL HARDWARE FUNCTION

2.1 I/O Ports

The 47C1270/1670 have 15 I/O ports (53 pins) each as follows:

① K0	;	4-bit input	(shared with the comparator input)
② P0	;	1-bit output	(shared with the PWM output)
③ P1, P2	;	4-bit output	
④ R6	;	4-bit input/output	
⑤ R7	;	4-bit input/output	(shared with the low-frequency reasonator connection pins and the watchdog timer output)
⑥ R8	;	4-bit input/output	(shared with external interrupt request input and timer/counter input)
⑦ R9	;	3-bit input/output	(shared with serial port)
⑧ P4, PC	;	4-bit output	(shared with segment output)
⑨ R5	;	4-bit input/output	(shared with segment output)
⑩ R3, RA, RB	;	4-bit input/output	(shared with digit output)
⑪ KE	;	1-bit sense input	(shared with hold request/release signal input)

As the description has been provide with priority on ports (①, ② and ⑧~⑩) changed from 47C1260/1660.
Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

2.2.1 I/O Ports

(1) Port K0 (K03 - K00)
Port K0 is a 4-bit input-only port. Port K0 is shared with the A/D converter(comparator) input. The K0 port input selector(OP13) determines whether this port is to be used digital or comparator input. The most significant bit of the K0 port input selector is set to "1" for digital input and to "0" for comparator input. The K0 port input selector is initialized to "0" during reset. A pull-up or pull-down resistor can be contained by the mask option.

K0 port (Port address IP00)

3	2	1	0
K03 (CIN3)	K02 (CIN2)	K01 (CIN1)	K00 (CIN0)

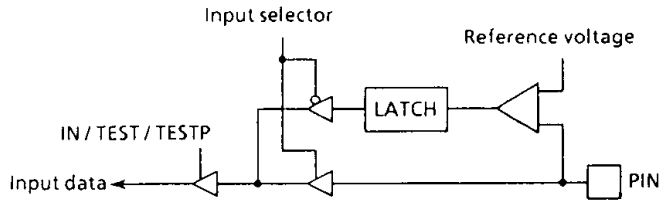


Figure 2-1. Port K0

(2) Port P0 (P00)

The 1-bit output with a latch. The P00 pin is also used for pulse width modulation ($\overline{PWM}$) output. When this pin is used for ($\overline{PWM}$) output, the latch should be set to "1". When using P00 as the output pin, the $\overline{PWM}$ output should be set to "H" level (the PWM data latch is set to "0"). The P00 output latch is initialized to "1" during reset.

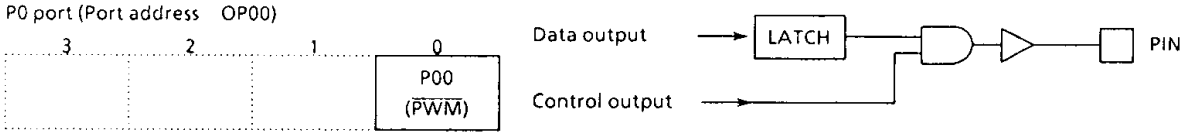


Figure 2-2. Port P0

(3) Ports P4 (P43-P40), PC (PC3-PC0)

The 4-bit high breakdown voltage output ports with latch, which can directly drive Vacuum Fluorescent Tubes (VFT). The latch data can be read by input instructions. The latch is initialized to "0" during reset. Ports P4, PC are shared with the segment output. When these pins are used for segment output, the latch should be cleared to "0". The VFT display should be set to blanking mode, however, when these ports are used for normal output (when display is enabled, access by instruction is not possible).

Each set, clear and test bit of ports P4, R5, R6 and R7 can be operated using the L-register indirect addressing bit manipulation instructions [SET @L], [CLR @L], [TEST @L] in accordance with the L-register contents.

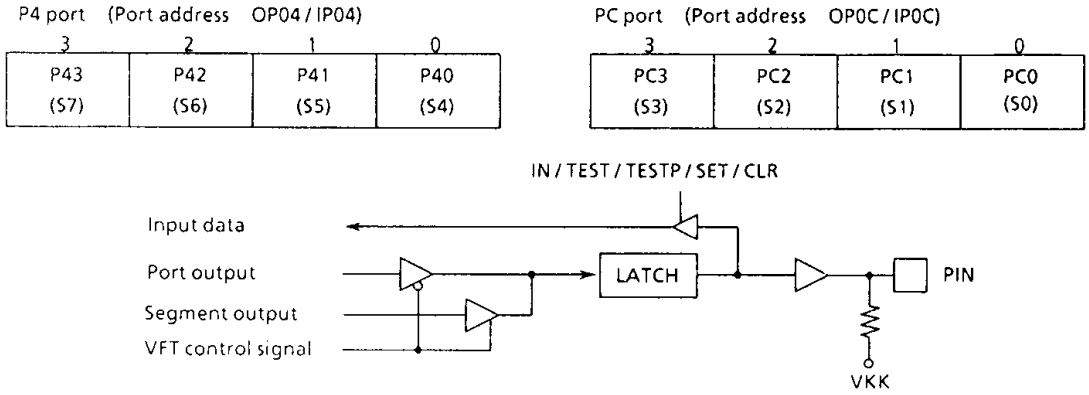


Figure 2-3. Ports P4, PC

(4) Port R5 (R53 - R50)

The 4-bit high breakdown voltage I/O ports with latch, which can directly drive Vacuum Fluorescent Tubes (VFT). The latch should be cleared to "0" when used as an input port. The latch is initialized to "0" during reset. Port R5 is also used for segment output. The latch should be set to "0" for segment output. The VFT display should be set to blanking mode, however, when this port is used for normal output (when display is enabled, access by instruction is not possible). Pins which are not set for segment output can be used for normal I/O port. Each set, clear and test bit of ports R5, P4, R6 and R7 can be operated using the L-register indirect adressing bit manipulation instructions in accordance with the L-register contents.

(5) Ports R3 (R33 - R30), RA (RA3 - RA0), RB (RB3 - RB0).

The 4-bit high breakdown voltage I/O ports with latch, which can directly drive Vacuum Fuolrescent Tubes (VFT). The latch should be cleared to "0" when used as an input port. The latch is initialized to "0" during reset.

Ports R3, RA and RB are also used for digit output. The latch should be cleared to "0" for digit output. Pins not connected to VFT can be used for normal I/O ports. However the port output instruction is effective even when VFT display is enabled. Consequently, caution must be exercised since the output data for the display is destroyed when an output instruction is sent to a pin being used for display.

R5 port (Port address OP05 / IP05)

3	2	1	0
R53 (S11)	R52 (S10)	R51 (S9)	R50 (S8)

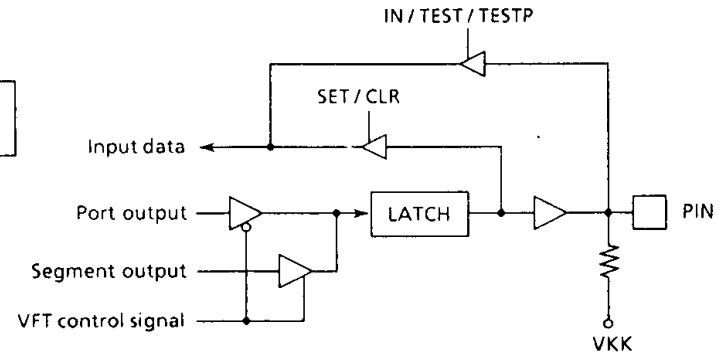


Figure 2-4. Port R5

R3 port (Port address OP03 / IP03)

3	2	1	0
R33 (G12)	R32 (G13)	R31 (G14)	R30 (G15)

RA port (Port address OP0A / IP0A)

3	2	1	0
RA3 (G8)	RA2 (G9)	RA1 (G10)	RA0 (G11)

RB port (Port address OP0B / IP0B)

3	2	1	0
RB3 (G4)	RB2 (G5)	RB1 (G6)	RB0 (G7)

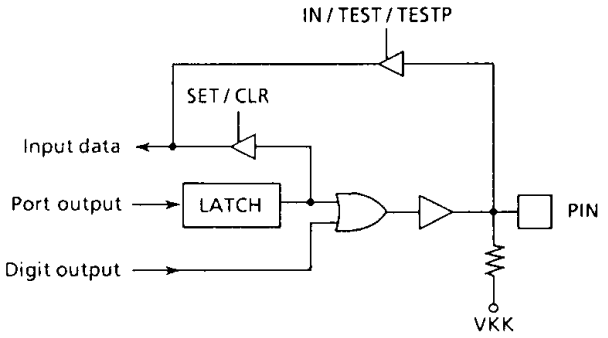


Figure 2-5. Ports R3, RA, RB

2.1.2 Port (G/S) for driving VFT

The G/S port is a digit/segment output port for driving VFT. Output instructions for the G/S port are not possible. The display control and display mode setting command registers (OP1A, OP1B) determine whether this port is used for segment output or digit output. The latch is initialized to "0" during reset.

Port G/S

3	2	1	0
G3 (S15)	G2 (S14)	G1 (S13)	G0 (S12)

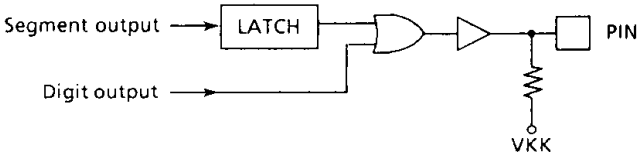


Figure 2-6. Port G/S

2.1.3 Power supply pin for driving VFT

The 28 pins of the R3, P4, R5, RA, RB, PC and G/S ports are P-channel open drain construction with pull-down resistor. Each pin is connected to a VKK pin via a pull-down resistor (TYP. 80kΩ) . Thus, Vacuum Fluorescent Tubes (VFT) can be driven by applying a negative (–) voltage (– 35V max) to the VKK pin, without using external resistor.

Port Address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p,b	SET @L CLR @L TEST @L
00_H	K0 input port (A/D conversion input)	P0 output port Note2 (D/A converter output)	○	○	○	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○	○	○	–
02	P2 output latch	P2 output port	○	○	○	○Note3	○	○	–
03	R3 input port	R3 output port	○	○	○	–	○	○	–
04	P4 output latch	P4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RA input port	RA output port	○	○	○	–	○	○	–
0B	RB input port	RB output port	○	○	○	–	○	○	–
0C	PC output latch	PC output port	○	○	○	–	○	○	–
0D	REMO-CON count value	REMO-CON offset value	○	○	○	–	–	–	–
0E	SIO, power saving operation status	REMO-CON control	○	○	○	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	$\overline{HOLD}$ Pin Status	Hold operation mode control	○	○	–	–	–	–	–
11	——	——	–	–	–	–	–	–	–
12	——	A/D converter input control	–	○	–	–	–	–	–
13	SK0, DTB Status	K0 port input selector, DTB	○	○	–	–	–	–	–
14	——	——	–	–	–	–	–	–	–
15	——	Watchdog timer control	–	○	–	–	–	–	–
16	——	System clock control	–	○	–	–	–	–	–
17	——	PWM buffer selector	–	○	–	–	–	–	–
18	——	PWM transmission buffer	–	○	–	–	–	–	–
19	——	Interval timer interrupt control	–	○	–	–	–	–	–
1A	VFT status input	VFT drive control	○	○	–	–	–	–	–
1B	——	Setting of VFT display mode	–	○	–	–	–	–	–
1C	——	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	——	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	——	Serial interface control 1	–	○	–	–	–	–	–
1F	——	Serial interface control 2	–	○	–	–	–	–	–

Note1. "——" means the reserved state. Unavailable for the user program.

Note2. As concerns the port address "00", IN and TEST instruction operate portK0, and OUT instruction operate portP0.

Note3. The 5-8 bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Table 2-1. Port Address Assignments and Available I/O Instructions

2.2 VFT Controller/Driver Circuit

The 47C1270/1670 have the high breakdown voltage output buffer that directly drive the Vacuum Fluorescent Tubes (VFT) and its control circuit.

2.2.1 VFT Controller/Driver Function

① Twenty-eight high breakdown voltage output buffers are built in.
- Digit output 12 (G4-G15)
- Segment output 12 (S0-S11)
- Digit/segment output 4 (G0 / S12-G3 / S15)

There is also the VKK pin used for the VFT drive power supply.

② The dynamic lighting system makes it possible to select *n* segment x *m* digits by program.
- $n = 1\text{-}12 + i$, $m = 1\text{-}16 - i$ ($i = 0\text{-}4$)

③ Pins not used for VFT drive can be used as general-purpose ports (excluding port G/S).

④ Display data are automatically transferred to the high breakdown voltage output buffer.

⑤ A dimmer function enables brightness level adjustment.

⑥ A key scan function makes it possible to utilize segment output pins for key strobe output.

2.2.2 VFT Drive Circuit Configuration

Figure 2-7 shows VFT Drive Circuit

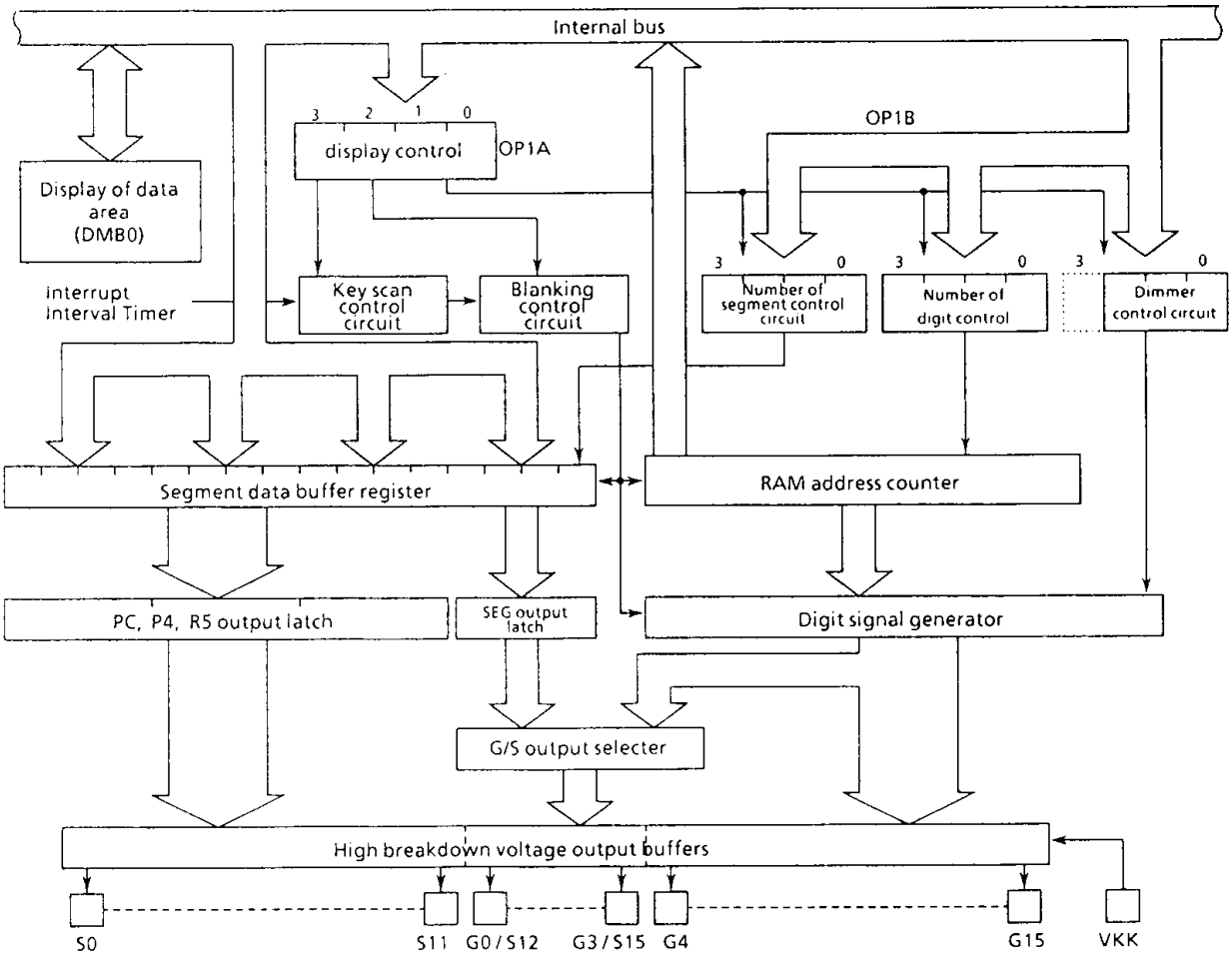
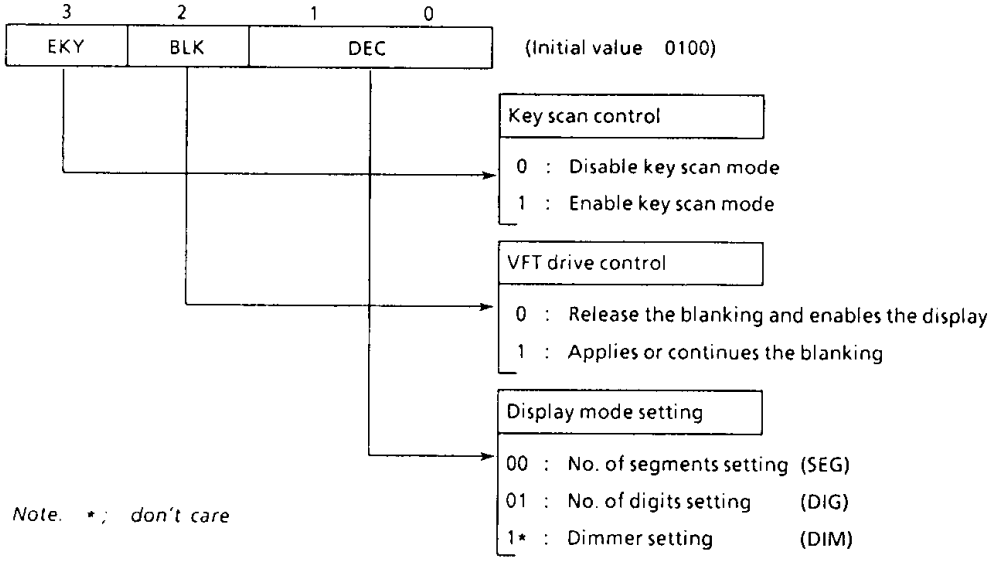


Figure 2-7. VFT drive circuit

2.2.3 Control of VFT drive circuit

VFT drive circuit is controlled by the command register (OP1A and OP1B).
The display mode is set by OP1B after number of segment, number of digit and dimmer time are selected by the lower two bit of OP1A.
Also operation of VFT drive circuit can be monitored by the status register (IP1A).

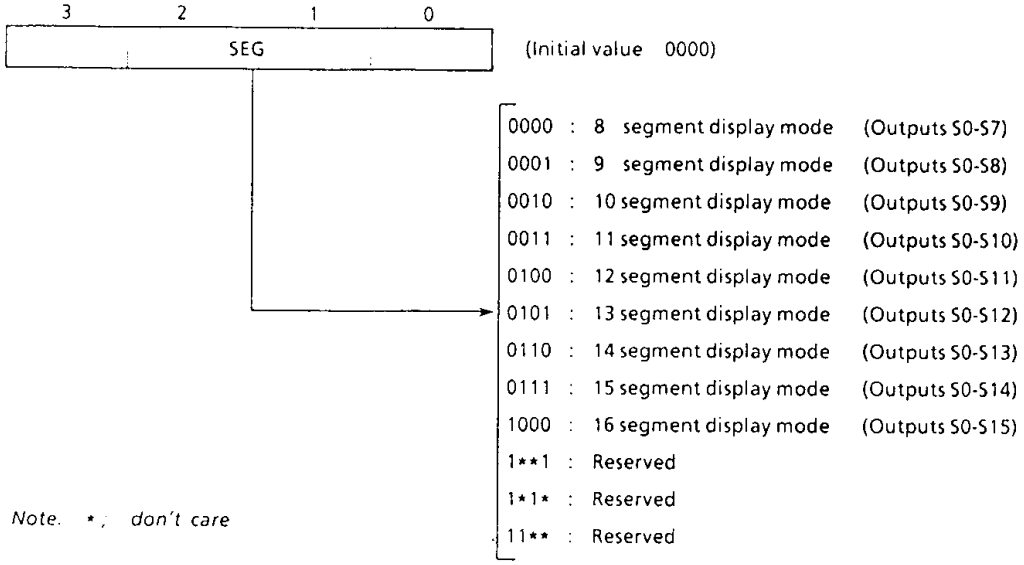
Display control command register (Port address OP1A)



*Note. *; don't care*

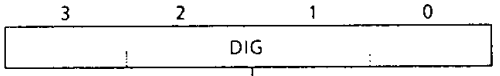
Display mode setting command register (Port address OP1B)

a. Sets number of segments



*Note. *; don't care*

b. Sets number of digits

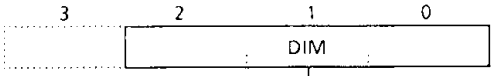


(Initial value 0000)

0000	:	1 digit display	(Output G0 only)
0001	:	2 digits display	(Output G0-G1)
0010	:	3 digits display	(Output G0-G2)
0011	:	4 digits display	(Output G0-G3)
0100	:	5 digits display	(Output G0-G4)
0101	:	6 digits display	(Output G0-G5)
0110	:	7 digits display	(Output G0-G6)
0111	:	8 digits display	(Output G0-G7)
1000	:	9 digits display	(Output G0-G8)
1001	:	10 digits display	(Output G0-G9)
1010	:	11 digits display	(Output G0-G10)
1011	:	12 digits display	(Output G0-G11)
1100	:	13 digits display	(Output G0-G12)
1101	:	14 digits display	(Output G0-G13)
1110	:	15 digits display	(Output G0-G14)
1111	:	16 digits display	(Output G0-G15)

Note. For G/S ports, segment output has priority over digit output ; therefore G0 to G3 are not output if any of 13 to 16 segment display modes is selected.

c. Sets dimmer time (dight output time)

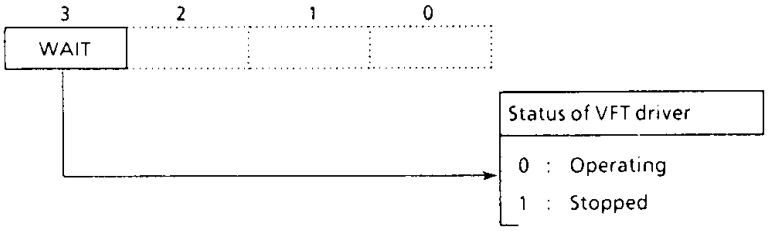


(Initial value *000)

000	:	$(14/16) \times t_{SEG}$ [sec]
001	:	$(12/16) \times t_{SEG}$
010	:	$(10/16) \times t_{SEG}$
011	:	$(8/16) \times t_{SEG}$
100	:	$(6/16) \times t_{SEG}$
101	:	$(4/16) \times t_{SEG}$
110	:	$(2/16) \times t_{SEG}$
111	:	$(1/16) \times t_{SEG}$

Note. t_{SEG} : Normal 2 operation (interval timer input clock ; fs) ..... $2^3/fs$ [sec]
Normal 1 operation and Normal 2 operation (interval timer input clock ; $fc/2^7$) ..... $2^{10}/fc$

VFT drive control status register (Port address IP1A)



(1) Display mode setting

The display mode setting command register (Port address OP1B) is multiplexed for setting the 3 following display modes.

① Number of segments setting
② Number of digits setting
③ Dimmer time setting

Data written to DEC the display control command register (OP1A) determines which of ① to ③ is to be set.

Example : Setting of the display mode to 8 segments, 8 digits, 14/16 t_{SEG}[sec], the key scan function is enabled and display starts.

```
LD      A, #0000B  ;  OP1B ← 0000B (8-segment to display mode is set)
OUT     A, %OP1B
LD      A, #0101B  ;  OP1A ← 0101B (OP1B is set to specify the number of digits)
OUT     A, %OP1A
LD      A, #0111B  ;  OP1B ← 0111B (8-digit display mode is set)
OUT     A, %OP1B
LD      A, #1000B  ;  OP1A ← 1000B (Key scan function is set and display start is
OUT     A, %OP1A      specified)
```

Figure 2-8 shows the pin assignments for the numbers of segments and digits.
If the number of segments is 12 (S0 to S11) , the number of digits can be set to 16 (G0 to G15) . If the number of segments is set to 13 to 16, the number of digits 15 to 12.
When using the 16-segment display mode, the digits are output from G4.
Port G/S (digit/segment) automatically becomes either the segment output pin or digit output pin in accordance with the number of segments set.

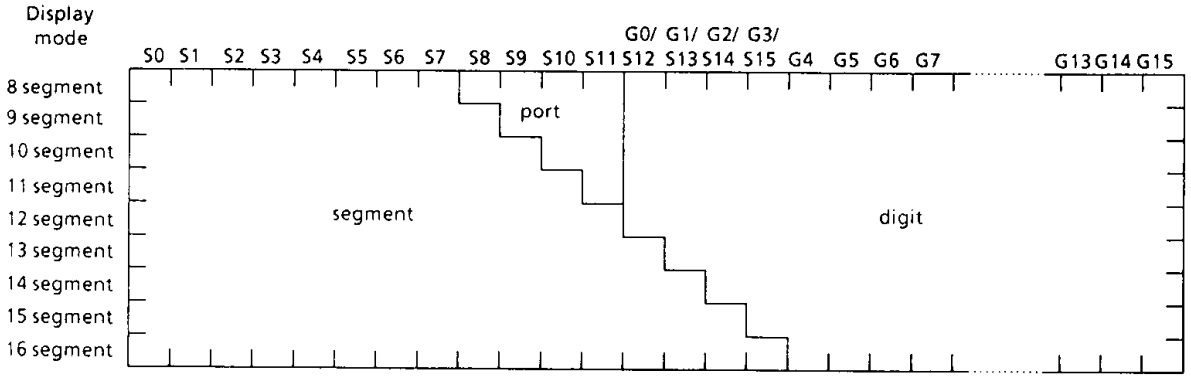


Figure 2-8. Number of segments setting and the pin assignment

(2) Display data setting

Normally, the conversion of data to VFT display data is performed by instruction (mainly using ROM data reference instructions) . Converted display data stored to the display data area are automatically transferred to the VFT drive circuit and output to the high breakdown voltage output buffer. Consequentry, display patterns can be varied by merely changing the data in the display data area.
There is a one-to-one correspondence between the VFT segments (dots) and the bits stored to the display data area of the data memory. A segment lights when the corresponding bit is "1". Sections of the display data area of the data memory not being used for VFT data are used as normal data memory.
The display data area is normally located as RAM addresses shown in Figure 2-9 (a) but, only in the 8-segment display mode, the display data is concentrated as shown is Figure 2-9 (b) for more effective use of the RAM.

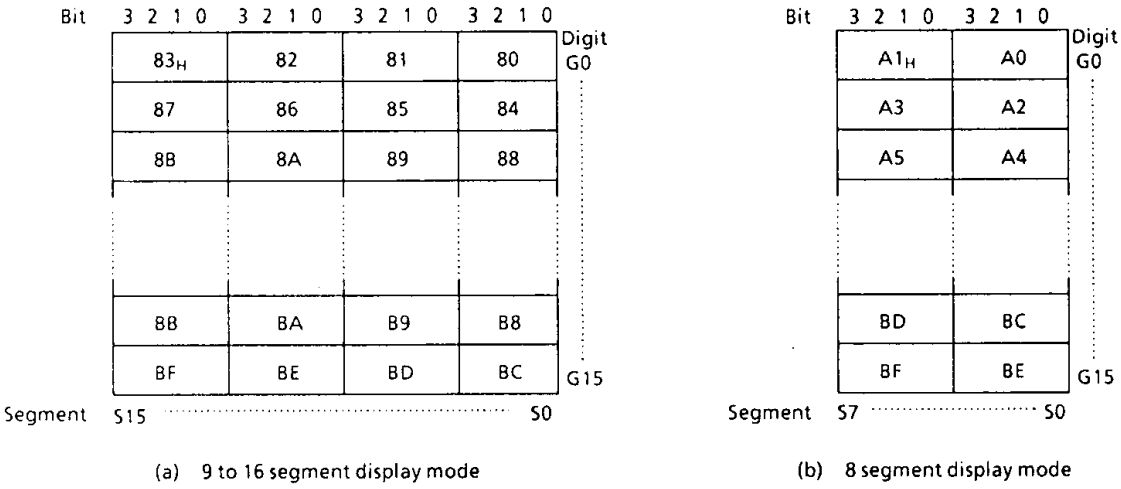


Figure 2-9. VFT display data area (Bank 0)

2.2.4 Display operation

Requests for transfer of display data from the VFT drive circuit are sent to the CPU. After execution of an instruction is completed (after completion of timer/counter processing, or receiving of an interrupt) , the CPU sends the segment data in the display data area to the driver, and this operation is performed in one instruction cycle. The display data area (Bank 0) is accessed automatically even when DMB is held at "1". The data transfer cycle occurs while the VFT drive circuit is the operating status (BLK = 0). The data transfer cycle is inserted at a maximum frequency of once per $(2^8/fc) \div (2^3/fc)$ or once per $(2/fs) \div (2^3/fc)$ instruction cycle. During operation with fc = 4.19 MHz and fs = 32.8KHz, instruction is at the rate of once per cycle of 32 instructions. Figure 2-10 shows the VFT drive waveform.

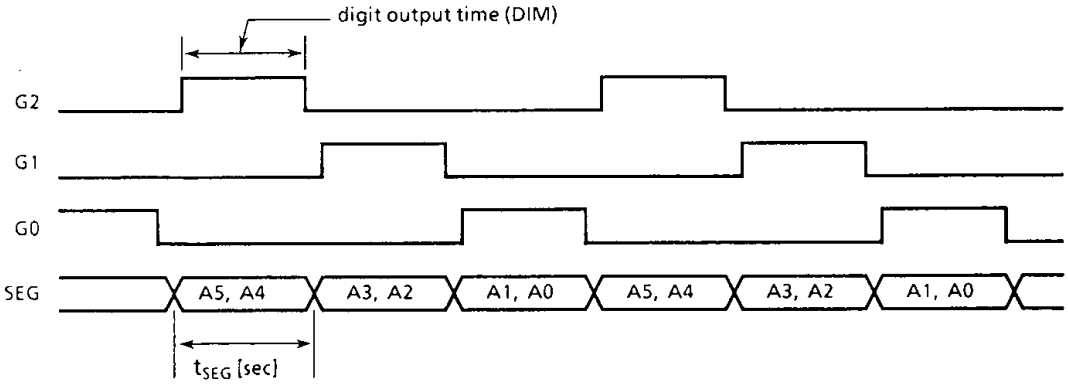


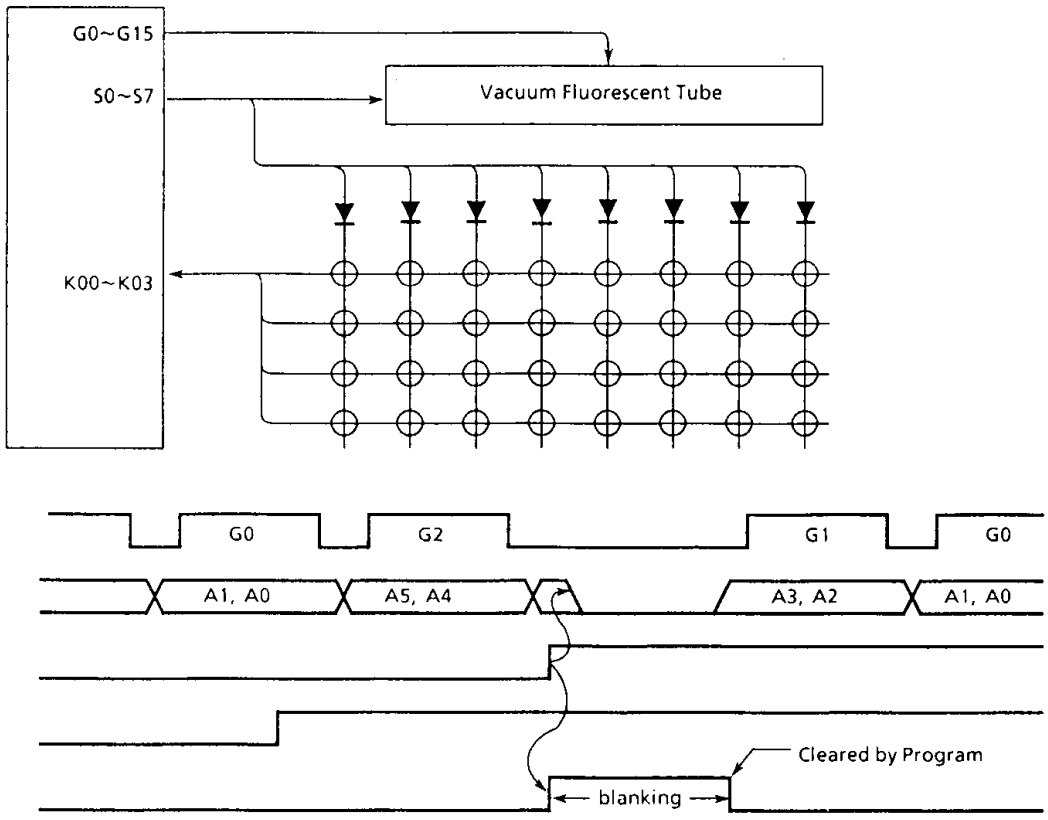
Figure 2-10. VFT drive waveform (3 digit display)

2.2.5 Key scan Function

During display, data output from the segment output pin by instruction is disabled by the hardware but use is possible for the key strobe.

If a program writes "1" to EKY of the display control command register, BLK for that register synchronoized with an interval timer interrupt request is automatically set to "1" and the display is blanked. Segment output pins can be accessed by instructions during blanking ; therefore, key scan is

possible by entering the key scan program in the interval timer interrupt service routine.
When EKY is set to "1", however, blanking results when an interval timer interrupt request is generated even when, for example, the receiving of interrupts is disabled by the interrupt enable master F/F (EIF). Ports not being used for segment output can be used as normal ports but caution is necessary because the output latch is cleared to "0" by the blanking.
The interval timer interrupt frequency varies depending on the key reading speed required and the display quality but, normally, 512Hz or 128Hz (when fc = 4.19MHz) is approriate. Blanking continues until BLK is set to "0" by the interrupt service routine and the display is restarted with the next data transfer cycle after clearing.



Note. *In case of blanking time is set as 1-digit, clear BLK under less than (14/16) × tseg ÷ (2^3/fc) instruction cycle after the ITMR interrupt request*

Figure 2-11. The example of thirty-two matrix configuration and key scan timing

2.2.6 Port Function

(1) Hight breakdown voltage buffer
When a Vacuum Fluorescent Tube is being driven, the port output latch is cleared to "0" . The port output latch is initialized to "0" during reset (the G/S port cannot be accessed by instructions because it is the vacuum fluorescent tube drive port) .
When using as a normal input/output pin, caution is required because of being pulled down to the VKK pin voltage internally.

a. During output
The pins are brought to the VKK pin voltage by the built-in pulldown resistor for "L" level output ;
consequently, as shown in Figure 2-12, diode grounding is necessary to prevent the VKK pin voltage being applied to the external circuitry.

b. During input
The port output latch is cleared to "0" when inputting external data.
The input threshold value is same as for the K0 port but, because of the pulldown to the VKK pin voltage, RK (typ. 80kΩ) must be fully driven.

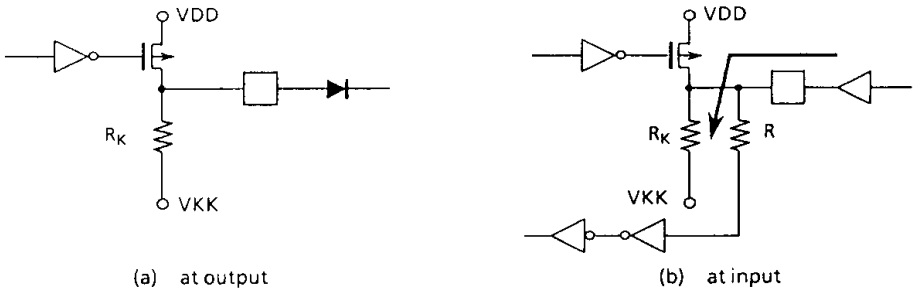


Figure 2-12. Input/Output interface

(2) Low power operation
When switching from the Normal operation (VFT drive is possible) to the SLOW operation or the hold operation, the VFT drive circuit is blanked and the high breakdown voltage port status becomes as follows.

a. Port G/S (digit/segment output)
"0" is output.
b. Ports R3, RA, RB (digit output)
Digit output is cleared to "0" and the latch data ("0" during VFT display) is output.
c. Ports PC, P4, R5 (segment output)
The latch data is cleared to "0" and "0" and "0" is output.

The high breakdown voltage port can also be accessed by instructions during slow operation.

2.3 4bit A/D Conversion (Comparator) Input

The comparator input is analog input to discriminate key input or AFC (Auto Frequency Control) signal. It's composed of 4-bit D/A converter, comparator and control circuit. Analog input level (CIN0-CIN3) can be detected as 16-stage by setting reference voltage.
The comparator input can also be used as K0 port (digital input) . To use as K0 port, set the most significant bit of the port address OP13 to "1".

Note. When the comparator input is selected, the comparator consumes typically 700μA current at VDD = 5V. To reduce the power consumption, K0 port should be set to digital input mode. In the HOLD mode, the comparator current is automatically cut off by hardware.

2.3.1 Circuit of Comparator input

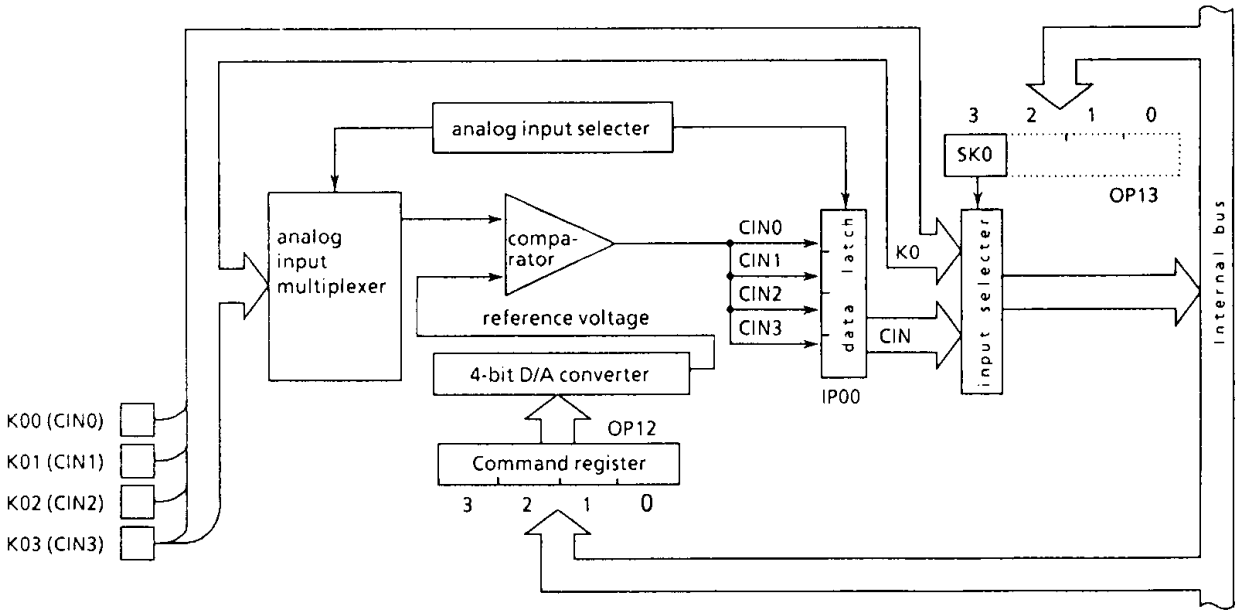


Figure 2-13. Circuit of comparator input

2.3.2 Control of Comparator input

K0 port input selecter command register (port address OP13)

3	2	1	0	
SK0	(DTB)			(Initial value 011*)

0 : CIN comparator input
1 : K0 digital input

K0 port input selecter Status register (port address IP13)

3	2	1	0
SSK0	(SDTB)		0

0 : CIN comparator input
1 : K0 digital input

Figure 2-14. Command register, Status register

Reference voltage (Vref) is set by command register (port address OP12), and it is determined by the following form.

$V_{REF} = V_{DD} \times (n + 1) / 16$ [V] $(n = 0 \sim 15)$

After initialization sequence, 4-channel comparator inputs continue comparison operation successively.

Since 2-instruction cycles are required to complete comparison of 1-channel, it is necessary to wait for 8-instruction cycles after setting a reference voltage, and then read the port address IP00.

When analog input voltage is higher than reference voltage, comparator data latch is set to "1".

At the initialization sequence, OP12 is set to "0".

There is not latch when used to port K0.

OP12				Vref. [V]
3	2	1	0	
0	0	0	0	0.31
0	0	0	1	0.62
0	0	1	0	0.94
0	0	1	1	1.25
0	1	0	0	1.56
0	1	0	1	1.87
0	1	1	0	2.19
0	1	1	1	2.50
1	0	0	0	2.81
1	0	0	1	3.12
1	0	1	0	3.44
1	0	1	1	3.75
1	1	0	0	4.06
1	1	0	1	4.37
1	1	1	0	4.69
1	1	1	1	5.00

Table 2-2. Reference Voltage

2.4 D/A conversion (Pulse Width Modulation) Output Circuitry PWM

The 47C1270/1670 has one 14-bit resolution pulse width modulation ($\overline{PWM}$) output channel which can easily be used for D/A converter output by connecting an external low-pass filter.

$\overline{PWM}$ output is from pin P00 (PWM), which is used for both $\overline{PWM}$ and P00 output. The P00 output latch should be set to "1" when this pin is used for PWM output.

$\overline{PWM}$ output is controlled by the buffer selector (OP17) and the data transfer buffer (OP18). PWM data written to the data transfer buffer can be sent to the PWM data latch by writing "C_H" to the buffer selector to switch to $\overline{PWM}$ output. PWM data transferred to the PWM data latch remain intact until overwritten.

The resetting and holding operations clear the buffer selector, data transfer buffer and PWM data latch to "0" ($\overline{PWM}$ outputs is "H" level).

2.4.1 Circuitry Configuration

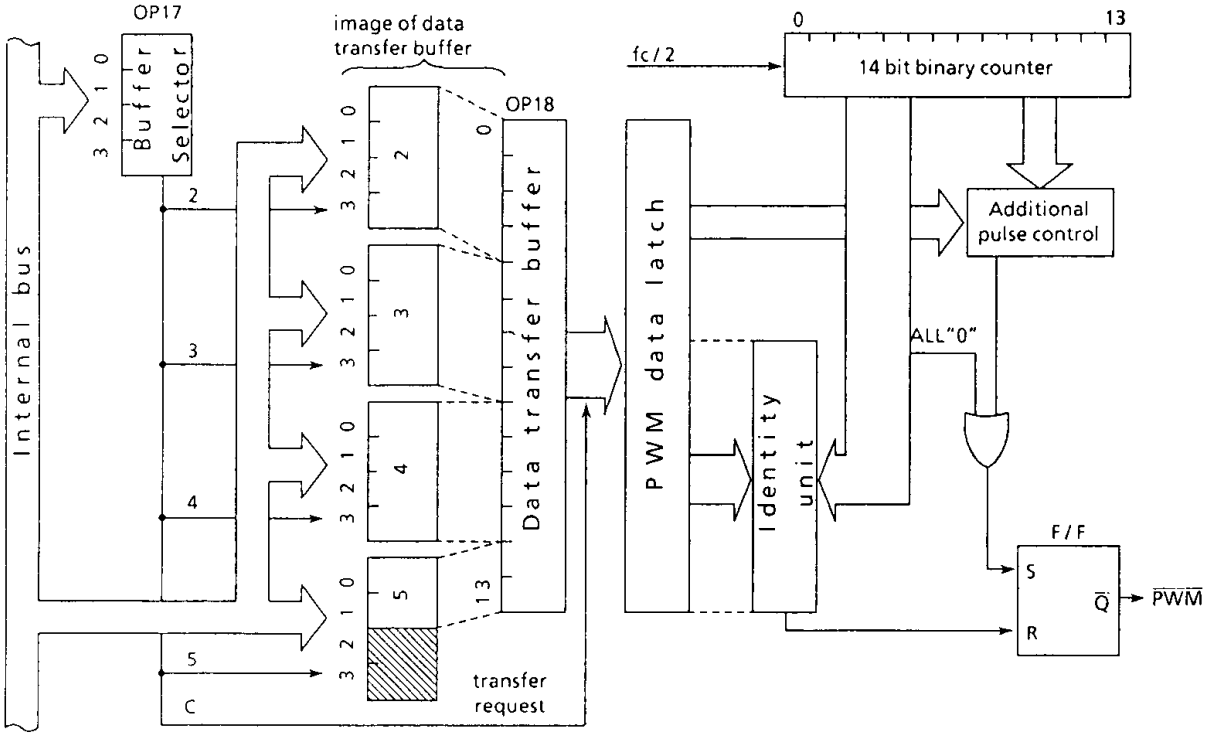


Figure 2-15. Pulse Width Modulation

2.4.2 Pulse Width Modulation Wave form

$\overline{PWM}$ output is a 14-bit resolution pulse output and one cycle is $T_M = 2^{15}/fc$ (8192μsec. when fc = 4MHz).

The upper 8 bits of the PWM data latch control the pulse width of the pulse output with a cycle T_S ($T_S = T_M/64$).

The low level pulse has a pulse width of $n \times t_0$ ($t_0 = 2/fc$) with a cycle T_S when the 8-bit data are n ($n = 0$ to 255).

The lower 6 bits control the position where the additional pulses with width t_0 are output in the 64 intervals T_S (i) (i = 0 to 63) of the TM cycle. The low level pulse width is $(n + 1)\ t_0$ during the interval where the additional pulses are output. The additional pulses are output at m points in the 64 intervals T_S (i) when the 6-bit data are m ($m = 0$ to 63). Figure 2-16 shows the $\overline{PWM}$ output timing and Table 2-3 shows the relationship between the 6-bit data and the intervals where the additional pulses are output.

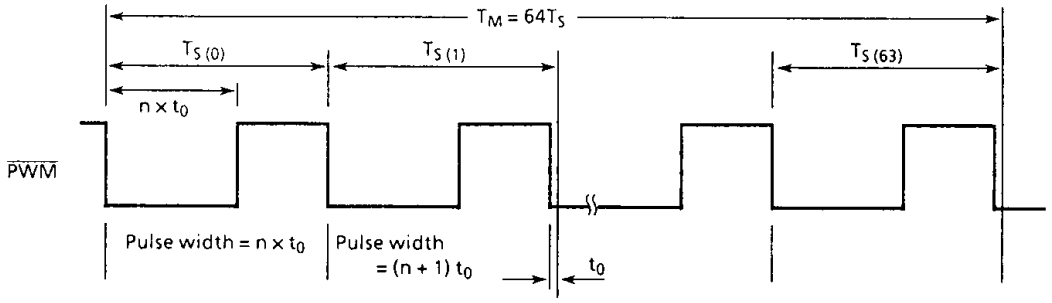


Figure 2-16. $\overline{PWM}$ output timing (It is shown to the additional pulse T_S (1) and T_S (63))

Bit position of 6 bits data	Relative position of TS where the additional pulse is generated (No i of TSi (0<i<63) is listed)
Bit 0	32
Bit 1	16, 48
Bit 2	8, 24, 40, 56
Bit 3	4, 12, 20, 28, 36, 44, 52, 60
Bit 4	2, 6, 10, 14, 18, 22, 26, 30, ·····, 58, 62
Bit 5	1, 3, 5, 7, 9, 11, 13, 15, 17, ·····, 59, 61, 63

Note. When corresponding bit is "1", it is output.

Table 2-3. Correspondence between 6 bits data and the additional pulse generated T_S periods

2.4.3 Control of pulse width modulation circuit. (Data transfer)

$\overline{PWM}$ output is controlled by writing the output data to the data transfer buffer (OP18). The output data are written in selections using the buffer selector (OP17). In the data transfer buffer, the respective sections of data are assigned buffer numbers and written as indicated in Table 2-4.

① The buffer number of the buffer to which the data are to be written is written to the buffer selector (OP17).

② The corresponding PWM data are written to the selected buffer.

③ The output data are written to the transfer buffer by repeating the operations in items ① and ② above.

④ When writing is completed, "C" is written to the buffer selector by program.

While the output data are being written to the transfer buffer, the previous PWM data are being output. When "C" is written to the buffer selector, the output data are sent to the PWM data latch and $\overline{PWM}$ output is enabled.

The time from when "C" is written the buffer selector until $\overline{PWM}$ output is enabled is $2^{15}/fc$ (8192μsec. at 4MHz) maximum.

Buffer number (OP17)	Corresponding bit (OP18)	
2	Bit of transfer buffer	0 ~ 3
3	〃	4 ~ 7
4	〃	8 ~11
5	〃	12 ~13
C	Nothing	

Table 2-4. Correspondence between the buffer number of the data transfer buffer and bit

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	R7 port, XOUT	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	P0 - P2, R6, R8, R9 port	− 0.3 to 10	
	V_{OUT3}	Sourse open drain pin	− 35 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P1, P2 port	30	mA
	I_{OUT2}	P0, R6 - R 9port	3.2	
	I_{OUT3}	P4, R5, PC port	− 12	
	I_{OUT4}	R3, RA, RB, G / S port	− 25	
Output Current (Total)	ΣI_{OUT1}	P1, P2 port	120	mA
	ΣI_{OUT3}	P4, R5, PC port	− 80	
	ΣI_{OUT4}	R3, RA, RB, G / S port	− 100	
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperatuer (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, Topr = − 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the SLOW mode	2.7		
			in the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	KHz

Note . Input Voltage VIH3, VIL3 : In the SLOW mode or HOLD mode

D.C. CHARACTERISTICS (V_{SS} = 0V, Topr = – 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	K0port, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Open drain R port					
Input Resistance	R_{IN1}	KO port with pull-up/pull-dwon		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Pull-down Resistance	R_K	Sourse open drain	V_{DD} = 5.5V, V_{KK} = – 30V	—	80	—	
Output Leakage Cnrrent	I_{LO1}	Sink open drain port	V_{DD} = 5.5V, V_{IN} = 5.5V	—	—	2	μA
	I_{LO2}	Source open drain port	V_{DD} = 5.5V, V_{OUT} = – 32V	—	—	– 2	
Output High Voltage	V_{OH}	P4, R5, PC port	V_{DD} = 4.5V, I_{OH} = – 5mA	2.4	—	—	V
Output Low Voltage	V_{OL}	P0, R6~R9 port	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Output High current	I_{OH}	R3, RA, RB, G / S port	V_{DD} = 4.5V, V_{OH} = 2.4V	—	– 15	—	mA
Output Low current	I_{OL}	P1, P2 port	V_{DD} = 4.5V, V_{OL} = 1.0V	—	20	—	mA
Supply Current (In the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	—	3	6	mA
Supply Current (In the SLOW mode)	I_{DDS}		V_{DD} = 3.0V, fs = 32.768KHz	—	30	—	μA
Supply Current (In the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1: Typ. values show those when Topr = 25°C, VDD = 5V.

Note 2: Input Current I_{IN1}, I_{IN2} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: IDD, IDDH; VIN = 5.3V/0.2V
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.
IDDS; VIN = 2.8V/0.2V, low frequency clock is only oscillated (connecting XTIN,XTOUT). The comparator input is disable. The current through pull-down resistor of souce open drain port is not included.

A / D CONVERSION CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, Topr = – 40 to 70°C)

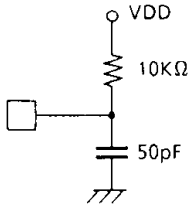
PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Input Voltage range	V_{AIN}	CIN3 - CIN0		V_{SS}	—	V_{DD}	V
Error				—	—	$\pm\frac{1}{2}$	LSB

A.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, Topr = – 40 to 70°C)

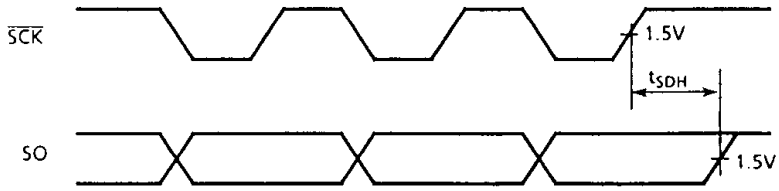
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	1.33	—	20	μs
		in the SLOW mode	235	—	267	
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	—	—	ns
Low level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	—	—	ns

Note . Shift Data Hold Time

External circuit for $\overline{SCK}$ pin and SO pin.

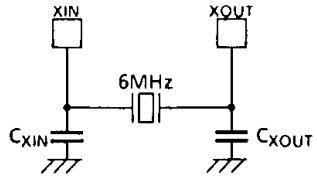


Serial Port (completion of transmission)

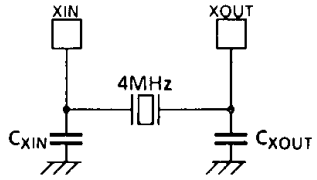


RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70°C)

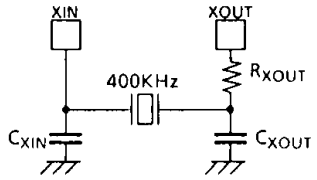
(1) 6MHz
Ceramic Resonator
CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF



(2) 4MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF

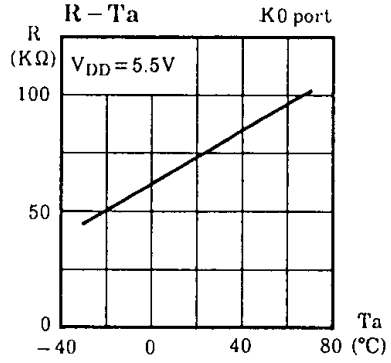


(3) 400KHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

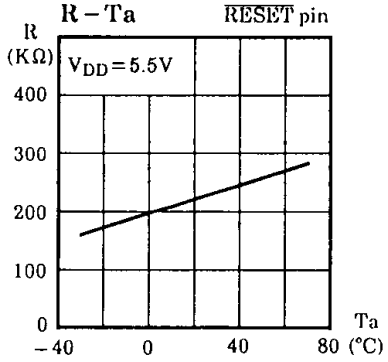


TYPICAL CHARACTERISTICS

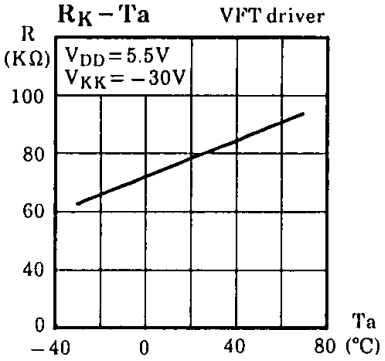
R – Ta K0 port



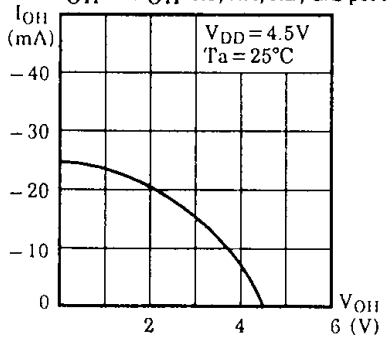
R – Ta RESET pin



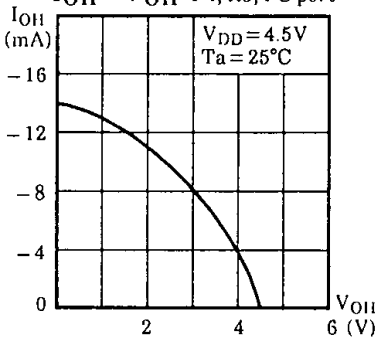
R_K – Ta VFT driver



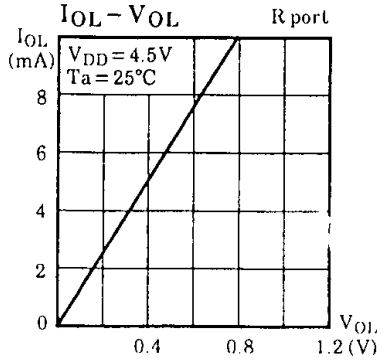
I_{OH} – V_{OH} R3, RA, RB, G/S port



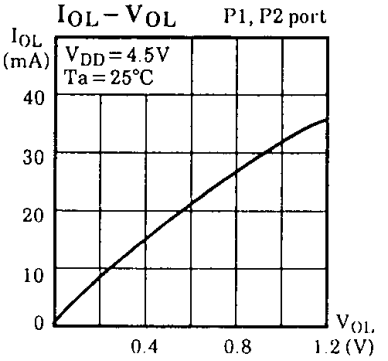
I_{OH} – V_{OH} P4, R5, PC port



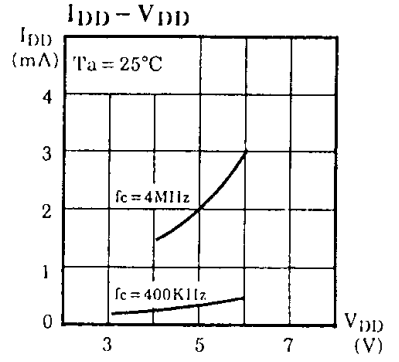
I_{OL} – V_{OL} R port



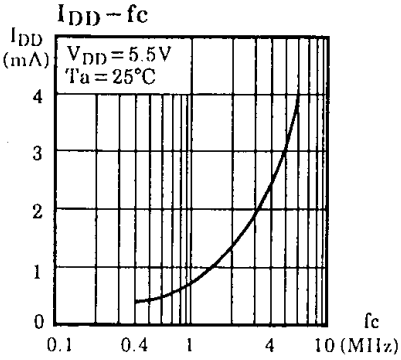
I_{OL} – V_{OL} P1, P2 port



I_{DD} – V_{DD}



I_{DD} – fc



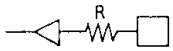
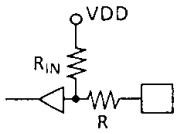
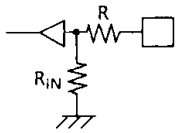
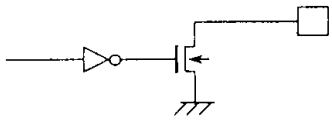
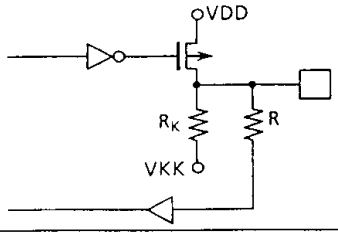
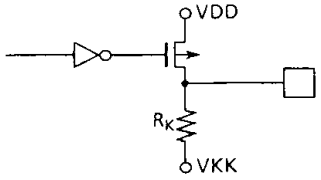
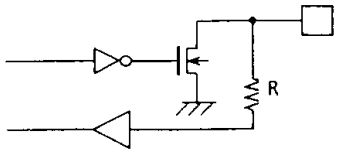
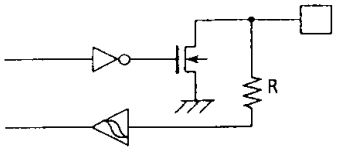
INPUT/OUTPUT CIRCUITRY

(1) control pins

Input/Output circuitries of the 47C1270/1670 control pins are similar to the 47C1260/1660.

(2) I/O ports

The input/output circuitries of the 47C1270/1670 I/O ports are shown below, any one of the circuitries can be chosen by code (MA, MB, MC) as a mask option.

PORT	I/O	Input/Output Circuitry (Code)			REMARKS
		MA	MB	MC	
K0	Input				Pull-up/ Pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P0 P1 P2	Output				Sink open drain output Initial "Hi-Z" High drive current (P1, P2) I_{OL} = 20mA (typ.)
R3 R5 RA RB	I/O				Source open drain output Initial "Hi-Z" High-breakdown voltage R_K = 80KΩ (typ.) R = 1KΩ (typ.)
P4 PC G/S	Output				Source open drain output Initial "Hi-Z" High-breakdown voltage R_K = 80KΩ (typ.)
R6 R7	I/O				Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	Output				Sink open drain output Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)

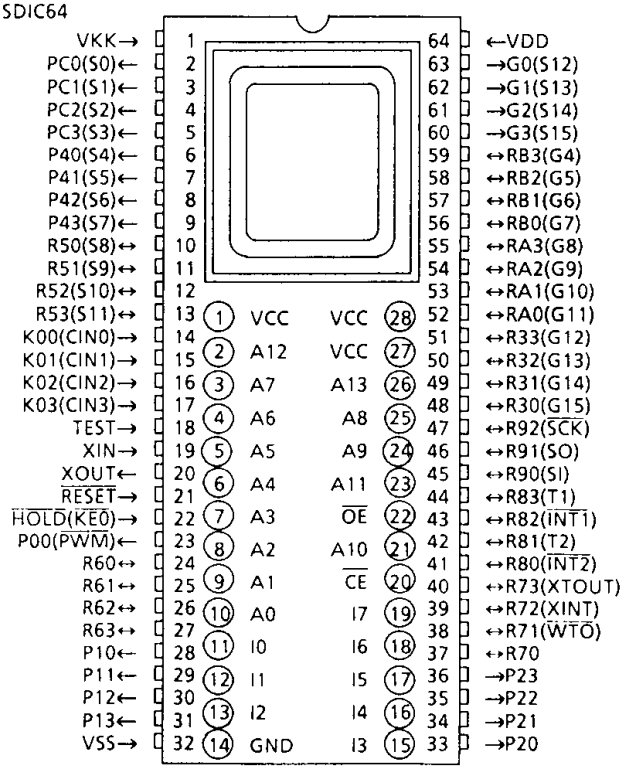
CMOS 4-BIT MICROCONTROLLER

TMP47C007E

The 47C007, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C1270/1670 application systems (programs).
The 47C007 is pin compatible with the 47C1270/1670 which are mask-programed ROM devices.

PIN ASSIGNMENT (TOP VIEW)

SDIC64



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A13 - A0	Output	Program memory address output
I7 - I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5to6.0V	–	–	150	ns
Data Setup Time	t_{IS}	C_L = 100pF	150	–	–	ns
Data Hold Time	t_{IH}	Topr = – 40to70°C	50	–	–	ns

NOTES FOR USE

(1) Program memory

The program area are as shown in Figure1.

When this chip is used as evaluator of the 47C1270, data conversion table for [OUTB @HL] instruction must be allocated at two areas and they must be the same contents as shown in Figure1.

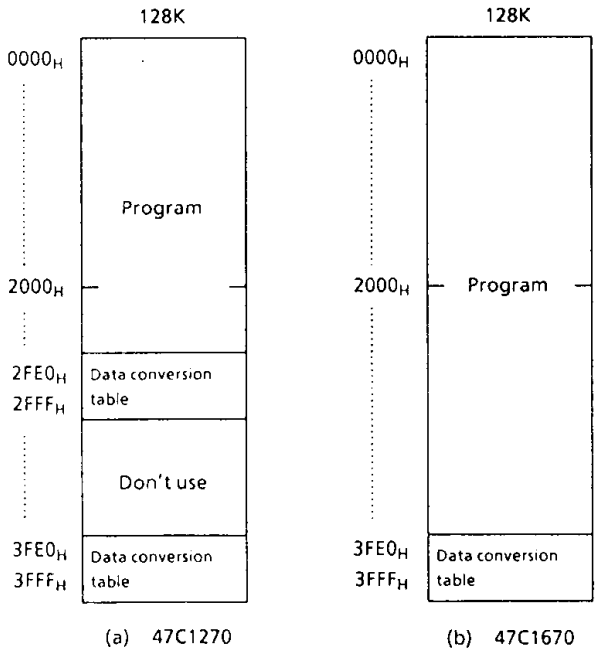


Figure 1. Program area

(2) Data memory

47C007 contains three 256 x 4-bit data memory banks (bank 0, bank 1 and bank 2).

(3) I/O ports

Input/Output circuitries of I/O ports in the 47C007 are similar to the code MA of the 47C1270/1670. When this chip is used as evaluator with other I/O code (MB and MC), it is nacessary to provide the external resistors (See Figure 2).

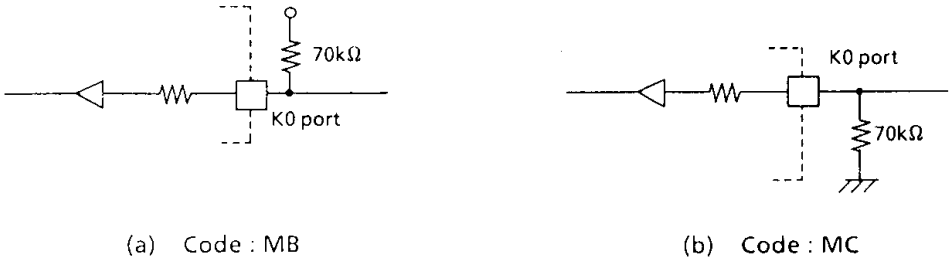


Figure 2. I/O code and external circuitry