CMOS 4-BIT MICROCONTROLLER

TMP47C25N
TMP47C25F

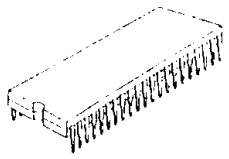
The 47C25 is a high performance 4-bit single chip microcomputer based on the TLCS-47 CMOS series with a DTMF generator and a large capacity RAM for repertory dialing applications, and which is suitable for utilization in telephones. The 47C25 is also capable of operation with low voltages such as those supplied by telephone line.

PART No.	ROM	RAM	PACKAGE
TMP47C25N	2048 x 8-bit	384 x 4-bit	SDIP42
TMP47C25F			QFP44

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 8.3μs (at 1.929MHz)
- ◆Low voltage operation : 2.5V min.
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All source have independent latches each, and multiple interrupt control is available.
- ◆I/O port (32 pins)
  - Input 2 ports 5 pins
  - I/O 7 ports 27 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with 4-bit buffer
  External/internal clock, and leading/trailing edge shift mode
- ◆DTMF (Dual Tone Multi Frequency) Output
  - DTMF output with one instruction
  - Single tone output function
- ◆RAM for repertory dial : 384 x 4 bits max.
- ◆Hold function
  - Battery/Capacitor back-up
  - Hold function is controlled by port K0.
- ◆Real Time Emulator: BM47215A

SDIP42



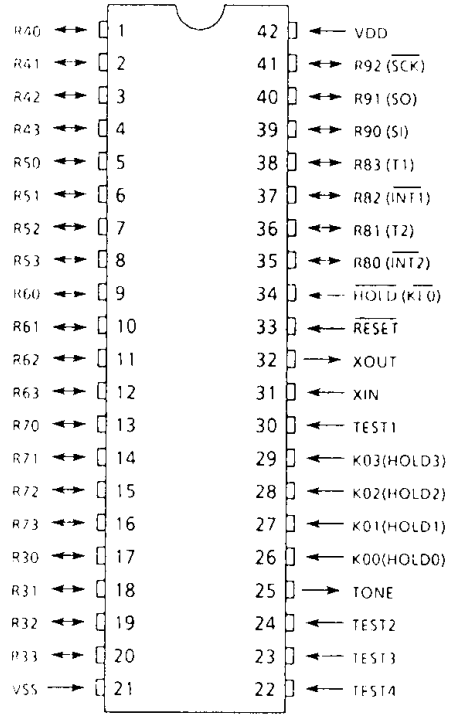
TMP47C25N

QFP44

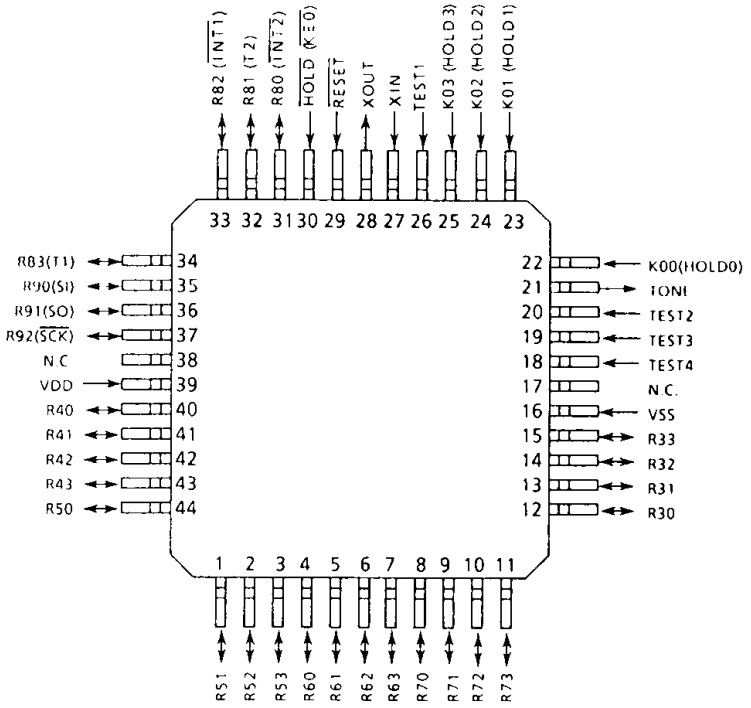
TMP47C25F

PIN ASSIGNMENTS (TOP VIEW)

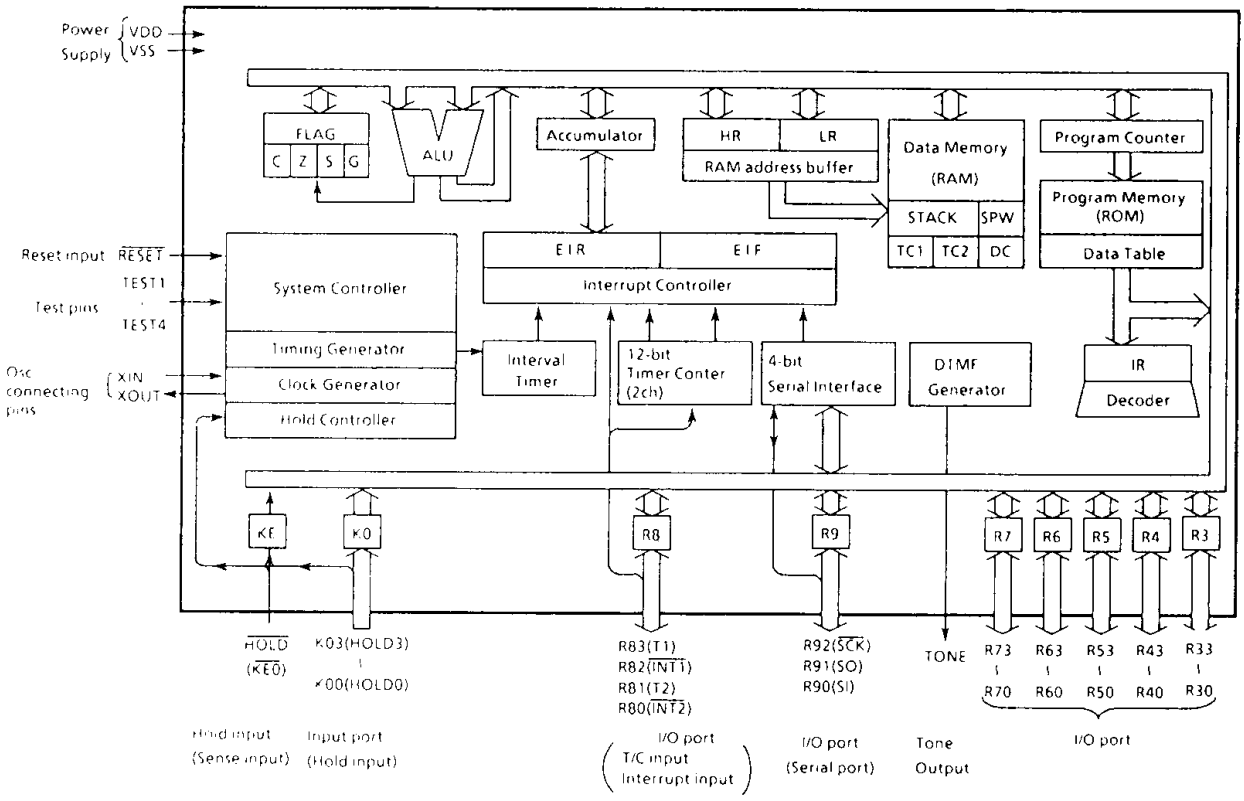
(1) SDIP42



(2) QFP44



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (HOLD3) - K00 (HOLD0)	Input (Input)	4-bit input port	Hold request/release signal input (Active "H")
R33 - R30	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R43 - R40			
R53 - R50			
R63 - R60			
R73 - R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or Timer/Counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
TONE	Output	Tone output	
XIN	Input	Resonator connecting pins.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input	Hold request/release signal input	Sense input
TEST4-TEST1	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+2.5 to 6.0V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C25, the configuration and functions of hardwares are described.
As the description has been provided with priority on those parts differing from the 47C200A, the technical data sheets for the 47C200A shall also be referred to.
The instruction cycle of the 47C25 is different from the 47C200A. One instruction cycle is composed of 16 basic clocks in the 47C25, but 8 basic clocks in the 47C200A. And so, the instruction execution time of the 47C25 is twice as the 47C200A.

1. SYSTEM CONFIGURATION

(1) Data Memory
(2) I/O Ports
(3) DTMF Generator
(4) Hold Controller

2. INTERNAL CPU FUNCTION

2.1 Data Memory

The 47C25 data memory includes the RAM (384 x 4-bit). First 128 x 4-bit RAM is the same as the data memory of the 47C200A. Extended 256 x 4-bit RAM is mainly used for storing repertory dialing data and is controlled by the RAM address register, RAM data buffer register and RAM command register.

(1) RAM (256 x 4-bit) Command Register

The RAM command register (OP0D/IP0D) controls the reading or writing of data, and whether RAM is to be accessed or put in stand-by mode.
In the stand-by mode, RAM consumes a minimum quantity of power.

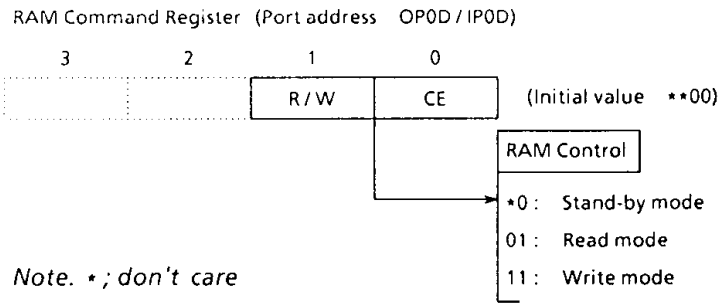


Figure 2-1. RAM Command Register

(2) RAM (256 x 4-bit) Address Register

The RAM address register is an 8-bit register to specify addresses for the RAM, and initialized to "0" during reset. The upper 4 bits are accessed with port address OP0B or IP0B and the lower 4 bits are accessed with port address OP0A or IP0A.

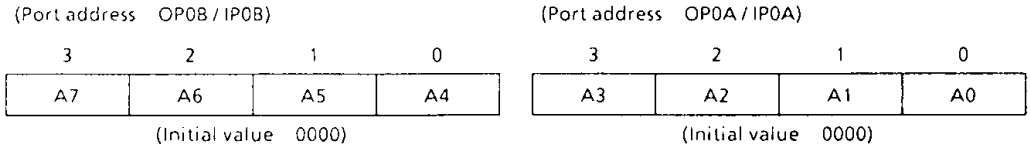


Figure 2-2. RAM Address Register

(3) RAM (256 x 4-bit) Data Buffer Register

The RAM data buffer register is a 4-bit register to read or write RAM data. When writing data to RAM, access is by means of port address OP0C. Port address IP0C is used for access when reading data from RAM.

RAM Data Buffer Register (Port address OP0C / IP0C)

3	2	1	0
D3	D2	D1	D0

Figure 2-3. RAM Data Buffer Register

2.1.1 Access for RAM (256 x 4-bit)

To write data to RAM, load the address into the RAM address register and the data into the RAM data buffer register (OP0C), then put the RAM command register in the write mode. The data will be written to the specified RAM address by this operation. The data are latched in the RAM data buffer register, therefore, RAM data buffer register operation is not necessary when the same data are written continuously.

To read data from RAM, set the RAM command register to read mode and load the address not latched in the RAM data buffer register.

Example 1 : To write data "9" to address 82_H and data "5" to address 83_H in RAM.

```
OUT     #3,  %OP0D    ; Sets RAM to write mode.
OUT     #8,  %OP0B    ; Sets "82H" to RAM address register.
OUT     #2,  %OP0A
OUT     #9,  %OP0C    ; Writes data "9" to RAM.
OUT     #3,  %OP0A    ; Sets "3" to lower 4 bits of RAM address register
OUT     #5,  %OP0C    ; Writes data "5" to RAM.
```

Example 2 : To read data from address $B1_H$ in RAM and store to Acc.

```
OUT     #1,  %OP0D    ; Sets read mode for RAM.
OUT     #0BH,%OP0B    ; Sets "B1H" to RAM address register.
OUT     #1,  %OP0A
IN      %OP0C,A       ; Reads data from RAM and stores to Accumulator.
```

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Ports

The 47C25 has 9 I/O ports (32 pins) each as follows:

① K0 ; 4-bit input(shared with hold request/release signal input)
② R3 ; 4-bit input/output
③ R4, R5, R6, R7 ; 4-bit input/output
④ R8 ; 4-bit input/output (shared with external interrupt input and timer/counter input)
⑤ R9 ; 3-bit input/output (shared with serial port)
⑥ KE ; 1-bit sense input (shared with hold request/release signal input)

The ports K0 and R3 of 47C25 differ from those of the 47C200A. The 47C25 has no output port (P1, P2).
Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port K0 (K03 - K00)

The 4-bit input port with pull-up resistors, shared by hold request/release signal input.

Port K0 (Port address IP00)

3	2	1	0
K03 (HOLD3)	K02 (HOLD2)	K01 (HOLD1)	K00 (HOLD0)

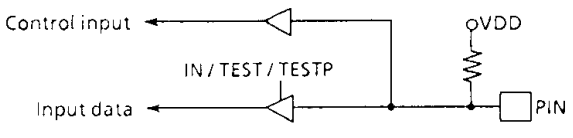


Figure 3-1. Port K0

Port address (**)	Port		Input/Output instructions						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	ROW register	ROW register	○	○	○	○ (Note2)	○	○	–
02	COLUMN register	COLUMN register	○	○	○	–	○	○	–
03	R3 input port	R3 output port	○	○	○	–	○	○	○
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	○
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RAM address register	RAM address register	○	○	○	–	○	○	–
0B	RAM address register	RAM address register	○	○	○	–	○	○	–
0C	RAM data buffer register	RAM data buffer register	○	○	○	–	○	○	–
0D	RAM command register	RAM command register	○	○	○	–	○	○	–
0E	SIO, hold status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	○	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	——	–	–	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial Interface control	–	○	–	–	–	–	–

Note 1. *"——" means the reserved state. Unavailable for the user programs.*

Note 2. *The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ROW register and COLUMN register.*

Table 3-1. Port Address Assignments and Available I/O Instructions

(2) Port R3 (R33-R30)

The 4-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during the reset.

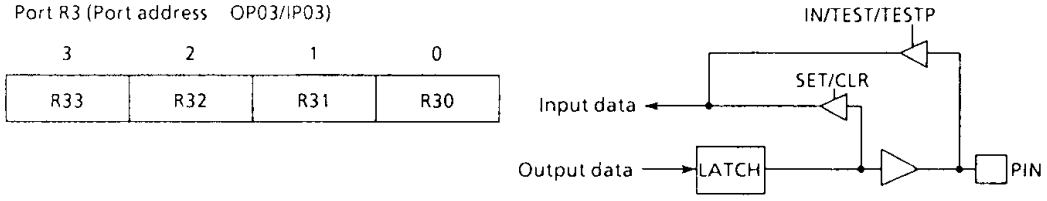


Figure 3-2. Port R3

3.2 DTMF Generator

The 47C25 has a DTMF generator which generates dialing signals for tone dialing type telephones. There are two groups of tone dial signals, one group of 4 sine wave low frequencies and another group of 4 sine wave high frequencies. All of these frequencies can be selected individually and combined with a frequency from the other group for a total of 16 different DTMF composite waves.

(DTMF ; Dual Tone Multi Frequency)

3.2.1 Configuration of DTMF Generator

Figure 3-3 shows configuration of the DTMF generator. The 47C25 generates two stepped, quasi sine waves for tone dial signals which can be combined and output. The high or low group of frequencies is selected by setting frequency selection codes into the ROW and COLUMN registers.

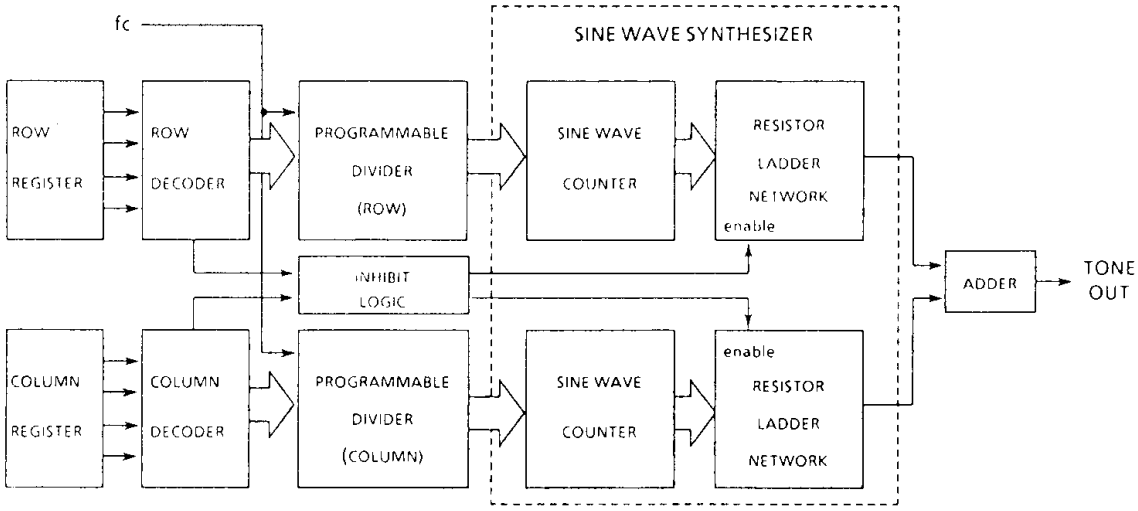
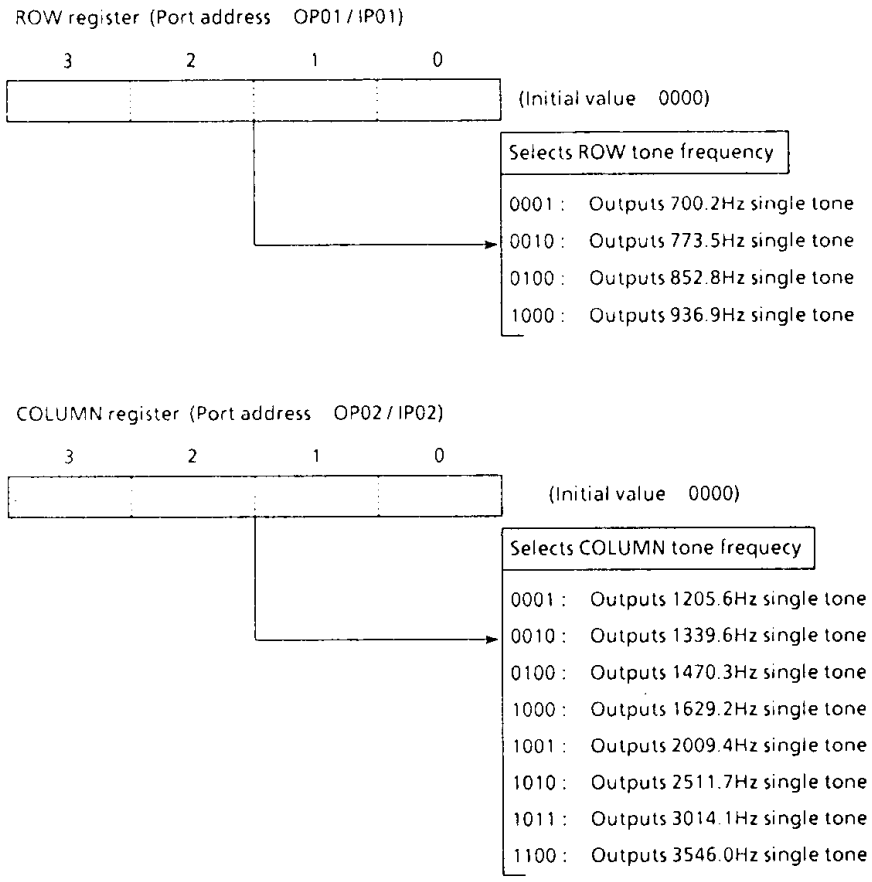


Figure 3-3. DTMF Generator Configuration

3.2.2 Control of DTMF Generator

Tone output controlled by ROW register (OP01/IP01) and COLUMN register (OP02/IP02). Both registers are initialized to "0" during reset.

Tones are output by loading frequency selection codes shown in Figure 3-4 into the ROW and COLUMN regisers. In this case either ROW or COLUMN register is disabled, another register remains to be enabled, and so single tone can be output by loading an ineffective code into the register. The [OUTB @HL] instruction can set 8-bit data into both registers (the upper 4 bits of the ROM data is set to the COLUMN register and the lower 4 bits is set to the ROW register) at the same time, and DTMF signal is output without single tone output.



Note. When the frequency selection codes "1101", "1010", "1011", and "1100" are selected for COLUMN register, the ROW tone is always disabled.

Figure 3-4. ROW, COLUMN Register

Example: 8 bits of data corresponding to the 5 bits of data linking the content of carry flag and the contents of data memory RAM address 90_H are read from the ROM, frequency selection codes are loaded into the ROW and COLUMN registers, and dual tone is output.

```
LD      HL,#90H  ; HL ← 90H(Sets the address of the data memory)
OUTB    @HL      ; Sets the ROM data into ROW and COLUMN register
```

Table 3-2 shows the corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys. Table 3-3 shows the deviation between the 47C25 tone output frequency and standard frequency.

		COLUMN register (OP02 / IP02)		
	Frequency selection code	0001 (1209)	0010 (1336)	0100 (1477)
ROW register (OP01 / IP01)	0001 (697)	1	2	3
	0010 (770)	4	5	6
	0100 (852)	7	8	9
	1000 (941)	*	0	#
		Standard telephone dial key		

Contents of ( ) are standard frequencies, unit : Hz

Table 3-2. Corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys

ROW Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	700.2	697	+ 0.46
0	0	1	0	773.5	770	+ 0.45
0	1	0	0	852.8	852	+ 0.09
1	0	0	0	936.9	941	- 0.44

COLUMN Tone						
0	0	0	1	1205.6	1209	- 0.28
0	0	1	0	1339.6	1336	+ 0.27
0	1	0	0	1470.3	1477	- 0.46
1	0	0	0	1629.2	1633	- 0.23

Table 3-3. Tone output frequencies and deviation from standard

3.2.3 Test mode for tone output

The 47C25 includes a test mode for checking tone output waveforms. Tones can be output by the circuit shown in figure 3-5. ROW data are inputted from the R4 port and COLUMN data are inputted from the R5 port, and any desired single or dual tones can be output by setting the frequncy selection codes shown in Figure 3-4. Figure 3-6 shows a single tone wavefrom and Figure 3-7 shows a dual tone waveform.

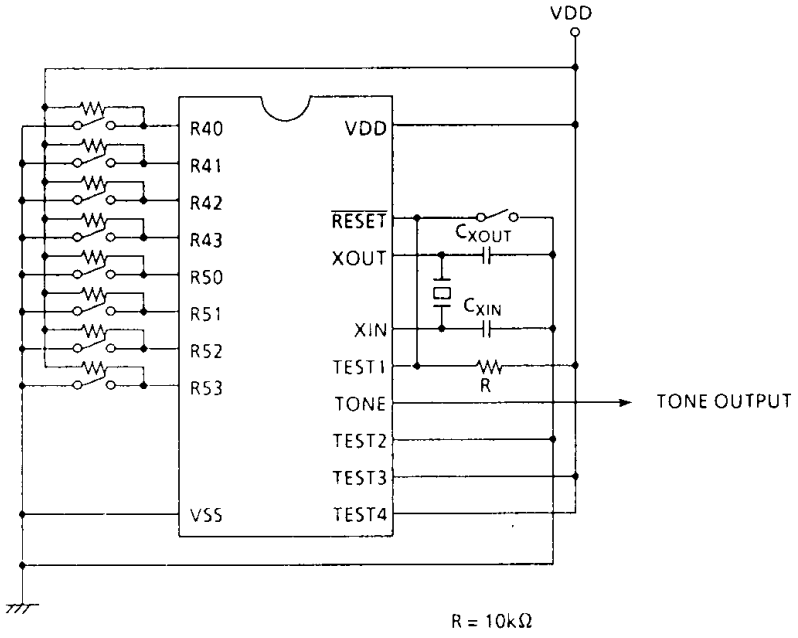


Figure 3-5. Tone test circuit

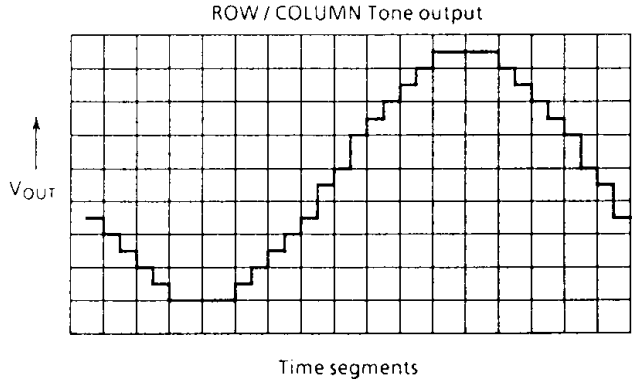


Figure 3-6. Single tone waveform

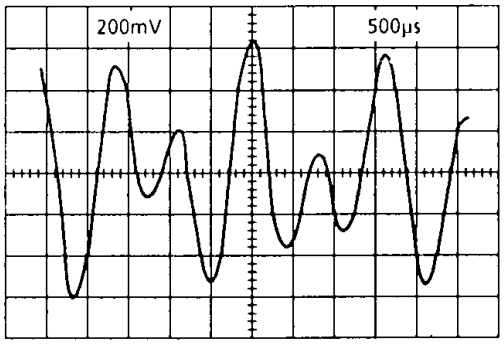


Figure 3-7. Dual tone waveform

4. POWER SAVING FUNCTION

The 47C25 has the hold operating mode intended to save the power.

4.1 Hold Operating Mode

The 47C25 has a $\overline{\text{HOLD}}$ pin and port K0 as hold control pins. Therefore, in the case of port K0 for key inputs, the Hold operating mode can be released by key inputs. Figure 4-1 shows the hold control circuit of the 47C25. Hold operating mode of 47C25 is same as 47C200A, excepting those aforementioned. For details, refer to the technical data sheets for the 47C200A.

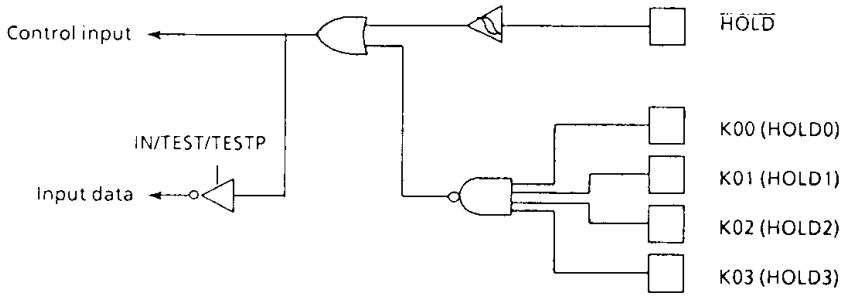


Figure 4-1. Hold control circuit

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
Input Voltage	V_{IN}		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	− 0.5 to 10	
Output Current (Per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 60°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 60	°C

RECOMMENDED OPERATING CONDITION (V_{SS} = 0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	2.5	6.0	V
			in the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc			1.929		MHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the HOLD mode.

D.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.5 to 6.0V, T_{opr} = − 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, $\overline{RESET}$, TEST1 to TEST 4, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Low Current	I_{IL}	Port R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	−	−	− 2	mA
Input Resistance	R_{IN1}	Port K0		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Port R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	± 2	μA
Output High Voltage	V_{OH}	Port R (push-pull)	V_{DD} = 4.5V, I_{OH} = − 200μA	2.4	−	−	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
Supply Current (in the Normal mode)	I_{DD}		Except TONE generating V_{DD} = 2.5V, fc = 1.929MHz	−	0.4	0.5	mA
	I_{DDT}		TONE generating V_{DD} = 2.5V, fc = 1.929MHz	−	1.5	2.5	
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	μA

Note 1. *Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.*

Note 2. *Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained.*

Note 3. *Suply Current : V_{IN} = 2.3V / 0.2V*
The K0 port is open when the pull-up/pull-down resistor is contained.
The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

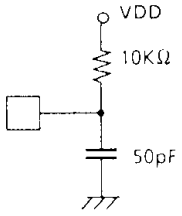
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.5 to 6.0V, T_{opr} = – 30 to 60°C)

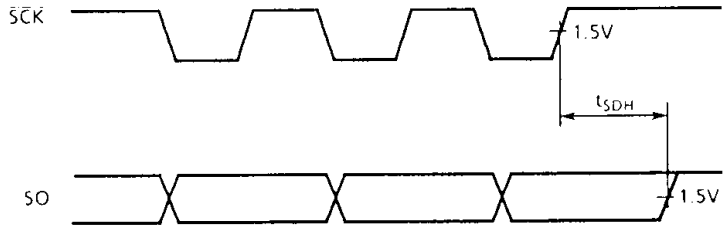
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		8.3			μs
Shift Data Hold Time	t_{SDH}		0.5tcy – 300	–	–	ns

Note. Shift Data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



TONE OUTPUT CHARACTERISTICS

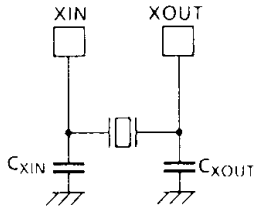
(V_{SS} = 0V, V_{DD} = 2.5 to 6.0V, T_{opr} = – 30 to 60 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	$R_L \geq$ 10KΩ, V_{DD} = 2.5V	70	105	140	mVrms
Pre-Emphasis High Band (COL / ROW)	PEHB	PEHB = 20log (COL / ROW)	1	2	3	dB
Output Distortion	DIS		–	–	10	%
Frequency Stability	Δf	Except error of osc. frequency	–	–	0.5	%

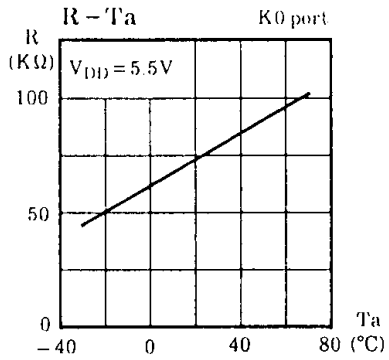
RECOMMENDED OSCILLATING CONDITIONS

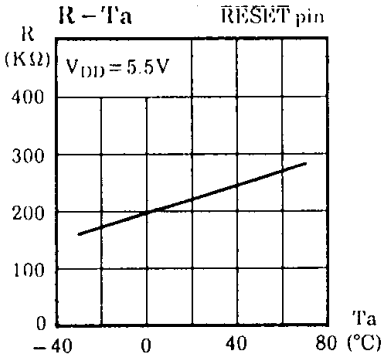
(V_{SS} = 0V, V_{DD} = 2.5 to 6.0V, T_{opr} = – 30 to 60°C)

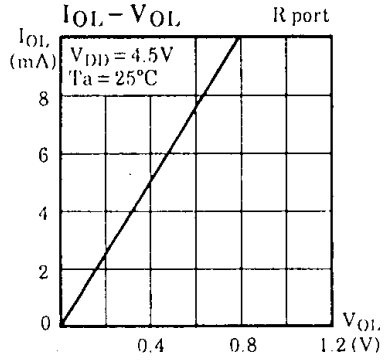
1.929MHz
Ceramic Resonator
CSA1.92MG901 (MURATA) $C_{XIN} = C_{XOUT}$ = 47pF
KBR - 1.92MS-TM1 (KYOCERA) $C_{XIN} = C_{XOUT}$ = 47pF

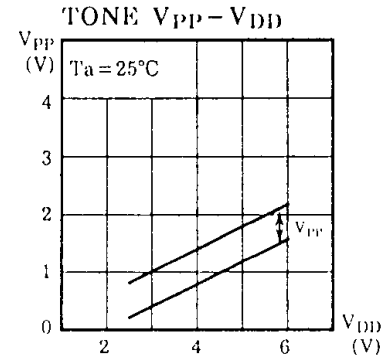


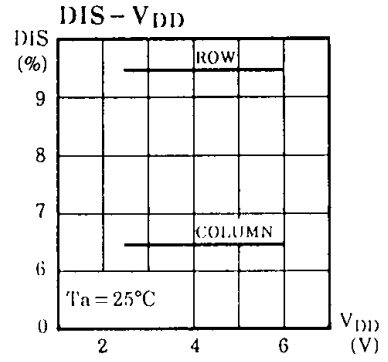
TYPICAL CHARACTERISTICS

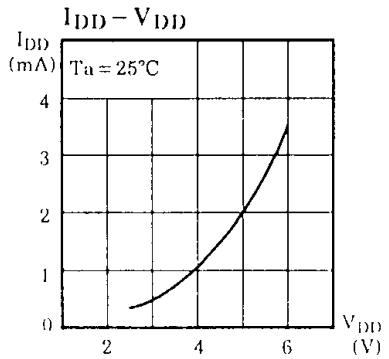


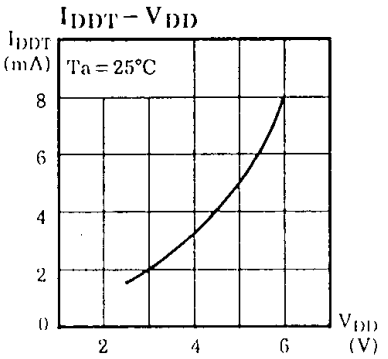








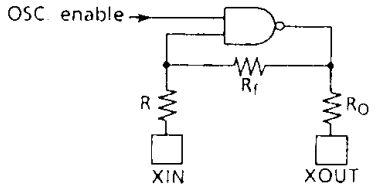
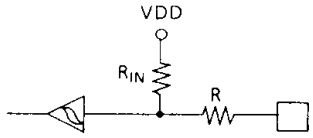
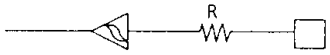
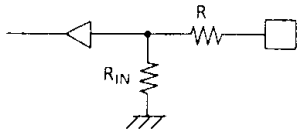




INPUT/OUTPUT CIRCUITRY

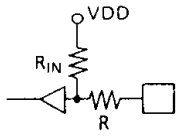
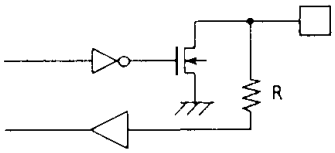
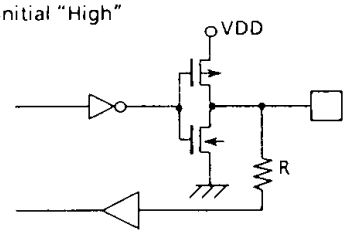
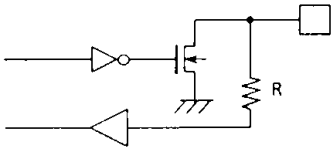
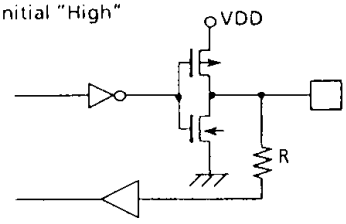
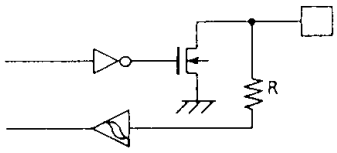
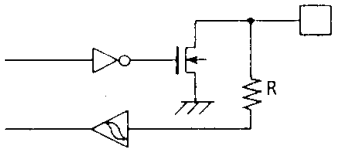
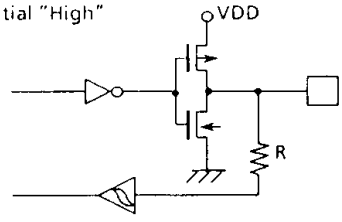
(1) Control pins

Input/Output circuitries of the 47C25 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins R = 1KΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2KΩ (typ.)
$\overline{RESET}$	Input		Hysteresis input Pull-up resistor R_{IN} = 220KΩ (typ.) R = 1KΩ (typ.)
HOLD (KE0)	Input (Input)		Hysteresis input R = 1KΩ (typ.)
TEST1 TEST2 TEST3 TEST4	Input		Pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)

(2) I/O ports

The input/output circuitries of the 47C25 I/O ports are shown below, any one of the circuitries can be chosen by a code (UB, UE, UH) as a mask option.

<table>
<tr><th>PORT</th><th>I/O</th><th colspan="2">INPUT/OUTPUT CIRCUITRY and CODE</th><th>REMARKS</th></tr>
<tr><td>K0</td><td>Input</td><td colspan="2"> 
</td><td>Pull-upresistor
R_{IN} = 70KΩ (typ.)
R = 1KΩ (typ.)</td></tr>
<tr><td rowspan="2">R3
R4
R5
R6</td><td rowspan="2">I/O</td><td>UB</td><td>UE, UH</td><td rowspan="2">Sink open drain or
Push-pull output
R = 1KΩ (typ.)</td></tr>
<tr><td>Initial "Hi-Z"
 
</td><td>Initial "High"
 
</td></tr>
<tr><td>R7</td><td>I/O</td><td>UB, UE</td><td>UH</td><td>Sink open drain or
Push-pull output
R = 1KΩ (typ.)</td></tr>
<tr><td></td><td></td><td>Initial "Hi-Z"
 
</td><td>Initial "High"
 
</td><td></td></tr>
<tr><td>R8</td><td>I/O</td><td colspan="2"> 
</td><td>Sink open drain
output
Initial "Hi-Z"
Hysteresis input
R = 1KΩ (typ.)</td></tr>
<tr><td rowspan="2">R9</td><td rowspan="2">Output</td><td>UB, UE</td><td>UH</td><td rowspan="2">Sink open drain or
Push-pull output
Hysteresis input
R = 1KΩ (typ.)</td></tr>
<tr><td>Initial "Hi-Z"
 
</td><td>Initial "High"
 
</td></tr>
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