CMOS 4-BIT MICROCONTROLLER

TMP47C236AN, TMP47C336AN

The 47C236A/336A are based on the TLCS-47 CMOS series. The 47C236A/336A have on-screen display circuit (OSD) to display characters and marks which indicate channel or time on TV screen, A/D converter input, D/A converter output which is suitable for application to the digital tuning system such as TV.

PART No.	ROM	RAM	PACKAGE
TMP47C236AN	2048 x 8-bit	128 x 4-bit	30-SDIP
TMP47C336AN	3072 x 8-bit	192 x 4-bit	

FEATURES

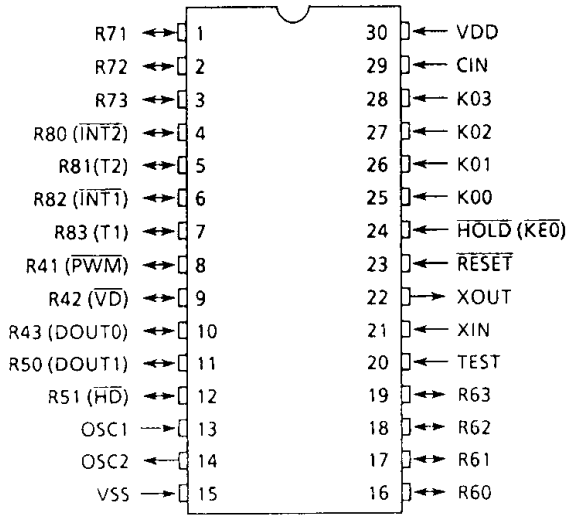
- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9μs (at 4.2 MHz)
- ◆89 basic instructions
  Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches, and multiple interrupt control is available
- ◆I/O port (22 pins)
  - Input 2 ports 5 pins
  - I/O 5ports 17 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Display on screen circuit
  - Number of characters 16 kinds
  - Number of characters displayed 3 columns
  - Composition of a character 8 x 8 dots
  - Size of character 2 kinds
  - Color of character 3 kinds
  - Display position Upper right corner
  - Fadeout function
- ◆Pulse width modulation output
  - 6-bit resolution 1 channels
- ◆3-bit A/D converter input
  Auto frequency control signal (S-shaped curve) detection
- ◆Horizontal synchronous signal is detected by timer/counter
- ◆Remote control signal preprocessing capability
- ◆High current outputs
  LED direct drive capability (typ. 10mA x 4 bits)
- ◆HOLD function
  Battery/Capacitor back-up
- ◆Real Time Emulator : BM47C336A

SDIP30

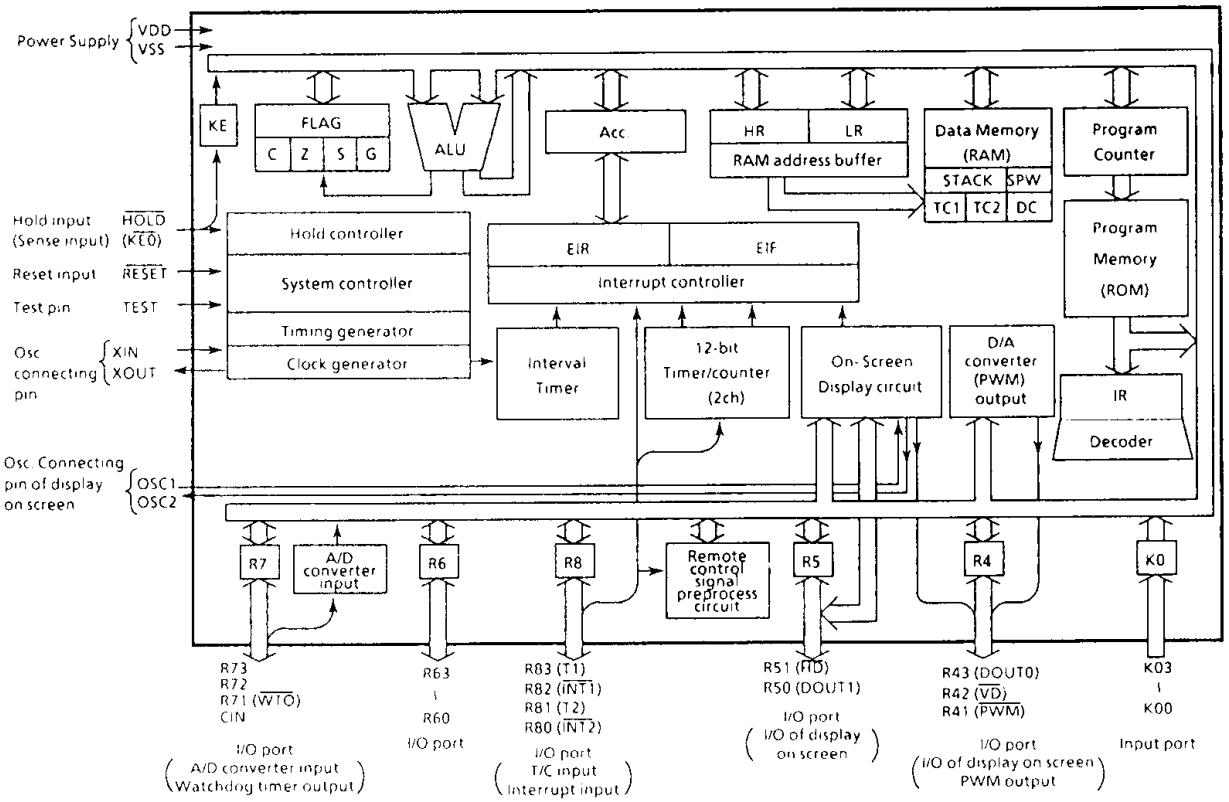
TMP47C236AN
TMP47C336AN

PIN ASSIGNMENT (TOP VIEW)

30-SDIP



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 ~ K00	Input	4-bit input port	
R43 (DOUT0)	I/O (Output)	3-bit I/O port with latch. When used as input port, D/A converter output pin and OSD output pin, the latch must be set to "1".	OSD output
R42 ($\overline{VD}$)			Horizontal sync signal input
R41 ($\overline{PWM}$)			6-bit D/A converter output
R51 ($\overline{HD}$)	I/O (Input)	4-bit I/O port with latch. When used as input port, resonator connecting pin for and OSD output pin, the latch must be set to "1".	Horizontal sync signal input
R50 (DOUT1)	I/O (Output)		OSD output
R63 ~ R60	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R73 ~ R71	I/O	3-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt and timer/counter input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
CIN	I/O (Input)	Input pin	3-bit A/D converter input
OSC1, OSC2	Input, Output	Resonator connecting pin of display on screen circuit	
XIN, XOUT	Input, Output	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	HOLD request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C236A/336A, the configuration and functions of hardwares are described.
As the description is provided with priority on those parts differing from the 47C200A/400A, the technical data sheets for the 47C200A shall also be referred to.
Note : The 47C236A/336A have no serial port, differing from the 47C200A/400A.

1. SYSTEM CONFIGURATION

(1) Internal CPU Function
Same as 47C200A/400A, except ROM and RAM capacity.

(2) Peripheral Hardware Function

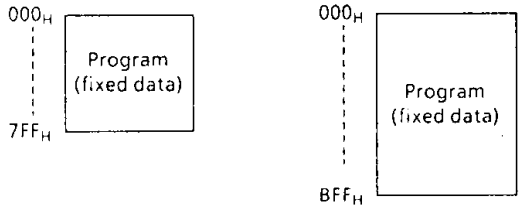
①	I/O port		
②	Interval Timer	⑤	A/D converter (comparator) input
③	Timer/Counter	⑥	D/A converter (Pulse Width Modulation) output
④	On-screen display (OSD) control circuit	⑦	Remote control signal pre-process circuit

This section describes functions of ④ to ⑦ and ROM · RAM capacity.

2. INTERNAL CPU FUNCTION

2.1 Program Memory (ROM)

For the 47C236A, programs are stored to addresses 000-7FF$_H$ (2048 × 8 bits) . And for the 47C336A, programs are stored to addresses 000-BFF$_H$ (3072 × 8 bits). Also, the table look-up instructions [LDH A,@DC +] and [LDL A, @DC] store to the accumulator the permanent data at addresses 000-7FF$_H$ and 000-BFF$_H$. The 5-bit 8-bit data conversion instruction [OUTB @HL] can not be used.



(a) 47C236A (b) 47C336A

Figure 2-1. Configuration of Program Memory (ROM)

2.2 Data memory (RAM)

TMP47C236A has 128 × 4 bits (address 00$_H$ through 0F$_H$ and 90$_H$ through FF$_H$) of the data memory (RAM), and the 47C336A has 192 × 4 bits (addresses 00$_H$ through 7F$_H$ and C0$_H$ through FF$_H$).

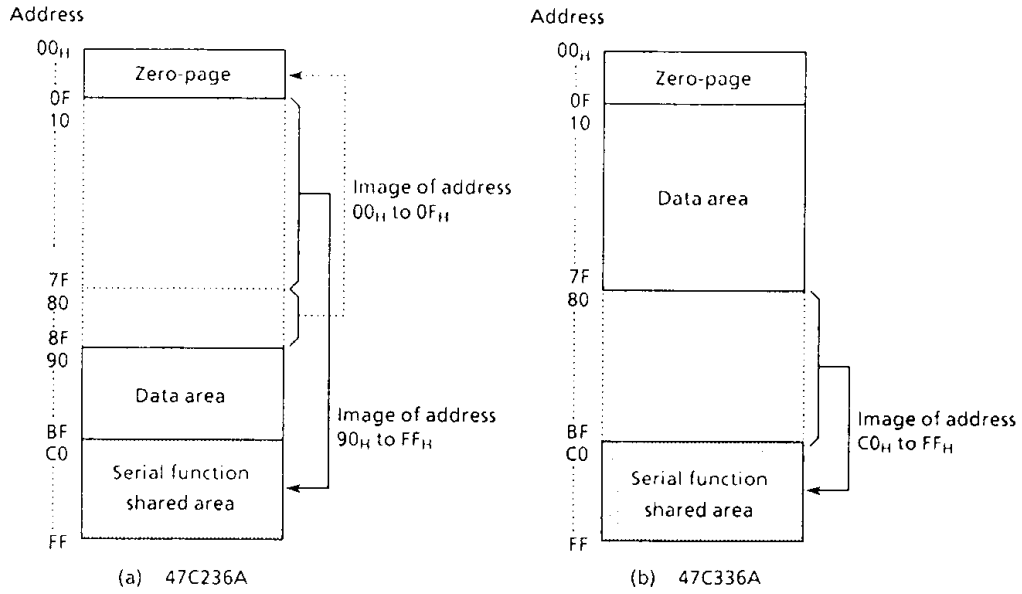


Figure 2-2. Data Memory Capacity and Address Assignment

Note. With the 47C236A, the most significant bit of the RAM address is always regarded as "0", so that addresses 90_H-FF_H may be accessed as addresses 10_H-$7F_H$. However, programming should be performed assuming that the RAM is assigned to addresses 00_H- $0F_H$ and 90_H-FF_H as shown in Figure 2-2 (a) by considering the application software evaluation with a piggyback or development tools.
And with the 47C336A, the RAM at addresses $C0_H$-FF_H is accessed when addresses 80_H-BF_H are addressed by a program, but when creating programs for evaluating software for piggybacks or development tools, assign the data memory to addresses 00_H-$7F_H$ or to addresses $C0_H$-FF_H, same as the 47C236A.

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O ports

The 47C236A/336A has 7 I/O Ports (24 Pins) each as follow.

①	K0 port	;	4-bit input
②	R4 port	;	3-bit input/output (R42 pin is shared by OSD output. R41, R42 pins is shared by D/A converter output)
③	R5 port	;	4-bit input/output (R53, R52 pins is shared by Resonator connecting pin for OSD R51, R50 pins is shared by I/O port)
④	R6 port	;	4-bit input/output
⑤	R7 port	;	4-bit input/output (R70 pins is shared by AFC comparator input)
⑥	R8 port	;	4-bit input/output (shared by external interrupt input and timer/counter input)
⑦	KE port	;	1-bit sense input (shared by hold request/release signal input)

This section describes ports of ②, ③, ⑤ which are changed from the 47C200A / 400A.
The 47C236A/336A has no P1, P2 and R9, therefore 5-bit 8-bit data conversion instruction [OUTB @HL] can not use.
Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A,%p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p,b TESTP %p,b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	——	——	–	–	–	–	–	–	–
02	——	——	–	–	–	–	–	–	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	——	——	–	–	–	–	–	–	–
0A	——	OSD data control register (1st digit)	–	○	○	–	–	–	–
0B	——	OSD data control register (2nd digit)	–	○	○	–	–	–	–
0C	——	OSD data control register (3rd digit)	–	○	○	–	–	–	–
0D	Remote control count register	Remote control offset register	–	○	○	–	–	–	–
0E	Status input	Remote control preprocess register	○	○	○	–	–	○	–
0F	——	——	–	–	–	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	Comparator input control	–	○	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	Watchdog timer control	–	○	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	PWM buffer selector	–	○	–	–	–	–	–
18	Undefined	PWM data transfer buffer	–	○	–	–	–	–	–
19	Undefined	Interval timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	OSD control 1	–	○	–	–	–	–	–
1B	Undefined	OSD control 2	–	○	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	$\overline{HD}$ counter control	–	○	–	–	–	–	–

Note 1 : "——" means the reserved state. Unavailable for the user programs.

Table 3-1. Port Address Assignment and Input/Output Instructions

(1) Port R4 (R43-R41)

3-bit I/O port with latch. When used as input port, the latch must be set to "1". The latch is initialized to "1".

This pin is used both as R43 for OSD output, and as R41 and R42 for D/A converter output. When used for OSD output, select DOUT0 to enable OSD. To use for D/A converter, set the latch to "1".

Also, when this pin is used as R43 for OSD output, "1" is read at the R43 pin and the $\overline{VD}$ is read at the R42 pin, during the input instruction is executed. There is no R40 pin, but "1" is read in during the input instruction is executed.

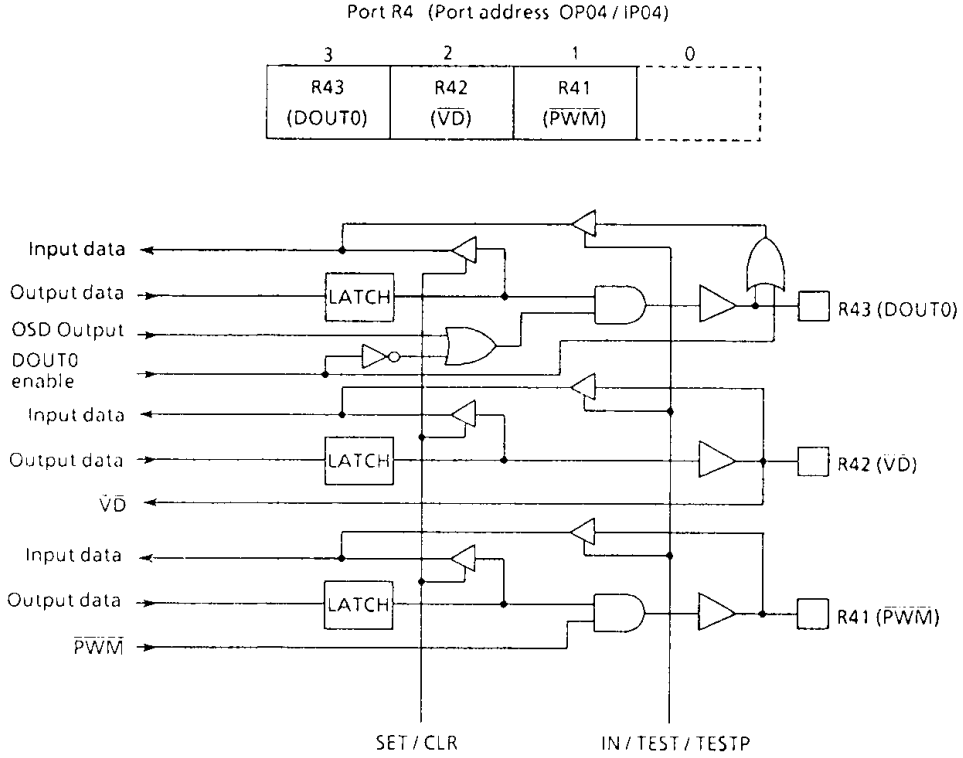


Figure 3-1. Port R4

(2) Port R5 (R51-R50)

This is a 2-bit input/output port with latch. When used as an input port, set the latch to "1". The R50 pin is used to disable OSD display. The latch is initialized to "1" by resetting.

The R51 pin is also used as the HD (horizontal sync signal) input pin. When used as the $\overline{HD}$ input pin, set the latch to "1". Like the R43 pin, the R50 pin is also used as the OSD output pin. When an input instruction is executed with OSD display enabled, "1" is read at the R50 pin and VD is read at the R51 pin. There are no R53 or R52 pins but "1" is read when an input instruction is executed.

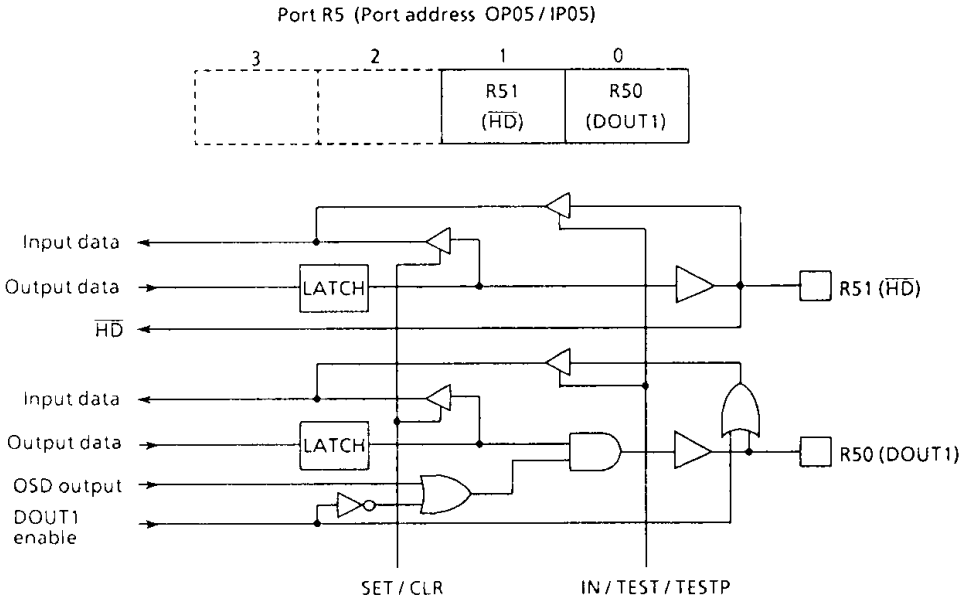


Figure 3-2. Port R5

(3) Port R7 (R73-R71) and CIN pin

Port R7 is 3-bit I/O ports with latch. When used as an input port, the latch should be set to "1". The latch is initialized to "1" during reset.

CIN pin is the A/D converter (comparator) input for the detection of AFC (Auto Frequency Control) signal. When used a comparator, the bit-3 of command register (OP12) is set to "1". CIN is the comparator input which has a programmable 3-bit D/A converter as a reference voltage source, and its data is read in the bit-0 of IP07.

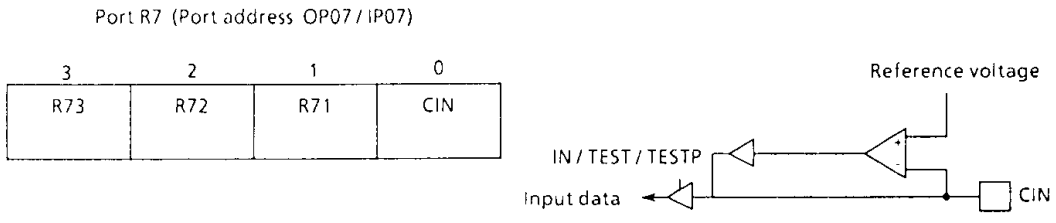


Figure 3-3. Port R7

3.2 On-Screen Display (OSD) Circuit

This built-in on-screen display circuit displays characters and symbols on the TV screen. Display size is 3 columns x 1 line, with a choice of 16 character patterns.
Fadeout is also possible when the display is turned off.

3.2.1 OSD Circuit Function

(1)	Number of characters	16 kinds
(2)	Number of characters displayed	3 characters
(3)	Composition of a character	8 x 8 dots
(4)	Size of character	2 kinds
(5)	Color of character	3 kinds
(6)	Display position variable	upper right corner of the TV screen
(7)	Fadeout function	

3.2.2 OSD Circuit Configuration

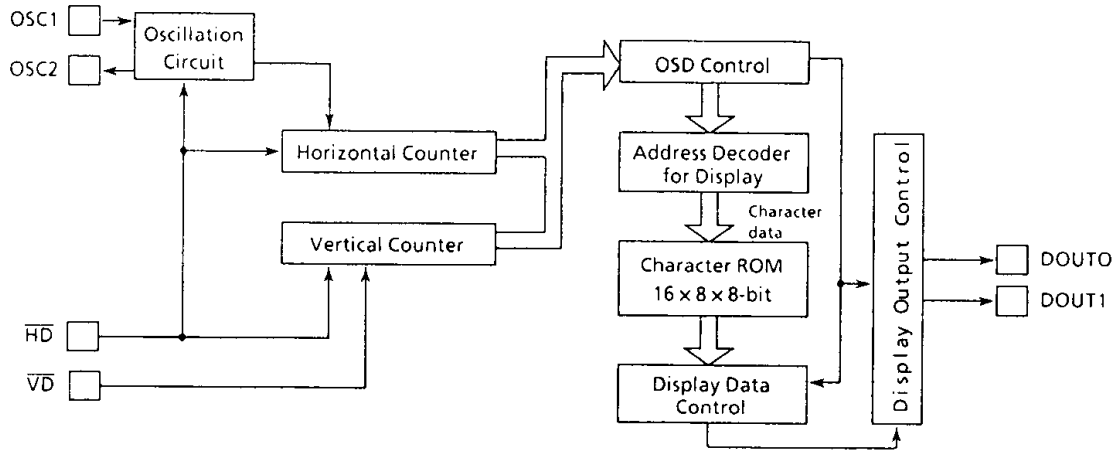


Figure 3-4. OSD Circuit

3.2.3 Character Display and Data Table for Display

The 16 character types are stored in the character ROM and the user can set optional patterns as shown in Figure 3-7. The character ROM contains 16 characters (character codes 00-0F$_H$) with an 8 x 8 dot configuration. Each character bit corresponds to one bit in the character ROM. "1" turns on the bit (dot) and "0" turns off the bit (dot).
When submitting programs, place the character data at address 1000$_H$ and following (addresses 1000-107F$_H$). Figure 3-5 shows typical character (8 x 8 bits) addresses and data. Figure 3-6 shows the standard pattern hex list.

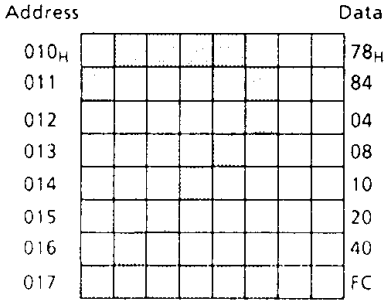


Figure 3-5. Example of Character

Note : Each character has an 8-byte data area. The starting address is the value of the character ROM address (00-0F$_H$) contained by the upper 4 bits of the 7-bit program area (00-7F$_H$).

Address																
000_H	78	84	84	84	84	84	84	78	10	30	10	10	10	10	10	38
010	78	84	04	08	10	20	40	FC	78	84	04	18	04	04	84	78
020	18	28	48	88	88	FC	08	08	FC	80	80	F8	04	04	84	78
030	78	84	80	F8	84	84	84	78	FC	04	04	08	10	20	20	20
040	78	84	84	78	84	84	84	78	78	84	84	7C	04	04	84	78
050	10	28	44	82	FE	82	82	82	82	82	82	82	82	44	28	10
060	02	04	08	10	10	20	40	80	7C	82	40	38	04	02	82	7C
070	FC	82	82	FC	80	80	80	80	00	00	00	00	00	00	00	00

Figure 3-6. Example Character Data (address 2000_H~)

3.2.7 Character ROM (Example Character)

The character data consist of the characters and symbols shown in Figure 3-7 as Example patterns. Optional character patterns can also be set by the user.

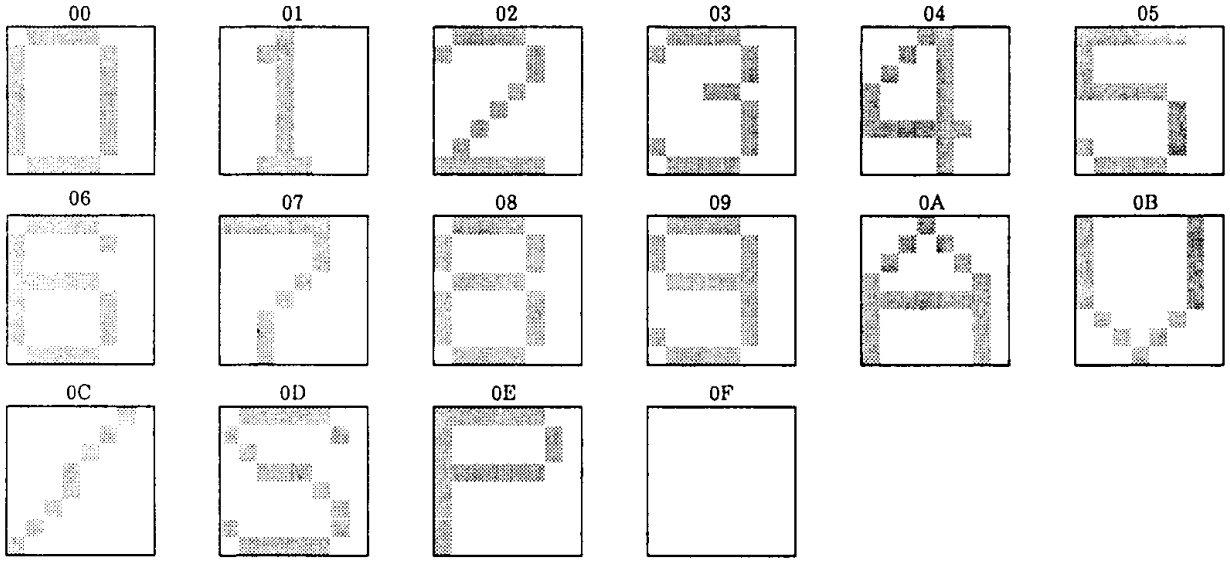


Figure 3-7. Address of the Character ROM and Character Pattern

3.2.5 Control of OSD Circuit

The OSD circuit is controlled by command registers 1 and 2 (OP1A, OP1B) and character code control registers 1, 2 and 3 (OP0A, OP0B, OP0C). OP1A controls the OSD output pin and OP1B controls character size and the display off method (display normally off, fadeout). Character code control registers OP0A, OP0B and OP0C correspond to the first, second and third display characters, respectively.

When all settings are completed and bit 3 (EOSD) of OP1B is set to "1", the character data read from the character ROM address indicated by the character code control register is output to the DOUT pin.

OSD control register 1
(Port address : OP1A Initial value 0000)

3	2	1	0
IV1	IV0	EDT1	EDT0

IV1	DOUT1 output buffer polarities
0	: DOUT1 active High
1	: 〃 Low

IV0	DOUT0 output buffer polarities
0	: DOUT0 active High
1	: 〃 Low

EDT1	Selects DOUT 1
0	: R50 pin
1	: DOUT1

EDT0	Selects DOUT 0
0	: R43 pin
1	: DOUT0

OSD control register 2
(Port address : OP1B Initial value 0000)

3	2	1	0
EOSD	EFOT	FTIM	CS

EOSD	OSD display control
0	: OSD display disable
1	: OSD display enable

EFOT	Display OFF Control
0	: normally display OFF
1	: fadeout

FTIM	Select fadeout time
0	: 16 T_{VD}
1	: 32 T_{VD}

CS	Selects character
0	: small character
1	: large character

Note. T_{VD} *: The period of vertical synchronous signal*

Figure 3-8. Congrol Command Register

Character code control register
The first display character
(Port address: OP0A initial value 0000)

3	2	1	0

The second display character
(Port address: OP0B initial value 0000)

3	2	1	0

The third display character
(Port address : OP0C initial value 0000)

3	2	1	0

Figure 3-9. Character Code Control Register

(1) Display Start Position

The display always starts at the upper right corner of the screen. The display start position of the first character is shown below.

Horizontal display start position	(small character)	$HS_S = 252T_{OSC}$
"	(large character)	$HS_L = 188T_{OSC}$
Vertical display start position		$V_S = 38T_{HD}$

Notes. T_{HD} : The period of horizontal synchronous signal
T_{OSC} : The period of OSD clock oscillation

(2) Display Character Size

Two different character sizes can be selected for screen display, but not for individual characters. Large characters are selected by setting bit 0 (CS) of command register OP1B to "1" and small characters are selected by setting bit 0 to "0". Table 3-2 shows the display character sizes.

	small character	large character
dot size	$2T_{HD} \times 2T_{OSC}$	$4T_{HD} \times 4T_{OSC}$
character size	$16T_{HD} \times 16T_{OSC}$	$32T_{HD} \times 32T_{OSC}$

Table 3-2. Character Size

(3) Fadeout Function

The OSD circuit of the 47C236A/336A has a built-in fadeout function that gradually fades the display from the bottom when turned off. The fadeout functions is controlled by bits 3 and 2 (EOSD, EFOT) of command register OP1B. The fadeout function is activated by setting bits 3 and 2 of command register OP1B to "01" in normal display status. The display is turned off normally by setting bits 3 and 2 to "00". The fadeout function is disabled when EOSD is "1".
Two different fadeout times can be selected by setting bit 1 (FTIM) of command register OP1B.

(4) Control of OSD Output and Color to Display

OSD output goes to the DOUT1 and DOUT0 pins, each of which can be enabled/disabled independently. Display is enabled by setting EDT1 and EDT2 when EOSD = 1. Since DOUT1 and DOUT0 are independent of each other, three colors can be output by using each for one color and both together for a composite color by connecting to the R, G and B pins. Figure 3-10 shows a typical TV screen image as an output example.

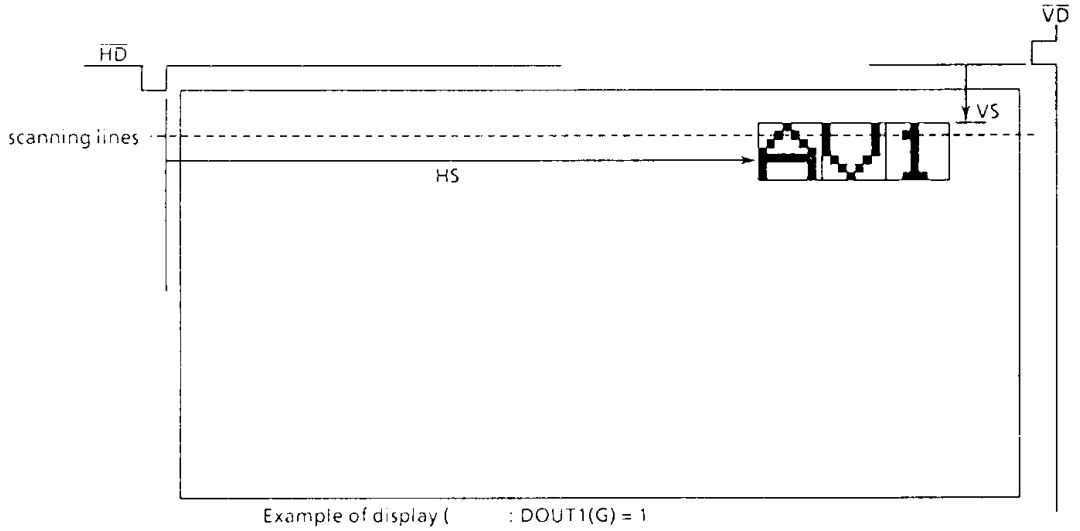


Figure 3-10. TV screen image

3.3 3-bit A/D Converter (Comparator) Input

Comparator input consists of a 3-bit D/A converter and a comparator. The AFC input voltage level can be detected in 8 stages by distinguishing bit 0 of IP07 while varying the comparison voltage (D/A converter output voltage) of the comparator with the command registe (OP12).
The comparator is disabled after a reset.

3.3.1 Circuit Configuration

Figure 3-11 shows the comparator input circuit configuration.

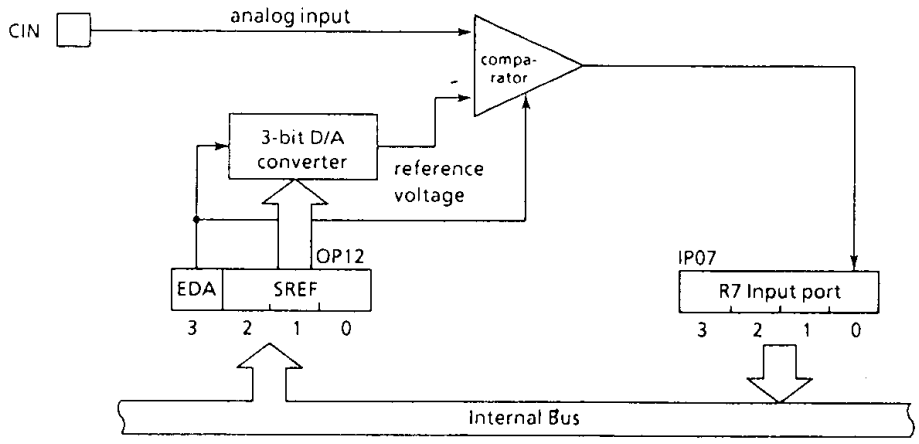


Figure 3-11. Comparator Input Circuit

3.3.2 Control of Comparator Input

The comparison voltage of the comparator is set with the lower 3 bits of the command register (OP12).
Table 3-3 shows the comparison voltage when Vdd = 5V.

Comparator input control command register (Port address OP12)

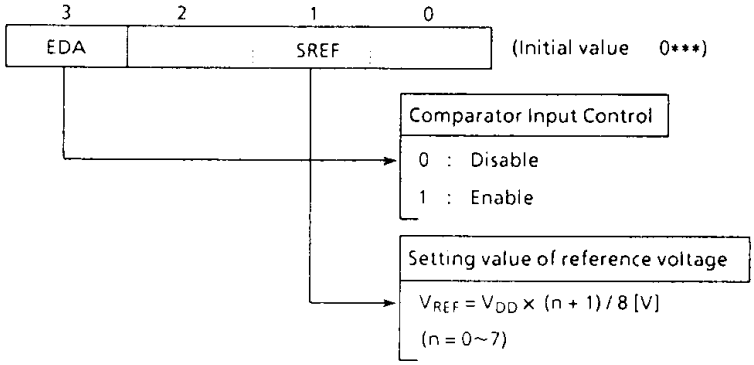


Figure 3-12. Control Command Register

OP12			Reference voltage [V]
2	1	0	
0	0	0	0.62
0	0	1	1.25
0	1	0	1.87
0	1	1	2.50
1	0	0	3.12
1	0	1	3.75
1	1	0	4.37
1	1	1	5.00

Table 3-3. Reference Voltage

3.4 D/A Converter (PWM) Output

47C236A/336A have one built-in pulse width modulation ($\overline{PWM}$) output channel. D/A converter output can easily be obtained by attaching a low-pass filter. PWM output goes to the R41 ($\overline{PWM}$) port. When this port is used for $\overline{PWM}$ output, set the corresponding R41 output latch to "1". The R41 output latch is initialized to "1" during resets. $\overline{PWM}$ output is controlled by the buffer selector (OP17) and data transfer buffer (OP18). Writing "CH" to the buffer selector sends $\overline{PWM}$ data written to the data transfer buffer to the $\overline{PWM}$ data latch and switches to $\overline{PWM}$ output. The $\overline{PWM}$ data sent to the $\overline{PWM}$ data latch are held until overwritten.

The buffer selector, data transfer buffer and $\overline{PWM}$ data latch are cleared to "0" ($\overline{PWM}$ output at "1" level) during resets and holds.

3.4.1 Circuit Configuration

Figure 3-13 shows the pulse width modulation circuit configuration.

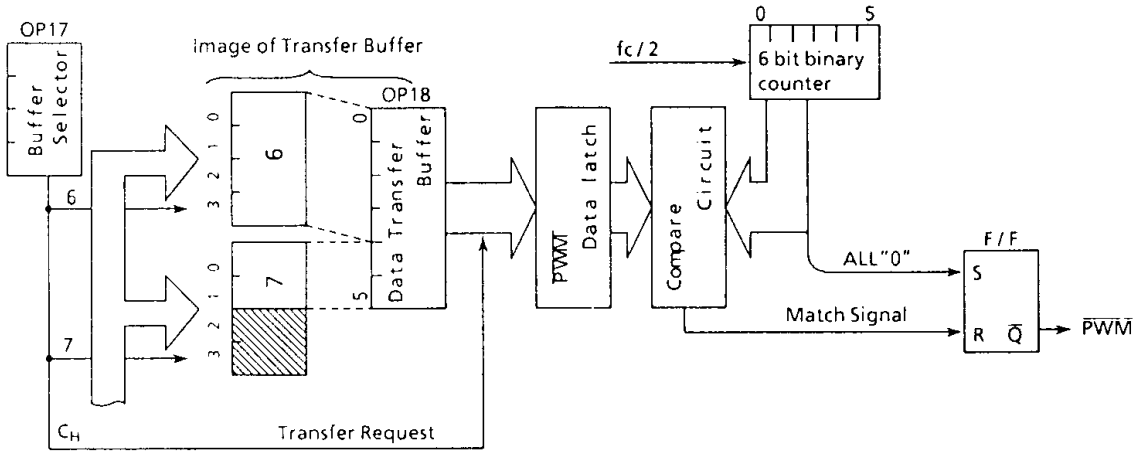


Figure 3-13. Pulse Width Modulation Circuit

3.4.2 Output Waveform of PWM Circuit

$\overline{PWM}$ Output

With 6-bit resolution PWM output, one cycle is TN = 2^7/fc [sec] . When 6-bit data are k (k = 0-63), the low level pulse width is k × t_0. Figure 3-14 shows the PWM output timing.

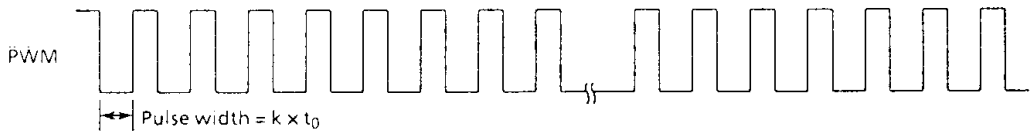


Figure 3-14. $\overline{PWM}$ Output Timing

3.4.3 Control of PWM Circuit (Data transfer)

$\overline{PWM}$ output is controlled by writing output data to the data transfer buffer (OP18). Output data are written in segments using the buffer selector (OP17). Buffer numbers are assigned to the segmented data transfer buffer and the data are written using the following procedure in accordance with the chart shown in Table 3-4.

① Write the numbers of the buffers to which data are to be written to the buffer selector (OP17).
② Write the corresponding PWM data to the selected buffer (OP18).
③ Repeat steps ① and ② until all of the output data have been written to the transfer buffer.
④ When all of the output data have been written, write "C_H" to the buffer selector.

The previous PWM data are output while the next output data are being written to the transfer buffer. A maximum time of 2^9/fc[sec] (at 4MHz, 128 μS) is required from the time "C_H" is written to the buffer selector until $\overline{PWM}$ output is switched.

Buffer Number (OP17)	Correspondence to bit (OP18)		Mode	PWM Output
6	Bit of PWM	3 ~ 0	Write	Preceding data
7	〃	5 ~ 4	〃	〃
C	None		Transfer	Present data

Table 3-4. The Bit and Buffer Number of Data Transfer Buffer

3.5 Remote Control Pre-processor

The remote control pre-processor counts the edge-to-edge time of the input pulse and generates an interrupt request each time that the switching edge of an input pulse is detected. Remote control signal waveform which has been rectified by the receiver is inputed to the R80 ($\overline{INT2}$) pin.

3.5.1 Circuit Configuration

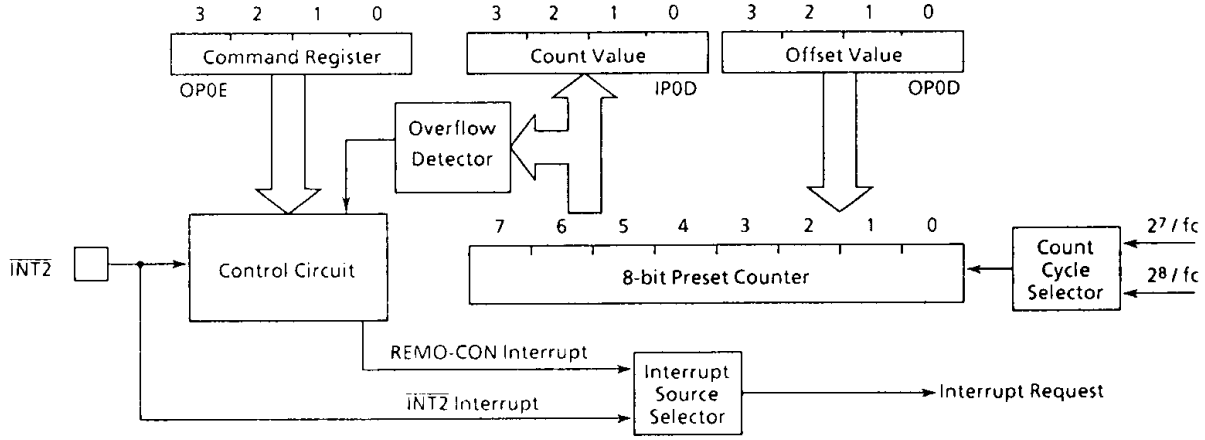


Figure 3-15. Remote Control Pre-processor

3.5.2 Control of Remote Control Pre-processor

The remote control pre-processor is controlled by the command register (OP0E) Also, external interrupt 2 is used to interrupt source. At reset, INT2 is selected, so a remote control discrimination (REMO-CON) interrupt is selected by command. Interrupt enable master F/F (EIF) and interrupt enable register (EIR) are used to enable/disable remote control discrimination interrupt. The interrupt priority is the same as for external interrupt 2.

REMO-CON pre-processor command register (Port address OP0E)

3	2	1	0
ERM	EDGE	CK32	ELD

(initial value 0000)

Select of interrupt source

0 : INT2 Interrupt (Trailing edge)
1 : REMO-CON Interrupt (Swithching edge)

Select of edge for interrupt

0 : At trailing edge
1 : At leading edge

Counter clock cycle

Example : At fc = 4.19MHz

0 : 2^8 / fc [sec] ..... 64 [μs]
1 : 2^7 / fc 32

load of offset value

1 : Enable (Cleares after loading)

NOTE. EDGE, CK32, ELD is available when ERM = 1.

Figure 3-16. Command Register

(1) 8-bit preset counter

This is a binary counter which counts the time from edge to next edge. A value of offset value register (OP0D) are loaded to the lower 4 bits and the value of the upper 4 bits are stored to the count value register (IP0D).

Offset value is loaded in the following cases :

① When ELD (bit 0 of the OP0E) is set to "1".
② When there is an overflow of the lower 4 bits.
③ When an edge is detected.

Count value is stored in the following cases :

① When the upper 4 bits are all "1".
② When an edge is detected.

(2) Reference time and detection time

The reference time must be created before measuring the pulse width of the remote control signal waveform. Reference time is set the value shown in Table 3-5 by the count cycle of the preset counter selected with the OP0E and the offset value set to the OP0D. Therfore, the product of the reference time and the count value read from the IP0D becomes the detecion time.
However, a worst error of the detection time is equivalent to reference time.

Count clock cycle	Offset value (HEX)	Reference time (n = 0 to 15)
2^7 / fc [sec]	0 to F	$(2^{11} - n \times 2^7)$ / fc [sec]
2^8 / fc	0 to F	$(2^{12} - n \times 2^8)$ / fc

Table 3-5. Set value of reference time

(3) Remote control pre-processing operation

First, set the offset value for creating the reference time to the OP0D. The offset value is loaded to the lower 4 bits of preset counter by setting ELD to "1". ERM can also be set to "1" at the same time. Setting ERM starts counting. ELD is cleared after loading but it is automatically loaded during the count by an overflow of the lower 4 bits.
After storing the count value in the IP0D by detecting the switching edge (leading/trailing) of the input pulse, the preset counter again loads the offser value to the lower 4 bits, clears to "0" the upper 4 bits and restarts counting.
An interrupt request is genarated at this time. Therfore, read the count value in the interrupt service routine. The next interrupt is disabled until the stored count value is read. Switching edges can select in one by one using EDGE.
If the upper 4 bits of counter becomes "1111_B" before the next edge is accepted, it is judged to be an overflow and the interrupt is generated.
In this case, IP0D is set to "F_H" and it can be identified to be the overflow interruption. The input pulse width of both "H" and "L" levels must be more than 192/fc [sec]. If any shorter pulse than 192/fc [sec] may be expected, put the dummy instruction [IN %IP0D, A] reading out from count value register in the main routine.
Even if ERM is "0", when an INT2 interrupt sourse is enabled (determined by EIF,EIR), an interrupt request is generated by a falling edge of input pulse.
Figure 3-17. shows the operation timing the remoto control pre-processor.

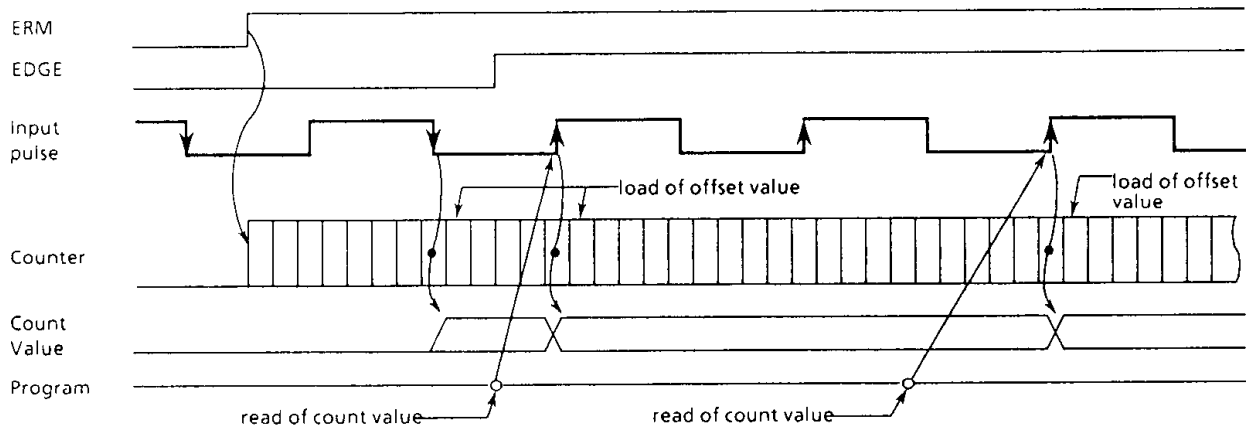
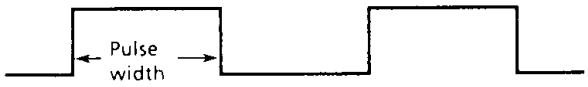


Figure 3-17. Timing chart

Example: To store a count value to RAM [10_H] that pulse width of input pulse is measured.




```
Main routin
        OUT     #5, %OP0D       ; Offset value register set to "5".
        OUT     #0FH, %OP0E     ; Interrupt enable with setting count cycle to 32 µsec,
                                  leading edge detection mode.
        CLR     0, 0            ; Clear to RAM [00H]0 as interrupt status flog.
        LD      A, #0001B       ; Interrupt enable
        XCH     A, EIR
        EICLR   IL, #111110B
        :
INT2 service routin
        TEST    0, 0            ; Skip, if interrupt status flag is "0".
        B       ST0
        LD      HL, #10H        ; HL ← 10H
        IN      %IP0D, @HL      ; RAM [10H] ← Count value
        CLR     0, 0            ; Clearing interrupt status flag.
        OUT     #0EH, %OP0E     ; Se to leading edge detection mode.
        B       SEND
ST0:    SET     0, 0            ; Setting interrupt status flag.
        OUT     #0AH, %OP0E     ; Set to trailing edge detection mode.
        IN      %IP0D, A        ; Dummy
SEND:           :
```

※ Calculation of pulse width with the avobe program when the count value stored to the RAM [10_H] is "9".
When the clock frequency is 32µs (fc = 4.19MHz) and the offser value is "5", the refrence time will be as follows :

$$(2^{11} - 5 \times 2^4) / fc = 336\ [\mu s]$$

Thus, the detection time (pulse width) will be 336 x 9 = 3.02[ms] (including an error of 336µs max.)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3~7	V
Input Voltage	V_{IN}		− 0.3~V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.3~V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R7 port	− 0.3~10	
Output Voltage (per 1 pin)	I_{OUT1}	R6 port	10	mA
	I_{OUT2}	R4, R5, R7, R8 port	3.2	
Output Current (Total)	ΣI_{OUT1}	R6 port	40	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55~125	°C
Operating Temperature	T_{opr}		− 20~70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, Topr = − 20~70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	4.2	MHz
	fosc	OSC1, OSC2		6	10	

Notes. Input Voltage V_{IH3}, V_{IL3} : in the HOLD mode

D.C. CHARACTERISTICS (V_{SS} = 0V, Topr = −20~70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	K0 port, TEST, RESET, HOLD	V_{DD} = 5.5V, V_{IN} = 5.5V/0V	−	−	±2	μA
	I_{IN2}	R port (open drain)					
Input Resistance	R_{IN1}	K0 port with pull-up		30	70	150	KΩ
	R_{IN2}	RESET		100	220	450	
Output Leakage Current	I_{LO}	Open drain port	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
Output High Voltage	V_{OH}	R6 Port	V_{DD} = 4.5V, I_{OH} = −200μA	2.4	−	−	V
Output Low Voltage	V_{OL}	XOUT を除く	V_{DD} = 4.5V, I_{OL} = −1.6mA	−	−	0.4	V
Output Low Current	I_{OL}	R6 port	V_{DD} = 4.5V, V_{OL} = 1.0V	−	10	−	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	−	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up /pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 5.3V/0.2V
The K0 port is open when the pull-up / pull-down resistor is contained.
The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

A/D CONVERTER CHARACTERISTICS

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max.	UNIT
Analog input voltage	V_{AIN}	CIN		V_{SS}	−	V_{DD}	V
A/D conversion error	−			−	−	$\pm\frac{1}{4}$	LSB

A.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5~6.0V, T_{opr} = −20~70°C)

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle time	t_{cy}		1.9	−	20	μs
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	−	−	ns
Low level Clock Pulse Width	t_{WCL}					

RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70°C)

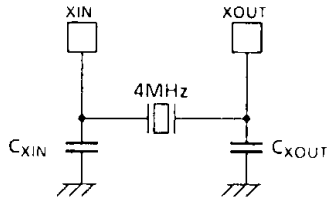
(1) 4MHz

Ceramic Resonator

CSA4.00MG	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30pF

Crystal Oscillator

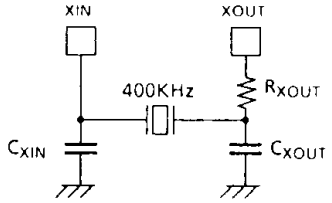
204B-6F 4.0000	(TOYOCOM)	$C_{XIN} = C_{XOUT}$ = 20pF



(2) 400KHz

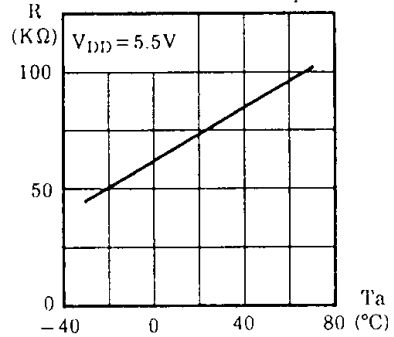
Ceramic Resonator

CSB400B	(MURATA)	$C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ
KBR-400B	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

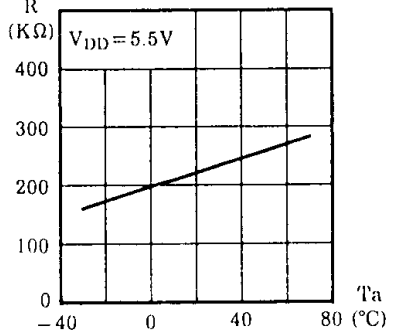


TYPICAL CHARACTERISTICS

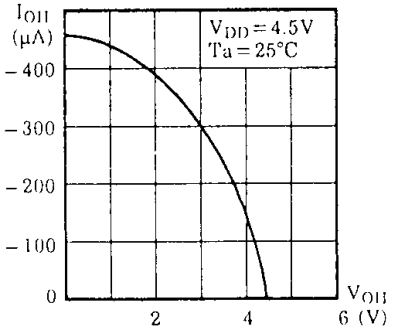
R – Ta K0 port



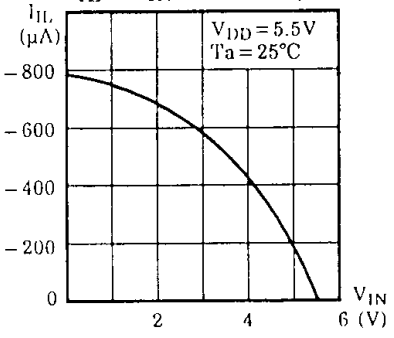
R – Ta $\overline{\text{RESET}}$ pin



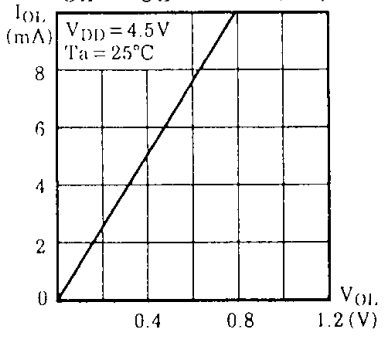
I_{OH} – V_{OH} CMOS R port



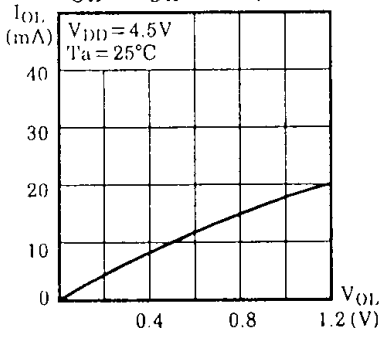
I_{IL} – V_{IN} CMOS R port



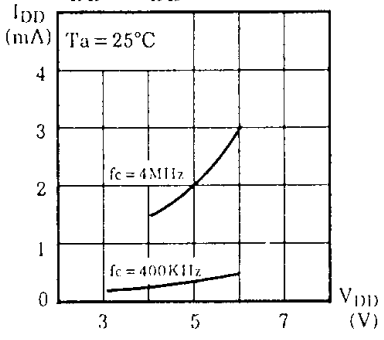
I_{OL} – V_{OL} R4, R5, R7, R8 port



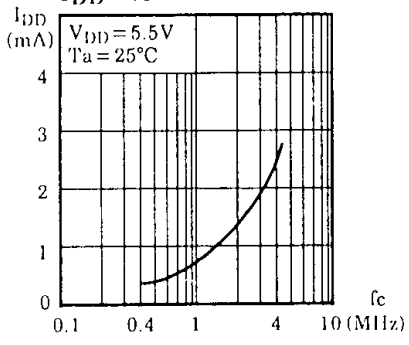
I_{OL} – V_{OL} R6 port



I_{DD} – V_{DD}



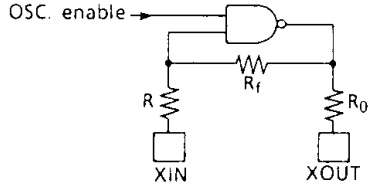
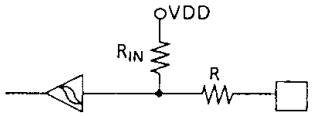
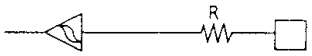
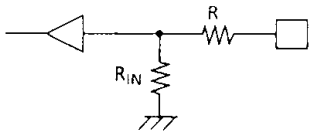
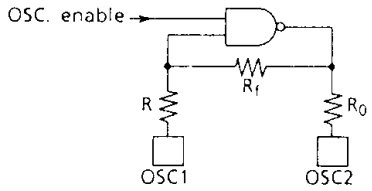
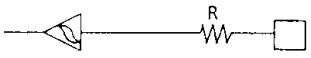
I_{DD} – fc



Input/Output Circuitry

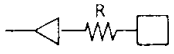
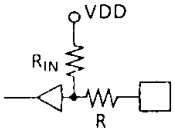
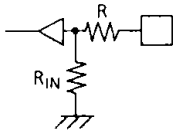
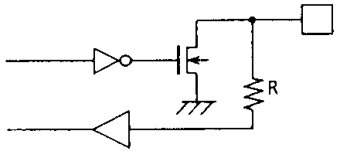
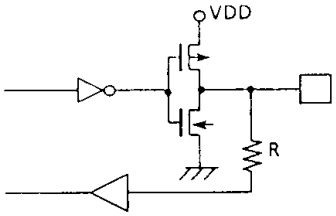
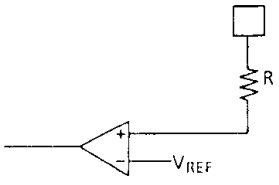
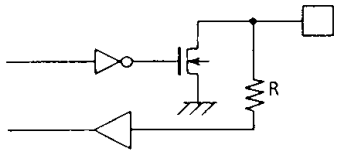
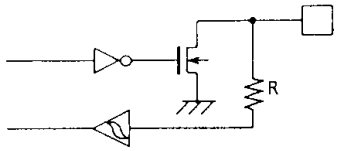
(1) Control pins

Input/output circuitries of the 47C236A/336A control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins R = 1KΩ (typ.) Rf = 1.5MΩ (typ.) RO = 2KΩ (typ.)
$\overline{\text{RESET}}$	Input		Hysteresis input Contained pull-up resistor RIN = 220KΩ (typ.) R = 1KΩ (typ.)
$\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$)	Input (Input)		Hysteresis input (Sense input) R = 1KΩ (typ.)
TEST	Input		Contained pull-down resistor RIN = 70KΩ (typ.) R = 1KΩ (typ.)
OSC1 OSC2	Input Output		Oscilation terminals for DOS R = 1KΩ (typ.) Rf = 1.5MΩ (typ.) RO = 2KΩ (typ.)
$\overline{\text{HD}}$ $\overline{\text{VD}}$	Input		Synchronous signal input Hysteresis input R = 1KΩ (typ.)

(2) I/O port

The input/output circuitries of the 47C236A/336A I/O port are shown below, any one of the circuitries can be chosen by a code (PD-PF) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input	PD:  PE:  PF: 	Pull-up/Pull-down resistor R_{IN} = 70kΩ (typ.) R = 1kΩ (typ.)
R4 R5	I/O		Sink open drain output Initial "Hi-Z" R = 1kΩ (typ.)
R6	I/O		Push-pull output Initial "Low" High drive current output I_{OL} = 10mA (typ.) R = 1kΩ (typ.)
R7	I/O	CIN:  R71-R73: 	Sink open drain output Initial "Hi-Z" Comparater input (R70) R = 1kΩ (typ.)
R8	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1kΩ (typ.)