### CMOS 4-Bit Microcontroller

# TMP47C212AN, TMP47C412AN

The TMP47C212A/412A are the high speed and high performance 4-bit single chip microcomputer with high breakdown voltage outputs of driving Vacuum Fluorescent Tube (VFT) directly which have pull-down resistors based on the TLCS-47 series.

Part No.	ROM	RAM	Package	OTP
TMP47C212AN	2048 × 8-bit	128 × 4-bit	D CDID42 COO 1 70	TNADAZDA10AN
TMP47C412AN	4096 × 8-bit	256 × 4-bit	P-SDIP42-600-1.78	TMP47P410AN

#### **Features**

- ◆4-bit single chip microcomputer
- ♦Instruction execution time: 1.9  $\mu$ s (at 4.2 MHz)
- ♦90 basic instructions
  - Table look-up instructions
  - 5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting: 15 levels max.
- ♦6 interrupt sources (External: 2, Internal: 4)

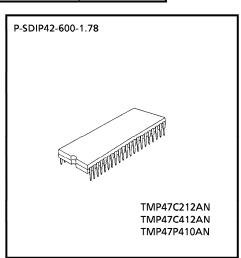
All sources have independent latches each, and multiple interrupt control is available.

- ◆I/O port (35 pins)
  - Input 2 ports 5 pins Output 5 ports 20 pins 10 pins I/O 3 ports
- ◆Interval Timer
- ◆Two 12-bit Timer / Counters

Timer, event counter, and pulse width measurement

- ◆Serial Interface with 4-bit buffer
  - External / internal clock, and leading/trailing edge shift mode
- ◆ High breakdown voltage outputs with pull-down resistor VFT direct drive capability (max.  $42 \text{ V} \times 20 \text{ bits}$ )
- ♦ Hold function

Battery / Capacitor back-up ◆Real Time Emulator: BM4721A



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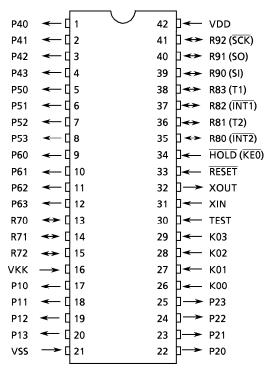
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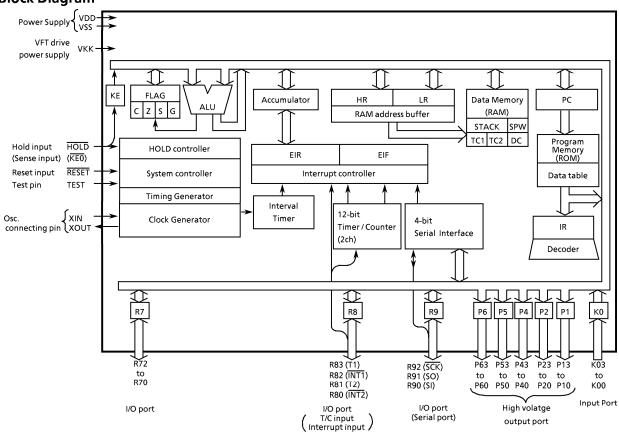
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## Pin Assignment (Top View)

P-SDIP42-600-1.78



## **Block Diagram**



# **Pin Function**

Pin Name	Input / Output	Func	tions	
K03 to K00	Input	4-bit input port		
P13 to P10	Output	4-bit output port with latch (High breakdo 8-bit data are output by the 5-bit to 8-bit d	•	
P43 to P40 P53 to P50 P63 to P60	Output	4-bit output port with latch (High breakdo	wn voltage output)	
R72 to R70	I/O	3-bit I/O port with latch. When used as input port, the latch must be	e set to "1".	
R83 (T1)  R82 (INT1)  R81 (T2)  R80 (INT2)	I/O (Input)	4-bit I/O port with latch.  When used as input port, external interrupt input pin, or Timer / Counter external input pin, the latch must be set to "1".	Timer / Counter 1 external input  External interrupt 1 input  Timer / Counter 2 external input  External interrupt 2 input	
R92 (SCK)	I/O (I/O)	3-bit I/O port with latch.	Serial clock I/O	
R91 (SO) R90 (SI)	I/O (Output) I/O (Input)	when used as input port or serial port, the latch must be set to "1".	Serial data output Serial data input	
XIN	Input Output	Resonator connecting pins. For inputting external clock, XIN is used an	nd XOUT is opened.	
RESET	Input	Reset signal input		
HOLD (KEO)	Input (Input)	Hold request / release signal input	Sense input	
TEST	Input	Test pin for out-going test. Be opened or f	ixed to low level.	
VDD	Power Supply	+ 5 V 0 V (GND)		
VKK		VFT drive power supply		

### **Operational Description**

The TMP47C212A/412A have high breakdown voltage output ports with pull-down resistor which are changed from the TMP47C200B/400B. The hardware configuration and operation are similar to the TMP47C200B/400B, except high breakdown voltage output ports with pull-down resistors, so refer to the technical data sheets for the TMP47C200B/400B.

The TMP47C212A/412A can not use the TMP47P410A as the OTP type without the external pull-down resisters. The technical data sheets for the TMP47P410A shall also be referred to.

#### 1. I/O Ports

The TMP47C212A/412A have 10 I/O ports (35 pin) each as follows.

① K0 ; 4-bit input

② P1, P2 ; 4-bit output (High Breakdown voltage output) ③ P4, P5, P6 ; 4-bit output (High Breakdown voltage output)

4 R7 ; 3-bit input/output

⑤ R8 ; 4-bit input/output (shared by external interrupt input and Timer/Counter

input)

⑥ R9 ; 3-bit input/output (shared by hold request/release signal input)
 ⑦ KE ; 1-bit sense input (shared by hold request/release signal input)

This section describes ports of ②, ③, ④ which are changed from the TMP47C200B/400B.

Table 1-1 lists the port address assignments and the I/O instructions that can access the ports.

The TMP47P410A can be used as OTP type but it is necessary to set the pull-down resistor externally. Threfore the technical data sheets for the TMP47P410A.

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#### (1) Ports P1/P2 and Ports P4/P5/P6

These are 4-bit, with latch, high breakdown voltage output ports capable of directly driving Vacuum Fluorescent Tube (VFT). Latch data are read an input instruction is executed. During reset, the latch is initialized to "0".

Pull-down resistor is connected to the 20 pins of the five ports P1, P2, P4, P5 and P6 in a P-channel open drain configuration.

Each pin is connected to the VKK pin through pull-down resistor (80 k $\Omega$ ); consequently, VFT can be driven by applying a minus voltage (35 V max) to the VKK pin without connecting external resistor. 8-bit data can be output through ports P1 and P2 by using the 5-bit to 8-bit data conversion instruction; therefore, these ports can also be effectively utilized as segment output pins.

Ports P4, P5 and P6 can be set and cleared in 1-bit units using the L-register indirect addressing bit manipulation instruction; therefore, these ports can also be effectively utilized as digit output pins. Figure 1-2 shows an example of driving a VFT 8-segment × 12-digit display.

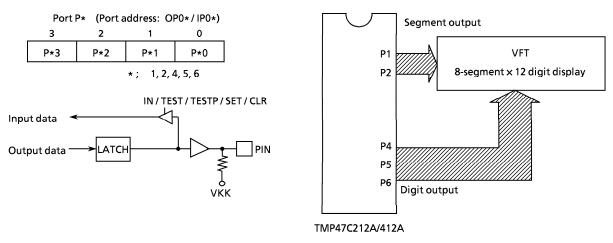


Figure 1-1. Ports P1, P2, P4, P5, P6

Figure 1-2. Example of driving a VFT

#### (2) Port R7

The 3-bit I/O port with latch, when used as an input, the latch must be set to "1". The latch is initialized to "1" during the reset. "1" is written to it when an input instruction is executed. They are the same as those of the TMP47C200B/400B, except pin R73 is included actually in Port R7.

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Table 1-1. Port address assignments and available I/O instructions

		rable 1-1. Port address assignments and available I/O instructions	assignment	anu avallatu	e I/O Instruc	tions			
Port		Port			Input/C	Input/Output instructions	tions	i	
address (**)	Input (IP**)	Outpot (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
H00	K0 input port		0				-	0	ŀ
10	P1 output latch	P1 output port	0	0	0	0	0	0	ı
02	P2 output latch	P2 output port	0	0	0	O (Note2)	0	0	1
03			I	I	ı	1	ı	ı	I
04	P4 output latch	P4 output port	0	0	0	1	0	0	0
90	P5 output latch	P5 output port	0	0	0	ı	0	0	0
90	P6 output latch	P6 output port	0	0	0	1	0	0	0
07	R7 input port	R7 output port	0	0	0	1	0	0	0
80	R8 input port	R8 output port	0	0	0	ı	0	0	
60	R9 input port	R9 output port	0	0	0	ı	0	0	1
0 V			ı	1	1	ı	ı	ı	ı
0B			ı	1	ŀ	ı	ı	ı	ı
00			I	-	ŀ	I	ı	ı	ı
00			1	I	1	I	ı	ı	ı
0E	SIO, Hold status		0	1	1		a.e.	0	ı
0F	Serial receive buffer	Serial transmit buffer	0	0	0	ı	I	ı	l
10 <sub>H</sub>	Undefind	Hold operating mode control	1	0	ı	ı	1	1	-
1	Undefind		I	I	ı	1	1	ı	1
12	Undefind	1	1	1	i	ı	ı	1	1
13	Undefind		ı	1	I	ı	ł	ı	1
14	Undefind		ı	!	ı	1	1	ı	ı
15	Undefind		l	1	I	1	1	ı	ı
16	Undefind		1	1	I	ı	ı	ı	I
17	Undefind		1	ı	ı	ı	ı	1	ı
18	Undefind		1	1	1	ı	ı	ı	ı
19	Undefind	Interval Timer interrupt control	1	0	ı	ı	ı		
1A	Undefind	-	1	ı	1	1	1	ı	
18	Undefind		1	1	1	1	ı	1	l
1C	Undefind	Timer/Counter 1 control	ı	0	ı	1	1	ı	ı
0	Undefind	Timer/Counter 2 control	ł	0	1	ı	ı	1	1
1E	Undefind		ı	1	ı	ı	I	1	ı
1.5	Undefind	Serial interface control	ı	0	1	1	-		ı

Note 1: "——" means the reserved state. Unavailable for the user programs.

Note 2: The 5-bit to 8-bit data conversion insruction [OUTB @HL], automatic access to ports P1 and P2.

## **Port Condition by RESET Operation**

The transition of Port condition by RESET operation is shown as below.

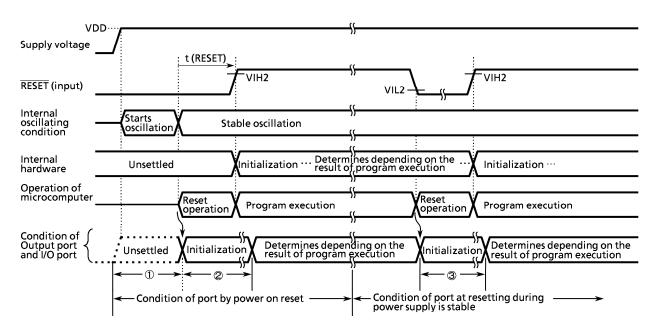


Figure 1-3. Port condition by reset operation

- Note 1: t(RESET) > 24/fc
- Note 2: VIL2: Stands for low level input voltage of RESET pin.
  VIH2: Stands for high level input voltage of RESET pin.
- Note 3: The condition of each port is unstable until the reset operation is started (① in the above Figure). Thus, when using port as an output pin, in the term of ①, to prevent the malfunction of external application circuit, insert the circuit outside of microcomputer between the output pin of Port and input pin of external application circuit.
- Note 4: The term starting from reset operation to the program which accesses port is executed (②, ③ in the above Figure), the condition of port becomes on the status of initialization by Reset operation. The initial condition of port differs from I/O circuit by each port, refer to the section of "INPUT/OUTPUT CIRCUITRY". Thus, when using Port as an output pin, in the term of the above ② and ③, the voltage level on the signal that connects with the output pin of Port to the input pin of external application circuit should be determined by the external circuitry such as pull-up resistor and/or pull-down resistor.

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# **Input / Output Circuitry**

## (1) Control pins

The input/output circuitries of the TMP47C212A/412A control pins are similar to those of the TMP47C200B/400B.

## (2) I/O ports

The input/output circuitries of the TMP47C212A/412A I/O ports are shown below, any one of the circuitries can be chosen by a code (NA, NB, NC) as a mask option.

Port	I/O	Inp	out / Output Circuitry and Code	)	Remarks
		NA	NB	NC	
К0	Input	<1 <sup>R</sup> W□	oVDD R <sub>IN</sub> ₹ R	R <sub>IN</sub>	Pull-up/pull-down resistor $R_{IN} = 70 \ k\Omega \ (typ.)$ $R = 1 \ k\Omega \ (typ.)$
P1 P2 P4 P5 P6	Output	_	OVDD R <sub>K</sub>		Source open drain Initial "Hi-Z" High breakdown voltage Pull-down resistor $R_K = 80 \ k\Omega$ (typ.)
R7	1/0		→ R R		Sink open drain Initial "Hi-Z" $R=1~k\Omega~(typ.)$
R8 R9	1/0		→ N N R R		Sink open drain Initial "Hi-Z" Hysteresis input $R=1~k\Omega$ (typ.)

### **Electrical Characteristics**

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	$V_{DD}$		– 0.5 to 7	٧
Input Voltage	$V_{IN}$		– 0.5 to V <sub>DD</sub> + 0.5	٧
	V <sub>OUT1</sub>	Except sink open drain pin	– 0.5 to V <sub>DD</sub> + 0.5	
Output Voltage	V <sub>OUT2</sub>	Sink open drain pin	– 0.5 to 10	V
	V <sub>OUT3</sub>	Source open drain pin	– 35 to V <sub>DD</sub> + 0.5	
	l <sub>OUT1</sub>	Ports P1, P2	- 2	
Output Current (Per 1 pin)	I <sub>OUT2</sub>	Ports P4, P5, P6	<b>– 2</b> 5	mA
	I <sub>OUT3</sub>	Ports R7, R8, R9	3.5	
Output current (Total)	Σ I <sub>OUT</sub>	Ports P4, P5, P6	- 100	mA
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (Time)	Tsld		260 (10 s)	°C
Storage Temprature	Tstg		– 55 to 125	°C
Oparating Temprature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Opeating Conditions

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
Complex Valtage	.,		In the Normal mode	4.5	6.0	\ \ \
Supply Voltage	$V_{DD}$		In the HOLD mode	2.0	6.0	V
	V <sub>IH1</sub>	Except Hysteresis Input	V >4.5V	$V_{DD} \times 0.7$		
Input High Voltage	$V_{IH2}$	Hysteresis Input	V <sub>DD</sub> ≧4.5 V	$V_{DD} \times 0.75$	$V_{DD}$	V
	V <sub>IH3</sub>		V <sub>DD</sub> <4.5 V	$V_{DD} \times 0.9$		
	V <sub>IL1</sub> Except Hysteresis Input		V <sub>DD</sub> ≧ 4.5 V		$V_{DD} \times 0.3$	
Input Low Voltage	$V_{IL2}$	Hysteresis Input	V <sub>DD</sub> = 4.5 V	0	$V_{DD} \times 0.25$	V
	$V_{IL3}$		V <sub>DD</sub> <4.5 V		$V_{DD} \times 0.1$	
Clock Frequency	fc			0.4	4.2	MHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input voltage  $V_{IH3}$ ,  $V_{IL3}$ : In the SLOW or HOLD mode.

**DC Characteristics** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 6.0 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis Input		_	0.7	_	٧
In an of Command	I <sub>IN1</sub>	Port K0, TEST, RESET, HOLD	V <sub>DD</sub> = 5.5 V,		1	± 2	•
Input Current	I <sub>IN2</sub>	Port R (open drain)	V <sub>IN</sub> = 5.5 V / 0 V				μΑ
Innut Posistance	R <sub>IN1</sub>	Port K0 with pull-up/poll-down		30	70	150	kΩ
Input Resistance	R <sub>IN2</sub>	RESET		100	220	450	K77
Output	I <sub>LO1</sub>	Port R (Sink open drain)	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	_	-	2	
Coutput Leakage Current I <sub>LO2</sub>	I <sub>LO2</sub>	Port P (Source open drain)	$V_{DD} = 5.5 \text{ V}, \ V_{OUT} = -32 \text{ V}$	_	_	- 2	μΑ
Output High Voltage	V <sub>OH2</sub>	Ports P1, P2	$V_{DD} = 4.5 \text{ V}, I_{OH} = -1.6 \text{ mA}$	2.4	-	_	V
Output riigii voitage	V <sub>OH3</sub>	Ports P4, P5, P6	$V_{DD} = 4.5 \text{ V}, I_{OH} = -10 \text{ mA}$	2.4	ı	-	V
Output Low Current	V <sub>OL</sub>	Ports R7, R8, R9	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	1	1	0.4	V
Pull-Down Resistance	R <sub>K</sub>	Source open drain	$V_{DD} = 5.5 \text{ V}, \ V_{KK} = -30 \text{ V}$	_	80	_	kΩ
Supply Current (in the Normal mode)	I <sub>DD</sub>		$V_{DD} = 5.5 V$ , fc = 4 MHz	1	3	6	mA
Supply Current (in the HOLD mode)	I <sub>DDH</sub>		V <sub>DD</sub> = 5.5 V	1	0.5	10	μΑ

Note 1: Typ. values show those at Topr =  $25^{\circ}$ C,  $V_{DD} = 5 V$ .

Note 2: Input Current I  $_{IN1}$ : The current through resistor is not included, when the pull-up/pull-down resistor is

contained.

Note 3: Supply Current:  $V_{IN} = 5.3 \text{ V} / 0.2 \text{ V}$ 

The K0 port is open when the pull-up / pull-down resistor is contained. The voltage applied to the R port is within the valid range  $V_{IL}$  or  $V_{IH.}$ 

**AC Characteristics** 

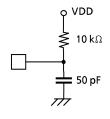
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 6.0 \text{ V}, \text{ Topr} = -30 \text{ to } 70^{\circ}\text{C})$ 

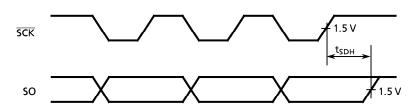
Parameter	Symbol	Condtions	Min	Тур.	Max	Unit
Instruction Cycle Time	t <sub>cy</sub>		1.9	_	20	μS
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation	80			
Low Level Clock Pulse Width	t <sub>WCL</sub>	For external clock operation	80			ns
Shift Data Hold Time	t <sub>SDH</sub>		0.5 tcy – 0.3		_	μS

Note: Shift data Hold Time:

External circuit for SCK pin and SO pin

Serial port (completion of transmission)





**Recommended Oscillating Conditions** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 6.0 \text{ V}, Topr = -30 \text{ to } 70^{\circ}\text{C})$ 

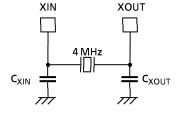
(1) 4 MHz

**Ceramic Resonator** 

CSA4.00MG (MURATA)  $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ KBR-4.00MS (KYOCERA)  $C_{XIN} = C_{XOUT} = 30 \text{ pF}$ 

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM)  $C_{XIN} = C_{XOUT} = 20 pF$ 



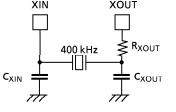
(2) 400 kHz

**Ceramic Resonator** 

CSB400B (MURATA)

KBR-400B (KYOCERA)

$$\begin{split} &C_{XIN} = C_{XOUT} = 220 \text{ pF, } R_{XOUT} = 6.8 \text{ } k\Omega \\ &C_{XIN} = C_{XOUT} = 100 \text{ pF, } R_{XOUT} = 10 \text{ } k\Omega \end{split}$$



## **Typical Characteristics**

